DDR4 SDRAM LRDIMM Addendum

MTA72ASS16G72LZ – 128GB

Introduction

- Information provided here is in addition to or supersedes information provided in the Micron DDR4 LRDIMM Core data sheet.
- DDR4 functionality and operations supported as defined in the component data sheet
- Features and specifications supported in the Micron DDR4 LRDIMM Core data sheet
- 288-pin, command/address/control-registered, data-buffered, load-reduced dual in-line memory module (LRDIMM)
- Fast data transfer rates: PC4-3200, PC4-2933
- 128GB (16 Gig x 72)
- Quad-rank, using 32Gb TwinDie DDR4
- Each die with 16 internal banks; 4 groups of 4 banks each

Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_{OPER} ≤ 95°C)	None
• Package	
– 288-pin DIMM (Green)	Z
• Frequency/CAS latency	
– 0.625ns @ CL = 22 (DDR4-3200)	-3G2
– 0.682ns @ CL = 21 (DDR4-2933)	-2G9

Figure 1: 288-Pin LRDIMM (R/C-E2)

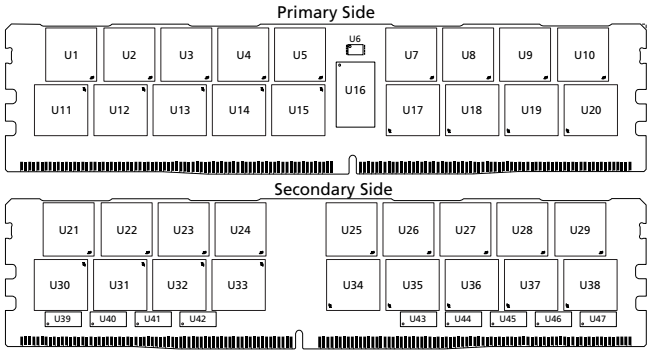


Figure 2: 288-Pin LRDIMM (R/C-D3)

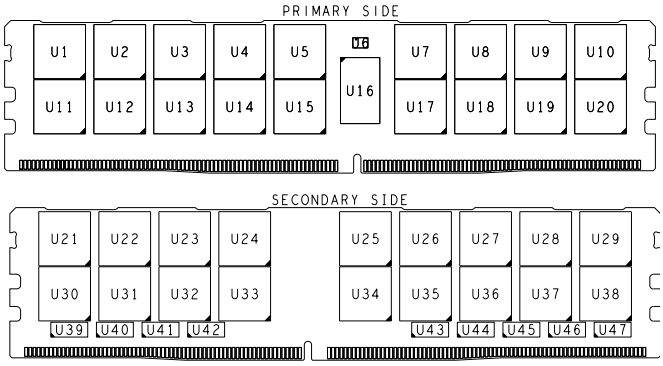


Table 1: Addressing

Parameter	128GB
Row address	256K A[17:0]
Column address	1K A[9:0]
Device bank group address	4 BG[1:0]
Device bank address per group	4 BA[1:0]
Device configuration	32Gb TwinDie (8 Gig x 4), 16 Banks
Package rank address	4 CS_n[3:0]

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Table 2: Part Numbers and Timing Parameters – 128GB Modules

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles ($CL-_nRCD-_nRP$)
MTA72ASS16G72LZ-3G2__	128GB	16 Gig x 72	25.6 GB/s	0.625ns/3200 MT/s	22-22-22
MTA72ASS16G72LZ-2G9__			23.47 GB/s	0.682ns/2933 MT/s	21-21-21

Notes: 1. Base device: MT40A8G4, 32Gb TwinDie DDR4 SDRAM. The data sheet for the base device can be found on micron.com.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes (ex. MTA72ASS16G72LZ-3G2F1).

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DQ Map

Table 3: Component-to-Module DQ Map, Front (R/C - E2)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	7	155	U2	0	15	166
	1	5	148		1	13	159
	2	6	10		2	14	21
	3	4	3		3	12	14
U3	0	23	177	U4	0	31	188
	1	21	170		1	29	181
	2	22	32		2	30	43
	3	20	25		3	28	36
U5	0	CB7	199	U7	0	39	247
	1	CB5	192		1	37	240
	2	CB6	54		2	38	102
	3	CB4	47		3	36	95
U8	0	47	258	U9	0	55	269
	1	45	251		1	53	262
	2	46	113		2	54	124
	3	44	106		3	52	117
U10	0	63	280	U12	0	2	12
	1	61	273		1	1	150
	2	62	135		2	3	157
	3	60	128		3	0	5
U13	0	8	16	U14	0	16	27
	1	10	23		1	18	34
	2	9	161		2	17	172
	3	11	168		3	19	179
U15	0	26	45	U16	0	CB2	56
	1	25	183		1	CB1	194
	2	27	190		2	CB3	201
	3	24	38		3	CB0	49
U17	0	34	104	U18	0	42	115
	1	32	97		1	40	108
	2	35	249		2	43	260
	3	33	242		3	41	253
U19	0	50	126	U20	0	56	130
	1	48	119		1	58	137
	2	51	271		2	57	275
	3	49	264		3	59	282

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Table 4: Component-to-Module DQ Map, Back (R/C - E2)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U21	0	61	273	U22	0	53	262
	1	63	280		1	55	269
	2	60	128		2	52	117
	3	62	135		3	54	124
U23	0	45	251	U24	0	37	240
	1	47	258		1	39	247
	2	44	106		2	36	95
	3	46	113		3	38	102
U25	0	CB5	192	U26	0	29	181
	1	CB7	199		1	31	188
	2	CB4	47		2	28	36
	3	CB6	54		3	30	43
U27	0	21	170	U28	0	13	159
	1	23	177		1	15	166
	2	20	25		2	12	14
	3	22	32		3	14	21
U29	0	5	148	U30	0	58	137
	1	7	155		1	56	130
	2	4	3		2	59	282
	3	6	10		3	57	275
U31	0	48	119	U32	0	40	108
	1	50	126		1	42	115
	2	49	264		2	41	253
	3	51	271		3	43	260
U33	0	32	97	U34	0	CB1	194
	1	34	104		1	CB2	56
	2	33	242		2	CB0	49
	3	35	249		3	CB3	201
U35	0	25	183	U36	0	18	34
	1	26	45		1	16	27
	2	24	38		2	19	179
	3	27	190		3	17	172
U37	0	10	23	U38	0	1	150
	1	8	16		1	2	12
	2	11	168		2	0	5
	3	9	161		3	3	157

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Table 5: Component-to-Module DQ Map, Front (R/C - D3)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	6	10	U2	0	14	21
	1	4	3		1	12	14
	2	7	155		2	15	166
	3	5	148		3	13	159
U3	0	22	32	U4	0	30	43
	1	20	25		1	28	36
	2	23	177		2	31	188
	3	21	170		3	29	181
U5	0	CB6	54	U7	0	38	102
	1	CB4	47		1	36	95
	2	CB7	199		2	39	247
	3	CB5	192		3	37	240
U8	0	46	113	U9	0	54	124
	1	44	106		1	52	117
	2	47	258		2	55	269
	3	45	251		3	53	262
U10	0	62	135	U12	0	2	12
	1	60	128		1	0	5
	2	63	280		2	3	157
	3	61	273		3	1	150
U13	0	10	23	U14	0	18	34
	1	8	16		1	16	27
	2	11	168		2	19	179
	3	9	161		3	17	172
U15	0	26	45	U16	0	CB2	56
	1	24	38		1	CB0	49
	2	27	190		2	CB3	201
	3	25	183		3	CB1	194
U17	0	34	104	U18	0	42	115
	1	32	97		1	40	108
	2	35	249		2	43	260
	3	33	242		3	41	253
U19	0	50	126	U20	0	58	137
	1	48	119		1	56	130
	2	51	271		2	59	282
	3	49	264		3	57	275

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Table 6: Component-to-Module DQ Map, Back (R/C - D3)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U21	0	60	128	U22	0	52	117
	1	62	135		1	54	124
	2	61	273		2	53	262
	3	63	280		3	55	269
U23	0	44	106	U24	0	36	95
	1	46	113		1	38	102
	2	45	251		2	37	240
	3	47	258		3	39	247
U25	0	CB4	47	U26	0	28	36
	1	CB6	54		1	30	43
	2	CB5	192		2	29	181
	3	CB7	199		3	31	188
U27	0	20	25	U28	0	12	14
	1	22	32		1	14	21
	2	21	170		2	13	159
	3	23	177		3	15	166
U29	0	4	3	U30	0	56	130
	1	6	10		1	58	137
	2	5	148		2	57	275
	3	7	155		3	59	282
U31	0	48	119	U32	0	40	108
	1	50	126		1	42	115
	2	49	264		2	41	253
	3	51	271		3	43	260
U33	0	32	97	U34	0	CB0	49
	1	34	104		1	CB2	56
	2	33	242		2	CB1	194
	3	35	249		3	CB3	201
U35	0	24	38	U36	0	16	27
	1	26	45		1	18	34
	2	25	183		2	17	172
	3	27	190		3	19	179
U37	0	8	16	U38	0	0	5
	1	10	23		1	2	12
	2	9	161		2	1	150
	3	11	168		3	3	157

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I_{DD} Specifications

Table 7: DDR4 I_{DD} Specifications and Conditions (0°C ≤ T_C ≤ 85°C) – 128GB (Die Revision B)

Values are for the MT40A8G4 DDR4 TwinDie SDRAM only and are computed from values specified in the 32Gb (8 Gig x 4) component data sheet

Parameter	Symbol	3200	2933	Units
One bank ACTIVATE-PRECHARGE current	I_{CDD0}	3402	3384	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I_{PP} current	I_{CPP0}	234	234	mA
One bank ACTIVATE-READ-PRECHARGE current	I_{CDD1}	3582	3564	mA
Precharge standby current	I_{CDD2N}	3258	3240	mA
Precharge standby ODT current	I_{CDD2NT}	3330	3312	mA
Precharge power-down current	I_{CDD2P}	3096	3096	mA
Precharge quite standby current	I_{CDD2Q}	3168	3168	mA
Active standby current	I_{CDD3N}	3726	3708	mA
Active standby I_{PP} current	I_{CPP3N}	216	216	mA
Active power-down current	I_{CDD3P}	3564	3546	mA
Burst read current	I_{CDD4R}	5418	5274	mA
Burst write current	I_{CDD4W}	5274	5148	mA
Distributed refresh current (1x REF)	I_{CDD5R}	3744	3726	mA
Distributed refresh I_{PP} current (1x REF)	I_{CPP5R}	252	252	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I_{CDD6N}	3528	3528	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I_{CDD6E}	4500	4500	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I_{CDD6R}	2844	2844	mA
Auto self refresh current (25°C)	I_{CDD6A} (25°C)	2502	2502	mA
Auto self refresh current (45°C)	I_{CDD6A} (45°C)	2844	2844	mA
Auto self refresh current (75°C)	I_{CDD6A} (75°C)	3420	3420	mA
Auto self refresh current (95°C)	I_{CDD6A} (95°C)	4500	4500	mA
Auto self refresh I_{PP} current	I_{CPP6X}	504	504	mA
Bank interleave read current	I_{CDD7}	6606	6480	mA
Bank interleave read I_{PP} current	I_{CPP7}	360	360	mA
Maximum power-down current	I_{CDD8}	2880	2880	mA

Notes: 1. When T_C > 85°C, the I_{DD} and I_{PP} values must be derated. Refer to the base device data sheet I_{DD} and I_{PP} specification tables for derating values for the applicable die-revision.

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Table 8: DDR4 I_{DD} Specifications and Conditions (0°C ≤ T_C ≤ 85°C) – 128GB (Die Revision F)

Values are for the MT40A8G4 DDR4 TwinDie SDRAM only and are computed from values specified in the 32Gb (8 Gig x 4) component data sheet

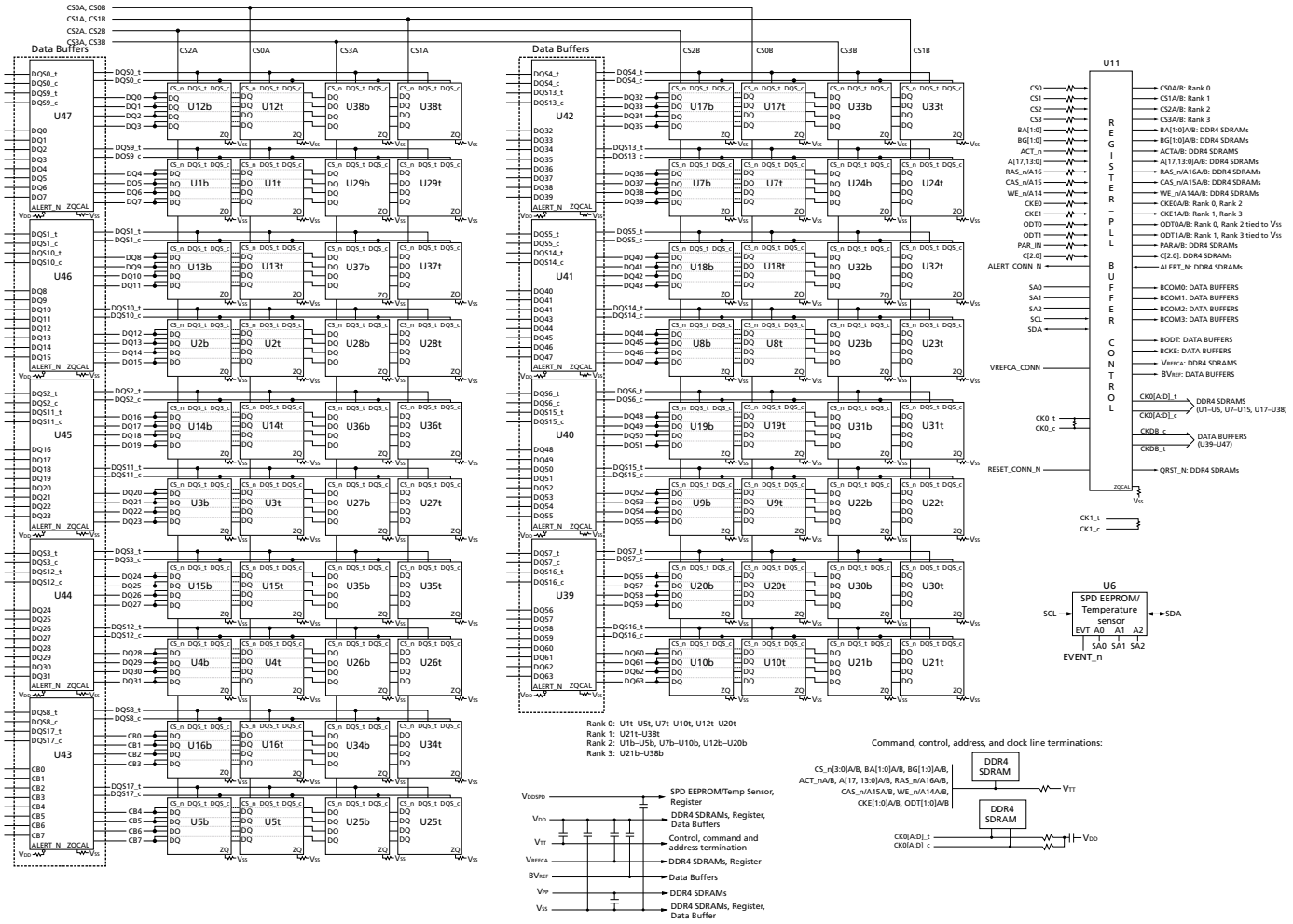
Parameter	Symbol	3200	Units
One bank ACTIVATE-PRECHARGE current	I_{CDD0}	3042	mA
One bank ACTIVATE-PRECHARGE, wordline boost, I_{PP} current	I_{CPP0}	162	mA
One bank ACTIVATE-READ-PRECHARGE current	I_{CDD1}	3240	mA
Precharge standby current	I_{CDD2N}	2862	mA
Precharge standby ODT current	I_{CDD2NT}	2970	mA
Precharge power-down current	I_{CDD2P}	2736	mA
Precharge quite standby current	I_{CDD2Q}	2808	mA
Active standby current	I_{CDD3N}	3132	mA
Active standby I_{PP} current	I_{CPP3N}	144	mA
Active power-down current	I_{CDD3P}	2916	mA
Burst read current	I_{CDD4R}	4338	mA
Burst write current	I_{CDD4W}	3780	mA
Distributed refresh current (1x REF)	I_{CDD5R}	3276	mA
Distributed refresh I_{PP} current (1x REF)	I_{CPP5R}	180	mA
Self refresh current: Normal temperature range (0°C to 85°C)	I_{CDD6N}	3276	mA
Self refresh current: Extended temperature range (0°C to 95°C)	I_{CDD6E}	4608	mA
Self refresh current: Reduced temperature range (0°C to 45°C)	I_{CDD6R}	2088	mA
Auto self refresh current (25°C)	I_{CDD6A} (25°C)	1764	mA
Auto self refresh current (45°C)	I_{CDD6A} (45°C)	2088	mA
Auto self refresh current (75°C)	I_{CDD6A} (75°C)	3204	mA
Auto self refresh current (95°C)	I_{CDD6A} (95°C)	4608	mA
Auto self refresh I_{PP} current	I_{CPP6X}	216	mA
Bank interleave read current	I_{CDD7}	6912	mA
Bank interleave read I_{PP} current	I_{CPP7}	306	mA
Maximum power-down current	I_{CDD8}	2592	mA

Notes: 1. When T_C > 85°C, the I_{DD} and I_{PP} values must be derated. Refer to the base device data sheet I_{DD} and I_{PP} specification tables for derating values for the applicable die-revision.

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Functional Block Diagram

Figure 3: Functional Block Diagram



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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