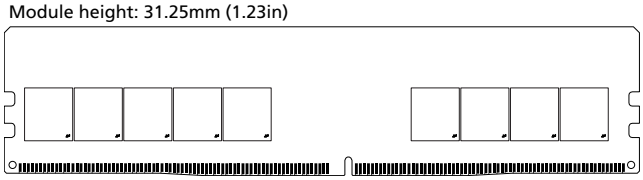
# DDR4 SDRAM UDIMM

## MTA9ASF2G72AZ – 16GB

## Features

- DDR4 functionality and operations supported as defined in the component data sheet
- 288-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rate: PC4-3200
- 16GB (2 Gig x 72)
- $V_{DD}$ = 1.20V (NOM)
- $V_{PP}$ = 2.5V (NOM)
- $V_{DDSPD}$ = 2.5V (NOM)
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Low-power auto self refresh (LPASR)
- Data bus inversion (DBI) for data bus
- On-die $V_{REFDQ}$ generation and calibration
- Single-rank
- On-board $I^2C$ temperature sensor with integrated serial presence-detect (SPD) EEPROM
- 16 internal banks; 4 groups of 4 banks each
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

**Figure 1: 288-Pin UDIMM (MO-309, R/C D2)**




| Options | Marking |
|---|---|
| • Operating temperature | |
| – Commercial ($0°C \le T_{OPER} \le 95°C$) | None |
| • Package | |
| – 288-pin DIMM (halogen-free) | Z |
| • Frequency/CAS latency | |
| – 0.625ns @ CL = 22 (DDR4-3200) | -3G2 |

**Table 1: Key Timing Parameters**

| Speed Grade | PC4- | Data Rate (MT/s) CL = 24 | 22 | 21 | 20\ 19 | 18\ 17 | 16\ 15 | 14\ 13 | 12\ 11 | 10\ 9 | $^tRCD$ ns | $^tRP$ ns | $^tRC$ ns |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| -3G2 | 3200 | 3200, 2933 | 3200, 2933 | 2933 | 2666\ 2666 | 2400\ 2400 | 2133\ 2133 | 1866\ 1866 | 1600\ 1600 | 1333\ – | 13.75 | 13.75 | 45.75 |
| -2G9 | 2933 | – | 2933 | 2933 | 2666\ 2666 | 2400\ 2400 | 2133\ 2133 | 1866\ 1866 | 1600\ 1600 | 1333\ – | 14.32 (13.75)[1] | 14.32 (13.75)[1] | 46.32 (45.75)[1] |
| -2G6 | 2666 | – | – | – | 2666\ 2666 | 2400\ 2400 | 2133\ 2133 | 1866\ 1866 | 1600\ 1600 | 1333\ – | 14.25 (13.75)[1] | 14.25 (13.75)[1] | 46.25 (45.75)[1] |


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**Table 1: Key Timing Parameters (Continued)**

| Speed Grade | PC4- | Data Rate (MT/s) CL = 24 | 22 | 21 | 20\ 19 | 18\ 17 | 16\ 15 | 14\ 13 | 12\ 11 | 10\ 9 | $^{t}$RCD ns | $^{t}$RP ns | $^{t}$RC ns |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| -2G3 | 2400 | – | – | – | – | 2400\ 2400 | 2133\ 2133 | 1866\ 1866 | 1600\ 1600 | 1333\ – | 14.16 (13.75)[1] | 14.16 (13.75)[1] | 46.16 (45.75)[1] |
| -2G1 | 2133 | – | – | – | – | – | 2133\ 2133 | 1866\ 1866 | 1600\ 1600 | 1333\ 1333 | 14.06 (13.5)[1] | 14.06 (13.5)[1] | 47.06 (46.5)[1] |

Note: 1. Down-bin timing, refer to component data sheet Speed Bin Tables for details.

**Table 2: Addressing**

| Parameter | 16GB |
|---|---|
| Row address | 128K A[16:0] |
| Column address | 1K A[9:0] |
| Device bank group address | 4 BG[1:0] |
| Device bank address per group | 4 BA[1:0] |
| Device configuration | 16Gb (2 Gig x 8), 16 banks |
| Module rank address | CS0_n |

**Table 3: Part Numbers and Timing Parameters – 16GB Modules**

Base device: MT40A2G8,[1] 16Gb DDR4 SDRAM

| Part Number[2] | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL-$_{n}$RCD-$_{n}$RP) |
|---|---|---|---|---|---|
| MTA9ASF2G72AZ-3G2__ | 16GB | 2 Gig x 72 | 25.6 GB/s | 0.625ns/3200 MT/s | 22-22-22 |

Notes: 1. The data sheet for the base device can be found at micron.com.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MTA9ASF2G72AZ-3G2B1.


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# Pin Assignments

The pin assignment table below is a comprehensive list of all possible pin assignments for DDR4 UDIMM modules. See Functional Block Diagram for pins specific to this module.

**Table 4: Pin Assignments**

| 288-Pin DDR4 UDIMM Front | | | | | | | | 288-Pin DDR4 UDIMM Back | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1 | NC | 37 | $V_{SS}$ | 73 | $V_{DD}$ | 109 | $V_{SS}$ | 145 | NC | 181 | DQ29 | 217 | $V_{DD}$ | 253 | DQ41 |
| 2 | $V_{SS}$ | 38 | DQ24 | 74 | CK0_t | 110 | DM5_n/ DBI5_n, NC | 146 | $V_{REFCA}$ | 182 | $V_{SS}$ | 218 | CK1_t | 254 | $V_{SS}$ |
| 3 | DQ4 | 39 | $V_{SS}$ | 75 | CK0_c | 111 | NC | 147 | $V_{SS}$ | 183 | DQ25 | 219 | CK1_c | 255 | DQS5_c |
| 4 | $V_{SS}$ | 40 | DM3_n/ DBI3_n, NC | 76 | $V_{DD}$ | 112 | $V_{SS}$ | 148 | DQ5 | 184 | $V_{SS}$ | 220 | $V_{DD}$ | 256 | DQS5_t |
| 5 | DQ0 | 41 | NC | 77 | $V_{TT}$ | 113 | DQ46 | 149 | $V_{SS}$ | 185 | DQS3_c | 221 | $V_{TT}$ | 257 | $V_{SS}$ |
| 6 | $V_{SS}$ | 42 | $V_{SS}$ | 78 | EVENT_n, NF | 114 | $V_{SS}$ | 150 | DQ1 | 186 | DQS3_t | 222 | PARITY | 258 | DQ47 |
| 7 | DM0_n/ DBI0_n, NC | 43 | DQ30 | 79 | A0 | 115 | DQ42 | 151 | $V_{SS}$ | 187 | $V_{SS}$ | 223 | $V_{DD}$ | 259 | $V_{SS}$ |
| 8 | NC | 44 | $V_{SS}$ | 80 | $V_{DD}$ | 116 | $V_{SS}$ | 152 | DQS0_c | 188 | DQ31 | 224 | BA1 | 260 | DQ43 |
| 9 | $V_{SS}$ | 45 | DQ26 | 81 | BA0 | 117 | DQ52 | 153 | DQS0_t | 189 | $V_{SS}$ | 225 | A10_AP | 261 | $V_{SS}$ |
| 10 | DQ6 | 46 | $V_{SS}$ | 82 | RAS_n/ A16 | 118 | $V_{SS}$ | 154 | $V_{SS}$ | 190 | DQ27 | 226 | $V_{DD}$ | 262 | DQ53 |
| 11 | $V_{SS}$ | 47 | CB4/ NC | 83 | $V_{DD}$ | 119 | DQ48 | 155 | DQ7 | 191 | $V_{SS}$ | 227 | NC | 263 | $V_{SS}$ |
| 12 | DQ2 | 48 | $V_{SS}$ | 84 | CS0_n | 120 | $V_{SS}$ | 156 | $V_{SS}$ | 192 | CB5, NC | 228 | WE_n/ A14 | 264 | DQ49 |
| 13 | $V_{SS}$ | 49 | CB0/ NC | 85 | $V_{DD}$ | 121 | DM6_n/ DBI6_n, NC | 157 | DQ3 | 193 | $V_{SS}$ | 229 | $V_{DD}$ | 265 | $V_{SS}$ |
| 14 | DQ12 | 50 | $V_{SS}$ | 86 | CAS_n/ A15 | 122 | NC | 158 | $V_{SS}$ | 194 | CB1, NC | 230 | NC | 266 | DQS6_c |
| 15 | $V_{SS}$ | 51 | DM8_n/ DBI8_n, NC | 87 | ODT0 | 123 | $V_{SS}$ | 159 | DQ13 | 195 | $V_{SS}$ | 231 | $V_{DD}$ | 267 | DQS6_t |
| 16 | DQ8 | 52 | NC | 88 | $V_{DD}$ | 124 | DQ54 | 160 | $V_{SS}$ | 196 | DQS8_c | 232 | A13 | 268 | $V_{SS}$ |
| 17 | $V_{SS}$ | 53 | $V_{SS}$ | 89 | CS1_n, NC | 125 | $V_{SS}$ | 161 | DQ9 | 197 | DQS8_t | 233 | $V_{DD}$ | 269 | DQ55 |
| 18 | DMI_n/ DBI1_n, NC | 54 | CB6/ DBI8_n, NC | 90 | $V_{DD}$ | 126 | DQ50 | 162 | $V_{SS}$ | 198 | $V_{SS}$ | 234 | NC | 270 | $V_{SS}$ |
| 19 | NC | 55 | $V_{SS}$ | 91 | ODT1, NC | 127 | $V_{SS}$ | 163 | DQS1_c | 199 | CB7, NC | 235 | NC | 271 | DQ51 |
| 20 | $V_{SS}$ | 56 | CB2/ NC | 92 | $V_{DD}$ | 128 | DQ60 | 164 | DQS1_t | 200 | $V_{SS}$ | 236 | $V_{DD}$ | 272 | $V_{SS}$ |
| 21 | DQ14 | 57 | $V_{SS}$ | 93 | NC | 129 | $V_{SS}$ | 165 | $V_{SS}$ | 201 | CB3, NC | 237 | NC | 273 | DQ61 |
| 22 | $V_{SS}$ | 58 | RESET_n | 94 | $V_{SS}$ | 130 | DQ56 | 166 | DQ15 | 202 | $V_{SS}$ | 238 | SA2 | 274 | $V_{SS}$ |
| 23 | DQ10 | 59 | $V_{DD}$ | 95 | DQ36 | 131 | $V_{SS}$ | 167 | $V_{SS}$ | 203 | CKE1, NC | 239 | $V_{SS}$ | 275 | DQ57 |


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**Table 4: Pin Assignments (Continued)**

| 288-Pin DDR4 UDIMM Front | | | | | | | | 288-Pin DDR4 UDIMM Back | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 24 | $V_{SS}$ | 60 | CKE0 | 96 | $V_{SS}$ | 132 | DM7_n/ DBI7_n, NC | 168 | DQ11 | 204 | $V_{DD}$ | 240 | DQ37 | 276 | $V_{SS}$ |
| 25 | DQ20 | 61 | $V_{DD}$ | 97 | DQ32 | 133 | NC | 169 | $V_{SS}$ | 205 | NC | 241 | $V_{SS}$ | 277 | DQS7_c |
| 26 | $V_{SS}$ | 62 | ACT_n | 98 | $V_{SS}$ | 134 | $V_{SS}$ | 170 | DQ21 | 206 | $V_{DD}$ | 242 | DQ33 | 278 | DQS7_t |
| 27 | DQ16 | 63 | BG0 | 99 | DM4_n/ DBI4_n, NC | 135 | DQ62 | 171 | $V_{SS}$ | 207 | BG1 | 243 | $V_{SS}$ | 279 | $V_{SS}$ |
| 28 | $V_{SS}$ | 64 | $V_{DD}$ | 100 | NC | 136 | $V_{SS}$ | 172 | DQ17 | 208 | ALERT_n | 244 | DQS4_c | 280 | DQ63 |
| 29 | DM2_n/ DBI2_n, NC | 65 | A12/BC_n | 101 | $V_{SS}$ | 137 | DQ58 | 173 | $V_{SS}$ | 209 | $V_{DD}$ | 245 | DQS4_t | 281 | $V_{SS}$ |
| 30 | NC | 66 | A9 | 102 | DQ38 | 138 | $V_{SS}$ | 174 | DQS2_c | 210 | A11 | 246 | $V_{SS}$ | 282 | DQ59 |
| 31 | $V_{SS}$ | 67 | $V_{DD}$ | 103 | $V_{SS}$ | 139 | SA0 | 175 | DQS2_t | 211 | A7 | 247 | DQ39 | 283 | $V_{SS}$ |
| 32 | DQ22 | 68 | A8 | 104 | DQ34 | 140 | SA1 | 176 | $V_{SS}$ | 212 | $V_{DD}$ | 248 | $V_{SS}$ | 284 | $V_{DDSPD}$ |
| 33 | $V_{SS}$ | 69 | A6 | 105 | $V_{SS}$ | 141 | SCL | 177 | DQ23 | 213 | A5 | 249 | DQ35 | 285 | SDA |
| 34 | DQ18 | 70 | $V_{DD}$ | 106 | DQ44 | 142 | $V_{PP}$ | 178 | $V_{SS}$ | 214 | A4 | 250 | $V_{SS}$ | 286 | $V_{PP}$ |
| 35 | $V_{SS}$ | 71 | A3 | 107 | $V_{SS}$ | 143 | $V_{PP}$ | 179 | DQ19 | 215 | $V_{DD}$ | 251 | DQ45 | 287 | $V_{PP}$ |
| 36 | DQ28 | 72 | A1 | 108 | DQ40 | 144 | NC | 180 | $V_{SS}$ | 216 | A2 | 252 | $V_{SS}$ | 288 | $V_{PP}$ |


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# Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for DDR4 modules. All pins listed may not be supported on this module. See Functional Block Diagram for pins specific to this module.

**Table 5: Pin Descriptions**

| Symbol | Type | Description |
|---|---|---|
| Ax | Input | **Address inputs:** Provide the row address for ACTIVATE commands and the column address for READ/WRITE commands in order to select one location out of the memory array in the respective bank (A10/AP, A12/BC_n, WE_n/A14, CAS_n/A15, and RAS_n/A16 have additional functions; see individual entries in this table). The address inputs also provide the op-code during the MODE REGISTER SET command. A17 is only defined for x4 SDRAM. |
| A10/AP | Input | **Auto precharge:** A10 is sampled during READ and WRITE commands to determine whether an auto precharge should be performed on the accessed bank after a READ or WRITE operation (HIGH = auto precharge; LOW = no auto precharge). A10 is sampled during a PRECHARGE command to determine whether the precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by the bank group and bank addresses. |
| A12/BC_n | Input | **Burst chop:** A12/BC_n is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH = no burst chop; LOW = burst chopped). See Command Truth Table in the DDR4 component data sheet. |
| ACT_n | Input | **Command input:** ACT_n defines the ACTIVATE command being entered along with CS_n. The input into RAS_n/A16, CAS_n/A15, and WE_n/A14 are considered as row address A16, A15, and A14. See Command Truth Table. |
| BAx | Input | **Bank address inputs:** Define the bank (with a bank group) to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. |
| BGx | Input | **Bank group address inputs:** Define the bank group to which a REFRESH, ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. Also determine which mode register is to be accessed during a MODE REGISTER SET command. BG[1:0] are used in the x4 and x8 configurations. x16-based SDRAM only has BG0. |
| C0, C1, C2 (RDIMM/LRDIMM only) | Input | **Chip ID:** These inputs are used only when devices are stacked; that is, 2H, 4H, and 8H stacks for x4 and x8 configurations using through-silicon vias (TSVs). These pins are not used in the x16 configuration. Some DDR4 modules support a traditional DDP package, which uses CS1_n, CKE1, and ODT1 to control the second die. All other stack configurations, such as a 4H or 8H, are assumed to be single-load (master/slave) type configurations where C0, C1, and C2 are used as chip ID selects in conjunction with a single CS_n, CKE, and ODT. Chip ID is considered part of the command code. |
| CKx_t<br>CKx_c | Input | **Clock:** Differential clock inputs. All address, command, and control input signals are sampled on the crossing of the positive edge of CK_t and the negative edge of CK_c. |
| CKEx | Input | **Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, device input buffers, and output drivers. Taking CKE LOW provides PRECHARGE POWER-DOWN and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is asynchronous for self refresh exit. After $V_{REFCA}$ has become stable during the power-on and initialization sequence, it must be maintained during all operations (including SELF REFRESH). CKE must be maintained HIGH throughout read and write accesses. Input buffers (excluding CK_t, CK_c, ODT, RESET_n, and CKE) are disabled during power-down. Input buffers (excluding CKE and RESET_n) are disabled during self refresh. |
| CSx_n | Input | **Chip select:** All commands are masked when CS_n is registered HIGH. CS_n provides external rank selection on systems with multiple ranks. CS_n is considered part of the command code (CS2_n and CS3_n are not used on UDIMMs). |


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**Table 5: Pin Descriptions (Continued)**

| Symbol | Type | Description |
|---|---|---|
| ODTx | Input | **On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR4 SDRAM. When enabled, ODT ($R_{TT}$) is applied only to each DQ, DQS_t, DQS_c, DM_n/DBI_n/TDQS_t, and TDQS_c signal for x4 and x8 configurations (when the TDQS function is enabled via the mode register). For the x16 configuration, $R_{TT}$ is applied to each DQ, DQSU_t, DQSU_c, DQSL_t, DQSL_c, UDM_n, and LDM_n signal. The ODT pin will be ignored if the mode registers are programmed to disable $R_{TT}$. |
| PARITY | Input | **Parity for command and address:** This function can be enabled or disabled via the mode register. When enabled in MR5, the DRAM calculates parity with ACT_n, RAS_n/A16, CAS_n/A15, WE_n/A14, BG[1:0], BA[1:0], A[16:0]. Input parity should be maintained at the rising edge of the clock and at the same time as command and address with CS_n LOW. |
| RAS_n/A16<br>CAS_n/A15<br>WE_n/A14 | Input | **Command inputs:** RAS_n/A16, CAS_n/A15, and WE_n/A14 (along with CS_n) define the command and/or address being entered and have multiple functions. For example, for activation with ACT_n LOW, these are addresses like A16, A15, and A14, but for a non-activation command with ACT_n HIGH, these are command pins for READ, WRITE, and other commands defined in Command Truth Table. |
| RESET_n | CMOS Input | **Active LOW asynchronous reset:** Reset is active when RESET_n is LOW and inactive when RESET_n is HIGH. RESET_n must be HIGH during normal operation. |
| SAx | Input | **Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the $I^2C$ bus. |
| SCL | Input | **Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the $I^2C$ bus. |
| DQx, CBx | I/O | **Data input/output and check bit input/output:** Bidirectional data bus. DQ represents DQ[3:0], DQ[7:0], and DQ[15:0] for the x4, x8, and x16 configurations, respectively. If cyclic redundancy checksum (CRC) is enabled via the mode register, the CRC code is added at the end of the data burst. Any one or all of DQ0, DQ1, DQ2, or DQ3 may be used for monitoring of internal $V_{REF}$ level during test via mode register setting MR[4] A[4] = HIGH; training times change when enabled. |
| DM_n/DBI_n/<br>TDQS_t (DMU_n,<br>DBIU_n), (DML_n/<br>DBIl_n) | I/O | **Input data mask and data bus inversion:** DM_n is an input mask signal for write data. Input data is masked when DM_n is sampled LOW coincident with that input data during a write access. DM_n is sampled on both edges of DQS. DM is multiplexed with the DBI function by the mode register A10, A11, and A12 settings in MR5. For a x8 device, the function of DM or TDQS is enabled by the mode register A11 setting in MR1. DBI_n is an input/output identifying whether to store/output the true or inverted data. If DBI_n is LOW, the data will be stored/output after inversion inside the DDR4 device and not inverted if DBI_n is HIGH. TDQS is only supported in x8 SDRAM configurations (TDQS is not valid for UDIMMs). |
| SDA | I/O | **Serial Data:** Bidirectional signal used to transfer data in or out of the EEPROM or EEPROM/TS combo device. |
| DQS_t<br>DQS_c<br>DQSU_t<br>DQSU_c<br>DQSL_t<br>DQSL_c | I/O | **Data strobe:** Output with read data, input with write data. Edge-aligned with read data, centered-aligned with write data. For x16 configurations, DQSL corresponds to the data on DQ[7:0], and DQSU corresponds to the data on DQ[15:8]. For the x4 and x8 configurations, DQS corresponds to the data on DQ[3:0] and DQ[7:0], respectively. DDR4 SDRAM supports a differential data strobe only and does not support a single-ended data strobe. |
| ALERT_n | Output | **Alert output:** Possesses functions such as CRC error flag and command and address parity error flag as output signal. If a CRC error occurs, ALERT_n goes LOW for the period time interval and returns HIGH. If an error occurs during a command address parity check, ALERT_n goes LOW until the on-going DRAM internal recovery transaction is complete. During connectivity test mode, this pin functions as an input. Use of this signal is system-dependent. If not connected as signal, ALERT_n pin must be connected to $V_{DD}$ on DIMMs. |
| EVENT_n | Output | **Temperature event:** The EVENT_n pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. This pin has no function (NF) on modules without temperature sensors. |


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**Table 5: Pin Descriptions (Continued)**

| Symbol | Type | Description |
|---|---|---|
| TDQS_t<br>TDQS_c<br><br>(x8 DRAM-based RDIMM only) | Output | **Termination data strobe:** When enabled via the mode register, the DRAM device enables the same $R_{TT}$ termination resistance on TDQS_t and TDQS_c that is applied to DQS_t and DQS_c. When the TDQS function is disabled via the mode register, the DM/TDQS_t pin provides the data mask (DM) function, and the TDQS_c pin is not used. The TDQS function must be disabled in the mode register for both the x4 and x16 configurations. The DM function is supported only in x8 and x16 configurations. DM, DBI, and TDQS are a shared pin and are enabled/disabled by mode register settings. For more information about TDQS, see the DDR4 DRAM component data sheet (TDQS_t and TDQS_c are not valid for UDIMMs). |
| $V_{DD}$ | Supply | **Module power supply:** 1.2V (TYP). |
| $V_{PP}$ | Supply | **DRAM activating power supply:** 2.5V –0.125V/+0.250V. |
| $V_{REFCA}$ | Supply | Reference voltage for control, command, and address pins. |
| $V_{SS}$ | Supply | Ground. |
| $V_{TT}$ | Supply | Power supply for termination of address, command, and control $V_{DD}/2$. |
| $V_{DDSPD}$ | Supply | Power supply used to power the $I^2C$ bus for SPD. |
| RFU | – | Reserved for future use. |
| NC | – | **No connect:** No internal electrical connection is present. |
| NF | – | **No function:** May have internal connection present, but has no function. |


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# DQ Map

**Table 6: Component-to-Module DQ Map**

| Component Reference Number | Component DQ | Module DQ | Module Pin Number | Component Reference Number | Component DQ | Module DQ | Module Pin Number |
|---|---|---|---|---|---|---|---|
| U1 | 0 | 3 | 157 | U2 | 0 | 11 | 168 |
| | 1 | 1 | 150 | | 1 | 9 | 161 |
| | 2 | 2 | 12 | | 2 | 10 | 23 |
| | 3 | 0 | 5 | | 3 | 8 | 16 |
| | 4 | 7 | 155 | | 4 | 15 | 166 |
| | 5 | 5 | 148 | | 5 | 13 | 159 |
| | 6 | 6 | 10 | | 6 | 14 | 21 |
| | 7 | 4 | 3 | | 7 | 12 | 14 |
| U3 | 0 | 19 | 179 | U4 | 0 | 27 | 190 |
| | 1 | 17 | 172 | | 1 | 25 | 183 |
| | 2 | 18 | 34 | | 2 | 26 | 45 |
| | 3 | 16 | 27 | | 3 | 24 | 38 |
| | 4 | 23 | 177 | | 4 | 31 | 188 |
| | 5 | 21 | 170 | | 5 | 29 | 181 |
| | 6 | 22 | 32 | | 6 | 30 | 43 |
| | 7 | 20 | 28 | | 7 | 28 | 36 |
| U5 | 0 | CB3 | 201 | U6 | 0 | 35 | 249 |
| | 1 | CB1 | 194 | | 1 | 33 | 242 |
| | 2 | CB2 | 56 | | 2 | 34 | 104 |
| | 3 | CB0 | 49 | | 3 | 32 | 97 |
| | 4 | CB7 | 199 | | 4 | 39 | 247 |
| | 5 | CB5 | 192 | | 5 | 37 | 240 |
| | 6 | CB6 | 54 | | 6 | 38 | 102 |
| | 7 | CB4 | 47 | | 7 | 36 | 95 |
| U7 | 0 | 43 | 260 | U8 | 0 | 51 | 271 |
| | 1 | 41 | 253 | | 1 | 49 | 264 |
| | 2 | 42 | 115 | | 2 | 50 | 126 |
| | 3 | 40 | 108 | | 3 | 48 | 119 |
| | 4 | 47 | 258 | | 4 | 55 | 269 |
| | 5 | 45 | 251 | | 5 | 53 | 262 |
| | 6 | 46 | 113 | | 6 | 54 | 124 |
| | 7 | 44 | 106 | | 7 | 52 | 117 |


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**Table 6: Component-to-Module DQ Map (Continued)**

| Component Reference Number | Component DQ | Module DQ | Module Pin Number | Component Reference Number | Component DQ | Module DQ | Module Pin Number |
|---|---|---|---|---|---|---|---|
| U9 | 0 | 59 | 282 | | | | |
| | 1 | 57 | 275 | | | | |
| | 2 | 58 | 137 | | | | |
| | 3 | 56 | 130 | | | | |
| | 4 | 63 | 280 | | | | |
| | 5 | 61 | 273 | | | | |
| | 6 | 62 | 135 | | | | |
| | 7 | 60 | 128 | | | | |


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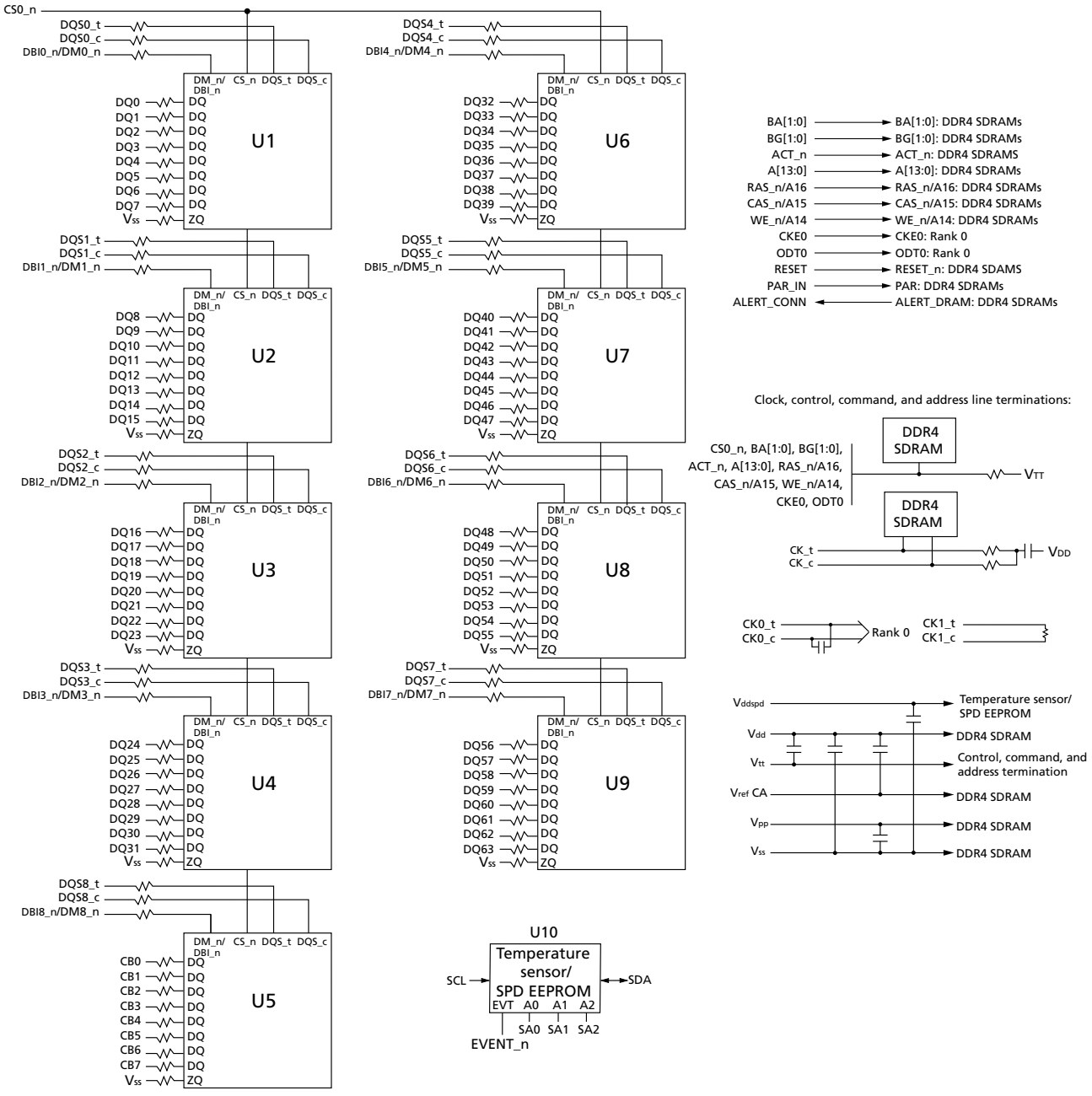
# Functional Block Diagram

### Figure 2: Functional Block Diagram




Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.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# General Description

High-speed DDR4 SDRAM modules use DDR4 SDRAM devices with two or four internal memory bank groups. DDR4 SDRAM modules utilizing 4- and 8-bit-wide DDR4 SDRAM devices have four internal bank groups consisting of four memory banks each, providing a total of 16 banks. 16-bit-wide DDR4 SDRAM devices have two internal bank groups consisting of four memory banks each, providing a total of eight banks. DDR4 SDRAM modules benefit from DDR4 SDRAM's use of an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE operation for the DDR4 SDRAM effectively consists of a single 8*n*-bit-wide, four-clock data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR4 modules use two sets of differential signals: DQS_t and DQS_c to capture data and CK_t and CK_c to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

## Fly-By Topology

DDR4 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR4.

## Module Manufacturing Location

Micron Technology manufactures modules at sites world-wide. Customers may receive modules from any of the following manufacturing locations:

**Table 7: DRAM Module Manufacturing Locations**

| Manufacturing Site Location | Country of Origin Specified on Label |
|---|---|
| Boise, USA | USA |
| Aguadilla, Puerto Rico | Puerto Rico |
| Xian, China | China |
| Singapore | Singapore |


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# Address Mapping to DRAM

## Address Mirroring

To achieve optimum routing of the address bus on DDR4 multi rank modules, the address bus will be wired as shown in the table below, or mirrored. For quad rank modules, ranks 1 and 3 are mirrored and ranks 0 and 2 are non-mirrored. Highlighted address pins have no secondary functions allowing for normal operation when cross-wired. Data is still read from the same address it was written. However, Load Mode operations require a specific address. This requires the controller to accommodate for a rank that is "mirrored." Systems may reference DDR4 SPD to determine if the module has mirroring implemented or not. See the JEDEC DDR4 SPD specification for more details.

**Table 8: Address Mirroring**

| Edge Connector Pin | DRAM Pin, Non-mirrored | DRAM Pin, Mirrored |
|---|---|---|
| A0 | A0 | A0 |
| A1 | A1 | A1 |
| A2 | A2 | A2 |
| A3 | A3 | A4 |
| A4 | A4 | A3 |
| A5 | A5 | A6 |
| A6 | A6 | A5 |
| A7 | A7 | A8 |
| A8 | A8 | A7 |
| A9 | A9 | A9 |
| A10 | A10 | A10 |
| A11 | A11 | A13 |
| A13 | A13 | A11 |
| A12 | A12 | A12 |
| A14 | A14 | A14 |
| A15 | A15 | A15 |
| A16 | A16 | A16 |
| A17 | A17 | A17 |
| BA0 | BA0 | BA1 |
| BA1 | BA1 | BA0 |
| BG0 | BG0 | BG1 |
| BG1 | BG1 | BG0 |


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# Temperature Sensor with SPD EEPROM Operation

## Thermal Sensor Operations

The integrated thermal sensor continuously monitors the temperature of the module PCB directly below the device and updates the temperature data register. Temperature data may be read from the bus host at any time, which provides the host real-time feedback of the module's temperature. Multiple programmable and read-only temperature registers can be used to create a custom temperature-sensing solution based on system requirements and JEDEC JC-42.2.

## EVENT_n Pin

The temperature sensor also adds the EVENT_n pin (open-drain), which requires a pull-up to $V_{DDSPD}$. EVENT_n is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration registers. EVENT_n is not used by the serial presence-detect (SPD) EEPROM.

EVENT_n has three defined modes of operation: interrupt, comparator, and TCRIT. In interrupt mode, the EVENT_n pin remains asserted until it is released by writing a 1 to the clear event bit in the status register. In comparator mode, the EVENT_n pin clears itself when the error condition is removed. Comparator mode is always used when the temperature is compared against the TCRIT limit. In TCRIT only mode, the EVENT_n pin is only asserted if the measured temperature exceeds the TCRIT limit; it then remains asserted until the temperature drops below the TCRIT limit minus the TCRIT hysteresis.

## SPD EEPROM Operation

DDR4 SDRAM modules incorporate SPD. The SPD data is stored in a 512-byte, JEDEC JC-42.4-compliant EEPROM that is segregated into four 128-byte, write-protectable blocks. The SPD content is aligned with these blocks as shown in the table below.

| Block | Range | | Description |
|---|---|---|---|
| 0 | 0–127 | 000h–07Fh | Configuration and DRAM parameters |
| 1 | 128–255 | 080h–0FFh | Module parameters |
| 2 | 256–319 | 100h–13Fh | Reserved (all bytes coded as 00h) |
| | 320–383 | 140h–17Fh | Manufacturing information |
| 3 | 384–511 | 180h–1FFh | End-user programmable |

The first 384 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR4 SDRAM Modules." The remaining 128 bytes of storage are available for use by the customer.

The EEPROM resides on a two-wire $I^2C$ serial interface and is not integrated with the memory bus in any manner. It operates as a slave device in the $I^2C$ bus protocol, with all operations synchronized by the serial clock. Transfer rates of up to 1 MHz are achievable at 2.5V (NOM).

Micron implements reversible software write protection on DDR4 SDRAM-based modules. This prevents the lower 384 bytes (bytes 0 to 383) from being inadvertently programmed or corrupted. The upper 128 bytes remain available for customer use and are unprotected.


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# Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 9: Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Units | Notes |
|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ supply voltage relative to $V_{SS}$ | –0.4 | 1.5 | V | 1 |
| $V_{DDQ}$ | $V_{DDQ}$ supply voltage relative to $V_{SS}$ | –0.4 | 1.5 | V | 1 |
| $V_{PP}$ | Voltage on $V_{PP}$ pin relative to $V_{SS}$ | –0.4 | 3.0 | V | 2 |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | –0.4 | 1.5 | V | |

**Table 10: Operating Conditions**

| Symbol | Parameter | Min | Nom | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ supply voltage | 1.14 | 1.2 | 1.26 | V | 1 |
| $V_{PP}$ | DRAM activating power supply | 2.375 | 2.5 | 2.75 | V | 2 |
| $V_{REFCA(DC)}$ | Input reference voltage command/ address bus | 0.49 × $V_{DD}$ | 0.5 × $V_{DD}$ | 0.51 × $V_{DD}$ | V | 3 |
| $I_{VTT}$ | Termination reference current from $V_{TT}$ | –750 | – | 750 | mA | |
| $V_{TT}$ | Termination reference voltage (DC) – command/address bus | 0.49 × $V_{DD}$ - 20mV | 0.5 × $V_{DD}$ | 0.51 × $V_{DD}$ + 20mV | V | 4 |
| $I_{IN}$ | Input leakage current; any input excluding ZQ; 0V < $V_{IN}$ < 1.1V | –2.0 | – | 2.0 | µA | 5 |
| $I_{ZQ}$ | Input leakage current; ZQ | –50.0 | – | 10.0 | µA | 5, 6 |
| $I_{OZpd}$ | Output leakage current; $V_{OUT}$ = $V_{DD}$; DQ is High-Z | – | – | 10.0 | µA | 7 |
| $I_{OZpu}$ | Output leakage current; $V_{OUT}$ = $V_{SS}$; DQ is High-Z; ODT is disabled with ODT input HIGH | –50.0 | – | – | µA | 7 |
| $I_{VREFCA}$ | $V_{REFCA}$ leakage; $V_{REFCA}$ = $V_{DD}$/2 (after DRAM is initialized) | –2.0 | – | 2.0 | µA | 5 |

Notes:
1. $V_{DDQ}$ tracks with $V_{DD}$; $V_{DDQ}$ and $V_{DD}$ are tied together.
2. $V_{PP}$ must be greater than or equal to $V_{DD}$ at all times.
3. $V_{REFCA}$ must not be greater than 0.6 x $V_{DD}$. When $V_{DD}$ is less than 500mV, $V_{REF}$ may be less than or equal to 300mV.
4. $V_{TT}$ termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.
5. Multiply by the number of DRAM die on the module.
6. Tied to ground. Not connected to edge connector.
7. Multiply by the number of module ranks and then times the number of die per package.


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**Table 11: Thermal Characteristics**

| Symbol | Parameter/Condition | Value | Units | Notes |
|---|---|---|---|---|
| $T_C$ | Commercial operating case temperature | 0 to 85 | °C | 1, 2, 3 |
| $T_C$ | | >85 to 95 | °C | 1, 2, 3, 4 |
| $T_{OPER}$ | Normal operating temperature range | 0 to 85 | °C | 5, 7 |
| $T_{OPER}$ | Extended temperature operating range (optional) | >85 to 95 | °C | 5, 7 |
| $T_{STG}$ | Non-operating storage temperature | –55 to 100 | °C | 6 |
| $RH_{STG}$ | Non-operating Storage Relative Humidity (non-condensing) | 5 to 95 | % | |
| NA | Change Rate of Storage Temperature | 20 | °C/hour | |

Notes:
1. Maximum operating case temperature; $T_C$ is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum $T_C$ during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum $T_C$ during operation.
4. If $T_C$ exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 3.9µs interval refresh rate.
5. The refresh rate must double when 85°C < $T_{OPER}$ ≤ 95°C.
6. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.
7. For additional information, refer to technical note TN-00-08: "Thermal Applications" available at micron.com.


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# DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR4 component data sheets. Component specifications are available at micron.com. Module speed grades correlate with component speed grades, as shown below.

**Table 12: Module and Component Speed Grades**

DDR4 components may exceed the listed module speed grades; module may not be available in all listed speed grades

| Module Speed Grade | Component Speed Grade |
|---|---|
| -3G2 | -062E |
| -2G9 | -068 |
| -2G6 | -075 |
| -2G3 | -083 |
| -2G1 | -093E |

## Design Considerations

### Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

### Power

Operating voltages are specified at the edge connector of the module, not at the DRAM. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.

### $I_{DD}$, $I_{PP}$, and $I_{DDQ}$ Specifications

$I_{DD}$ and $I_{PP}$ values are only for the DDR4 SDRAM, and calculated from values in the supporting component data sheet. $I_{PP}$ and $I_{DDQ}$ currents are not included in $I_{DD}$ currents. $I_{DD}$ and $I_{DDQ}$ currents are not included in $I_{PP}$ currents. Micron does not specify $I_{DDQ}$ currents. In DRAM module application, $I_{DDQ}$ cannot be measured separately because $V_{DD}$ and $V_{DDQ}$ use a merged-power layer in the module PCB.


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# $I_{DD}$ Specifications

### Table 13: DDR4 $I_{DD}$ Specifications and Conditions – 16GB (Die Revision B)

Values are for the MT40A2G8 DDR4 SDRAM only and are computed from values specified in the 16Gb (2 Gig x 8) component data sheet

| Parameter | Symbol | 3200 | Units |
|---|---|---|---|
| One bank ACTIVATE-PRECHARGE current | $I_{DD0}$ | 567 | mA |
| One bank ACTIVATE-PRECHARGE, word line boost, $I_{PP}$ current | $I_{PP0}$ | 36 | mA |
| One bank ACTIVATE-READ-PRECHARGE current | $I_{DD1}$ | 666 | mA |
| Precharge standby current | $I_{DD2N}$ | 468 | mA |
| Precharge standby ODT current | $I_{DD2NT}$ | 504 | mA |
| Precharge power-down current | $I_{DD2P}$ | 387 | mA |
| Precharge quite standby current | $I_{DD2Q}$ | 423 | mA |
| Active standby current | $I_{DD3N}$ | 720 | mA |
| Active standby $I_{PP}$ current | $I_{PP3N}$ | 27 | mA |
| Active power-down current | $I_{DD3P}$ | 621 | mA |
| Burst read current | $I_{DD4R}$ | 1818 | mA |
| Burst write current | $I_{DD4W}$ | 1647 | mA |
| Burst refresh current (1x REF) | $I_{DD5R}$ | 729 | mA |
| Burst refresh $I_{PP}$ current (1x REF) | $I_{PP5R}$ | 45 | mA |
| Self refresh current: Normal temperature range (0°C to 85°C) | $I_{DD6N}$ | 666 | mA |
| Self refresh current: Extended temperature range (0°C to 95°C) | $I_{DD6E}$ | 1161 | mA |
| Self refresh current: Reduced temperature range (0°C to 45°C) | $I_{DD6R}$ | 234 | mA |
| Auto self refresh current (25°C) | $I_{DD6A}$ | 135 | mA |
| Auto self refresh current (45°C) | $I_{DD6A}$ | 234 | mA |
| Auto self refresh current (75°C) | $I_{DD6A}$ | 657 | mA |
| Auto self refresh current (95°C) | $I_{DD6A}$ | 1161 | mA |
| Auto self refresh $I_{PP}$ current | $I_{PP6X}$ | 81 | mA |
| Bank interleave read current | $I_{DD7}$ | 1764 | mA |
| Bank interleave read $I_{PP}$ current | $I_{PP7}$ | 90 | mA |
| Maximum power-down current | $I_{DD8}$ | 360 | mA |


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# Temperature Sensor with SPD EEPROM

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the $I^2C$ bus shared with the serial presence-detect (SPD) EEPROM. Refer to JEDEC JC-42.4 EE1004 and TSE2004 device specifications for complete details.

## SPD Data

For the latest SPD data, refer to Micron's SPD page: micron.com/SPD.

**Table 14: Temperature Sensor with SPD EEPROM Operating Conditions**

| Parameter/Condition | Symbol | Min | Nom | Max | Units |
|---|---|---|---|---|---|
| Supply voltage | $V_{DDSPD}$ | 1.7 | 2.5 | 3.3 | V |
| Input low voltage: logic 0; all inputs | $V_{IL}$ | –0.5 | – | $V_{DDSPD}$ × 0.3 | V |
| Input high voltage: logic 1; all inputs | $V_{IH}$ | $V_{DDSPD}$ × 0.7 | – | $V_{DDSPD}$ + 0.5 | V |
| Output low voltage: 3mA sink current $V_{DDSPD}$ > 2V | $V_{OL}$ | – | – | 0.4 | V |
| Input leakage current: (SCL, SDA) $V_{IN}$ = $V_{DDSPD}$ or $V_{SSSPD}$ | $I_{LI}$ | – | – | ±5 | µA |
| Output leakage current: $V_{OUT}$ = $V_{DDSPD}$ or $V_{SSSPD}$, SDA in High-Z | $I_{LO}$ | – | – | ±5 | µA |

Notes:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 TSE2004 device specifications for complete details.
2. Operation at $^tSCL$ > 100 kHz may require $V_{DDSPD}$ ≤ 2.2.
3. All voltages referenced to $V_{DDSPD}$.

**Table 15: Temperature Sensor and EEPROM Serial Interface Timing**

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Clock frequency | $^fSCL$ | 10 | 1000 | kHz |
| Clock pulse width HIGH time | $^tHIGH$ | 260 | – | ns |
| Clock pulse width LOW time | $^tLOW$ | 500 | – | ns |
| Detect clock LOW timeout | $^tTIMEOUT$ | 25 | 35 | ms |
| SDA rise time | $^tR$ | – | 120 | ns |
| SDA fall time | $^tF$ | – | 120 | ns |
| Data-in setup time | $^tSU:DAT$ | 50 | – | ns |
| Data-in hold time | $^tHD:DI$ | 0 | – | ns |
| Data out hold time | $^tHD:DAT$ | 0 | 350 | ns |
| Start condition setup time | $^tSU:STA$ | 260 | – | ns |
| Start condition hold time | $^tHD:STA$ | 260 | – | ns |
| Stop condition setup time | $^tSU:STO$ | 260 | – | ns |
| Time the bus must be free before a new transition can start | $^tBUF$ | 500 | – | ns |
| Write time | $^tW$ | – | 5 | ms |
| Warm power cycle time off | $^tPOFF$ | 1 | – | ms |


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**Table 15: Temperature Sensor and EEPROM Serial Interface Timing (Continued)**

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Time from power-on to first command | $^{t}$INIT | 10 | – | ms |

Notes:
1. Table is provided as a general reference. Consult JEDEC JC-42.4 TSE2004 device specifications for complete details.
2. Operation at $^{t}$SCL > 100 kHz may require $V_{DDSPD}$ ≤ 2.2.


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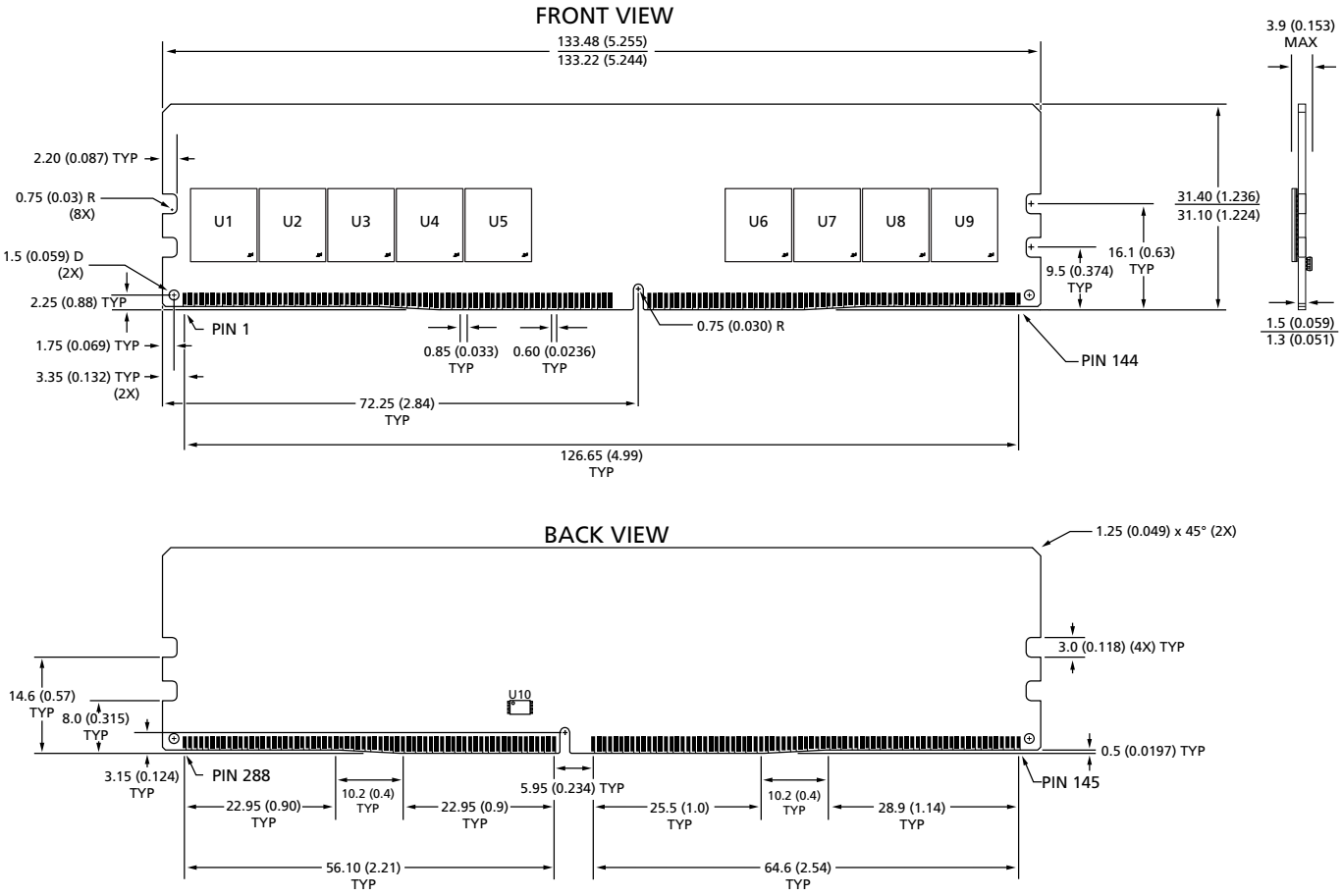
# Module Dimensions

**Figure 3: 288-Pin DDR4 UDIMM**




Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.

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