DDR5 SDRAM RDIMM Addendum

MTC20F104XS1RC – 48GB
24Gb Die Revision B

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR5 RDIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 RDIMM core data sheet
- 288-pin, DDR5 registered dual in-line memory module (DDR5 RDIMM)
- Fast data transfer rate: PC5-4800, PC5-5600, PC5-6400
- 48GB (6 Gig x 80)
- Single-rank
- 32 internal banks; 8 groups of 4 banks each

Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_{OPER} ≤ 95°C)	C
• Frequency/CAS latency	
– 0.416ns @ CL = 40 (DDR5-4800)	48B
– 0.357ns @ CL = 46 (DDR5-5600)	56B
– 0.312ns @ CL = 52 (DDR5-6400)	64B

Figure 1: 288-Pin DDR5 RDIMM (R/C-C0)

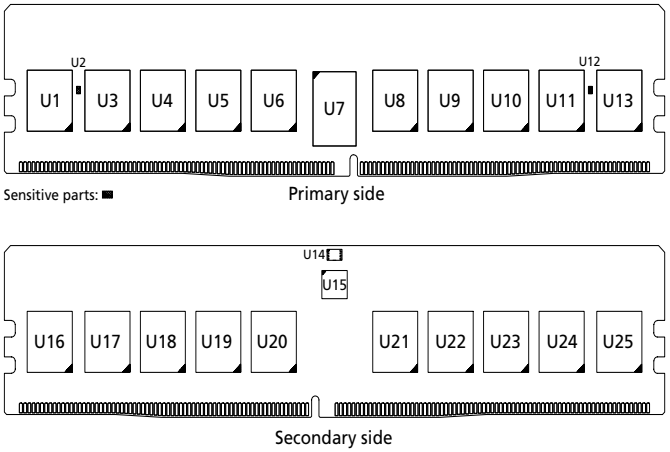

Figure 2: 288-Pin DDR5 RDIMM (R/C-C1)

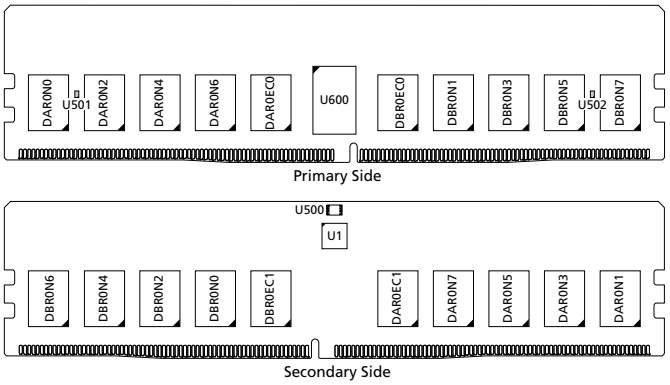

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Table 1: Addressing

Parameter	48GB
Row address[1]	96K (R0-R16)[2]
Column address[1]	2K (C0-C10)
Device bank group address[1]	8 (BG0-BG2)
Device bank address per bank group[1]	4 (BA0-BA1)
Device configuration	24Gb (6Gb x 4), 32 banks
Module rank address	1 (CS0_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.
2. For non-binary densities, a quarter of the row address space is invalid. When the MSB address bit is HIGH, the MSB-1 address shall be LOW.

Table 2: Part Numbers and Timing Parameters – 48GB Modules

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles ($CL-_nRCD-_nRP$)	Designation[2]
MTC20F104XS1RC48BB1	48GB	6Gb x 80 (EC8)	38.4 GB/s	0.416ns/4800 MT/s	40-39-39	Production
MTC20F104XS1RC56BB1	48GB	6Gb x 80 (EC8)	44.8 GB/s	0.357ns/5600 MT/s	46-45-45	Preliminary
MTC20F104XS1RC64BB1	48GB	6Gb x 80 (EC8)	51.2 GB/s	0.312ns/6400 MT/s	52-52-52	Preliminary
MTC20F104XS1RC64BB2	48GB	6Gb x 80 (EC8)	51.2 GB/s	0.312ns/6400 MT/s	52-52-52	Preliminary

Notes: 1. Base device: MT60B6G4, 24Gb DDR5 SDRAM Die Revision B. The data sheet for the base device can be found on micron.com.
2. **Production**: Although considered final, these specifications are subject to change as further product development and data characterization sometimes occur. **Preliminary**: For evaluation and reference purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specifications. **Advance**: Contains initial descriptions of products still under development. For evaluation purposes only and are subject to change by Micron without notice. Products are only warranted by Micron to meet Micron's production data sheet specification.

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DQ Map

Table 3: Component-to-Module DQ Map (R/C-C0)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	3A	154	U3	0	11A	165
	1	0A	7		1	8A	18
	2	1A	9		2	9A	20
	3	2A	152		3	10A	163
U4	0	19A	176	U5	0	27A	187
	1	16A	29		1	24A	40
	2	17A	31		2	25A	42
	3	18A	174		3	26A	185
U6	0	CB3A	198	U8	0	CB3B	243
	1	CB0A	51		1	CB0B	96
	2	CB1A	53		2	CB1B	98
	3	CB2A	196		3	CB2B	241
U9	0	7B	254	U10	0	15B	265
	1	4B	107		1	12B	118
	2	5B	109		2	13B	120
	3	6B	252		3	14B	263
U11	0	23B	276	U13	0	31B	287
	1	20B	129		1	28B	140
	2	21B	131		2	29B	142
	3	22B	274		3	30B	285
U16	0	24B	133	U17	0	16B	122
	1	27B	280		1	19B	269
	2	26B	278		2	18B	267
	3	25B	135		3	17B	124
U18	0	8B	111	U19	0	0B	100
	1	11B	258		1	3B	247
	2	10B	256		2	2B	245
	3	9B	113		3	1B	102
U20	0	CB4B	89	U21	0	CB4A	58
	1	CB7B	236		1	CB7A	205
	2	CB6B	234		2	CB6A	203
	3	CB5B	91		3	CB5A	60

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Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U22	0	28A	47	U23	0	20A	36
	1	31A	194		1	23A	183
	2	30A	192		2	22A	181
	3	29A	49		3	21A	38
U24	0	12A	25	U25	0	4A	14
	1	15A	172		1	7A	161
	2	14A	170		2	6A	159
	3	13A	27		3	5A	16

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Table 4: Component-to-Module DQ Map (R/C-C1)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
DAR0EC0	0	CB3A	198	DAR0EC1	0	CB4A	58
	1	CB0A	51		1	CB7A	205
	2	CB1A	53		2	CB6A	203
	3	CB2A	196		3	CB5A	60
DAR0N0	0	3A	154	DAR0N1	0	4A	14
	1	0A	7		1	7A	161
	2	1A	9		2	6A	159
	3	2A	152		3	5A	16
DAR0N2	0	11A	165	DAR0N3	0	12A	25
	1	8A	18		1	15A	172
	2	9A	20		2	14A	170
	3	10A	163		3	13A	27
DAR0N4	0	19A	176	DAR0N5	0	20A	36
	1	16A	29		1	23A	183
	2	17A	31		2	22A	181
	3	18A	174		3	21A	38
DAR0N6	0	27A	187	DAR0N7	0	28A	47
	1	24A	40		1	31A	194
	2	25A	42		2	30A	192
	3	26A	185		3	29A	49
DBR0EC0	0	CB3B	243	DBR0EC1	0	CB4B	89
	1	CB0B	96		1	CB7B	236
	2	CB1B	98		2	CB6B	234
	3	CB2B	241		3	CB5B	91
DBR0N0	0	0B	100	DBR0N1	0	7B	254
	1	3B	247		1	4B	107
	2	2B	245		2	5B	109
	3	1B	102		3	6B	252
DBR0N2	0	8B	111	DBR0N3	0	15B	265
	1	11B	258		1	12B	118
	2	10B	256		2	13B	120
	3	9B	113		3	14B	263
DBR0N4	0	16B	122	DBR0N5	0	23B	276
	1	19B	269		1	20B	129
	2	18B	267		2	21B	131
	3	17B	124		3	22B	274

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Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
DBR0N6	0	24B	133	DBR0N7	0	31B	287
	1	27B	280		1	28B	140
	2	26B	278		2	29B	142
	3	25B	135		3	30B	285

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I_{DD} Specifications

Table 5: DDR5 I_{DD} Specifications and Conditions – 48GB (Die Revision B)

Module I_{DD} is based on PMIC VIN_BULK 12V input current and typical operating range of temperature. Each I_{DD} parameter includes PMIC efficiency, RCD current and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

Parameter	Symbol	4800	5600	6400	Units
Operating one bank ACTIVATE-PRECHARGE current	I_{DD0}	270	TBD	TBD	mA
Operating four bank ACTIVATE-PRECHARGE current	I_{DD0F}	338	TBD	TBD	mA
Precharge standby current	I_{DD2N}	241	TBD	TBD	mA
Precharge standby non-target command	I_{DD2NT}	315	TBD	TBD	mA
Precharge power-down current	I_{DD2P}	239	TBD	TBD	mA
Active standby current	I_{DD3N}	262	TBD	TBD	mA
Active power-down current	I_{DD3P}	257	TBD	TBD	mA
Operating burst read current	I_{DD4R}	689	TBD	TBD	mA
Operating burst write current	I_{DD4W}	848	TBD	TBD	mA
Operating burst write with write CRC current	I_{DD4WC}	834	TBD	TBD	mA
Burst refresh (normal refresh mode) current	I_{DD5B}	677	TBD	TBD	mA
Burst refresh (fine granularity refresh mode) current	I_{DD5F}	653	TBD	TBD	mA
Burst refresh (same bank refresh mode) current	I_{DD5C}	362	TBD	TBD	mA
Self refresh current	I_{DD6N}	146	TBD	TBD	mA
Operating bank interleave read current	I_{DD7}	963	TBD	TBD	mA
Maximum power saving deep power down mode current	I_{DD8}	203	TBD	TBD	mA

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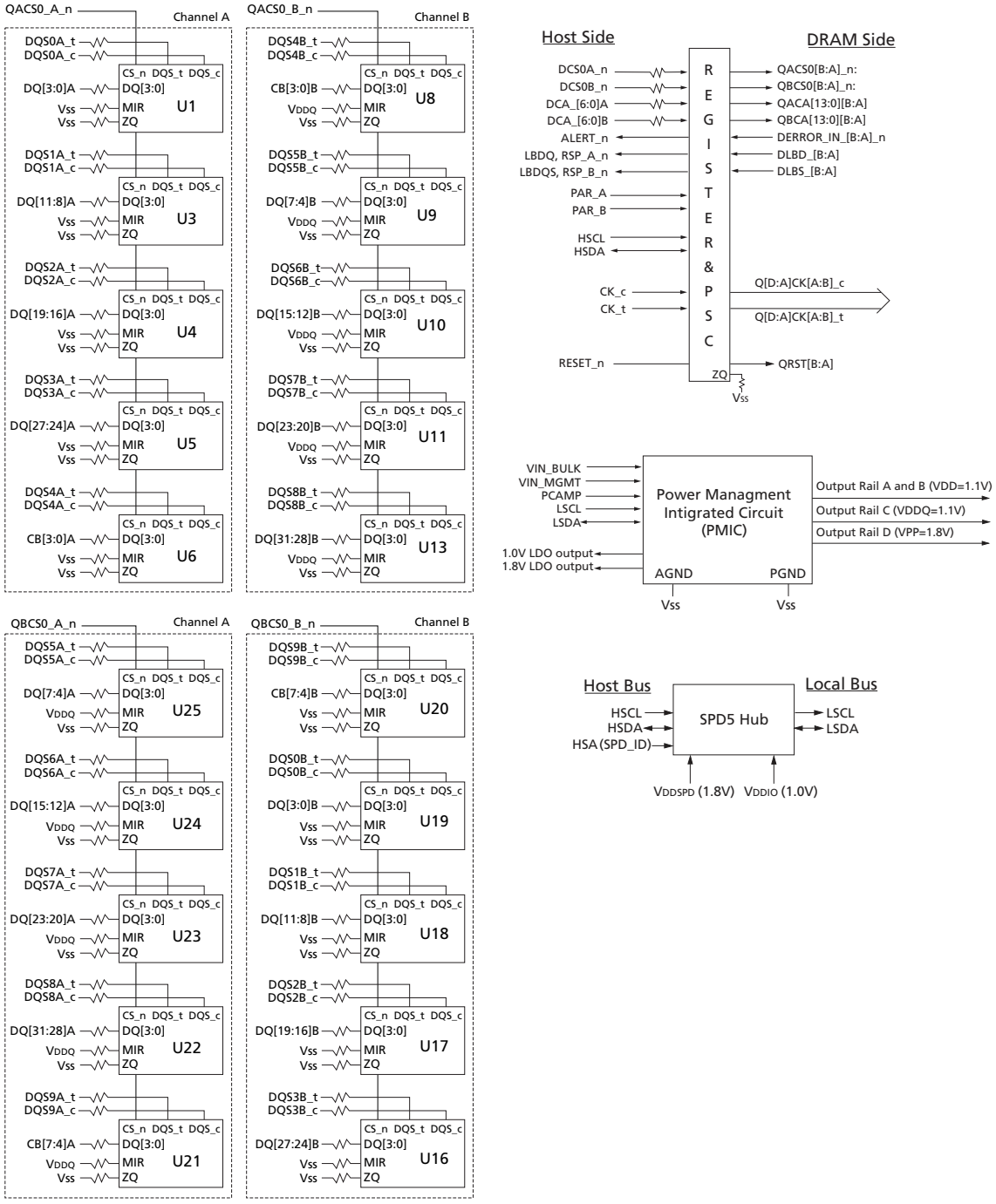
Functional Block Diagram

Figure 3: Functional Block Diagram



Notes: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.
2. Functional block diagram is for reference only.

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Revision History

Rev. D – 01/2024

- Added 6400 MPN with PCB tie bar change

Rev. C – 01/2023

- Added IDD limits for 48B, and changed part status for 48B to "Production"
- Removed Micron Confidential marking
- Changed data sheet status to Production

Rev. B – 11/2022

- Added MIR state to Functional Block Diagram
- Added PCB drawing to Features page
- Added values for R/C C-1 DQ map

Rev. A – 04/2022

- Preliminary Release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein.
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