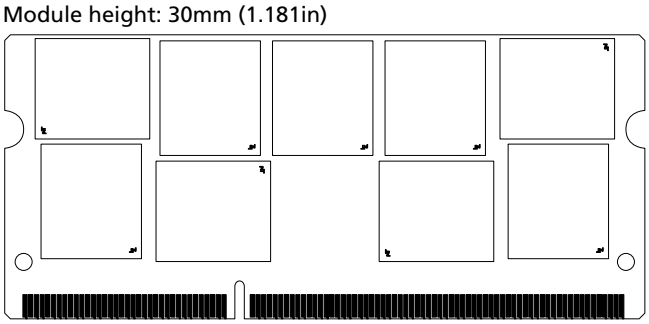
# 1.35V DDR3L SDRAM SODIMM

## MT18KSF51272HZ – 4GB
## MT18KSF1G72HZ – 8GB

## Features

- DDR3L functionality and operations supported as defined in the component data sheet
- 204-pin, small outline dual in-line memory module (SODIMM) with ECC
- Fast data transfer rates: PC3-12800, PC3-10600
- 4GB (512 Meg x 72), 8GB (1 Gig x 72)
- $V_{DD}$ = 1.35V (1.283–1.45V)
- $V_{DD}$ = 1.5V (1.425–1.575V)
- Backward compatible to $V_{DD}$ = 1.5V ±0.075V
- $V_{DDSPD}$ = 3.0–3.6V
- Supports ECC error detection and correction
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals
- Dual-rank
- On-board $I^2C$ temperature sensor with integrated serial presence-detect (SPD) EEPROM
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the mode register set (MRS)
- Selectable BC4 or BL8 on-the-fly (OTF)
- Gold edge contacts
- Halogen-free
- Fly-by topology
- Terminated control, command, and address bus

**Figure 1: 204-Pin SODIMM (R/C D1)**




| Options | Marking |
|---|---|
| • Operating temperature | |
| – Commercial (0°C ≤ $T_A$ ≤ +70°C) | None |
| • Package | |
| – 204-pin DIMM (halogen-free) | Z |
| • Frequency/CAS latency | |
| – 1.25ns @ CL = 11 (DDR3-1600) | -1G6 |
| – 1.5ns @ CL = 9 (DDR3-1333) | -1G4 |

**Table 1: Key Timing Parameters**

| Speed Grade | Industry Nomenclature | Data Rate (MT/s) | | | | | | | $^tRCD$ (ns) | $^tRP$ (ns) | $^tRC$ (ns) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | CL = 11 | CL = 10 | CL = 9 | CL = 8 | CL = 7 | CL = 6 | CL = 5 | | | |
| -1G6 | PC3-12800 | 1600 | 1333 | 1333 | 1066 | 1066 | 800 | 667 | 13.125 | 13.125 | 48.125 |
| -1G4 | PC3-10600 | – | 1333 | 1333 | 1066 | 1066 | 800 | 667 | 13.125 | 13.125 | 49.125 |
| -1G1 | PC3-8500 | – | – | – | 1066 | 1066 | 800 | 667 | 13.125 | 13.125 | 50.625 |
| -1G0 | PC3-8500 | – | – | – | 1066 | – | 800 | 667 | 15 | 15 | 52.5 |
| -80B | PC3-6400 | – | – | – | – | – | 800 | 667 | 15 | 15 | 52.5 |


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### Table 2: Addressing

| Parameter | 4GB | 8GB |
|---|---|---|
| Refresh count | 8K | 8K |
| Row address | 32K A[14:0] | 64K A[15:0] |
| Device bank address | 8 BA[2:0] | 8 BA[2:0] |
| Device configuration | 2Gb (256 Meg x 8) | 4Gb (512 Meg x 8) |
| Column address | 1K A[9:0] | 1K A[9:0] |
| Module rank address | 2 S#[1:0] | 2 S#[1:0] |

### Table 3: Part Numbers and Timing Parameters – 4GB Modules

Base device: MT41K256M8,[1] 2Gb 1.35V DDR3L SDRAM

| Part Number[2] | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL-$^{t}$RCD-$^{t}$RP) |
|---|---|---|---|---|---|
| MT18KSF51272HZ-1G6__ | 4GB | 512 Meg x 72 | 12.8 GB/s | 1.25ns/1600 MT/s | 11-11-11 |
| MT18KSF51272HZ-1G4__ | 4GB | 512 Meg x 72 | 10.6 GB/s | 1.5ns/1333 MT/s | 9-9-9 |

### Table 4: Part Numbers and Timing Parameters – 8GB Modules

Base device: MT41K512M8,[1] 4Gb 1.35V DDR3L SDRAM

| Part Number[2] | Module Density | Configuration | Module Bandwidth | Memory Clock/ Data Rate | Clock Cycles (CL-$^{t}$RCD-$^{t}$RP) |
|---|---|---|---|---|---|
| MT18KSF1G72HZ-1G6__ | 8GB | 1 Gig x 72 | 12.8 GB/s | 1.25ns/1600 MT/s | 11-11-11 |
| MT18KSF1G72HZ-1G4__ | 8GB | 1 Gig x 72 | 10.6 GB/s | 1.5ns/1333 MT/s | 9-9-9 |

Notes:
1. The data sheet for the base device can be found on Micron's web site.
2. All part numbers end with a two-place code (not shown) that designates component and PCB revisions. Consult factory for current revision codes. Example: MT18KSF1G72HZ-1G6P1.


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# Pin Assignments

### Table 5: Pin Assignments

| 204-Pin DDR3 SODIMM Front | | | | | | | | 204-Pin DDR3 SODIMM Back | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1 | $V_{REFDQ}$ | 53 | $V_{SS}$ | 105 | A1 | 157 | DM5 | 2 | $V_{SS}$ | 54 | DQ28 | 106 | A2 | 158 | $V_{SS}$ |
| 3 | $V_{SS}$ | 55 | DQ24 | 107 | A0 | 159 | DQ42 | 4 | DQ4 | 56 | DQ29 | 108 | BA1 | 160 | DQ46 |
| 5 | DQ0 | 57 | DQ25 | 109 | $V_{DD}$ | 161 | DQ43 | 6 | DQ5 | 58 | $V_{SS}$ | 110 | $V_{DD}$ | 162 | DQ47 |
| 7 | DQ1 | 59 | DM3 | 111 | CK0 | 163 | $V_{SS}$ | 8 | $V_{SS}$ | 60 | DQS3# | 112 | CK1 | 164 | $V_{SS}$ |
| 9 | $V_{SS}$ | 61 | $V_{SS}$ | 113 | CK0# | 165 | DQ48 | 10 | DQS0# | 62 | DQS3 | 114 | CK1# | 166 | DQ52 |
| 11 | DM0 | 63 | DQ26 | 115 | $V_{DD}$ | 167 | DQ49 | 12 | DQS0 | 64 | $V_{SS}$ | 116 | $V_{DD}$ | 168 | DQ53 |
| 13 | DQ2 | 65 | DQ27 | 117 | A10/AP | 169 | $V_{SS}$ | 14 | $V_{SS}$ | 66 | DQ30 | 118 | NC | 170 | $V_{SS}$ |
| 15 | DQ3 | 67 | $V_{SS}$ | 119 | BA0 | 171 | DQS6# | 16 | DQ6 | 68 | DQ31 | 120 | NC | 172 | DM6 |
| 17 | $V_{SS}$ | 69 | CB0 | 121 | WE# | 173 | DQS6 | 18 | DQ7 | 70 | $V_{SS}$ | 122 | RAS# | 174 | DQ54 |
| 19 | DQ8 | 71 | CB1 | 123 | $V_{DD}$ | 175 | $V_{SS}$ | 20 | $V_{SS}$ | 72 | CB4 | 124 | $V_{DD}$ | 176 | DQ55 |
| 21 | DQ9 | 73 | $V_{SS}$ | 125 | CAS# | 177 | DQ50 | 22 | DQ12 | 74 | CB5 | 126 | ODT0 | 178 | $V_{SS}$ |
| 23 | $V_{SS}$ | 75 | DQS8# | 127 | S0# | 179 | DQ51 | 24 | DQ13 | 76 | DM8 | 128 | ODT1 | 180 | DQ60 |
| 25 | DQS1# | 77 | DQS8 | 129 | S1# | 181 | $V_{SS}$ | 26 | $V_{SS}$ | 78 | $V_{SS}$ | 130 | A13 | 182 | DQ61 |
| 27 | DQS1 | 79 | $V_{SS}$ | 131 | $V_{DD}$ | 183 | DQ56 | 28 | DM1 | 80 | CB6 | 132 | $V_{DD}$ | 184 | $V_{SS}$ |
| 29 | $V_{SS}$ | 81 | CB2 | 133 | DQ32 | 185 | DQ57 | 30 | RESET# | 82 | CB7 | 134 | DQ36 | 186 | DQS7# |
| 31 | DQ10 | 83 | CB3 | 135 | DQ33 | 187 | $V_{SS}$ | 32 | $V_{SS}$ | 84 | $V_{REFCA}$ | 136 | DQ37 | 188 | DQS7 |
| 33 | DQ11 | 85 | $V_{DD}$ | 137 | $V_{SS}$ | 189 | DM7 | 34 | DQ14 | 86 | $V_{DD}$ | 138 | $V_{SS}$ | 190 | $V_{SS}$ |
| 35 | $V_{SS}$ | 87 | CKE0 | 139 | DQS4# | 191 | DQ58 | 36 | DQ15 | 88 | NF/A15[1] | 140 | DM4 | 192 | DQ62 |
| 37 | DQ16 | 89 | CKE1 | 141 | DQS4 | 193 | DQ59 | 38 | $V_{SS}$ | 90 | A14 | 142 | DQ38 | 194 | DQ63 |
| 39 | DQ17 | 91 | BA2 | 143 | $V_{SS}$ | 195 | $V_{SS}$ | 40 | DQ20 | 92 | A9 | 144 | DQ39 | 196 | $V_{SS}$ |
| 41 | $V_{SS}$ | 93 | $V_{DD}$ | 145 | DQ34 | 197 | SA0 | 42 | DQ21 | 94 | $V_{DD}$ | 146 | $V_{SS}$ | 198 | EVENT# |
| 43 | DQS2# | 95 | A12 | 147 | DQ35 | 199 | $V_{DDSPD}$ | 44 | DM2 | 96 | A11 | 148 | DQ44 | 200 | SDA |
| 45 | DQS2 | 97 | A8 | 149 | $V_{SS}$ | 201 | SA1 | 46 | $V_{SS}$ | 98 | A7 | 150 | DQ45 | 202 | SCL |
| 47 | $V_{SS}$ | 99 | A5 | 151 | DQ40 | 203 | $V_{TT}$ | 48 | DQ22 | 100 | A6 | 152 | $V_{SS}$ | 204 | $V_{TT}$ |
| 49 | DQ18 | 101 | $V_{DD}$ | 153 | DQ41 | – | – | 50 | DQ23 | 102 | $V_{DD}$ | 154 | DQS5# | – | – |
| 51 | DQ19 | 103 | A3 | 155 | $V_{SS}$ | – | – | 52 | $V_{SS}$ | 104 | A4 | 156 | DQS5 | – | – |

Note: 1. Pin 88 is NF for 4GB; A15 for 8GB.


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# Pin Descriptions

The pin description table below is a comprehensive list of all possible pins for all DDR3 modules. All pins listed may not be supported on this module. See Pin Assignments for information specific to this module.

**Table 6: Pin Descriptions**

| Symbol | Type | Description |
|---|---|---|
| Ax | Input | **Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW, bank selected by BAx) or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. See the Pin Assignments table for density-specific addressing information. |
| BAx | Input | **Bank address inputs:** Define the device bank to which an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA define which mode register (MR0, MR1, MR2, or MR3) is loaded during the LOAD MODE command. |
| CKx, CKx# | Input | **Clock:** Differential clock inputs. All control, command, and address input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. |
| CKEx | Input | **Clock enable:** Enables (registered HIGH) and disables (registered LOW) internal circuitry and clocks on the DRAM. |
| DMx | Input | **Data mask (x8 devices only):** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. Although DM pins are input-only, DM loading is designed to match that of the DQ and DQS pins. |
| ODTx | Input | **On-die termination:** Enables (registered HIGH) and disables (registered LOW) termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to the following pins: DQ, DQS, DQS#, DM, and CB. The ODT input will be ignored if disabled via the LOAD MODE command. |
| Par_In | Input | **Parity input:** Parity bit for Ax, RAS#, CAS#, and WE#. |
| RAS#, CAS#, WE# | Input | **Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered. |
| RESET# | Input (LVCMOS) | **Reset:** RESET# is an active LOW asychronous input that is connected to each DRAM and the registering clock driver. After RESET# goes HIGH, the DRAM must be reinitialized as though a normal power-up was executed. |
| Sx# | Input | **Chip select:** Enables (registered LOW) and disables (registered HIGH) the command decoder. |
| SAx | Input | **Serial address inputs:** Used to configure the temperature sensor/SPD EEPROM address range on the $I^2C$ bus. |
| SCL | Input | **Serial clock for temperature sensor/SPD EEPROM:** Used to synchronize communication to and from the temperature sensor/SPD EEPROM on the $I^2C$ bus. |
| CBx | I/O | **Check bits:** Used for system error detection and correction. |
| DQx | I/O | **Data input/output:** Bidirectional data bus. |
| DQSx, DQSx# | I/O | **Data strobe:** Differential data strobes. Output with read data; edge-aligned with read data; input with write data; center-aligned with write data. |


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**Table 6: Pin Descriptions (Continued)**

| Symbol | Type | Description |
|---|---|---|
| SDA | I/O | **Serial data:** Used to transfer addresses and data into and out of the temperature sensor/SPD EEPROM on the $I^2C$ bus. |
| TDQSx, TDQSx# | Output | **Redundant data strobe (x8 devices only):** TDQS is enabled/disabled via the LOAD MODE command to the extended mode register (EMR). When TDQS is enabled, DM is disabled and TDQS and TDQS# provide termination resistance; otherwise, TDQS# are no function. |
| Err_Out# | Output (open drain) | **Parity error output:** Parity error found on the command and address bus. |
| EVENT# | Output (open drain) | **Temperature event:** The EVENT# pin is asserted by the temperature sensor when critical temperature thresholds have been exceeded. |
| $V_{DD}$ | Supply | **Power supply:** 1.35V (1.283–1.45V) backward-compatible to 1.5V (1.425–1.575V). The component $V_{DD}$ and $V_{DDQ}$ are connected to the module $V_{DD}$. |
| $V_{DDSPD}$ | Supply | **Temperature sensor/SPD EEPROM power supply:** 3.0–3.6V. |
| $V_{REFCA}$ | Supply | **Reference voltage:** Control, command, and address $V_{DD}/2$. |
| $V_{REFDQ}$ | Supply | **Reference voltage:** DQ, DM $V_{DD}/2$. |
| $V_{SS}$ | Supply | Ground. |
| $V_{TT}$ | Supply | **Termination voltage:** Used for control, command, and address $V_{DD}/2$. |
| NC | – | **No connect:** These pins are not connected on the module. |
| NF | – | **No function:** These pins are connected within the module, but provide no functionality. |



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# DQ Map

**Table 7: Component-to-Module DQ Map, Front**

| Component Reference Number | Component DQ | Module DQ | Module Pin Number | Component Reference Number | Component DQ | Module DQ | Module Pin Number |
|---|---|---|---|---|---|---|---|
| U1 | 0 | 2 | 13 | U2 | 0 | 23 | 50 |
| | 1 | 0 | 5 | | 1 | 21 | 42 |
| | 2 | 3 | 15 | | 2 | 19 | 51 |
| | 3 | 5 | 6 | | 3 | 20 | 40 |
| | 4 | 7 | 18 | | 4 | 22 | 48 |
| | 5 | 4 | 4 | | 5 | 16 | 37 |
| | 6 | 6 | 16 | | 6 | 18 | 49 |
| | 7 | 1 | 7 | | 7 | 17 | 39 |
| U3 | 0 | CB2 | 81 | U4 | 0 | 42 | 159 |
| | 1 | CB1 | 71 | | 1 | 45 | 150 |
| | 2 | CB3 | 83 | | 2 | 46 | 160 |
| | 3 | CB4 | 72 | | 3 | 40 | 151 |
| | 4 | CB6 | 80 | | 4 | 43 | 161 |
| | 5 | CB0 | 69 | | 5 | 44 | 148 |
| | 6 | CB7 | 82 | | 6 | 47 | 162 |
| | 7 | CB5 | 74 | | 7 | 41 | 153 |
| U5 | 0 | 59 | 193 | U6 | 0 | 14 | 34 |
| | 1 | 57 | 185 | | 1 | 9 | 21 |
| | 2 | 62 | 192 | | 2 | 11 | 33 |
| | 3 | 56 | 183 | | 3 | 8 | 19 |
| | 4 | 58 | 191 | | 4 | 10 | 31 |
| | 5 | 61 | 182 | | 5 | 13 | 24 |
| | 6 | 63 | 194 | | 6 | 15 | 36 |
| | 7 | 60 | 180 | | 7 | 12 | 22 |
| U7 | 0 | 29 | 56 | U8 | 0 | 38 | 142 |
| | 1 | 26 | 63 | | 1 | 33 | 135 |
| | 2 | 28 | 54 | | 2 | 35 | 147 |
| | 3 | 31 | 68 | | 3 | 37 | 136 |
| | 4 | 25 | 57 | | 4 | 39 | 144 |
| | 5 | 27 | 65 | | 5 | 32 | 133 |
| | 6 | 24 | 55 | | 6 | 34 | 145 |
| | 7 | 30 | 66 | | 7 | 36 | 134 |



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**Table 7: Component-to-Module DQ Map, Front (Continued)**

| Component Reference Number | Component DQ | Module DQ | Module Pin Number | Component Reference Number | Component DQ | Module DQ | Module Pin Number |
|---|---|---|---|---|---|---|---|
| U9 | 0 | 55 | 176 | U10 | 0 | 57 | 185 |
| | 1 | 53 | 168 | | 1 | 59 | 193 |
| | 2 | 54 | 174 | | 2 | 56 | 183 |
| | 3 | 52 | 166 | | 3 | 62 | 192 |
| | 4 | 51 | 179 | | 4 | 60 | 180 |
| | 5 | 48 | 165 | | 5 | 63 | 194 |
| | 6 | 50 | 177 | | 6 | 61 | 182 |
| | 7 | 49 | 167 | | 7 | 58 | 191 |

**Table 8: Component-to-Module DQ Map, Back**

| Component Reference Number | Component DQ | Module DQ | Module Pin Number | Component Reference Number | Component DQ | Module DQ | Module Pin Number |
|---|---|---|---|---|---|---|---|
| U11 | 0 | 45 | 150 | U12 | 0 | CB1 | 71 |
| | 1 | 42 | 159 | | 1 | CB2 | 81 |
| | 2 | 40 | 151 | | 2 | CB4 | 72 |
| | 3 | 46 | 160 | | 3 | CB3 | 83 |
| | 4 | 41 | 153 | | 4 | CB5 | 74 |
| | 5 | 47 | 162 | | 5 | CB7 | 82 |
| | 6 | 44 | 148 | | 6 | CB0 | 69 |
| | 7 | 43 | 161 | | 7 | CB6 | 80 |
| U13 | 0 | 21 | 42 | U14 | 0 | 0 | 5 |
| | 1 | 23 | 50 | | 1 | 2 | 13 |
| | 2 | 20 | 40 | | 2 | 5 | 6 |
| | 3 | 19 | 51 | | 3 | 3 | 15 |
| | 4 | 17 | 39 | | 4 | 1 | 7 |
| | 5 | 18 | 49 | | 5 | 6 | 16 |
| | 6 | 16 | 37 | | 6 | 4 | 4 |
| | 7 | 22 | 48 | | 7 | 7 | 18 |



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**Table 8: Component-to-Module DQ Map, Back (Continued)**

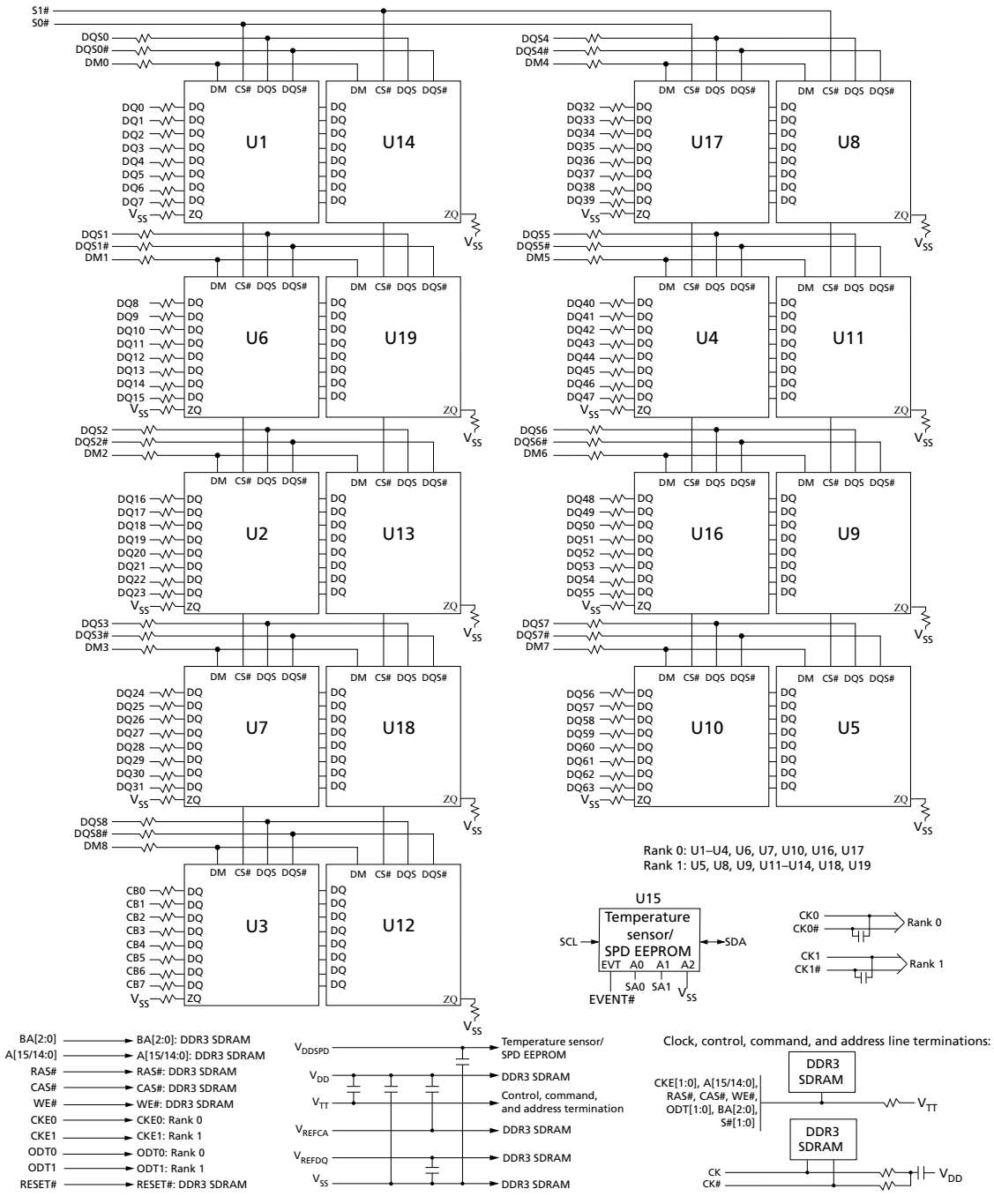
| Component Reference Number | Component DQ | Module DQ | Module Pin Number | Component Reference Number | Component DQ | Module DQ | Module Pin Number |
|---|---|---|---|---|---|---|---|
| U16 | 0 | 53 | 168 | U17 | 0 | 33 | 135 |
| | 1 | 55 | 176 | | 1 | 38 | 142 |
| | 2 | 52 | 166 | | 2 | 37 | 136 |
| | 3 | 54 | 174 | | 3 | 35 | 147 |
| | 4 | 49 | 167 | | 4 | 36 | 134 |
| | 5 | 50 | 177 | | 5 | 34 | 145 |
| | 6 | 48 | 165 | | 6 | 32 | 133 |
| | 7 | 51 | 179 | | 7 | 39 | 144 |
| U18 | 0 | 26 | 63 | U19 | 0 | 9 | 21 |
| | 1 | 29 | 56 | | 1 | 14 | 34 |
| | 2 | 31 | 68 | | 2 | 8 | 19 |
| | 3 | 28 | 54 | | 3 | 11 | 33 |
| | 4 | 30 | 66 | | 4 | 12 | 22 |
| | 5 | 24 | 55 | | 5 | 15 | 36 |
| | 6 | 27 | 65 | | 6 | 13 | 24 |
| | 7 | 25 | 57 | | 7 | 10 | 31 |



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# Functional Block Diagram

### Figure 2: Functional Block Diagram




Note: 1. The ZQ ball on each DDR3 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.


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# General Description

DDR3 SDRAM modules are high-speed, CMOS dynamic random access memory modules that use internally configured 8-bank DDR3 SDRAM devices. DDR3 SDRAM modules use DDR architecture to achieve high-speed operation. DDR3 architecture is essentially an 8*n*-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR3 SDRAM module effectively consists of a single 8*n*-bit-wide, one-clock-cycle data transfer at the internal DRAM core and eight corresponding *n*-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

DDR3 modules use two sets of differential signals: DQS, DQS# to capture data and CK and CK# to capture commands, addresses, and control signals. Differential clocks and data strobes ensure exceptional noise immunity for these signals and provide precise crossing points to capture input signals.

## Fly-By Topology

DDR3 modules use faster clock speeds than earlier DDR technologies, making signal quality more important than ever. For improved signal quality, the clock, control, command, and address buses have been routed in a fly-by topology, where each clock, control, command, and address pin on each DRAM is connected to a single trace and terminated (rather than a tree structure, where the termination is off the module near the connector). Inherent to fly-by topology, the timing skew between the clock and DQS signals can be easily accounted for by using the write-leveling feature of DDR3.

# Temperature Sensor with Serial Presence-Detect EEPROM

## Thermal Sensor Operations

The temperature from the integrated thermal sensor is monitored and converts into a digital word via the $I^2C$ bus. System designers can use the user-programmable registers to create a custom temperature-sensing solution based on system requirements. Programming and configuration details comply with JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

## Serial Presence-Detect EEPROM Operation

DDR3 SDRAM modules incorporate serial presence-detect. The SPD data is stored in a 256-byte EEPROM. The first 128 bytes are programmed by Micron to comply with JEDEC standard JC-45, "Appendix X: Serial Presence Detect (SPD) for DDR3 SDRAM Modules." These bytes identify module-specific timing parameters, configuration information, and physical attributes. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard $I^2C$ bus using the DIMM's SCL (clock) SDA (data), and SA (address) pins. Write protect (WP) is connected to $V_{SS}$, permanently disabling hardware write protection. For further information refer to Micron technical note TN-04-42, "Memory Module Serial Presence-Detect."



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# Electrical Specifications

Stresses greater than those listed may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions outside those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

**Table 9: Absolute Maximum Ratings**

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ supply voltage relative to $V_{SS}$ | –0.4 | 1.975 | V |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | –0.4 | 1.975 | V |

**Table 10: Operating Conditions**

| Symbol | Parameter | | Min | Nom | Max | Units | Notes |
|---|---|---|---|---|---|---|---|
| $V_{DD}$ | $V_{DD}$ supply voltage | | 1.283 | 1.35 | 1.45 | V | |
| | | | 1.425 | 1.5 | 1.575 | V | 1 |
| $V_{REFCA(DC)}$ | Input reference voltage command/address bus | | 0.49 × $V_{DD}$ | 0.5 × $V_{DD}$ | 0.51 × $V_{DD}$ | V | |
| $V_{REFDQ(DC)}$ | I/O reference voltage DQ bus | | 0.49 × $V_{DD}$ | 0.5 × $V_{DD}$ | 0.51 × $V_{DD}$ | V | |
| $I_{VTT}$ | Termination reference current from $V_{TT}$ | | –600 | – | 600 | mA | |
| $V_{TT}$ | Termination reference voltage (DC) – command/address bus | | 0.49 × $V_{DD}$ - 20mV | 0.5 × $V_{DD}$ | 0.51 × $V_{DD}$ + 20mV | V | 2 |
| $I_I$ | Input leakage current; Any input 0V ≤ $V_{IN}$ ≤ $V_{DD}$; $V_{REF}$ input 0V ≤ $V_{IN}$ ≤ 0.95V (All other pins not under test = 0V) | Address inputs, RAS#, CAS#, WE#, BA | –36 | 0 | 36 | µA | |
| | | S#, CKE, ODT, CK, CK# | –18 | 0 | 18 | | |
| | | DM | –4 | 0 | 4 | | |
| $I_{OZ}$ | Output leakage current; 0V ≤ $V_{OUT}$ ≤ $V_{DD}$; DQ and ODT are disabled; ODT is HIGH | DQ, DQS, DQS#, CB | –10 | 0 | 10 | µA | |
| $I_{VREF}$ | $V_{REF}$ supply leakage current; $V_{REFDQ}$ = $V_{DD/2}$ or $V_{REFCA}$ = $V_{DD/2}$ (All other pins not under test = 0V) | | –18 | 0 | 18 | µA | |
| $T_A$ | Module ambient operating temperature | | 0 | – | 70 | °C | 3, 4 |
| $T_C$ | DDR3 SDRAM component case operating temperature | | 0 | – | 95 | °C | 3, 4, 5 |

Notes:
1. Module is backward-compatible with 1.5V operation. Refer to device specification for details and operation guidance.
2. $V_{TT}$ termination voltage in excess of the stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.
3. $T_A$ and $T_C$ are simultaneous requirements.
4. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.
5. The refresh rate is required to double when 85°C < $T_C$ ≤ 95°C.


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# DRAM Operating Conditions

Recommended AC operating conditions are given in the DDR3 component data sheets. Component specifications are available at micron.com. Module speed grades correlate with component speed grades, as shown below.

**Table 11: Module and Component Speed Grades**

DDR3 components may exceed the listed module speed grades; module may not be available in all listed speed grades

| Module Speed Grade | Component Speed Grade |
|---|---|
| -2G1 | -093 |
| -1G9 | -107 |
| -1G6 | -125 |
| -1G4 | -15E |
| -1G1 | -187E |
| -1G0 | -187 |
| -80C | -25E |
| -80B | -25 |

# Design Considerations

### Simulations

Micron memory modules are designed to optimize signal integrity through carefully designed terminations, controlled board impedances, routing topologies, trace length matching, and decoupling. However, good signal integrity starts at the system level. Micron encourages designers to simulate the signal characteristics of the system's memory bus to ensure adequate signal integrity of the entire memory system.

### Power

Operating voltages are specified at the DRAM, not at the edge connector of the module. Designers must account for any system voltage drops at anticipated power levels to ensure the required supply voltage is maintained.



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# $I_{DD}$ Specifications

### Table 12: DDR3 $I_{DD}$ Specifications and Conditions – 4GB (Die Revision K)

Values are for the MT41K256M8 DDR3L SDRAM only and are computed from values specified in the 2Gb 1.35V (256 Meg x 8) component data sheet

| Parameter | Symbol | 1600 | 1333 | Units |
|---|---|---|---|---|
| Operating current 0: One bank ACTIVATE-to-PRECHARGE | $I_{DD0}$[1] | 459 | 450 | mA |
| Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE | $I_{DD1}$[1] | 576 | 558 | mA |
| Precharge power-down current: Slow exit | $I_{DD2P0}$[2] | 216 | 216 | mA |
| Precharge power-down current: Fast exit | $I_{DD2P1}$[2] | 252 | 252 | mA |
| Precharge quiet standby current | $I_{DD2Q}$[2] | 360 | 360 | mA |
| Precharge standby current | $I_{DD2N}$[2] | 378 | 378 | mA |
| Precharge standby ODT current | $I_{DD2NT}$[1] | 387 | 369 | mA |
| Active power-down current | $I_{DD3P}$[2] | 378 | 378 | mA |
| Active standby current | $I_{DD3N}$[2] | 576 | 540 | mA |
| Burst read operating current | $I_{DD4R}$[1] | 954 | 846 | mA |
| Burst write operating current | $I_{DD4W}$[1] | 981 | 873 | mA |
| Refresh current | $I_{DD5B}$[1] | 1728 | 1719 | mA |
| Self refresh temperature current: MAX $T_C$ = 85°C | $I_{DD6}$[2] | 216 | 216 | mA |
| Self refresh temperature current (SRT-enabled): MAX $T_C$ = 95°C | $I_{DD6ET}$[2] | 270 | 270 | mA |
| All banks interleaved read current | $I_{DD7}$[1] | 1512 | 1458 | mA |
| Reset current | $I_{DD8}$[2] | 252 | 252 | mA |

Notes:
1. One module rank in the active $I_{DD}$, the other rank in $I_{DD2P0}$.
2. All ranks in this $I_{DD}$ condition.



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## Table 13: DDR3 $I_{DD}$ Specifications and Conditions – 8GB (Die Revision E)

Values are for the MT41K512M8 DDR3L SDRAM only and are computed from values specified in the 4Gb 1.35V (512 Meg x 8) component data sheet

| Parameter | Symbol | 1600 | 1333 | Units |
|---|---|---|---|---|
| Operating current 0: One bank ACTIVATE-to-PRECHARGE | $I_{DD0}$[1] | 657 | 585 | mA |
| Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE | $I_{DD1}$[1] | 756 | 720 | mA |
| Precharge power-down current: Slow exit | $I_{DD2P0}$[2] | 324 | 324 | mA |
| Precharge power-down current: Fast exit | $I_{DD2P1}$[2] | 576 | 504 | mA |
| Precharge quiet standby current | $I_{DD2Q}$[2] | 576 | 504 | mA |
| Precharge standby current | $I_{DD2N}$[2] | 576 | 522 | mA |
| Precharge standby ODT current | $I_{DD2NT}$[1] | 513 | 477 | mA |
| Active power-down current | $I_{DD3P}$[2] | 684 | 630 | mA |
| Active standby current | $I_{DD3N}$[2] | 684 | 630 | mA |
| Burst read operating current | $I_{DD4R}$[1] | 1575 | 1422 | mA |
| Burst write operating current | $I_{DD4W}$[1] | 1287 | 1152 | mA |
| Refresh current | $I_{DD5B}$[1] | 2277 | 2214 | mA |
| Self refresh temperature current: MAX $T_C$ = 85°C | $I_{DD6}$[2] | 360 | 360 | mA |
| Self refresh temperature current (SRT-enabled): MAX $T_C$ = 95°C | $I_{DD6ET}$[2] | 450 | 450 | mA |
| All banks interleaved read current | $I_{DD7}$[1] | 2142 | 1872 | mA |
| Reset current | $I_{DD8}$[2] | 360 | 360 | mA |

Notes:
1. One module rank in the active $I_{DD}$, the other rank in $I_{DD2P0}$.
2. All ranks in this $I_{DD}$ condition.



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## Table 14: DDR3 $I_{DD}$ Specifications and Conditions – 8GB (Die Revision P)

Values are for the MT41K512M8 DDR3L SDRAM only and are computed from values specified in the 4Gb 1.35V (512 Meg x 8) component data sheet

| Parameter | Symbol | 1600 | Units |
|---|---|---|---|
| Operating current 0: One bank ACTIVATE-to-PRECHARGE | $I_{DD0}$[1] | 342 | mA |
| Operating current 1: One bank ACTIVATE-to-READ-to-PRECHARGE | $I_{DD1}$[1] | 477 | mA |
| Precharge power-down current: Slow exit | $I_{DD2P0}$[2] | 180 | mA |
| Precharge power-down current: Fast exit | $I_{DD2P1}$[2] | 198 | mA |
| Precharge quiet standby current | $I_{DD2Q}$[2] | 270 | mA |
| Precharge standby current | $I_{DD2N}$[2] | 288 | mA |
| Precharge standby ODT current | $I_{DD2NT}$[1] | 270 | mA |
| Active power-down current | $I_{DD3P}$[2] | 270 | mA |
| Active standby current | $I_{DD3N}$[2] | 360 | mA |
| Burst read operating current | $I_{DD4R}$[1] | 900 | mA |
| Burst write operating current | $I_{DD4W}$[1] | 999 | mA |
| Refresh current | $I_{DD5B}$[1] | 1458 | mA |
| Self refresh temperature current: MAX $T_C$ = 85°C | $I_{DD6}$[2] | 270 | mA |
| Self refresh temperature current (SRT-enabled): MAX $T_C$ = 95°C | $I_{DD6ET}$[2] | 417 | mA |
| All banks interleaved read current | $I_{DD7}$[1] | 1260 | mA |
| Reset current | $I_{DD8}$[2] | 234 | mA |

Notes:
1. One module rank in the active $I_{DD}$, the other rank in $I_{DD2P0}$.
2. All ranks in this $I_{DD}$ condition.



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# Temperature Sensor with Serial Presence-Detect EEPROM

The temperature sensor continuously monitors the module's temperature and can be read back at any time over the $I^2C$ bus shared with the SPD EEPROM. Refer to JEDEC standard No. 21-C page 4.7-1, "Definition of the TSE2002av, Serial Presence Detect with Temperature Sensor."

## Serial Presence-Detect

For the latest SPD data, refer to Micron's SPD page: micron.com/SPD.

**Table 15: Temperature Sensor with SPD EEPROM DC and Temperature Sensor Operating Conditions**

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Supply voltage | $V_{DDSPD}$ | 3.0 | 3.6 | V |
| Supply current: $V_{DD}$ = 3.3V | $I_{DD}$ | – | 2.0 | mA |
| Input high voltage: Logic 1; SCL, SDA | $V_{IH}$ | $V_{DDSPD}$ x 0.7 | $V_{DDSPD}$ + 1 | V |
| Input low voltage: Logic 0; SCL, SDA | $V_{IL}$ | –0.5 | $V_{DDSPD}$ x 0.3 | V |
| Output low voltage: $I_{OUT}$ = 2.1mA | $V_{OL}$ | – | 0.4 | V |
| Input Leakage Current (SCL, SDA) | $I_{LI}$ | – | ±5.0 | µA |
| Output Leakage Current | $I_{LO}$ | – | ±5.0 | µA |
| Temperature sensing range | – | –40 | 125 | °C |
| Temperature sensor accuracy (class B) | – | – | ±1.0 | °C |

**Table 16: Temperature Sensor and SPD EEPROM Serial Interface AC Timing**

| Parameter/Condition | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Clock frequency | $^{f}SCL$ | 10 | 400 | kHz |
| Clock pulse width HIGH time | $^{t}HIGH$ | 600 | – | ns |
| Clock pulse width LOW time | $^{t}LOW$ | 1300 | – | ns |
| SDA rise time | $^{t}R$ | 20 | 300 | ns |
| SDA fall time | $^{t}F$ | 20 | 300 | ns |
| Data in setup time | $^{t}SU:DAT$ | 100 | – | ns |
| Data in hold time | $^{t}HD:DI$ | 0 | – | ns |
| Data out hold time | $^{t}HD:DAT$ | 200 | 900 | ns |
| Start condition setup time | $^{t}SU:STA$ | 600 | – | ns |
| Start condition hold time | $^{t}HD:STA$ | 600 | – | ns |
| Stop condition setup time | $^{t}SU:STO$ | 600 | – | ns |
| Time between Stop Conditon and next Start Condition | $^{t}BUF$ | 1300 | – | ns |
| Write time | $^{t}W$ | – | 10 | ms |


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## EVENT# Pin

The temperature sensor also adds the EVENT# pin (open-drain). Not used by the SPD EEPROM, EVENT# is a temperature sensor output used to flag critical events that can be set up in the sensor's configuration register.

EVENT# has three defined modes of operation: interrupt mode, compare mode, and critical temperature mode. Event thresholds are programmed in the 0x01 register using a hysteresis. The alarm window provides a comparison window, with upper and lower limits set in the alarm upper boundary register and the alarm lower boundary register, respectively. When the alarm window is enabled, EVENT# will trigger whenever the temperature is outside the MIN or MAX values set by the user.

The interrupt mode enables software to reset EVENT# after a critical temperature threshold has been detected. Threshold points are set in the configuration register by the user. This mode triggers the critical temperature limit and both the MIN and MAX of the temperature window.

The compare mode is similar to the interrupt mode, except EVENT# cannot be reset by the user and returns to the logic HIGH state only when the temperature falls below the programmed thresholds.

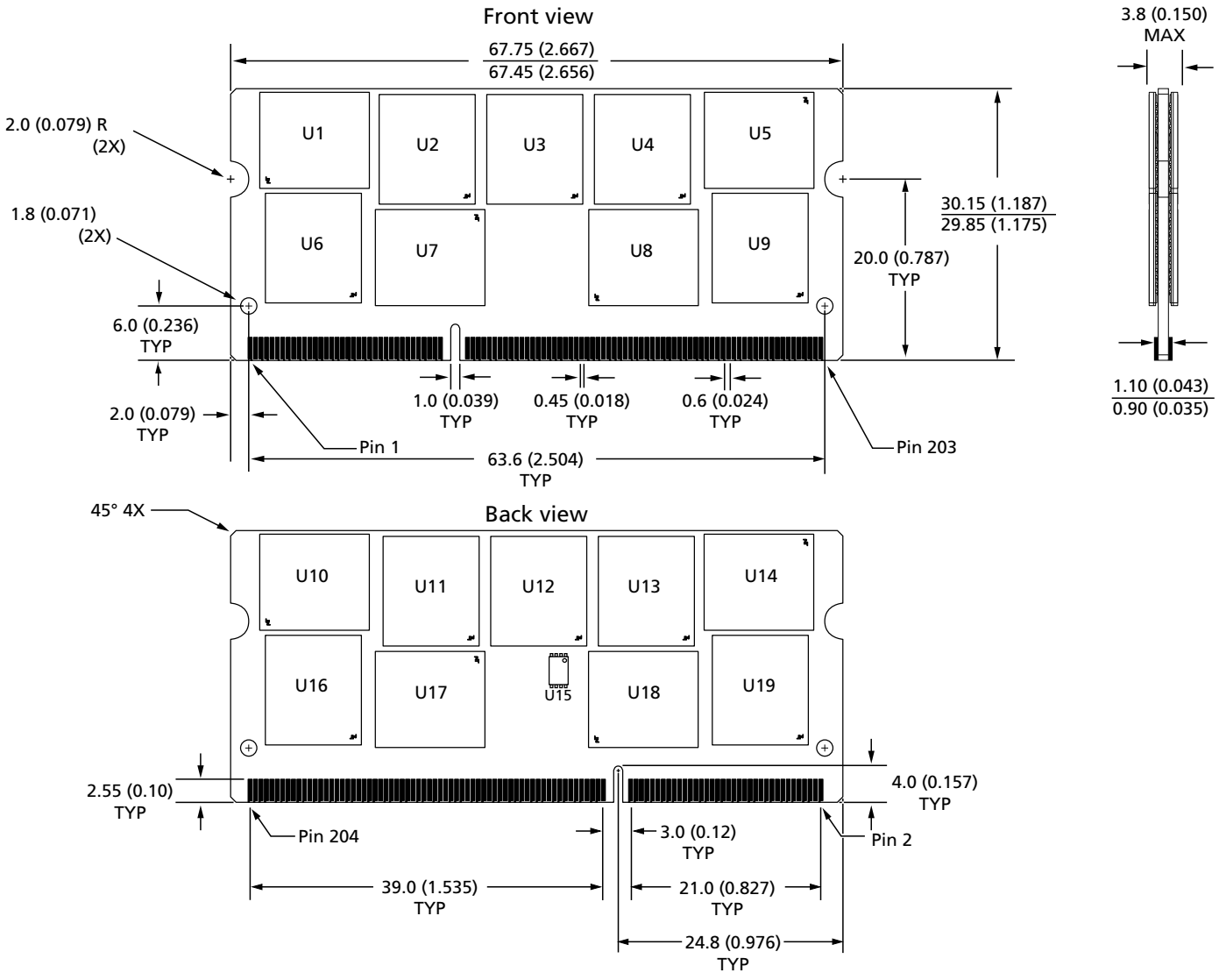
Critical temperature mode triggers EVENT# only when the temperature has exceeded the programmed critical trip point. When the critical trip point has been reached, the temperature sensor goes into comparator mode, and the critical EVENT# cannot be cleared through software.



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# Module Dimensions

**Figure 3: 204-Pin DDR3 SODIMM**




Notes:
1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.
2. The dimensional diagram is for reference only.
3. Tolerance on all dimensions ±0.15mm unless otherwise specified.

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.


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