DDR5 SDRAM SOEDIMM Addendum

MTC20C2085S1TC – 32GB
16Gb Die Revision A

Features

Information provided here is in addition to or supersedes information provided in the Micron DDR5 SODIMM Core data sheet.

- DDR5 functionality and operations supported as defined in the component data sheet
- Features and specifications defined in the Micron DDR5 SODIMM core data sheet
- 262-pin, DDR5 small-outline ECC dual in-line memory module (DDR5 SOEDIMM)
- Fast data transfer rate: PC5-4800
- 32GB (4Gig x 72)
- Dual-rank
- 32 internal banks; 8 groups of 4 banks each
- Supports ECC error detection and correction

Options	Marking
• Operating temperature	
– Commercial (0°C ≤ T_{OPER} ≤ 95°C)	C
• Frequency/CAS latency	
– 0.416ns @ CL = 40 (DDR5-4800)	48B

Figure 1: 262-Pin DDR5 SOEDIMM (R/C-E0)

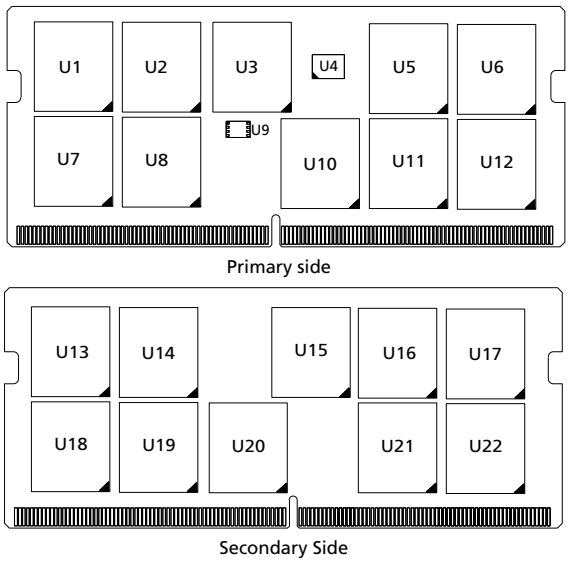

Table 1: Addressing

Parameter	32GB
Row address [1]	64K (R0-R15)
Column address [1]	1K (C0-C9)
Device bank group address [1]	8 (BG0-BG2)
Device bank address per bank group [1]	4 (BA0-BA1)
Device configuration	16Gb (2Gb x 8), 32 banks
Module rank address	2 (CS0_n, CS1_n)

Notes: 1. These parameters represent the logical address state of the CA bus for different commands. Refer to the command truth table in the component data sheet.

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Table 2: Part Numbers and Timing Parameters – 32GB Modules

Part Number	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Clock Cycles ($CL-_nRCD-_nRP$)
MTC20C2085S1TC48BA1	32GB	4Gb x 72	38.4 GB/s	0.416ns/4800 MT/s	40-39-39

Notes: 1. Base device: MT60B2G8, 16Gb DDR5 SDRAM Die Revision A. The data sheet for the base device can be found on micron.com.

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DQ Map

Table 3: Component-to-Module DQ Map

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U1	0	10A	35	U2	0	27A	80
	1	8A	31		1	24A	73
	2	11A	38		2	26A	77
	3	9A	34		3	25A	76
	4	15A	50		4	31A	92
	5	12A	45		5	28A	87
	6	13A	46		6	29A	88
	7	14A	49		7	30A	91
U3	0	CB3A	103	U5	0	7B	198
	1	CB0A	95		1	4B	191
	2	CB2A	99		2	5B	194
	3	CB1A	96		3	6B	195
	4	–	–		4	2B	183
	5	–	–		5	0B	179
	6	–	–		6	1B	180
	7	–	–		7	3B	184
U6	0	23B	240	U7	0	3A	16
	1	22B	237		1	0A	11
	2	21B	236		2	1A	12
	3	20B	233		3	2A	15
	4	18B	225		4	7A	30
	5	17B	222		5	5A	26
	6	16B	221		6	6A	27
	7	19B	226		7	4A	23
U8	0	18A	57	U10	0	CB2B	176
	1	16A	53		1	CB0B	168
	2	17A	54		2	CB3B	175
	3	19A	58		3	CB1B	172
	4	23A	72		4	–	–
	5	21A	68		5	–	–
	6	22A	69		6	–	–
	7	20A	65		7	–	–

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Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U11	0	12B	213	U12	0	31B	260
	1	15B	218		1	28B	255
	2	13B	214		2	29B	256
	3	14B	217		3	30B	259
	4	10B	203		4	26B	245
	5	8B	199		5	24B	241
	6	11B	206		6	27B	248
	7	9B	202		7	25B	244
U13	0	22B	237	U14	0	4B	191
	1	23B	240		1	7B	198
	2	20B	233		2	6B	195
	3	21B	236		3	5B	194
	4	17B	222		4	0B	179
	5	18B	225		5	2B	183
	6	19B	226		6	3B	184
	7	16B	221		7	1B	180
U15	0	CB0A	95	U16	0	24A	73
	1	CB3A	103		1	27A	80
	2	CB1A	96		2	25A	76
	3	CB2A	99		3	26A	77
	4	–	–		4	28A	87
	5	–	–		5	31A	92
	6	–	–		6	30A	91
	7	–	–		7	29A	88
U17	0	8A	31	U18	0	28B	255
	1	10A	35		1	31B	260
	2	9A	34		2	30B	259
	3	11A	38		3	29B	256
	4	12A	45		4	24B	241
	5	15A	50		5	26B	245
	6	14A	49		6	25B	244
	7	13A	46		7	27B	248

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Table 3: Component-to-Module DQ Map (Continued)

Component Reference Number	Component DQ	Module DQ	Module Pin Number	Component Reference Number	Component DQ	Module DQ	Module Pin Number
U19	0	15B	218	U20	0	CB0B	168
	1	12B	213		1	CB2B	176
	2	14B	217		2	CB1B	172
	3	13B	214		3	CB3B	175
	4	8B	199		4	–	–
	5	10B	203		5	–	–
	6	9B	202		6	–	–
	7	11B	206		7	–	–
U21	0	16A	53	U22	0	0A	11
	1	18A	57		1	3A	16
	2	19A	58		2	2A	15
	3	17A	54		3	1A	12
	4	21A	68		4	5A	26
	5	23A	72		5	7A	30
	6	20A	65		6	4A	23
	7	22A	69		7	6A	27

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I_{DD} Specifications

Table 4: DDR5 I_{DD} Specifications and Conditions – 32GB (Die Revision A)

Module I_{DD} is based on PMIC VIN_BULK 5V input current and typical operating range of temperature. Each I_{DD} parameter includes PMIC efficiency and all DRAM current on all supplies (V_{DD}, V_{DDQ}, and V_{PP}).

Parameter	Symbol	4800	Units
Operating one bank ACTIVATE-PRECHARGE current	I_{DD0}[1]	208	mA
Operating four bank ACTIVATE-PRECHARGE current	I_{DD0F}[1]	294	mA
Precharge standby current	I_{DD2N}[2]	187	mA
Precharge standby non-target command	I_{DD2NT}[1]	248	mA
Precharge power-down current	I_{DD2P}[2]	163	mA
Active standby current	I_{DD3N}[2]	227	mA
Active power-down current	I_{DD3P}[2]	203	mA
Operating burst read current	I_{DD4R}[1]	772	mA
Operating burst write current	I_{DD4W}[1]	1017	mA
Operating burst write with write CRC current	I_{DD4WC}[1]	935	mA
Burst refresh (normal refresh mode) current	I_{DD5B}[1]	584	mA
Burst refresh (fine granularity refresh mode) current	I_{DD5F}[1]	559	mA
Burst refresh (same bank refresh mode) current	I_{DD5C}[1]	296	mA
Self refresh current	I_{DD6N}[2]	140	mA
Operating bank interleave read current	I_{DD7}[1]	1109	mA
Maximum power saving deep power down mode current	I_{DD8}[2]	97	mA

Notes: 1. One module rank in this $I_{DD}/I_{DDQ}/I_{PP}$ condition, the other rank in $I_{DD2N}/I_{DDQ2N}/I_{PP2N}$.
2. Both ranks in this $I_{DD}/I_{DDQ}/I_{PP}$ condition.

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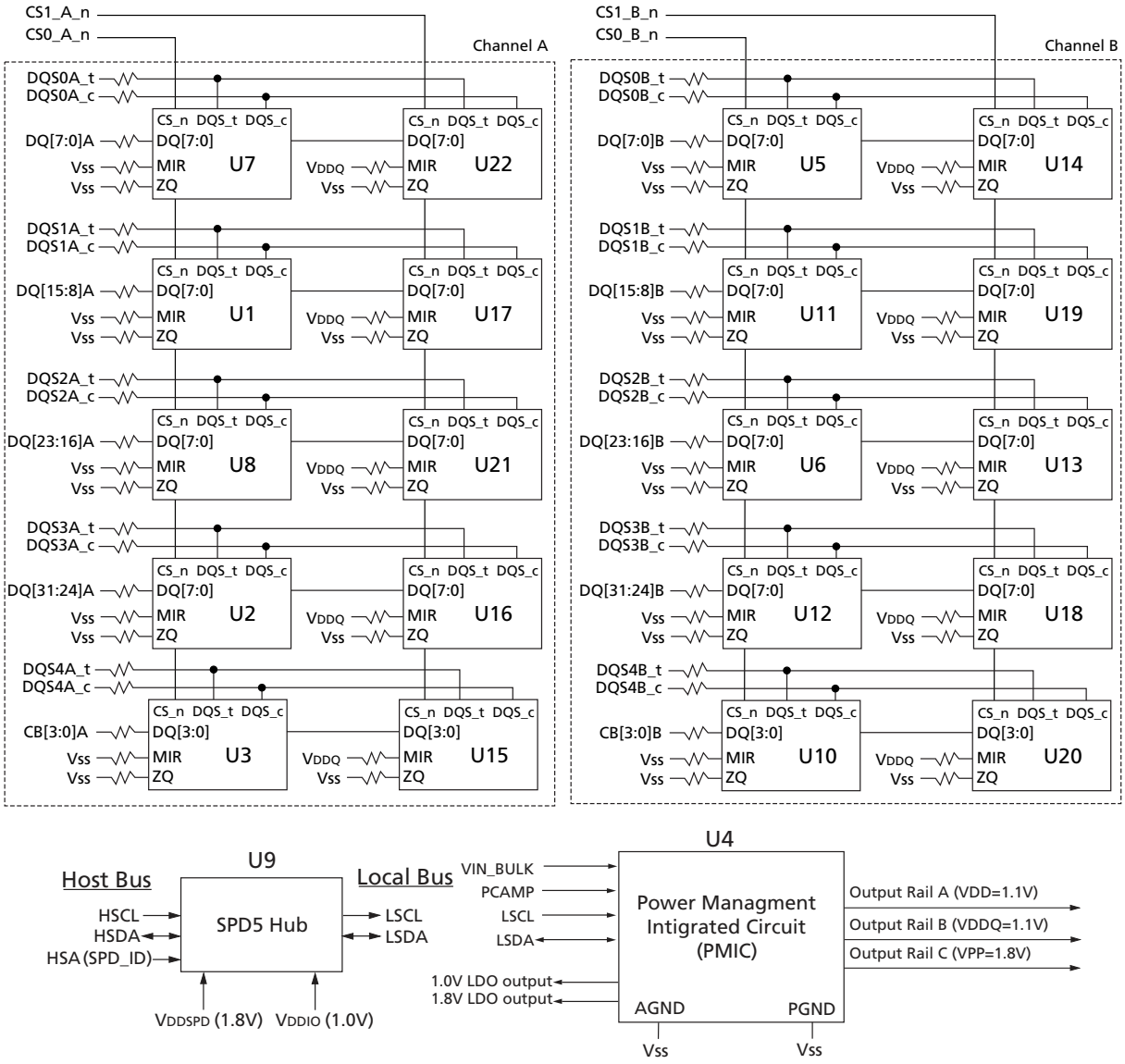
Functional Block Diagram

Figure 2: Functional Block Diagram



Note: 1. The ZQ ball on each DDR5 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

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Revision History

Rev. B – 12/2022

- Added MIR state to Functional Block Diagram
- Removed Micron Confidential designation

Rev. A – 01/2022

- Production Release

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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