2100AT PCIe NVMe NAND Flash SSD

MTFDHBL064, MTFDHBL128, MTFDHBL256, MTFDHBL512, MTFDHBM1T0, MTFDHBK1T0

Features

- Micron® 3D TLC NAND Flash
- PCIe Express base specification Rev 3.0
  - Gen3 x4 lanes
  - Backward compatibility
- NVMe Express Rev 1.3c compliant
  - Number of namespaces supported: Up to 4
  - Round robin arbitration: weighted
  - Autonomous power state transitions
  - Host memory buffer (HMB)
  - Boot partitions (2X 128MB)
  - RPMB (16MB)
  - End-to-end data protection
- Automotive Grade:
  - PPAP
  - AEC-Q104 for BGA
- Retention JESD47-compliant:
  - 5 years @55°C at 10% of TBW
  - 1 year @55°C at MAX TBW
- Package compliance:
  - RoHS certification
  - BGA, MSL3
- Capacity (unformatted)[1]: from 64GB to 1TB
- Physical capacity management (SLC mode)
- Endurance (TBW): Up to 480TB for 1024GB
- Security
  - TCG/Opal 2.0 compliant self-encrypting drive (SED)
  - Hardware-based AES-256 encryption engine
  - Digitally signed firmware
  - Firmware secure boot
- Self-monitoring, analysis, and reporting technology (SMART) command set
- Power loss protection for data-at-rest
- Performance[2]
  - Sequential 128KB READ: Up to 2000 MB/s
  - Sequential 128KB WRITE: Up to 1800 MB/s
  - Random 4KB READ: Up to 200,000 IOPS
  - Random 4KB WRITE: Up to 123,000 IOPS
- Latency[3]
  - Read (TYP): 85µs
  - Write (TYP): 40µs
- Reliability
  - MTTF: 3 million hours[4]
  - Static and dynamic wear leveling
  - Uncorrectable bit error rate (UBER): <1 sector per 10^{16} bits read
- Micron redundant array of independent NAND (RAIN) technology
- Low power consumption
  - Sleep: 3mW/5mW (PS4 and L1.2) BGA/M.2
- Operating temperature
  - Automotive (-40°C to +105°C)
  - Host-controlled thermal management
- Field upgradeable firmware
- Operating systems supported natively
  - Microsoft Windows® 10 and 11
  - Fedora® 30
  - Ubuntu® 19.04
  - openSUSE® Leap 15.1
  - Debian 10
  - Linux Mint 19.2
  - Chrome OS
- Form factor
  - BGA Type 1620, 16mm x 20mm x 1.2mm
  - BGA Type 1620, 16mm x 20mm x 1.6mm
  - M.2 Type 2230, 22mm x 30mm

Notes: 1. User capacity: 1GB = 1 billion bytes.
2. Typical I/O performance numbers as measured fresh-out-of-box (FOB) with HMB enabled.
3. 4KB, queue depth 1 transfers used for READ/WRITE latency values.
4. Mean time to failure (MTTF) based on population statistics not relevant to individual units.
5. Case surface temperature.

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Part Number Ordering

Verify valid part numbers by using Micron's part catalog search at www.micron.com. To compare features and specifications by device type, visit www.micron.com/products. Contact the factory for devices not found.

Figure 1: Part Number Ordering Information

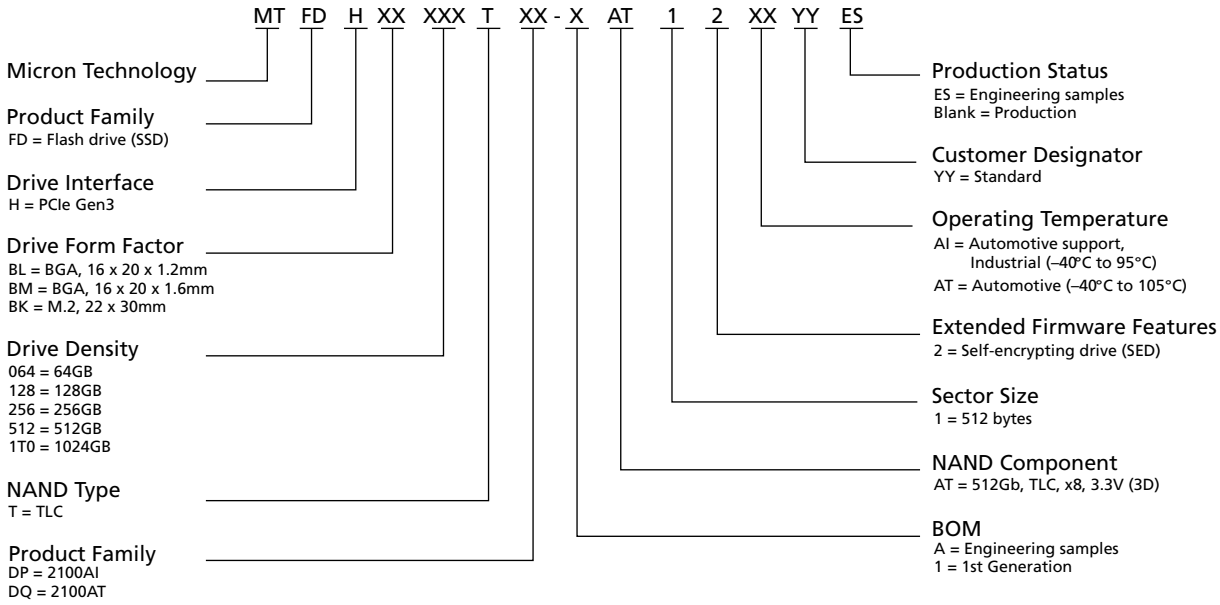

Table 1: Part Number Ordering Information

Part Number	Density	Package
MTFDHBL064TDQ-1AT12ATYY	64GB	BGA type 1620, 16mm x 20mm x 1.2mm
MTFDHBL128TDQ-1AT12ATYY	128GB	BGA type 1620, 16mm x 20mm x 1.2mm
MTFDHBL256TDQ-1AT12ATYY	256GB	BGA type 1620, 16mm x 20mm x 1.2mm
MTFDHBL512TDQ-1AT12ATYY	512GB	BGA type 1620, 16mm x 20mm x 1.2mm
MTFDHBM1T0TDQ-1AT12ATYY	1TB	BGA type 1620, 16mm x 20mm x 1.6mm
MTFDHBK1T0TDQ-1AT12ATYY	1TB	M.2 Type 2230 M-key, 22mm x 30mm x 2.4mm

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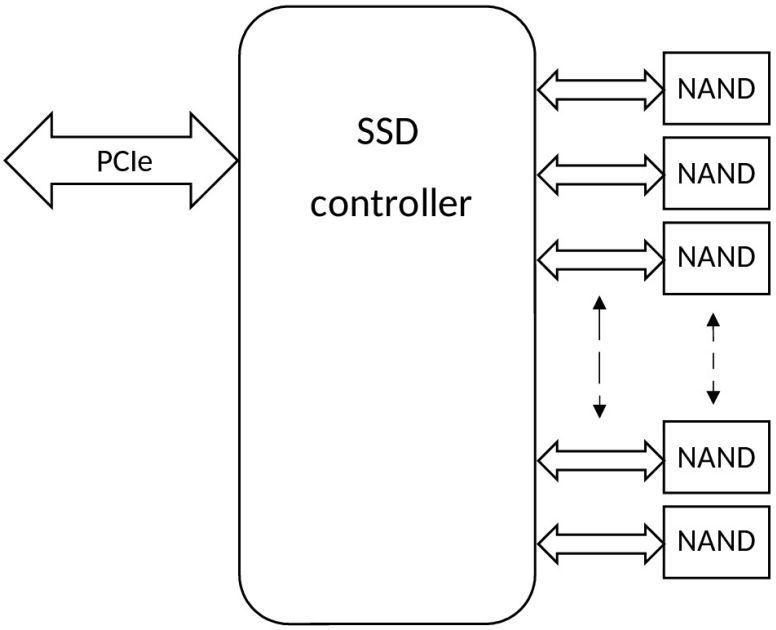
General Description

Micron's 2100AT solid state drive (SSD) uses a single-chip controller with a PCIe Gen3 interface connecting up to four PCIe lanes to Micron's 3D TLC NAND Flash.

The SSD is designed to use the PCIe interface efficiently during both READs and WRITEs while delivering bandwidth-focused, low latency performance through the innovative Nonvolatile Memory Express protocol. SSD technology enables enhanced boot times, faster application load times, reduced power consumption, and extended reliability.

The 2100AT is ideally suited for automotive and industrial applications, which require mass storage in a very small footprint.

Figure 2: Functional Block Diagram



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Performance

Measured performance can vary for a number of reasons. The major factors affecting drive performance are the capacity of the drive and the interface of the host. Additionally, overall system performance can affect the measured drive performance. When comparing drives, Micron recommends that all system variables be the same, with only the drive being tested allowed variations.

Performance numbers vary depending on the host system configuration.

For SSDs designed for the client and cloud computing markets, Micron specifies performance in FOB state and steady state. Data throughput measured in steady state may be lower than FOB state, depending on the nature of the data workload.

For a description of these performance states and of Micron's best practices for performance measurement, refer to Micron's technical marketing brief, Best Practices for SSD Performance Measurement, on www.micron.com.

Table 2: Drive Performance – Fresh Out of Box (PCIe 3.0 and x4 Lanes)

Parameter	64GB		128GB		256GB		512GB		1024GB		Unit
	HMB Off	HMB On	HMB Off	HMB On	HMB Off	HMB On	HMB Off	HMB On	HMB Off	HMB On	
Sequential read (128KB transfer)	550	550	1100	1100	2000	2000	2000	2000	2000	2000	MB/s
Sequential write (128KB transfer)	250	250	500	500	1000	1000	1700	1700	1800	1800	MB/s
Random read (4KB transfer)	12K	25K	20K	50K	38K	100K	65K	170K	105K	200K	IOPS
Random write (4KB transfer)	40K	50K	60K	85K	80K	110K	90K	120K	100K	123K	IOPS
READ latency (TYP)	85	85	85	85	85	85	85	85	85	85	µs
WRITE latency (TYP)	40	40	40	40	40	40	40	40	40	40	µs

Notes: 1. Performance values measured in FOB state using FIO with a queue depth of 32.
2. Drive write cache enabled.
3. NVMe power state 0.
4. 4KB transfers with a queue depth of 1 are used to measure READ/WRITE latency values.
5. 4KB transfers can be further improved with the support of HMB by the host.
6. System variations will affect measured results.

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Logical Block Address (LBA) Configuration

The drive is set to report the number of logical block addresses (LBA), which will ensure sufficient storage space for the specified capacity. Standard LBA settings (100% TLC), based on the IDEMA standard (LBA1-03), are shown below.

Table 3: Standard LBA Settings (100% TLC)

Capacity	Total 512 – Byte LBA		Max 512 – Byte LBA	
	Decimal	Hexadecimal	Decimal	Hexadecimal
64GB	125,045,424	7740AB0	125,045,423	7740AAF
128GB	250,069,680	EE7C2B0	250,069,679	EE7C2AF
256GB	500,118,192	1DCF32B0	500,118,191	1DCF32AF
512GB	1,000,215,216	3B9E12B0	1,000,215,215	3B9E12AF
1024GB	2,000,409,264	773BD2B0	2,000,409,265	773BD2AF

Note: See the Physical Capacity Management section for more options related to SLC vs. TLC configurations.

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Reliability

Micron's SSDs incorporate advanced technology for defect and error management. We use various combinations of hardware-based error correction algorithms and firmware-based static and dynamic wear-leveling algorithms.

Over the life of the SSD, uncorrectable errors may occur. An uncorrectable error is defined as data that is reported as successfully programmed to the SSD but when it is read out of the SSD, the data differs from what was programmed.

Table 4: Uncorrectable Bit Error Rate

Uncorrectable Bit Error Rate	Operation
<1 sector per 10^{16} bits read	READ

Mean Time To Failure

MTTF for the SSD can be predicted based on the component reliability data using the methods referenced in the Telcordia SR-332 reliability prediction procedures for electronic equipment.

Table 5: Mean Time to Failure

Capacity	MTTF (Operating Hours)
All capacities	at least 3 million

Notes: 1. The Mean Time To Failure (MTTF) reported in the above table is based on population statistics. Therefore, it is not relevant to individual unit.

Endurance

Endurance for the SSD can be predicted based on the usage conditions applied to the device. The table below shows the minimum drive lifetime for each SSD capacity based on predefined usage conditions noted below.

Table 6: Total Bytes Written

Capacity	TBW
64GB	30TB
128GB	60TB
256GB	120TB
512GB	240TB
1024GB	480TB

Notes: 1. Total Bytes Written (TBW) is validated with the drive 90% full.
2. SSD volatile write cache is enabled.
3. Access patterns used during reliability testing are 25% sequential and 75% random and consist of the following: 1% are 512B; 44% are 4 KiB; 35% are 64 KiB; and 20% are 128 KiB.
4. Host workload parameters, including write cache settings, I/O alignment, transfer sizes, randomness, and percent full, that are substantially different than the described notes may result in varied endurance results.
5. GB/day can be calculated by dividing the total bytes written value by (365 × number of years). For example: 100TB/5 years/365 days = 54GB/day for 5 years.

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Physical Capacity Management

At least one of the user-configurable namespaces (up to four) can be configured in "SLC mode" to meet the most demanding endurance requirements. This is the case of write-intensive applications or applications requiring long retention with limited writes. SLC mode also ensures higher performance.

Micron has defined the vendor-specific PHYSICAL CAPACITY MANAGEMENT command to perform physical space configuration. The PHYSICAL CAPACITY MANAGEMENT command is a vendor-specific NVMe ADMIN command. This command provides operations that are outside the scope of the NVMe standard and which, to date, have been implemented by multiple companies in vendor-specific ways. This command makes use of concepts defined in the NVMe standard.

See also Micron's technical note, TN-FD-49: 2100AI/AT Physical Capacity Management on www.micron.com. Alternatively, consult your sales representative for more information.

Endurance (SLC Mode)

Table 7: Total Bytes Written

SLC Mode Size [%]	Total Bytes Written (in Terabytes) TLC Vs. SLC				
	64GB	128GB	256GB	512GB	1024GB
0% (Default)	30 / 0	60 / 0	120 / 0	240 / 0	480 / 0
10%	27 / 50	54 / 100	108 / 200	216 / 400	432 / 800
20%	24 / 100	48 / 200	96 / 400	192 / 800	384 / 1600
30%	21 / 150	42 / 300	84 / 600	168 / 1200	336 / 2400
40%	18 / 200	36 / 400	72 / 800	144 / 1600	288 / 3200
50%	15 / 250	30 / 500	60 / 1000	120 / 2000	240 / 4000
100%	0 / 500	0 / 1000	0 / 2000	0 / 4000	0 / 8000

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Logical Block Address Configuration (SLC Mode)

Table 8: SLC LBA Settings

SLC Mode Size [%]	Total 512 - Byte LBA				
	64GB	128GB	256GB	512GB	1024GB
0% (Default)	0	0	0	0	0
10%	4,182,128	8,343,088	16,684,552	33,347,944	66,694,256
20%	8,343,088	16,684,552	33,347,944	66,694,256	133,367,344
30%	12. 523.592	25,026,016	50,030,864	100,040,568	200,059,976
40%	16,684,552	33,347,944	66,694,256	133,367,344	266,733,064
50%	20,845,520	41,689,408	83,357,648	166,713,664	333,406,160
100%	41,689,408	83,357,648	166,713,664	333,406,160	666,810,688

Table 9: TLC LBA Settings

SLC Mode Size [%]	Total 512 - Byte LBA				
	64GB	128GB	256GB	512GB	1024GB
0% (Default)	125,045,424	250,069,680	500,118,192	1,000,215,216	2,000,409,264
10%	112,542,992	225,064,824	450,108,488	900,195,808	1,800,370,448
20%	100,040,568	200,059,976	400,098,784	800,176,400	1,600,331,640
30%	87,538,144	175,055,120	350,089,080	700,157,000	1,400,292,832
40%	75,035,720	150,050,272	300,079,376	600,137,592	1,200,254,024
50%	62,533,296	125,045,424	250,069,680	500,118,192	1,000,215,216
100%	0	0	0	0	0

Table 10: Total LBA Settings

SLC Mode Size [%]	Total 512 - Byte LBA				
	64GB	128GB	256GB	512GB	1024GB
0% (Default)	125,045,424	250,069,680	500,118,192	1,000,215,216	2,000,409,264
10%	116,725,120	233,407,912	466,793,040	933,543,752	1,867,064,704
20%	108,383,656	216,744,528	433,446,728	866,870,656	1,733,698,984
30%	100,061,736	200,081,136	400,119,964	800,197,568	1,600,352,808
40%	91,720,272	183,398,216	366,773,632	733,504,936	1,466,987,088
50%	83,378,816	166,734,832	333,427,328	666,831,856	1,333,621,376
100%	41,689,408	83,357,648	166,713,664	333,406,160	666,810,688

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Performance (SLC Mode)

For SSDs designed for the client and cloud computing markets, Micron specifies performance in fresh-out-of-box (FOB) state and steady state. Data throughput measured in steady state may be lower than FOB state, depending on the nature of the data workload.

For a description of these performance states and of Micron's best practices for performance measurement, refer to Micron's technical marketing brief, Best Practices for SSD Performance Measurement, on www.micron.com.

Table 11: Drive Performance (SLC Mode = 100%) – Fresh Out of Box (PCIe 3.0 and x4 Lanes)

Nominal Capacity Vs. Actual Capacity	64GB		128GB		256GB		512GB		1024GB		Unit
	21GB		42GB		85GB		170GB		341GB		
Parameter	HMB Off	HMB On	HMB Off	HMB On	HMB Off	HMB On	HMB Off	HMB On	HMB Off	HMB On	
Sequential read (128KB transfer)	550	550	1100	1100	2000	2000	2000	2000	2000	2000	MB/s
Sequential write (128KB transfer)	250	250	500	500	1000	1000	1700	1700	1800	1800	MB/s
Random read (4KB transfer)	12K	25K	20K	50K	38K	100K	65K	170K	105K	200K	IOPS
Random write (4KB transfer)	48K	48K	90K	100K	160K	185K	170K	190K	189K	210K	IOPS
READ latency (TYP)	85	85	85	85	85	85	85	85	85	85	µs
WRITE latency (TYP)	40	40	40	40	40	40	40	40	40	40	µs

Notes: 1. Performance values measured in fresh-out-of-box (FOB) state using FIO with a queue depth of 32.
2. Drive write cache enabled.
3. NVMe power state 0.
4. 4KB transfers with a queue depth of 1 are used to measure READ/WRITE latency values.
5. 4KB transfers can be further improved with the support of HMB by the host.
6. System variations will affect measured results.

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Component Electrical Characteristics

Environmental conditions beyond those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

BGA Type

Table 12: Operating Ratings

Parameter / Condition	Nominal	Min	Max	Unit
PWR_1[5]	3.3	2.97	3.63	V
PWR_2[5]	1.2	1.14	1.26	V
PWR_3[5]	0.9	0.86	0.945	V
Operating temperature[1,4]	T_C	–40	105	°C
Sensor temperature[2,3]	T_S	–55	135	°C
Non-operating ambient temperature	–	–40	105	°C
Relative humidity (non-condensing)	–	5	95	%

Notes: 1. Operating temperature is the case surface temperature at the center of the top side of the device.
2. Temperature is measured by SMART. Sensor temperature represents the T_J of the SSD micro-controller. The reported temperature is expected to be slightly greater than the operating temperature, T_C. The temperature difference will be highest at heavy workload and without air-flow.
3. If SMART temperature (Log Identifier 02h) exceeds 115°C, performance will be throttled. Sensor temperature range has been characterized on limited samples.
4. Refer to Micron's technical note, TN-00-08: Thermal Applications for method and the criteria to ensure that the memory operates below its maximum allowable temperature.
5. Refer to Micron's technical note, TN-FD-50: 2100AI/AT SSD Power Supply Electrical Requirements for further information about power-on/off and power hold-off requirements for a robust design.

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Table 13: Power Consumption

Capacity	NVMe Power State 4 (PS4)	NVMe Power State 3 (PS3)	NVMe Power State 0 (PS0)			Unit
			Idle Power (IDLP)	Active Reads	Active Writes	
64GB	3	<80	<100	<3000	<3000	mW
128GB	3	<80	<100	<3000	<3000	mW
256GB	3	<80	<100	<3000	<3000	mW
512GB	3	<80	<150	<3000	<4000	mW
1024GB	3	<80	<200	<3000	<5000	mW

Notes: 1. Active reads/active writes power is an average power measurement performed using FIO with 128KB sequential read/write transfers respectively.
2. PCIe bus is set to L1.2 link state for PS4, PS3 and IDLP power measurements.

Table 14: Maximum Current per Power Rail

Parameter / Capacity	64GB		128GB		256GB		512GB		1024GB		Unit
	Active Read	Active Write	Active Read	Active Write	Active Read	Active Write	Active Read	Active Write	Active Read	Active Write	
PWR_1	75	75	115	115	170	165	175	290	195	290	mA
PWR_2	130	110	160	125	240	150	405	295	420	330	mA
PWR_3	1555	1295	1475	1220	1575	1320	1535	1280	1600	1345	mA

Notes: 1. The data is obtained from limited samples.
2. Average maximum current over any 8ms time interval.

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Modules Electrical Characteristics

Environmental conditions beyond those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

M.2 Type

Table 15: Operating Ratings

Parameter / Condition	Nominal	Min	Max	Unit
3.3V	3.3V	3.135	3.465	V
Power hold-off time after NVMe initialization[6]	–	1	–	s
Power hold-off period for delayed NVMe initialization[4, 6]	–	CAP.TO	–	s
Power-off minimum time[5]	–	1	–	s
Operating temperature[1]	T_C	–40	105	°C
Sensor temperature[2, 3]	T_S	–55	135	°C
Non-operating ambient temperature	–	–40	105	°C
Relative humidity (non-condensing)	–	5	95	%

Notes: 1. Operating temperature is the case surface temperature at the center of the top side of the device.
2. If SMART temperature (log identifier 02h) exceeds 115°C, performance will be throttled.
3. Temperature measured by SMART. Sensor temperature range has been characterized on limited samples.
4. Host will wait a minimum of *CAP.TO* seconds before power cycling the SSD. *CAP.TO* is located in PCI BAR0, Offset 00h, Bit [31:24] Timeout.
5. Each power supply must remain below 100mV for at least 1 second before the next power-on sequence.
6. Power hold-off conditions violation can be tolerated for a limited amount of times.

Table 16: Power Consumption

Capacity	NVMe Power State 4 (PS4)	NVMe Power State 3 (PS3)	NVMe Power State 0 (PS0)			Unit
			Idle Power (IDLP)	Active Reads	Active Writes	
128GB	5	<80	<100	<3000	<3000	mW
256GB	5	<80	<100	<3000	<3000	mW
512GB	5	<80	<150	<3000	<4000	mW
1024GB	5	<80	<200	<3000	<5000	mW

Notes: 1. Active reads/active writes power is an average power measurement performed using FIO with 128KB sequential read/write transfers.
2. PCIe bus is set to L1.2 link state for PS4, PS3 and IDLP power measurements.

Table 17: Shock and Vibration

Parameter	Specification
Nonoperating shock	1500G @ 0.5ms half sine
Nonoperating vibration	Random vibration 7–2000Hz

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Identify – Identify Controller Data Structure

Table 18: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
01:00	1344h	**PCI Vendor ID (VID):** Contains the Micron identifier assigned by the PCI SIG.
03:02	1344h	**PCI Subsystem Vendor ID (SSVID):** Contains the Micron identifier assigned by the PCI SIG for the subsystem.
23:04	Variable	**Serial Number (SN):** Contains the serial number for the NVM subsystem as an ASCII string.
63:24	Variable	**Model Number (MN):** Contains the model number for the NVM subsystem as an ASCII string.
71:64	Variable	**Firmware Revision (FR):** Contains the currently active firmware revision for the NVM subsystem.
72	06h	**Recommended Arbitration Burst (RAB):** This is the recommended arbitration burst size.
75:73	00h-A0h-75h	**IEEE OUI Identifier (IEEE):** Contains the organization unique identifier (24-bit OUI MA-L format).
76	00h	**Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC):** This field specifies multipath I/O and namespace sharing capabilities of the controller and NVM subsystem. Bits 7:3 are reserved Bit 2 = 0 the controller is associated with a PCI function Bit 1 = 0 the NVM subsystem contains only a single controller Bit 0 = 0 the NVM subsystem contains only a single PCI Express port
77	06h	**Maximum Data Transfer Size (MDTS):** This field indicates the maximum data transfer size between the host and the controller. The host should not submit a command that exceeds this transfer size. If a command is submitted that exceeds the transfer size, then the command is aborted with a status of Invalid Field in command. The value is in units of the minimum memory page size (4096 bytes) and is reported as a power of two (2^n).
79:78	0000h	**Controller ID (CNTLID):** Contains the NVM subsystem unique controller identifier associated with the controller.
83:80	10300h	**Version (VER):** This register indicates the major and minor version of the NVM Express specification that the controller implementation supports.
87:84	000249F0h	**RTD3 Resume Latency (RTD3R):** This field indicates the typical latency in micro-seconds resuming from Runtime D3 (RTD3).
91:88	00013880h	**RTD3 Entry Latency (RTD3E):** This field indicates the typical latency in microsec-onds to enter Runtime D3 (RTD3).
95:92	00000200h	**Optional Asynchronous Events Supported (OAES):** This field indicates the optional asynchronous events supported by the controller. A controller will not send optional asynchronous events before they are enabled by host software. Bits 31:10 are reserved Bit 9 = 1 the controller support sending firmware activation notices Bit 8 = 0 the controller does not support the namespace attribute changed event Bits 7:0 are reserved
239:96	–	Reserved
239:100	–	Reserved

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Table 18: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
255:240	–	Reserved
257:256	0000000000011111b	**Optional Admin Command Support (OACS):** This field indicates the optional admin commands supported by the controller. Bits 15:5 are reserved. Bit 4 = 1 the controller supports the DEVICE SELF TEST (DST) command Bit 3 = 1 the controller support the NAMESPACE MANAGEMENT and NAMESPACE ATTACHMENT commands Bit 2 = 1 the controller supports the FIRMWARE COMMIT and FIRMWARE IMAGE DOWNLOAD commands Bit 1 = 1 the controller supports the FORMAT NVM command Bit 0 = 1 the controller supports the SECURITY SEND and SECURITY RECEIVE commands
258	00h	**Abort Command Limit (ACL):** This field is used to convey the maximum number of concurrently outstanding ABORT commands supported by the controller. This is a 0's based value.
259	08h	**Asynchronous Event Request Limit (AERL):** This field is used to convey the maximum number of concurrently outstanding ASYNCHRONOUS EVENT REQUEST commands supported by the controller. This is a 0-based value.
260	00010010b	**Firmware Updates (FRMW):** This field indicates capabilities regarding firmware updates. Bits 7:5 are reserved Bit 4 = 1 the controller supports firmware activation without a reset Bits 3:1 = 1 the controller supports one single firmware slot Bit 0 = 0 the first firmware slot (slot 1) is read/write
261	00010010b	**Log Page Attributes (LPA):** This field indicates optional attributes for log pages that are accessed via the GET LOG PAGE command. Bits 7:4 are reserved. Bit 3 = 0 “Telemetry Host/Controller-Initiated Log Pages” not supported Bit 2 = 1 the controller supports extended data for Get Log Page (including extended Number of Dwords and Log Page Offset fields) Bit 1 = 1 the controller supports the Command Effects log page Bit 0 = 0 the controller does not support the SMART/Health Information log page on a per namespace basis
262	3Fh	**Error Log Page Entries (ELPE):** This field indicates the number of Error Information log entries that are stored by the controller. This field is a 0-based value.
263	4h	**Number of Power States Support (NPSS):** This field indicates the number of NVM Express power states supported by the controller. This is a 0-based value.
264	1	Reserved
265	00000001b	**Autonomous Power State Transition Attributes (APSTA):** This field indicates the attributes of the autonomous power state transition feature. Bits 7:1 are reserved Bit 0 = 1 the controller supports autonomous power state transitions
267:266	184h	**Warning Composite Temperature Threshold (WCTEMP):** This field indicates the minimum Composite Temperature field value (temperature value reported in the SMART/Health Information log) that indicates an overheating condition during which controller operation continues. Immediate remediation is recommended (for example, additional cooling or workload reduction). The platform should strive to maintain a composite temperature below this value.

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Table 18: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
269:268	18Ch	**Critical Composite Temperature Threshold (CCTEMP):** This field indicates the minimum Composite Temperature field value (temperature value reported in the SMART/Health Information log) that indicates a critical overheating condition (for example, automatic device shutdown).
271:270	32h	**Maximum Time for Firmware Activation (MTFA):** This field ndicates the maximum time the controller temporarily stops processing commands to activate the firmware image. The value is specified in 100 millisecond units.
275:272	4000h	**Host Memory Buffer Preferred Size (HMPRE)**
279:276	2000h	**Host Memory Buffer Minimum Size (HMMIN)**
295:280	Density specific	**Total NVM Capacity (TNVMCAP):** Total NVM capacity depends on density: 0xEE8156000 (64GB), 0x1DCF856000 (128GB), 0x3B9E656000 (256GB), 0x773C256000 (512GB), 0xEE77A56000 (1024GB)
311:296	Density specific	**Unallocated NVM Capacity (UNVMCAP):** Unallocated NVM Capacity is supported. Value change runtime depending on SSD usage.
315:312	00000001h	**Replay Protected Memory Block Support (RPMBS):** One single replay protected memory block partition is supported.
317:316	000Ah	**Extended Device Self-test Time (EDSTT):** This field indicates the nominal amount of time in one minute units that the controller takes to complete an extended DEVICE SELF TEST operation when in power state 0.
318	1	**Device Self-test Options (DSTO):** This field indicates the controller supports one DEVICE SELF TEST operation in progress at a time.
319	00h	**Firmware Update Granularity (FWUG):** This field indicates the controller supports the Firmware Upgrade Granularity.
321:320	0	**Keep Alive Support (KAS)** is not supported.
323:322	0001h	**Host Controlled Thermal Management Attributes (HCTMA):**This field indicates the attributes of the host controlled thermal management feature. Bits 15:1 are reserved Bit 0 = 1 the controller supports host-controlled thermal management
325:324	0111h (273K = 0°C)	**Minimum Thermal Management Temperature (MNTMT):** This field indicates the minimum temperature, in degrees Kelvin, that the host may request in the Thermal Management Temperature 1 field and Thermal Management Temperature 2 field of a SET FEATURES command.
327:326	0184h (388K = 115°C)	**Maximum Thermal Management Temperature (MXTMT):** This field indicates the maximum temperature, in degrees Kelvin, that the host may request in the Thermal Management Temperature 1 field and Thermal Management Temperature 2 field of a SET FEATURES command.
331:328	0007h	**Sanitize Capabilities (SANICAP):** This field indicates attributes for SANITIZE operations. If the SANITIZE command is supported, this field will be non-zero.
511:332	–	Reserved
512	66h	**Submission Queue Entry Size (SQES):** This field defines the required and maximum submission queue entry size when using the NVM command set. Bits 7:4 = 6 defines the maximum submission queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n) Bits 3:0 = 6 defines the required submission queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n)

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Table 18: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
513	44h	**Completion Queue Entry Size (CQES):** This field defines the required and maximum completion queue entry size when using the NVM command set. Bits 7:4 = 4 defines the maximum completion queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n) Bits 3:0 = 4 defines the required completion queue entry size when using the NVM command set. The value is in bytes and is reported as a power of two (2^n)
515:514	0	**Maximum Outstanding Commands (MAXCMD)** is not supported.
519:516	4	**Number of Namespaces (NN):** This field defines the maximum number of valid namespaces present for the controller.
521:520	0000000001010101b	**Optional NVM Command Support (ONCS):** This field indicates the optional NVM commands and features supported by the controller. Bits 15:7 are reserved. Bit 6 = 1 timestamp supported Bit 5 = 0 the controller does not support reservations Bit 4 = 1 the controller supports the save field in the SET FEATURES command and the select field in the GET FEATURES command Bit 3 = 0 the controller does not support the WRITE ZEROS command Bit 2 = 1 the controller supports the DATASET MANAGEMENT command Bit 1 = 0 the controller does not support the WRITE UNCORRECTABLE command Bit 0 = 1 the controller support the COMPARE command
523:522	0	**Fused Operation Support (FUSES)** is not supported.
524	00000111b	**Format NVM Attributes (FNA):** This field indicates attributes for the FORMAT NVM command. Bits 7:3 are reserved Bit 2 = 1 indicates cryptographic erase is supported as part of the secure erase functionality Bit 1 = 1 user data erase of a particular namespace as part of a format results in a user data erase of all namespaces Bit 0 = 1 all namespaces will be configured with the same attributes and a format of any namespace results in a format of all namespaces
525	00000001b	**Volatile Write Cache (VWC):** This field indicates attributes related to the presence of a volatile write cache in the implementation. Bits 7:1 are reserved Bit 0 = 1 volatile write cache is present. The host may issue FLUSH commands and control whether the volatile write cache is enabled with SET FEATURES specifying the volatile write cache feature identifier.
527:526	0	**Atomic Write Unit Normal (AWUN)** is not supported.
529:528	0	**Atomic Write Unit Power Fail (AWUPF)** is not supported.
530	1	**NVM Vendor Specific Command Configuration (NVSCC)**
531	–	Reserved
533:532	0	**Atomic Compare & Write Unit (ACWU)** is not supported.
535:534	–	Reserved
539:536	0	**SGL Support (SGLS):** SGL is not supported.
767:540	–	Reserved
1023:768	Variable	**NVM Subsystem NVMe Qualified Name (SUBNQN):** This field specifies the NVM Subsystem NVMe Qualified Name as a UTF-8 null-terminated string.

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Table 18: Identify – Identify Controller Data Structure

Bytes	Default Value	Description
2047:1024	–	Reserved
2079:2048	Density specific	**Power State 0 Descriptor (PSD0):** This field indicates the characteristics of power state 0. The format of this field is defined in the table.
2111:2080	Density specific	**Power State 1 Descriptor (PSD1):** This field indicates the characteristics of power state 1. The format of this field is defined in the table.
2143:2112	Density specific	**Power State 2 Descriptor (PSD2):** This field indicates the characteristics of power state 2. The format of this field is defined in the table.
2175:2144	MU04:30303030000271 000001388030008DEh MU01.1:303030300003A 9800001F40030008DEh	**Power State 3 Descriptor (PSD3):** This field indicates the characteristics of power state 3. The format of this field is defined in the table.
2207:2176	40404040000C35000002 71003000082h	**Power State 4 Descriptor (PSD4):** This field indicates the characteristics of power state 4. The format of this field is defined in the table.
327F:2208	–	Reserved.
3280	Variable	**Physical Capacity Management Attribute (PCMA):** This field indicates the attributes and support of the physical capacity management feature.
3281	Variable	**Maximum Namespaces in SLC Physical Configuration (MNSPC):** This field indicates the maximum amount of namespaces the SLC physical space can support in the current physical configuration.
3282	Variable	**Maximum Namespace in TLC Physical Configuration (MNTPC):** This field indicates the maximum amount of namespaces the TLC physical space can support in the current physical configuration.
3298:3283	Variable	**Total SLC NVM Capacity (TSNCAP):** This field indicates the total SLC NVM capacity in the NVM subsystem for the current physical configuration. The value is in bytes.
3314 : 3299	Variable	**Total TLC NVM Capacity (TTNCAP):** This field indicates the total TLC NVM capacity in the NVM subsystem for the current physical configuration. The value is in bytes.
4095:3315	–	Reserved

Table 19: Power State Descriptor Data Structure

Bits	Description
15:0	**Maximum Power (MP):** This field indicates the maximum power consumed by the NVM subsystem in this power state. The power in watts is equal to the value in this field multiplied by the scale specified in the Maximum Power Scale field.
23:16	Reserved
24	**Max Power Scale (MPS):** This field indicates the scale for the Maximum Power field. If this field is cleared to 0, then the scale of the Maximum Power field is in 0.01 watts. If this field is set to 1, then the scale of the Maximum Power field is in 0.0001 watts.
25	**Nonoperational State (NOPS):** This field indicates whether the controller processes I/O commands in this power state. If this field is cleared to 0, then the controller processes I/O commands in this power state. If this field is set to 1, then the controller does not process I/O commands in this power state.
31:26	Reserved
63:32	**Entry Latency (ENLAT):** This field indicates the maximum entry latency in microseconds associated with entering this power state.

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Table 19: Power State Descriptor Data Structure (Continued)

Bits	Description
95:64	**Exit Latency (EXLAT):** This field indicates the maximum exit latency in microseconds associated with exiting this power state.
100:96	**Relative Read Throughput (RRT):** This field indicates the relative read throughput associated with this power state. A lower value means higher read throughput.
103:101	Reserved
108:104	**Relative Read Latency (RRL):** This field indicates the relative READ latency associated with this power state. A lower value means lower READ latency.
111:109	Reserved
116:112	**Relative Write Throughput (RWT):** This field indicates the relative write throughput associated with this power state. A lower value means higher write throughput.
119:117	Reserved
124:120	**Relative Write Latency (RWL):** This field indicates the relative WRITE latency associated with this power state. A lower value means lower WRITE latency.
127:125	Reserved
143:128	**Idle Power (IDLP):** This field indicates the typical power consumed by the NVM subsystem over 30 seconds in this power state when idle. The measurement starts after the NVM subsystem has been idle for 10 seconds. The power in watts is equal to the value in this field multiplied by the scale indicated in the Idle Power Scale field.
149:144	Reserved
151:150	**Idle Power Scale (IPS):** This field indicates the scale for the Idle Power field.
159:152	Reserved
175:160	**Active Power (ACTP):** This field indicates the largest average power consumed by the NVM subsystem over a 10 second period in this power state with the workload indicated in the Active Power Workload field. The power in watts is equal to the value in this field multiplied by the scale indicated in the Active Power Scale field.
178:176	**Active Power Workload (APW):** This field indicates the workload used to calculate maximum power for this power state.
181:179	Reserved
183:182	**Active Power Scale (APS):** This field indicates the scale for the Active Power field.
255:184	Reserved

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Identify – Identify Namespace Data Structure

Table 20: Identify – Identify Namespace Data Structure

Byte	Default Value	Description
07:00	Variable	**Namespace Size (NSZE):** This field indicates the total size of the namespace in logical blocks. A namespace of size *n* consists of LBA 0 through (*n* - 1). The number of logical blocks is based on the formatted LBA size.
15:08	Variable	**Namespace Capacity (NCAP):** This field indicates the maximum number of logical blocks that may be allocated in the namespace at any point in time. The number of logical blocks is based on the formatted LBA size. A logical block is allocated when it is written with a WRITE or WRITE UNCORRECTABLE command. A logical block may be deallocated using the DATASET MANAGEMENT command.
23:16	Variable	**Namespace Utilization (NUSE):** This field indicates the current number of logical blocks allocated in the namespace. This field is equal to the Namespace Capacity field. The number of logical blocks is based on the formatted LBA size. When using the NVM command set: A logical block is allocated when it is written with a WRITE or WRITE UNCORRECTABLE command. A logical block may be deallocated using the DATASET MANAGEMENT command.
24	00000100b	**Namespace Features (NSFEAT):** This field defines features of the namespace. Bits 7:4 are reserved Bit 3 = 0 the NGUID and EUI64 fields for this namespace are reused by the controller Bit 2 = 1 the controller does support the Deallocated or Unwritten Logical Block error Bit 1 = 0 the controller does not support the fields NAWUN, NAWUPF, and NACWU for the namespace Bit 0 = 0 thin provisioning is not supported, the Namespace Size and Namespace Capacity fields report the same value
25	0	**Number of LBA Formats (NLBAF):** This field defines the number of supported LBA data sizes supported by the namespace. This is a 0-based value.
26	00000000b	**Formatted LBA Size (FLBAS):** This field indicates the LBA data size with which the namespace has been formatted. Bits 7:5 are reserved Bit 4 = 0 the controller does not support metadata Bits 3:0 = 0 indicates one of the two supported LBA formats indicated in this data structure
27	0	**Metadata Capabilities (MC)** is not supported.
28	0	**End-to-end Data Protection Capabilities (DPC)** is not supported.
29	0	**End-to-end Data Protection Type Settings (DPS)** is not supported.
30	0	**Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)** is not supported.
31	0	**Reservation Capabilities (RESCAP)** is not supported.
32	1VVVVVVVb	**Format Progress Indicator (FPI):** If a format operation is in progress, this field indicates the percentage of the namespace that remains to be formatted. Bit 7 = 1 the namespace supports the Format Progress Indicator defined by bits 6:0 in this field Bits 6:0 = Variable indicates the percentage of the namespace that remains to be formatted. (For example, a value of 25 indicates that 75% of the namespace has been formatted and 25% remains to be formatted.) A value of 0 indicates that the namespace is formatted with the format specified by the FLBAS field in this data structure.
33	–	Reserved
35:34	0	**Namespace Atomic Write Unit Normal (NAWUN)** is not supported.
37:36	0	**Namespace Atomic Write Unit Power Fail (NAWUPF)** is not supported.

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Table 20: Identify – Identify Namespace Data Structure

Byte	Default Value	Description
39:38	0	**Namespace Atomic Compare & Write Unit (NACWU)** is not supported.
41:40	0	**Namespace Atomic Boundary Size Normal (NABSN)** is not supported.
43:42	0	**Namespace Atomic Boundary Offset (NABO)** is not supported.
45:44	0	**Namespace Atomic Boundary Size Power Fail (NABSPF)** is not supported.
47:46	–	Reserved
63:48	Variable	**NVM Capacity (NVMCAP):** This field indicates the total size of the NVM allocated to this namespace. The value is in bytes.
103:64	–	Reserved
119:104	Variable	**Namespace Globally Unique Identifier (NGUID):** This field contains the 128-bit Name-space Globally Unique Identifier value.
127:120	Variable	**IEEE Extended Unique Identifier (EUI64):** This field contains the 64-bit IEEE Extended Unique Identifier value.
131:128	90000	**LBA Format 0 Support (LBAF0)**
135:132	–	**LBA Format 1 Support (LBAF1)** is not supported.
139:136	–	**LBA Format 2 Support (LBAF2)** is not supported.
... – ...	–	**...**
191:188	–	**LBA Format 15 Support (LBAF15)** is not supported
383:192	–	Reserved
384	Variable	**Namespace Physical NAND Configuration (NPNC):** Bits 7:2 are reserved Bit 1 = 1 for TLC operation Bit 0 = 1 for SLC operation of the Namespace
4095:385	–	Vendor specific

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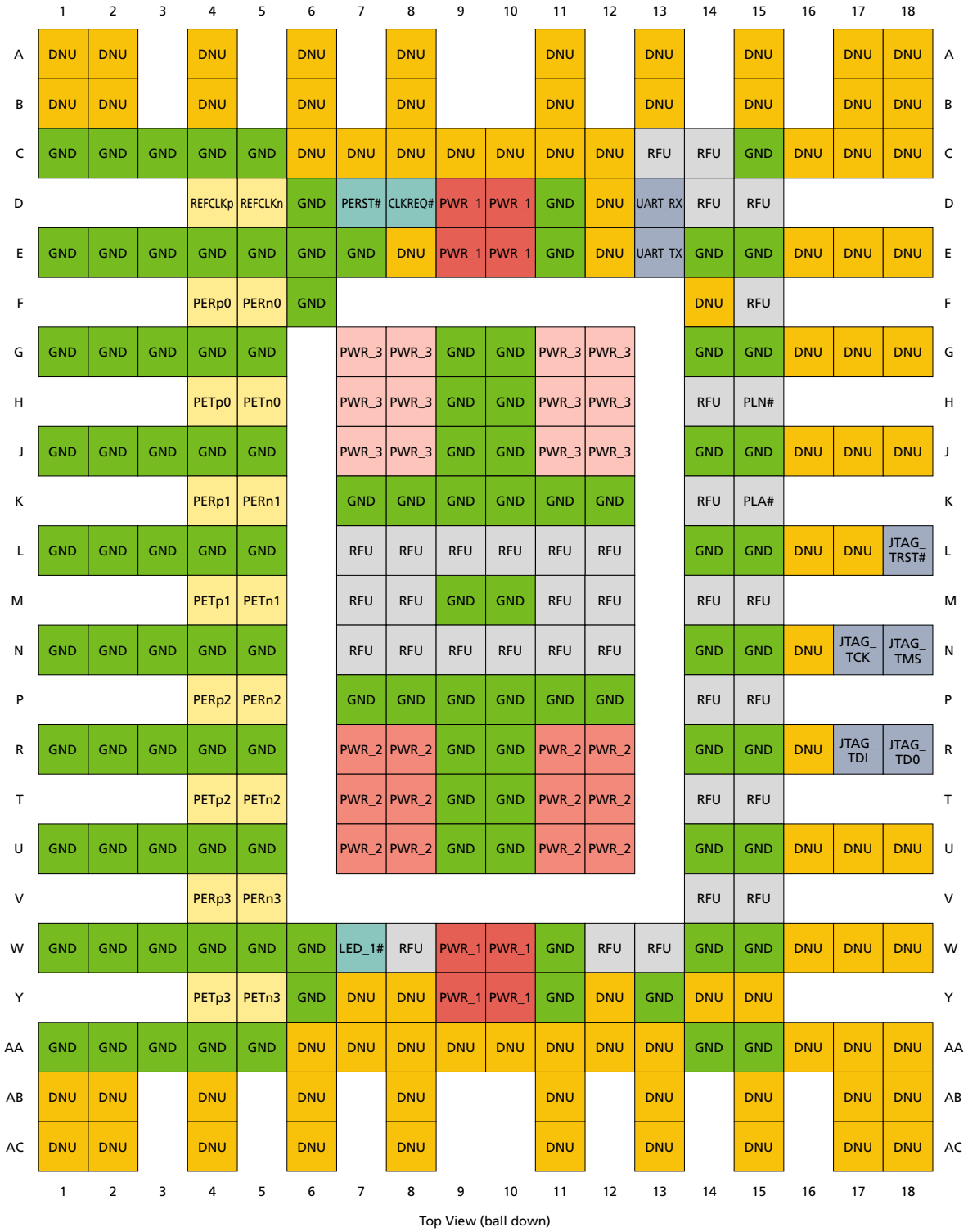
Interface Signals

BGA Type

Figure 3: Ballmap - BGA Type (Top View)



Top View (ball down)

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Table 21: BGA Signal Descriptions

Name	Type	Power Domain	Description
PETp0, PETn0	O		PCIe TX+ Lane 0, PCIe TX- Lane 0
PERp0, PERn0	I		PCIe RX+ Lane 0, PCIe RX- Lane 0
PETp1, PETn1	O		PCIe TX+ Lane 1, PCIe TX- Lane 1. It can be left floating
PERp1, PERn1	I		PCIe RX+ Lane 1, PCIe RX- Lane 1. It can be left floating
PETp2, PETn2	O		PCIe TX+ Lane 2, PCIe TX- Lane 2. It can be left floating
PERp2, PERn2	I		PCIe RX+ Lane 2, PCIe RX- Lane 2. It can be left floating
PETp3, PETn3	O		PCIe TX+ Lane 3, PCIe TX- Lane 3. It can be left floating
PERp3, PERn3	I		PCIe RX+ Lane 3, PCIe RX- Lane 3. It can be left floating
REFCLKp, REFCLKn	I		100 MHz reference clock+, 100 MHz reference clock–
CLKREQ#	OD	(1.8V)	Clock request
PERST#	I	(1.8V)	PCIe fundamental reset
LED_1#	OD	3.3V	Status indicator for system LED; optional for customer. It can use 100 ohms to LED tied to 3.3V
UART_RX	I	3.3V	Engineering test. It can be left floating[1]
UART_TX	O	3.3V	Engineering test. It can be left floating[1]
JTAG_TRST#	I	3.3V	Engineering test. It can be left floating[1]
JTAG__TDI	I	3.3V	Engineering test. It can be left floating[1]
JTAG__TDO	O	3.3V	Engineering test. It can be left floating[1]
JTAG__TCK	I	3.3V	Engineering test. It can be left floating[1]
JTAG__TMS	I	3.3V	Engineering test. It can be left floating[1]
PLN#	I	3.3V[6]	Power loss notification. Pull-up when not driven.
PLA#	O	3.3V[6]	Power loss acknowledgment (default HIGH).
PWR_1	I		3.3V power [7]
PWR_2	I		1.2V power
PWR_3	I		0.9V power
RFU	N/A	N/A	Reserved for future use[2]
DNU	N/A	N/A	Do not use[3]

Notes: 1. Engineering test signal should be routed to a test point pad. They are not intended for customer use because they have controlled access to insure security of data.
2. RFU signals are reserved for future use. These balls will be soldered to a platform board, but shall be electrically no-connect on the host or the module.
3. DNU signals are for manufacturing only. These balls will be soldered to a platform board, but will be electrically no connect on the host or the module.
4. Power domain (1.8V) is internally generated by an LDO.
5. Each PCIe in-band signal (PETxy/PERxy) requires AC coupling capacitance (75nF–500nF) close to the transmitter.
6. We recommend making a design compatible with both 3.3V and 1.8V.
7. We recommend making a design compatible with 2.5V for next generation SSD.

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Interface Connectors

M.2 Type

Figure 4: Connector - M.2 Type

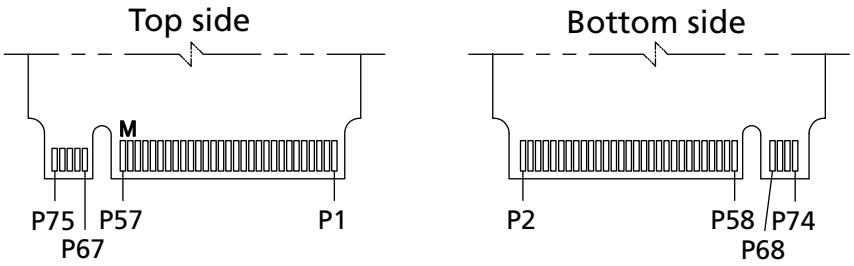

Table 22: Signal Assignments

Top Side			Bottom Side		
Pin #	**Signal Name**	**Description**	**Pin #**	**Signal Name**	**Description**
1	GND	Ground	2	3.3V	+3.3V
3	GND	Ground	4	3.3V	+3.3V
5	PETn3	PCIe TX– Lane 3	6	NC6	No connect
7	PETp3	PCIe TX+ Lane 3	8	PLN#	Power loss notification
9	GND	Ground	10	LED_1#	LED activity indicator
11	PERn3	PCIe RX– Lane 3	12	3.3V	+3.3V
13	PERp3	PCIe RX+ Lane 3	14	3.3V	+3.3V
15	GND	Ground	16	3.3V	+3.3V
17	PETn2	PCIe TX– Lane 2	18	3.3V	+3.3V
19	PETp2	PCIe TX+ Lane 2	20	NC20	No connect
21	GND	Ground	22	NC22	No connect
23	PERn2	PCIe RX– Lane 2	24	NC24	No connect
25	PERp2	PCIe RX+ Lane 2	26	NC26	No connect
27	GND	Ground	28	NC28	No connect
29	PETn1	PCIe TX– Lane 1	30	PLA#	Power loss acknowledge
31	PETp1	PCIe TX+ Lane 1	32	NC32	No connect
33	GND	Ground	34	NC34	No connect
35	PERn1	PCIe RX– Lane 1	36	NC36	No connect
37	PERp1	PCIe RX+ Lane 1	38	NC38	No connect
39	GND	Ground	40	NC40	No connect
41	PETn0	PCIe TX– Lane 0	42	NC42	No connect
43	PETp0	PCIe TX+ Lane 0	44	NC44	No connect
45	GND	Ground	46	NC46	No connect
47	PERn0	PCIe RX– Lane 0	48	NC48	No connect
49	PERp0	PCIe RX+ Lane 0	50	PERST#	PERST#

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Table 22: Signal Assignments (Continued)

Top Side			Bottom Side		
Pin #	**Signal Name**	**Description**	**Pin #**	**Signal Name**	**Description**
51	GND	Ground	52	CLKREQ#	CLKREQ#
53	REFCLKn	PCIe REFCLK–	54	PEWAKE#	No connect
55	REFCLKp	PCIe REFCLK+	56	UART_RX	Reserved – Engineering test
57	GND	Ground	58	UART_TX	Reserved – Engineering test
Mechanical M Key			**Mechanical M Key**		
67	NC67	No connect	68	SUSCLK	No connect
69	PEDET	No connect	70	3.3V	+3.3V
71	GND	Ground	72	3.3V	+3.3V
73	GND	Ground	74	3.3V	+3.3V
75	GND	Ground	–	–	–

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Commands

Table 23: Op Codes for Admin Commands

Codes not listed are reserved; All commands in the table are supported

Command Name	Op Code (hex)
DELETE I/O SUBMISSION QUEUE	00h
CREATE I/O SUBMISSION QUEUE	01h
GET LOG PAGE	02h
DELETE I/O COMPLETION QUEUE	04h
CREATE I/O COMPLETION QUEUE	05h
IDENTIFY	06h
ABORT	08h
SET FEATURES – SET ARBITRATION	09h - 01h
SET FEATURES – SET POWER MANAGEMENT	09h - 02h
SET FEATURES – SET LBA RANGE TYPE	09h - 03h
SET FEATURES – SET TEMPERATURE THRESHOLD	09h - 04h[1]
SET FEATURES – SET ERROR RECOVERY	09h - 05h
SET FEATURES – SET VOLATILE WRITE CACHE	09h - 06h
SET FEATURES – SET NUMBER OF QUEUES	09h - 07h
SET FEATURES – SET INTERRUPT COALESCE	09h - 08h
SET FEATURES – SET INTERRUPT VECTOR CONFIGURATION	09h - 09h
SET FEATURES – SET WRITE ATOMICITY	09h - 0Ah (not supported)
SET FEATURES – SET ASYNC EVENT CONFIGURATION	09h - 0Bh
SET FEATURES – SET AUTONOMOUS POWER STATE TRANSITION	09h - 0Ch
SET FEATURES – SET HOST MEMORY BUFFER	09h - 0Dh
SET FEATURES - TIMESTAMP	09h - 0Eh
SET FEATURES - KEEP ALIVE TIMER	09h - 0Fh (not supported)
SET FEATURES – HOST CONTROLLED THERMAL MANAGEMENT	09h - 10h
SET FEATURES – NON OPERATIONAL POWER STATE CONFIG	09h - 11h
SET FEATURES – SW PROGRESS MARKER	09h - 80h
SET FEATURES - RESERVATION PERSISTENCE	09h - 83h (not supported)
SET FEATURES – SET PLN/PLA FEATURES	09h - CAh
SET FEATURES – SLC REFLOW MFG STATE (Vendor Specific)	09h - C6h
SET FEATURES – BACKGROUND GARBAGE COLLECTION STATE	09h - DDh[2]
GET FEATURES – GET ARBITRATION	0Ah - 01h
GET FEATURES – GET POWER MANAGEMENT	0Ah - 02h
GET FEATURES – GET LBA RANGE TYPE	0Ah - 03h
GET FEATURES – GET TEMPERATURE THRESHOLD	0Ah - 04h[1]
GET FEATURES – GET ERROR RECOVERY	0Ah - 05h

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Command Name	Op Code (hex)
GET FEATURES – GET VOLATILE WRITE CACHE	0Ah - 06h
GET FEATURES – GET NUMBER OF QUEUES	0Ah - 07h
GET FEATURES – GET INTERRUPT COALESCE	0Ah - 08h
GET FEATURES – GET INTERRUPT VECTOR CONFIGURATION	0Ah - 09h
GET FEATURES – HOST CONTROLLED THERMAL MANAGEMENT	0Ah - 10h
GET FEATURES – NON OPERATIONAL POWER STATE CONFIG	0Ah - 11h
GET FEATURES – GET WRITE ATOMICITY	0Ah - 0Ah (not supported)
GET FEATURES – GET ASYNC EVENT CONFIGURATION	0Ah - 0Bh
GET FEATURES – GET AUTONOMOUS POWER STATE TRANSITION	0Ah - 0Ch
GET FEATURES – GET HOST MEMORY BUFFER	0Ah - 0Dh
GET FEATURES - TIMESTAMP	0Ah - 0Eh
GET FEATURES – SW PROGRESS MARKER	0Ah - 80h (not supported)
GET FEATURES – HOST IDENTIFIER	0Ah - 81h (not supported)
GET FEATURES – RESERVATION NOTIFICATION MASK	0Ah - 82h (not supported)
GET FEATURES – RESERVATION PERSISTENCE	0Ah - 83h (not supported)
GET FEATURES – SLC REFLOW MFG STATE (Vendor Specific)	0Ah - C6h
GET FEATURES – BACKGROUND GARBAGE COLLECTION STATE	09h - DDh[2]
ASYNCHRONOUS EVENT REQUEST	0Ch (not supported)
NAMESPACE MANAGEMENT	0Dh
FIRMWARE COMMIT / ACTIVATE	10h
FIRMWARE IMAGE DOWNLOAD	11h
DEVICE SELF TEST (DST)	14h
DIRECTIVE SEND	19h (not supported)
KEEP ALIVE	18h
DIRECTIVE RECEIVE	1Ah (not supported)
PHYSICAL CAPACITY MANAGEMENT (Vendor Specific)	C0h
LOCK PHYSICAL CONFIGURATION (Vendor Specific)	C4h
FORMAT NVM	80h
SECURITY SEND	81h
SECURITY RECEIVE	82h
SANITIZE - BLOCK ERASE	84h - 01h
SANITIZE - OVERWRITE	84h - 02h
SANITIZE - CRYPTO ERASE	84h - 03h

Notes: 1. Added light throttling feature. With MU05 firmware download, TMT1/TMT2 will be overwritten with the new default values of 0x0(Disabled)/0x184(115C); The previous default values were 0x184(115C)/0x0 (Disabled). No action for customers that are not changing the default values on previous firmware versions.
2. For workloads that are almost read only, background garbage collection can be enabled during idle time to avoid Read Disturb may occur over time; 0h - Background GC is Disabled (Default), 1h - Background GC is Enabled.

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Table 24: Op Codes for NVMe Commands

Codes not listed are reserved; All commands in the table are supported

Command Name	Op Code (hex)
FLUSH	00h
WRITE	01h
READ	02h
WRITE UNCORRECTABLE	04h (not supported)
COMPARE	05h[1]
WRITE ZEROs	08h (not supported)
DATASET MANAGEMENT – DEALLOCATE (AD)	09h[1]
DATASET MANAGEMENT – INTEGRAL DATA SET FOR WRITE (IDW)	09h[1]
DATASET MANAGEMENT – INTEGRAL DATA SET FOR READ (IDR)	09h[1]
RESERVATION REGISTER	0Dh (not supported)
RESERVATION REPORT	0Eh (not supported)
RESERVATION ACQUIRE	11h (not supported)
RESERVATION RELEASE	15h (not supported)

Notes: 1. 4KB LBA alignment is mandatory.

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Log Pages

The SSD supports log information as defined in the NVMe specification. Supported information is shown in the following tables:

- Error Information Log Entry (Log Identifier 01h)
- SMART/Health Information (Log Identifier 02h)
- Firmware Slot Information (Log Identifier 03h)
- Commands Supported and Effects (Log Identifier 05h)
- Device Self-Test Log (Log Identifier 06h)

Refer to *TN-FD-59: 2100AI/AT NVMe SMART and Vendor Unique Logs* for further details.

Table 25: Error Information Log Entry (Log Identifier 01h)

Bytes	Name	Description
7:0	Error count	This is a 64-bit incrementing error count, indicating a unique identifier for this error. The error count starts at 1h, is incremented for each unique error log entry, and is retained across power-off conditions. A value of 0h indicates an invalid entry; this value may be used when there are lost entries or when there are fewer errors than the maximum number of entries the controller supports.
9:8	Submission queue ID	This field indicates the submission queue identifier of the command associated with the error information. If the error is not specific to a particular command, then this field will be set to FFFFh.
11:10	Command ID	This field indicates the command Identifier of the command associated with the error. If the error is not specific to a particular command, then this field will be set to FFFFh.
13:12	Status field	This field indicates the status field for the command that completed. The status field is located in bits 15:01, bit 00 corresponds to the phase tag posted for the command. If the error is not specific to a particular command then this field reports the most applicable status value.
15:14	Parameter error location	This field indicates the byte and bit of the command parameter associated with the error, if applicable. If the parameter spans multiple bytes or bits, then the location indicates the first byte and bit of the parameter.
		Bit 7:0; Byte in command that contained the error. Valid values are 0 to 63.
		Bit 10:8; Bit in command that contained the error. Valid values are 0 to 7.
		Bit 15:11; Reserved.
		If the error is not specific to a particular command, then this field will be set to FFFFh.
23:16	LBA	This field indicates the first LBA that experienced the error condition, if applicable.
27:24	Namespace	This field indicates the namespace associated with the error, if applicable.
31:28	Reserved	Reserved
39:32	Command specific information	This field contains command specific information. If used, the command definition specifies the information returned.
63:40	Reserved	Reserved

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Table 26: SMART/Health Information (Log Identifier 02h)

Bytes	Name	Description
0	Critical warning	Indicates critical warnings for the state of the controller. Each bit corresponds to a critical warning type; multiple bits may be set. If a bit is cleared to 0, the critical warning does not apply. Critical warnings may result in an asynchronous event notification to the host.
		Bit 0; If set to 1, the available spare space has fallen below the threshold.
		Bit 1; If set to 1, the temperature has exceeded a critical threshold.
		Bit 2; If set to 1, the device reliability has been degraded due to significant media-related errors or any internal error that degrades device reliability.
		Bit 3; If set to 1, the media has been placed in read-only mode.
		Bit 4; If set to 1, the volatile memory backup device has failed.
		Bits 7:5; Reserved.
2:1	Temperature	Contains the temperature of the controller in units of Kelvin. If it exceeds the temperature threshold, an asynchronous event may be issued to the host.
3	Available spare	Contains a normalized percentage (0–100%) of the remaining available spare capacity.
4	Available spare threshold	When the available spare falls below the threshold indicated in this field, an asynchronous event may be issued to the host. The value is indicated as a normalized percentage (0–100%).
5	Percentage used	Contains an estimate of the percentage of the device life used based on the actual device usage and prediction of device life. A value of 100 indicates that the estimated endurance of the device has been consumed, but may not indicate a device failure. The value is allowed to exceed 100.
		Percentages greater than 254 will be represented as 255. This value will be updated once per power-on hour (when the controller is not in a sleep state).
31:6	Reserved	Reserved
47:32	Data units read	Contains the number of 512-byte data units the host has read from the controller; this value does not include metadata. This value is reported in thousands (that is, a value of 1 corresponds to 1000 units of 512 bytes read) and is rounded up. For the NVM command set, logical blocks read as part of COMPARE and READ operations will be included in this value.
63:48	Data units written	Contains the number of 512-byte data units the host has written to the controller; this value does not include metadata. This value is reported in thousands (that is, a value of 1 corresponds to 1000 units of 512 bytes written) and is rounded up. For the NVM command set, logical blocks written as part of WRITE operations will be included in this value.
79:64	Host READ commands	Contains the number of READ commands completed by the controller. For the NVM command set, this is the number of COMPARE and READ commands.
95:80	Host WRITE commands	Contains the number of WRITE commands completed by the controller. For the NVM command set, this is the number of WRITE commands.
111:96	Controller busy time	Contains the amount of time the controller is busy with I/O commands. The controller is busy when there is a command outstanding to an I/O queue (specifically, a command was issued via an I/O submission queue tail doorbell write and the corresponding completion queue entry has not yet been posted to the associated I/O completion queue. This value is reported in minutes.
127:112	Power cycles	Contains the number of POWER cycles.

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Table 26: SMART/Health Information (Log Identifier 02h) (Continued)

Bytes	Name	Description
143:128	Power on hours	Contains the number of power-on hours. This does not include time that the controller was powered and in a low-power state condition.
159:144	Unsafe shutdowns	Contains the number of unsafe shutdowns. This count is incremented when a shutdown notification (CC.SHN) is not received prior to loss of power.
175:160	Media and data integrity errors	Contains the number of occurrences where the controller detected an unrecovered data integrity error.
191:176	Number of error info log entries	Contains the number of error information log entries over the life of the controller.
195:192	Warning composite temperature time	Contains the amount of time in minutes that the controller is operational and the composite temperature is greater than or equal to the warning composite temperature threshold (WCTEMP) field and less than the critical composite temperature threshold (CCTEMP) field in the Identify controller data structure. If the value of the WCTEMP or CCTEMP field is 0h, then this field is always cleared to 0h regardless of the composite temperature value.
199:196	Critical composite temperature time	Contains the amount of time in minutes that the controller is operational and the composite temperature is greater the critical composite temperature threshold (CCTEMP) field in the Identify controller data structure. If the value of the CCTEMP field is 0h, then this field is always cleared to 0h regardless of the composite temperature value.
201:200	Temperature Sensor 1	Contains the highest NAND temperature.
215:202	Reserved	Reserved
219:216	Thermal Management Temperature 1 transition count	Contains the number of times the controller transitioned to lower power active power states or performed vendor-specific thermal management actions while minimizing the impact on performance in order to attempt to reduce the composite temperature because of the host-controlled thermal management feature. This counter will not wrap after it reaches its maximum value. A value of zero indicates that this transition has never occurred.
223:220	Thermal Management Temperature 2 transition count	Contains the number of times the controller transitioned to lower power active power states or performed vendor-specific thermal management actions regardless of the impact on performance in order to attempt to reduce the Composite Temperature because of the host-controlled thermal management feature. This counter will not wrap after it reaches its maximum value. A value of zero indicates that this transition has never occurred.
227:224	Total time for Thermal Management Temperature 1	Contains the number of seconds that the controller transitioned to lower power active power states or performed vendor-specific thermal management actions while minimizing the impact on performance in order to attempt to reduce the Composite Temperature because of the host-controlled thermal management feature. This counter will not wrap after it reaches its maximum value. A value of zero indicates that this transition has never occurred.
231:228	Total time for Thermal Management Temperature 2	Contains the number of seconds that the controller transitioned to lower power active power states or performed vendor-specific thermal management actions regardless of the impact on performance in order to attempt to reduce the composite temperature because of the host controlled thermal management feature. This counter will not wrap after it reaches its maximum value. A value of zero indicates that this transition has never occurred.
511:232	Reserved	Reserved

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Table 27: Firmware Slot Information (Log Identifier 03h)

Bytes	Name	Description
0	Active Firmware Info (AFI)	Specifies information about the active firmware revision. Bit 7 is reserved. Bits 6:4 indicates the firmware slot that is going to be activated at the next controller reset. Bit 3 is reserved. Bits 2:0 indicates the firmware slot from which the actively running firmware revision was loaded.
7:1	Reserved	Reserved
15:08	Firmware Revision for Slot 1 (FRS1)	Contains the revision of the firmware downloaded to firmware slot 1.
511:16	Reserved	Reserved

Table 28: Commands Supported and Effects (Log Identifier 05h)

Bytes	Name	Description
3:0	Admin Command Supported 0 (ACS0)	Contains the command effect data structure for the ADMIN command with an opcode value of 0h. The format of this field is defined by the NVM Express specification.
…	…	…
1023:1020	Admin Command Supported 255 (ACS255)	Contains the command effect data structure for the ADMIN command with an opcode value of 255. The format of this field is defined by the NVM Express specification.
1027:1024	I/O Command Supported 0 (IOCS0)	Contains the command effect data structure for the I/O command with an opcode value of 0h. The format of this field is defined by the NVM Express specification.
…	…	…
2047:2044	I/O Command Supported 255 (IOCS255)	Contains the command effect data structure for the I/O command with an opcode value of 255. The format of this field is defined by the NVM Express specification.
4095:2048	Reserved	Reserved

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Table 29: Device Self-Test Log (Log Identifier 06h)

Bytes	Name	Description
0	Current Device Self-Test Operation	Defines the current device self-test operation. Bits 7:4 are reserved. Bits 3:0 Value indicates the status of the current device self-test operation. Value 0h = No device self-test operation in progress. Value 1h = Short device self-test operation in progress. Value 2h = Extended device self-test operation in progress. Value Fh:3h = Reserved.
1	Current Device Self-Test Completion	Defines the completion status of the current device self-test. Bit 7 is reserved. Bits 6:0 indicates the percentage of the device self-test operation that is complete.
3:2	Reserved	Reserved
31:4	Newest Device Self-Test Result Data Structure	The format of this field is defined by the NVM Express specification.
…	…	…
563:536	20th Newest Device Self-Test Result Data Structure	The format of this field is defined by the NVM Express specification.

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TCG/Opal Support

Table 30: TCG/Opal Support Parameters

Property	Supported	Comments
TCG Storage Specifications		
OPAL: TCG Storage Security SubSystem Class	Specification 2.00	Revision 1.00, Feb 24, 2012
TCG Core Specification	Specification 2.00	Revision 2.00, Nov 4, 2011
TCG Storage Interface Interactions Specification	TCG Reference Specification	Specification Version 1.02 Revision 1.00 30 December, 2011
OPAL SSC 1.00 (backward compatibility)	Not supported	–
OPAL SSC Additional Feature Set Specification		
Additional DataStore Table	Supported	Specification 1.00 Revision 1.00, Feb 24, 2012
Single User Mode	Supported	Specification 1.00 Revision 1.00, Feb 24, 2012
TCG Storage Protection Mechanisms for Secrets	Supported	Specification Version 1.00 Revision 1.07 17 August, 2011
PSID – Physical Presence SID	Supported	Specification Version 1.00 Committee Draft Revision 1.05 February 9, 2011
GUDID (Globally Unique Serial Number)	Supported	Mandatory GUDID Proposal 11/03/2011 (Microsoft)
SID Authority Disable	Supported	SID Authority Disable Proposal 9/26/2011 (Microsoft)
Modifiable CommonName Columns	Supported	Modifiable CommonName Columns Proposal 7/22/2010 (Microsoft)
OPAL SSC Feature Set – Specific List		
ALL OPAL Mandatory Features	Supported	–
Close Session (optional)	Supported	Allows Tper to notify the host it has aborted a session
Restricted Command & Table (optional)	Not Supported	The interface control template enables Tper control over selected interface commands; the benefit is the reduction of undesired side effects
Type Table (not required)	Not Supported	–
Activate Method	Supported	–
Revert Method	Supported	–
Revert SP Method	Supported	–
Activate Method Within Transactions	Not Supported	As per OPAL, this behavior is out of the scope
Revert Method within Transactions	Not Supported	As per OPAL, this behavior is out of the scope
Revert SP Method within Transactions	Not Supported	As per OPAL, this behavior is out of the scope
Creation/Deletion of Tables/Rows after Manufacturing	Not Supported	As per OPAL, this behavior is out of the scope
Tper Feature		
COM ID Management Support	Not Supported	Dynamic COM ID allocation and management not supported
Buffer Management Support	Not Supported	Flow control

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Table 30: TCG/Opal Support Parameters (Continued)

Property	Supported	Comments
ACK/NACK Support	Not Supported	Session reliability
Async Support	Not Supported	Asynchronous protocol support with multiple commands per session
Geometry Reporting Feature		
ALIGN	Supported	OPAL 2.0 (only)
Logical Block Size	512 bytes	Logical block size = 512 bytes
Alignment Granularity	4096 Bytes	Page or Descriptor size <<Minimum AES LU size>>
Lowest Aligned LBA	0	–
OPAL SSC V2.00 Feature Descriptor		
Base COM ID	0x1000	0x1000-0xFFFF defined for COM ID management
Number of COM IDs	1	–
Range Crossing Behavior	0	If drive receives a READ or WRITE command that spans multiple LBA ranges and the LBA ranges are not locked, then: 1. Process the data transfer, if Range Crossing = 0 2. Terminate the command with "Other Invalid Command Parameter" if Range Crossing = 1
Number of Locking SP Admin Authorities Supported	4	As per OPAL 2.0, drive should support at least 4 admin
Number of Locking SP User Authorities Supported	16	As per OPAL 2.0, drive should support at least 8 users
Initial C_PIN_SID PIN Indicator	0x00	0x00 = The initial C_PIN_SID PIN value is equal to the C_PIN_MSID PIN value 0xFF = The initial C_PIN_SID PIN value is VU, and MAY not be equal to the C_PIN_MSID PIN value OPAL 2.0 (only) Customer-specific SID – Configurable
Behavior of C_PIN_SID PIN upon Ter Revert	0x00	0x00 = The C_PIN_SID PIN value becomes the value of the C_PIN_MSID PIN column after successful invocation of revert on the admin SP's object in the SP table 0xFF = The C_PIN_SID PIN value changes to a VU value after successful invocation of revert on the admin SP's object in the SP table and MAY NOT be equal to the C_PIN_MSID PIN value OPAL 2.0 (only)
DataStore Table Feature		
Maximum number of DataStore Tables	16	The maximum number of the DataStore tables that the Tper supports, including the DataStore table defined in OPAL SSC 2.0
Maximum total size of DataStore Tables	90MB	Specifies the maximum total size in bytes of all of the DataStore tables that Tper supports, including the DataStore table defined in OPAL SSC 2.0
MBR Table	128MB	–
Byte Table Access Granularity		

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Table 30: TCG/Opal Support Parameters (Continued)

Property	Supported	Comments
Mandatory Write Granularity	1	Tper enforces when the host invokes the set method on byte tables; it should be less than or equal to 8192; it should be less than or equal to Recommended Access Granularity, OPAL 2.0 (only)
Recommended Access Granularity	8192	Tper recommends when the host invokes the set or get method on byte tables; it should be less than or equal to 8192
Cryptographic Features		
AES Key Size	256 Bits	AES key is generated by using CTR DRBG algorithm (FIPS Compliant)
AES Mode	CBC	IV swapped
Number of Ranges/Band Supported	16 (15 user definable, 1 global range)	Now supporting 15 LBA ranges; range cross read and write allowed if LBA ranges are unlocked
Re-Encryption	Not Supported	–
Key Management		Cryptographic
Crypto Erase Completion Time <1s	Yes	–
Cryptographic Algorithms are Certified by FIPS-197	No	Designed to meet, no plans for certification
AES 256-Bit CBC/ECB Mode	Supported	ECB mode used only for generating the random key by CTR DRBG
CTR DRBG	Supported	–
SHA 256	Supported	–
RSA 2048 Signature Verification	Supported	–
Tper Communication Properties		
Max ComPacket Size	32256	in byte
Max Response ComPacket Size	32256	in byte
Max Packet Size	32236	in byte
Max Individual Token Size	32200	in byte
Max Packets	1	–
Max SubPackets	1	–
Max Sessions	1	Each session requires a set of buffers and variables
Max Transaction Limit	1	Transaction are inside sessions
Max Methods	1	Methods are contained in a transaction
Max Authentications	14	–
Def Session Timeout	Yes	The session timeout length (in milliseconds) used by the Tper by default
IEEE1667 (feature removed from MU03)		
Probe Silo	Supported	–
TCG Storage Silo	Supported	–

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Table 30: TCG/Opal Support Parameters (Continued)

Property	Supported	Comments
Other than Probe and TCG Storage Silo	Not Supported	–
IEEE1667 Major Version	2	-
IEEE1667 Minor Version	0	–
Maximum P_OUT Transfer Size	32768	256 sectors (128K)
Others		
FDE (ATA Security with Key Management)	Yes	–
Secure Firmware Download	Supported	Firmware image is validated by using SHA256 and RSA2048 algorithm

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PCI Header

Table 31: PCI Header Space Registers

Start Address	End Address	Symbol	Register Definition	Bits	Type	Default	Description
00h	03h	ID	Identifiers	31:16	RO	6001h	Device ID (DID)
				0:15	RO	1344h	Vendor ID (VID)
04h	05h	CMD	Command register	15:11	RO	0	Reserved
				10	RW	0	Interrupt disable
				9	RO	0	Fast back-to-back enable
				8	RW	0	SERR# enable
				7	RO	0	IDSEL STEPPING/WAIT cycle control
				6	RW	0	Parity error response enable
				5	RO	0	VGA palette snooping enable
				4	RO	0	Memory write and invalidate enable
				3	RO	0	Special cycle enable
				2	RW	0	Bus master enable
				1	RW	0	Memory space enable
				0	RW	0	I/O space enable
06h	07h	STS	Device status	15	RW1C	0	Detected parity error
				14	RW1C	0	Signaled system error
				13	RW1C	0	Received master abort
				12	RW1C	0	Received target abort
				11	RW1C	0	Signaled target abort
				10:9	RO	0	DEVSEL timing
				7	RO	0	Master data parity error detected
				8	RW1C	0	Fast back-to-back transaction capable
				6	RO	0	Reserved
				5	RO	0	66 MHz capable
				4	RO	0	Capabilities list
				3	RO	0	Interrupt status
				2:1	RO	0	Reserved
				0	RO	0	Reserved
08h	08h	RID	Revision ID	7:10	RO	0	Controller hardware revision ID
09h	0Bh	CC	Class codes	23:16	RO	1h	Base class code
				15:8	RO	8h	Sub class code
				7:0	RO	2h	Programming interface
0Ch	0Ch	CLS	Cache line size	7:0	RO	0	N/A

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Table 31: PCI Header Space Registers (Continued)

Start Address	End Address	Symbol	Register Definition	Bits	Type	Default	Description
0Dh	0Dh	MLT	Master latency timer	7:0	RO	0	N/A
0Eh	0Eh	HTYPE	Header type	7	RO	0	Multi-Function device
				6:0	RO	0	Reserved
0Fh	0Fh	BIST	Built-in self test	7:0	RO	0	Not supported
10h	13h	MLBAR (BAR0)	Memory register base address (lower 32-bit)	31:14	RW	0	Base address
				13:4	RO	0	Reserved
				3	RO	0	Prefetchable
				2:1	RO	2h	Address type (64-bit)
				0	RO	0	Memory space indicator (MEMSI)
14h	17h	MUBAR (BAR1)	Memory register base address (upper 32-bit)	31:0	RO	0	Base address
18h	1Bh	IDBAR (BAR2)	Index/Data pair register base address	31:0	RO	0	Not supported
1Ch	1Fh	BAR3	BAR3 register	31:0	RO	0	Reserved
20h	23h	BAR4	BAR4 register	31:0	RO	0	Vendor specific
24h	27h	BAR5	Vendor-Specific BAR5	31:0	RO	0	Vendor specific
28h	2Bh	CCPTR	CardBus CIS pointer	31:0	RO	0	N/A
2Ch	2Fh	SS	Subsystem identifiers	31:16	RO	See table below	Subsystem ID (SSID)
				15:0	RO	1344h	Subsystem vendor ID (SSVID)
30h	33h	EXPROM	Expansion ROM base address	31:17	RW	0	Expansion ROM base address
				16:1	RO	0	Reserved
				0	RW	0	Expansion ROM enable/disable
34h	34h	CAP	Capabilities pointer	7:0	RO	0	N/A
35h	3Bh	R	Reserved				
3Ch	3Dh	INTR	Interrupt information	15:8	RO	01h	Interrupt pin
				7:0	RW	FFh	Interrupt line
3Eh	3Eh	MGNT	Minimum grant	7:0	RO	0	N/A
3Fh	3Fh	MLAT	Maximum latency	7:0	RO	0	N/A

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Table 32: Subsystem ID (SSID)

Package	Density (GB)	Value
BGA	64	0400h
	128	0400h
	256	0400h
	512	1400h
	1024	2400h
M.2	128	0100h
	256	0100h
	512	1100h
	1024	2100h

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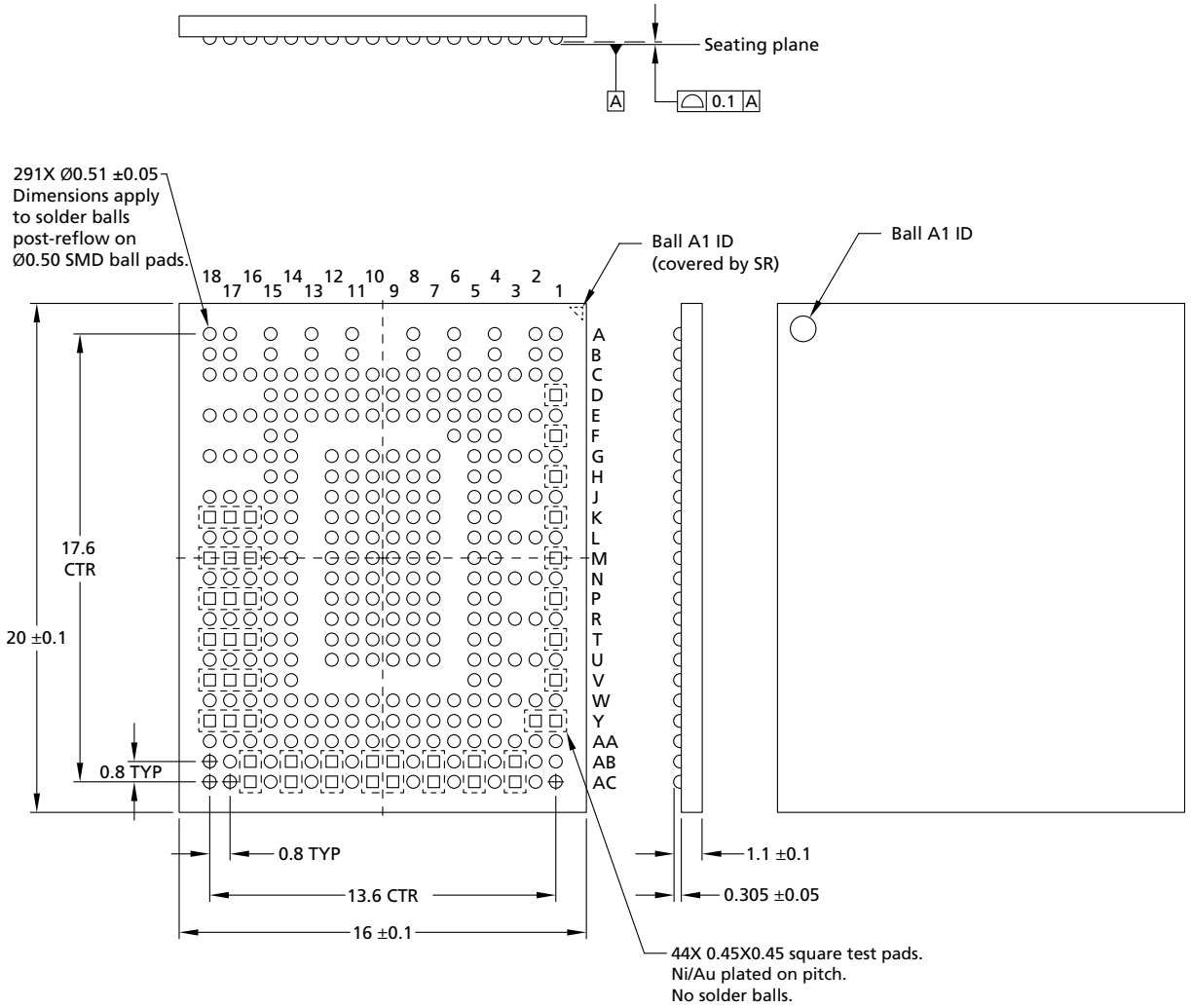
Package Physical Configuration

BGA Type 1620

Figure 5: BGA Type 1620 – 291-Ball 16mm x 20mm x 1.2mm (Package Code BL)



Notes: 1. All dimensions are in millimeters.
2. Ball diameter before soldering is 0.45mm. The solder ball composition is SAC405.
3. For optimal Solder Join Reliability (SJR) performance refer to CSN33 for recommended PCB pad dimension to align to the SMD ball pad size of the package.

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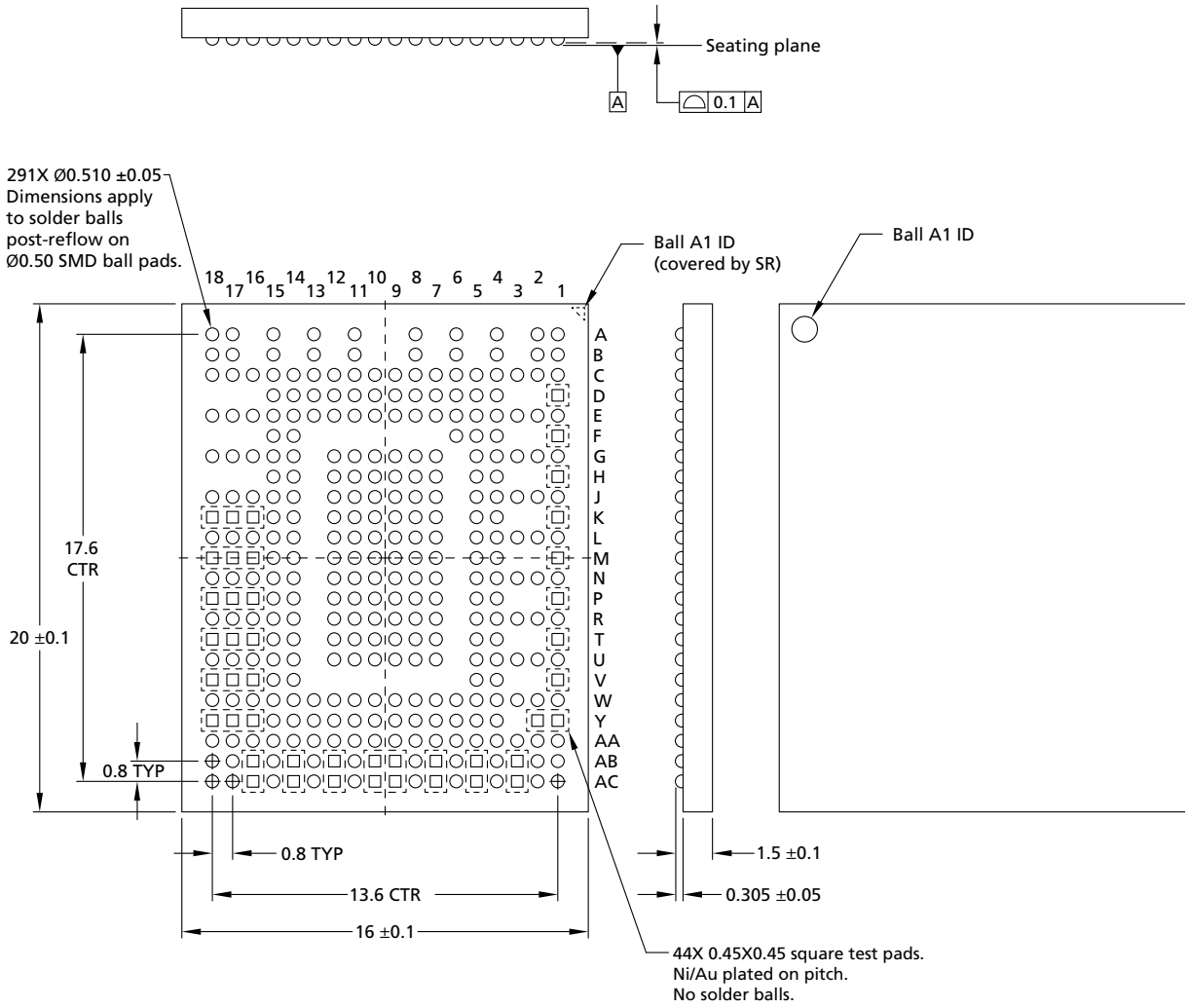
Figure 6: BGA Type 1620 – 291-Ball 16mm x 20mm x 1.6mm (Package Code BM)



Notes: 1. All dimensions are in millimeters.
2. Ball diameter before soldering is 0.45mm. The solder ball composition is SAC405.
3. For optimal Solder Join Reliability (SJR) performance refer to CSN33 for recommended PCB pad dimension to align to the SMD ball pad size of the package.

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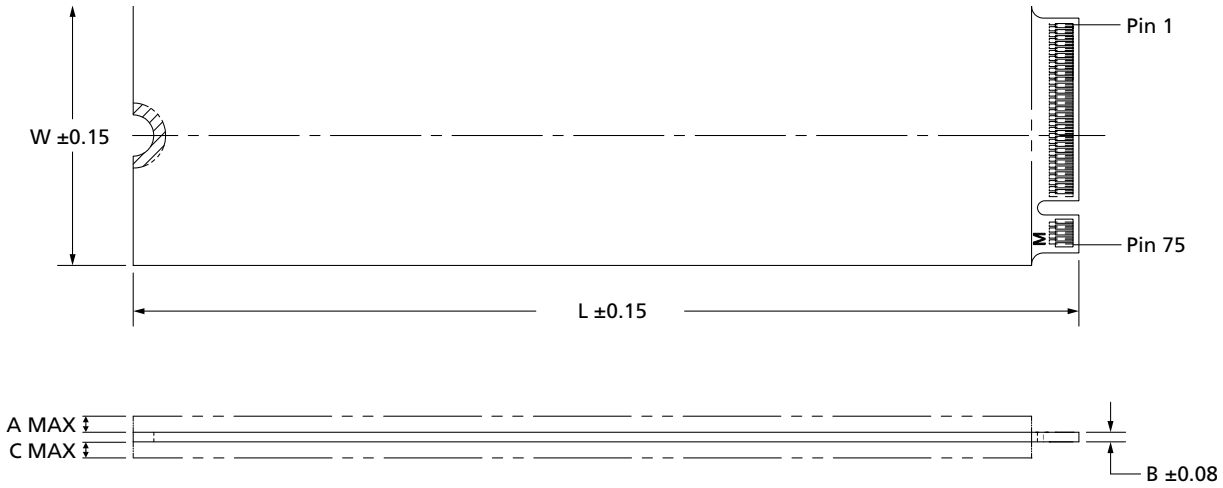
Modules Physical Configuration

M.2 Type 2230 (M-key)

Figure 7: M.2 Type 2230 Form Factor (Package Code BK)



Note: 1. All dimensions are in millimeters.

Table 33: M.2 Type 2230 Form Factor Dimensions

Capacity	Type	W	L	A	B	C	Unit
up to 512GB	2230	22.00	30.00	1.2	0.8	0.0	mm
1TB	2230	22.00	30.00	1.6	0.8	0.0	mm

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Compliance (M.2 only)

The SSDs into M.2 package comply with the following:

- Micron Green Standard
- CE (Europe): EN55032, EN55024 Class B, RoHS
- FCC: CFR Title 47, Part 15, Class B, CNS 15663
- UL/cUL: approval to UL-60950-1, 2nd Edition, IEC 60950-1:2005 (2nd Edition); EN 60950-1 (2006) + A11:2009+ A1:2010 + A12:2011 + A2:2013
- BSMI (Taiwan): approval to CNS 13438 Class B
- RCM (Australia, New Zealand): AS/NZS CISPR32 Class B
- KC RRL (Korea): approval to KN32 Class B, KN 35 Class B

  B 급 기기 (가정용 정보통신기기) 이 기기는 가정용으로 전자파적합등록을한 기기로서 주거 지역에서는 물론 모든지역에서 사용할 수 있습니다.

- W.E.E.E.: Compliance with EU WEEE directive 2012/19/EC. Additional obligations may apply to customers who place these products in the markets where WEEE is enforced.
- TUV (Germany): approval to IEC60950/EN60950
- V_{CCI} (Japan): 2015-04 Class B

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  取扱説明書に従って正しい取り扱いをして下さい。
  VCCI－B

- IC (Canada): ICES-003 Class B
  - This Class B digital apparatus complies with Canadian ICES-003.
  - Cet appareil numérique de la classe B est conforme à la norme NMB-003 du Canada.
- Morocco: EN55032, EN55024 Class B

FCC Rules

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

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References

- NVM Express, Revision 1.3c
- PCI Express Base Specification, Revision 3.0
- PCI Express Electromechanical Specification, PCI Express M.2 Specification Revision 1.1
- PCI-SIG Engineering Change Notice: Power Loss Notification Functions (Mar. 26, 2018)
- PCI-SIG Engineering Change Notice: 1.8V sideband, Power Loss Notification, USB 2.0, and higher power support (Nov. 28, 2018). To be considered for forward compatibility
- TCG Storage Architecture Core Specification Version 2.01 Revision 1.00
- TCG Storage Security Subsystem Class: Opal Specification Version 2.01 Revision 1.00
- IDEMA Standard LBA 1-03
- JEDEC Standard, Integrated Circuits Thermal Test Method Environmental Conditions JESD51-2A
- TN-FD-49: 2100 AI AT Physical Capacity Management
- TN-FD-50: 2100AI/AT SSD Power Supply Electrical Requirements
- TN-FD-52: Micron PCIe NVMe SSDs Usage Model Collection and Emulation
- TN-FD-53: 2100 AI/AT SSD Production Programming
- TN-FD-54: 2100AI/AT Power Loss Protection Notification/Acknowledge (PLN#/PLA#)
- TN-FD-56: Erase Methods for 2100AI/AT
- TN-FD-57: 2100AI/AT NVMe Shutdown
- TN-FD-58: 2100AI/AT NVMe PCIe SSD Verification in Customer Production
- TN-FD-59: 2100AI/AT NVMe SMART and Vendor Unique Logs

For further information on automotive and industrial Micron SSD, periodically check www.micron.com

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Revision History

Rev. F - 07/22

- For BGA Form Factor: 2.75mm x 2.75mm QR code for PSID code printed on package top marking from CQ4-2021
- Added Light Throttling feature and a new SET/GET FEATURE command (DDh) to cope with read intensive usage models. See Command section for more details
- Added support to Windows®11
- Removed from Operating Ratings Table the Power on/off and hold-off time requirements to avoid information duplication and better consistency. Reference to TN-FD-50 for these parameters aimed to robust system design
- Updated Electrical Characteristic sections: for IDLP power measurement, the PCIe state is L0s
- Updated: Total Bytes Written table in Physical Configuration Management section to show both SLC and TLC TBW
- Updated: Identify Controller Data Structure table (PSD3 field) and corrected typos (ACL, AERL, SANICAB field)
- Added Reference to *TN-FD-59: 2100AI/AT SMART & Vendor Specific Logs* in Log Pages section
- Updated: In the from page: “Automotive (-40°C to +105°C)”
- Updated Logical Block Address Configuration table for SLC Mode
- Updated Operating Ratings tables: added Power hold-off timings and Power-off time
- Updated Drive Performance table: Random write (4KB transfer) for 1TB capacity changed from 130K to 123K (FW MU05 onwards)
- Minor editorial changes and typo corrections

Rev. E - 01/21

- Added: AEC-Q104 compliance in the front page (apply to BGA Form Factor only)
- Added: RPMB and Boot partitions size in the front-page
- Updated: Values for HCTMA, MNTMT, MXTMT parameters
- Update Reference section: Removed reference to Pyrite Specification (Version 1.00 Revision 1.00)
- Discontinued: IEEE 1667 support from MU03 Firmware
- Removed: Rate of temperature change (both operating & unbiased) for both M.2 and BGA form factor
- Replaced: Options and Markings sections on front page with Operating system supported natively
- Minor editorial changes

Rev. D - 05/20

- Updated Table: Operating Ratings: Changed PWR_1 range for BGA and Specified "Ambient" for "Rate of temperature change" & "Non-operating temperature" for both BGA and M.2 form factors
- Updated Notes in Table: Maximum Current per Power Rail.
- Updated Table: BGA Signal Description. In-Band-Signals type are now specified if they are Input (I) or Output (O); CLKREQ# type changed from Input/Output (I/O) to Open Drain (OD)
- Added Table: Drive Performance With/Without HMB Enabled (SLC Mode=100%) – Fresh Out of Box
- Minor editorial changes

Rev. C - 02/20

- Updated Operating Rating table with Power-off minimum time for M.2

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- Minor editorial changes

Rev. B - 12/19

- Data Sheet maturity level changed from *Preliminary* to *Production*; *Preliminary* has been removed on the top right corner of each page
- Updated Table: BGA Signal Description. Note no.6 include PWR_1 recommendation for future SSD (from 3.3V to 2.5V)
- Updated Table: M.2 Signal Assignments. Added LED_1#, UART_RX and UART_TX
- Updated: MTTF from 2 million to 3 million
- Renamed Table: Maximum Ratings into Operating Ratings. Sensor temperature symbol changed
- Removed Table: Drive Performance With/Without HMB Enabled – Steady State. The server workload condition for performance calculation does not apply to 2100AI/AT SSD

Rev. A - 11/19

- Data Sheet maturity level changed from *Advance* to *Preliminary*; *Preliminary* put on the top right corner of each page
- Power domain for PLN#/PLA# is changed to 3.3V on BGA. Ensure design correctness for your board schematics. For further information search for *TN-FD-47 2100AI_AT PCIe Schematics Reference Design* Technical Note at http://www.micron.com
- Added M.2 package for 1TB
- Added a new Table for BGA: Maximum Current per Power Rail
- Updated Section: Identify Controller Data Structure
- Updated Table: Maximum Ratings.
- Updated Section: Commands.
- Updated Section: Log Pages.
- Updated Section: TCG/OPAL Support.
- Updated Section: Identify – Identify Namespace Data Structure
- Added Section: PCI Header
- Updated Table: Drive Performance With/Without HMB Enabled – Fresh Out of Box
- Updated Table: Drive Performance With/Without HMB Enabled – Steady State

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This data sheet contains minimum and maximum limits specified over the power supply and temperature range set forth herein. Although considered final, these specifications are subject to change, as further product development and data characterization sometimes occur.

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