# LX1662 / 62A, LX1663 /63A

## SINGLE-CHIP PROGRAMMABLE PWM CONTROLLERS WITH 5-BIT DAC

PRODUCTION DATA SHEET

## DESCRIPTION

**The LX1662/62A and LX1663/63A are Monolithic Switching Regulator Controller IC's** designed to provide a low cost, high performance adjustable power supply for advanced microprocessors and other applications requiring a very fast transient response and a high degree of accuracy.

**Short-Circuit Current Limiting without Expensive Current Sense Resistors.** Current-sensing mechanism can use PCB trace resistance or the parasitic resistance of the main inductor. The *LX1662A* and *LX1663A* have reduced current sense comparator threshold for optimum performance using a PCB trace. For applications requiring a high degree of accuracy, a conventional sense resistor can be used to sense current.

**Programmable Synchronous Rectifier Driver for CPU Core.** The main output is adjustable from 1.3V to 3.5V using a 5-bit code. The IC can read a VID signal set by a DIP switch on the motherboard, or hardwired into the processor's package (as in the case of Pentium® Pro and Pentium II processors). The 5-bit code adjusts the output voltage between 1.30 and 2.05V in 50mV increments and between 2.0 and 3.5V in 100mV increments, conforming to the Intel Corporation specification. The device can drive dual MOSFET's resulting in typical efficiencies of 85 - 90% even with loads in excess of 10 amperes. For cost sensitive applications, the bottom MOSFET can be replaced with a Schottky diode (non-synchronous operation).

**Smallest Package Size.** The LX1662 is available in a narrow body 14-pin surface mount IC package for space sensitive applications. The LX1663 provides the additional functions of Over Voltage Protection (OVP) and Power Good (PWRGD) output drives for applications requiring output voltage monitoring and protection functions.

**Ultra-Fast Transient Response Reduces System Cost.** The modulated offtime architecture results in the fastest transient response for a given inductor, reducing output capacitor requirements, and reducing the total regulator system cost.

**Over-Voltage Protection and Power Good Flag.** The OVP output in the LX1663 & LX1663A can be used to drive an SCR crowbar circuit to protect the load in the event of a short-circuit of the main MOSFET. The LX1663 & LX1663A also have a logiclevel Power Good Flag to signal when the output voltage is out of specified limits.

**IMPORTANT:** For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

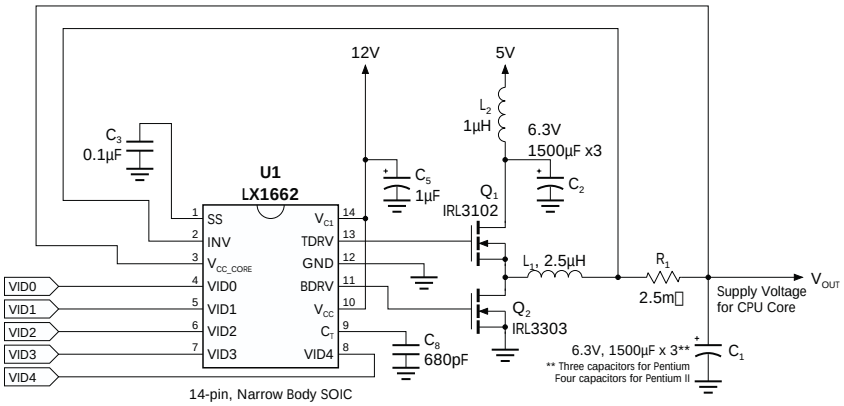
## KEY FEATURES

- 5-bit Programmable Output For CPU Core Supply
- No Sense Resistor Required For Short-Circuit Current Limiting
- Designed To Drive Either Synchronous Or Non-Synchronous Output Stages
- Lowest System Cost Possible For Price- Sensitive Pentium And Pentium II Class Applications
- Soft-Start Capability
- Modulated, Constant Off-Time Architecture For Fast Transient Response And Simple System Design
- Available Over-Voltage Protection (OVP) Crowbar Driver And Power Good Flag (LX1663 only)
- Small, Surface-Mount Packages

## KEY FEATURES

- Socket 7 Microprocessor Supplies (including Intel Pentium Processor, AMDK6TM And Cyrix® 6x86TM, Gx86TM and M2TM Processors)
- Pentium II and Deschutes Processor & L2-Cache Supplies
- Voltage Regulator Modules
- General Purpose DC:DC Converter Applications

## PRODUCT HIGHLIGHT




## PACKAGE ORDER INFO

| $T_A$ (°C) | N Plastic DIP 14-Pin | N Plastic DIP 16-Pin | D Plastic SOIC 14-Pin | D Plastic SOIC 16-Pin |
|---|---|---|---|---|
| | RoHS Compliant / Pb-free Transition DC:0503 | | RoHS Compliant / Pb-free Transition DC:0440 | |
| 0 to 70 | LX1662CN | LX1663CN | LX1662CD | LX1663CD |
| | LX1662ACN | LX1663ACN | LX1662ACD | LX1663ACD |

Note: Available in Tape & Reel. Append the letters 'TR' to the part number. (i.e. LX1663CD-TR)

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# SINGLE-CHIP PROGRAMMABLE PWM CONTROLLERS WITH 5-BIT DAC

## PRODUCTION DATA SHEET

## DEVICE SELECTION GUIDE

| DEVICE | Packages | OVP and Power Good | Current-Sense Comp. Thresh. (mV) | Optimal Load |
|---|---|---|---|---|
| **LX1662** | 14-pin SOIC & DIP | No | 100 | Pentium-class (<10A) |
| **LX1662A** | | | 60 | Pentium II (> 10A) |
| **LX1663** | 16-pin SOIC & DIP | Yes | 100 | Pentium-class (<10A) |
| **LX1663A** | | | 60 | Pentium II (> 10A) |

## ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage ($V_{C1}$) ..... 25V
Supply Voltage ($V_{CC}$) ..... 15V
Output Drive Peak Current Source (500ns) ..... 1.5A
Output Drive Peak Current Sink (500ns) ..... 1.5A
Input Voltage (SS, INV, $V_{CC_CORE}$, $C_T$, VID0-VID4) ..... -0.3V to 6V
Operating Junction Temperature
Plastic (N & D Packages) ..... 150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 10 Seconds) ..... 300°C
Peak Package Solder Reflow Temp. (40 second max. exposure).....260°C (+0, -5)

Note 1. Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of the specified terminal. Pin numbers refer to DIL packages only.

## THERMAL DATA

**N PACKAGE:**

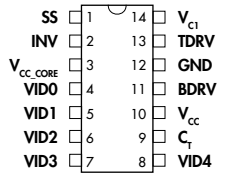
| THERMAL RESISTANCE-JUNCTION TO AMBIENT, $\theta_{JA}$ | 65°C/W |
|---|---|

**D PACKAGE:**

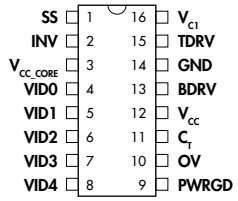
| THERMAL RESISTANCE-JUNCTION TO AMBIENT, $\theta_{JA}$ | 120°C/W |
|---|---|

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The $\theta_{JA}$ numbers are guidelines for the thermal performance of the device/pc-board system.
All of the above assume no ambient airflow

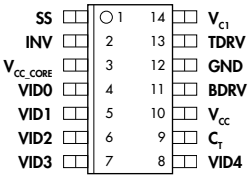
## PACKAGE PIN OUTS



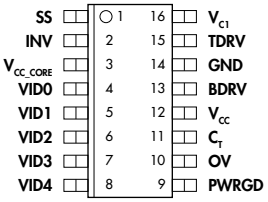

**N PACKAGE — 14-Pin**
**LX1662/1662A** (Top View)




**N PACKAGE — 16-Pin**
**LX1663/1663A** (Top View)




**D PACKAGE — 14-Pin**
**LX1662/1662A** (Top View)




**D PACKAGE — 16-Pin**
**LX1663/1663A** (Top View)

RoHS / Pb-free 100% Matte Tin Lead Finish



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## ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, $10.8 < V_{CC} < 13.2$, $0°C \le T_A \le 70°C$. Test conditions: $V_{CC}$ = 12V, T = 25°C. Use Application Circuit.)

| Parameter | Symbol | Test Conditions | LX1662/1663 (A) Min. | LX1662/1663 (A) Typ. | LX1662/1663 (A) Max. | Units |
|---|---|---|---|---|---|---|
| **Reference & DAC Section** (See Table 1 - Next Page) | | | | | | |
| Regulation Accuracy (See Table 1) | | (Less 40mV output adaptive positioning), $V_{CC}$ = 12V, $I_{LOAD}$ = 6A | -30 | | 30 | mV |
| Regulation Accuracy | | $1.8V \le V_{OUT} \le 2.8V$ | -1 | | 1 | % |
| **Timing Section** | | | | | | |
| Off Time Initial | OT | $V_{CC_CORE}$ = 1.3V, $C_T$ = 390pF | | 2 | | µs |
| | | $V_{CC_CORE}$ = 3.5V, $C_T$ = 390pF | | 1 | | µs |
| Off Time Temp Stability | | $V_{CC_CORE}$ = 1.3V to 3.5V | | 40 | | ppm |
| Discharging Current | $I_{DIS}$ | $V_{CC_CORE}$ = 1.3V, $V_{CT}$ = 1.5V | 180 | 210 | 240 | µA |
| Ramp Peak | $V_P$ | | | 2 | | V |
| Ramp Peak-Valley | $V_{RPP}$ | $V_{CC_CORE}$ = 1.3V | 0.9 | 1 | 1.1 | V |
| | | $V_{CC_CORE}$ = 3.5V | 0.37 | 0.42 | 0.47 | V |
| Ramp Valley Delay to Output | | 10% Overdrive | | 100 | | ns |
| **Error Comparator Section** | | | | | | |
| Input Bias Current | $I_B$ | $1.3V < V_{SS} = V_{INV} < 3.5V$ | | 0.8 | 2 | µA |
| Input Offset Voltage | $V_{IO}$ | | 36 | 41 | 46 | mV |
| $E_C$ Delay to Output | | 10% Overdrive | | 200 | | ns |
| **Current Sense Section** | | | | | | |
| Input Bias Current ($V_{CC_CORE}$ Pin) | $I_B$ | $1.3V < V_{INV} = V_{CC_CORE} < 3.5V$ | | 27 | 35 | µA |
| Pulse By Pulse $C_L$ LX1662/1663 | $V_{CLP}$ | Initial Accuracy | 85 | 100 | 115 | mV |
| LX1662A/1663A | | Initial Accuracy | 50 | 60 | 70 | mV |
| $C_S$ Delay to Output | | 10% Overdrive | | 200 | | ns |
| **Output Drivers Section** | | | | | | |
| Drive Rise Time | $T_R$ | $V_{C1} = V_{CC}$ = 12V, $C_L$ = 3000pF | | 70 | | ns |
| Drive Fall Time | $T_F$ | $V_{C1} = V_{CC}$ = 12V, $C_L$ = 3000pF | | 70 | | ns |
| Drive High | $V_{DH}$ | $V_{CC} = V_{CC}$ = 12V, $I_{SOURCE}$ = 20mA | | 11 | | V |
| | | $V_{CC} = V_{CC}$ = 12V, $I_{SINK}$ = 200mA | | 10 | | V |
| Drive Low | $V_{DL}$ | $V_{CC} = V_{CC}$ = 12V, $I_{SOURCE}$ = 20mA | | 0.06 | 0.1 | V |
| | | $V_{CC} = V_{CC}$ = 12V, $I_{SINK}$ = 200mA | | 0.8 | 1.2 | V |
| Output Pull Down | $V_{PD}$ | $V_{CC} = V_C$ = 0, $I_{PULL\ UP}$ = 2mA | | 0.8 | 1.4 | V |
| **UVLO and S.S. Section** | | | | | | |
| Start-Up Threshold | $V_{ST}$ | | 9.9 | 10.1 | 10.4 | V |
| Hysteresis | $V_{HYST}$ | | | 0.31 | | V |
| SS Sink Current | $I_{SD}$ | $V_{C1}$ = 10.1V | 2 | 5.5 | | mA |
| SS Sat Voltage | $V_{OL}$ | $V_{C1}$ = 9V, $I_{SD}$ = 200µA | | 0.15 | 0.6 | V |
| **Supply Current Section** | | | | | | |
| Dynamic Operating Current | $I_{CD}$ | $V_{CC} = V_{C1}$ = 12V, Out Freq = 200kHz, $C_L$ = 0 | | | 27 | mA |
| **Power Good / Over-Voltage Protection Section** (LX1663 Only) | | | | | | |
| Lower Threshold | | ($V_{CC_CORE}$ / $DAC_{OUT}$) | 88 | 90 | 92 | % |
| Hysteresis | | | | 1 | | % |
| Power Good Voltage Low | | $I_{PWRGD}$ = 5mA | | 0.5 | 0.7 | V |
| Over-Voltage Threshold | | ($V_{CC_CORE}$ / $V_{DAC}$) | 110 | 117 | 125 | % |
| OVP Sourcing Current | | $V_{OV}$ = 5V | 30 | 45 | | mA |

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## ELECTRICAL CHARACTERISTICS

**Table 1 - Adaptive Transient Voltage Output** (Output Voltage Setpoint — Typical)

| Processor Pins 0 = Ground, 1 = Open (Floating) | | | | | Output Voltage ($V_{CC_CORE}$) | |
|---|---|---|---|---|---|---|
| VID4 | VID3 | VID2 | VID1 | VID0 | 0.0A | Nominal Output* |
| 0 | 1 | 1 | 1 | 1 | 1.34V | 1.30V |
| 0 | 1 | 1 | 1 | 0 | 1.39V | 1.35V |
| 0 | 1 | 1 | 0 | 1 | 1.44V | 1.40V |
| 0 | 1 | 1 | 0 | 0 | 1.49V | 1.45V |
| 0 | 1 | 0 | 1 | 1 | 1.54V | 1.50V |
| 0 | 1 | 0 | 1 | 0 | 1.59V | 1.55V |
| 0 | 1 | 0 | 0 | 1 | 1.64V | 1.60V |
| 0 | 1 | 0 | 0 | 0 | 1.69V | 1.65V |
| 0 | 0 | 1 | 1 | 1 | 1.74V | 1.70V |
| 0 | 0 | 1 | 1 | 0 | 1.79V | 1.75V |
| 0 | 0 | 1 | 0 | 1 | 1.84V | 1.80V |
| 0 | 0 | 1 | 0 | 0 | 1.89V | 1.85V |
| 0 | 0 | 0 | 1 | 1 | 1.94V | 1.90V |
| 0 | 0 | 0 | 1 | 0 | 1.99V | 1.95V |
| 0 | 0 | 0 | 0 | 1 | 2.04V | 2.00V |
| 0 | 0 | 0 | 0 | 0 | 2.09V | 2.05V |
| 1 | 1 | 1 | 1 | 1 | 2.04V | 2.00V |
| 1 | 1 | 1 | 1 | 0 | 2.14V | 2.10V |
| 1 | 1 | 1 | 0 | 1 | 2.24V | 2.20V |
| 1 | 1 | 1 | 0 | 0 | 2.34V | 2.30V |
| 1 | 1 | 0 | 1 | 1 | 2.44V | 2.40V |
| 1 | 1 | 0 | 1 | 0 | 2.54V | 2.50V |
| 1 | 1 | 0 | 0 | 1 | 2.64V | 2.60V |
| 1 | 1 | 0 | 0 | 0 | 2.74V | 2.70V |
| 1 | 0 | 1 | 1 | 1 | 2.84V | 2.80V |
| 1 | 0 | 1 | 1 | 0 | 2.94V | 2.90V |
| 1 | 0 | 1 | 0 | 1 | 3.04V | 3.00V |
| 1 | 0 | 1 | 0 | 0 | 3.14V | 3.10V |
| 1 | 0 | 0 | 1 | 1 | 3.24V | 3.20V |
| 1 | 0 | 0 | 1 | 0 | 3.34V | 3.30V |
| 1 | 0 | 0 | 0 | 1 | 3.44V | 3.40V |
| 1 | 0 | 0 | 0 | 0 | 3.54V | 3.50V |

* Nominal = DAC setpoint voltage with no adaptive output voltage positioning.

***Note:***

**Adaptive Transient Voltage Output**

In order to improve transient response a 40mV offset is built into the Current Sense comparator. At high currents, the peak output voltage will be lower than the nominal set point , as shown in Figure 1. The actual output voltage will be a function of the sense resistor, output current and output ripple.

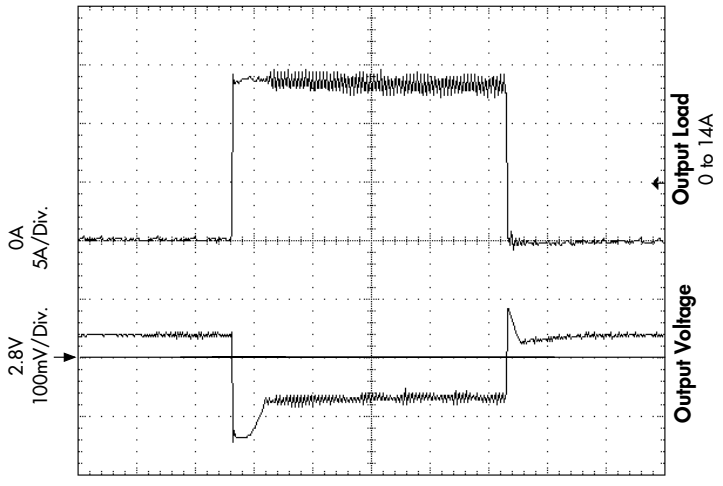


**FIGURE 1** — Output Transient Response
(Using 5mΩ sense resistor and 5µH output inductor)



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## CHARACTERISTICS CURVES

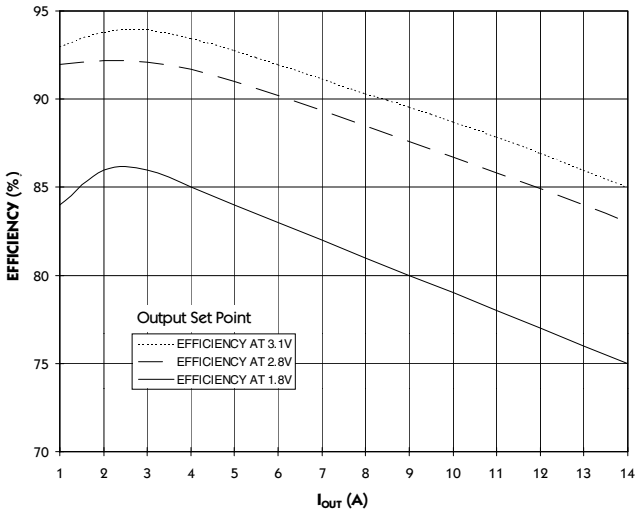


**FIGURE 2** — Efficiency Test Results: Non-Synchronous Operation, $V_{IN}$ = 5V

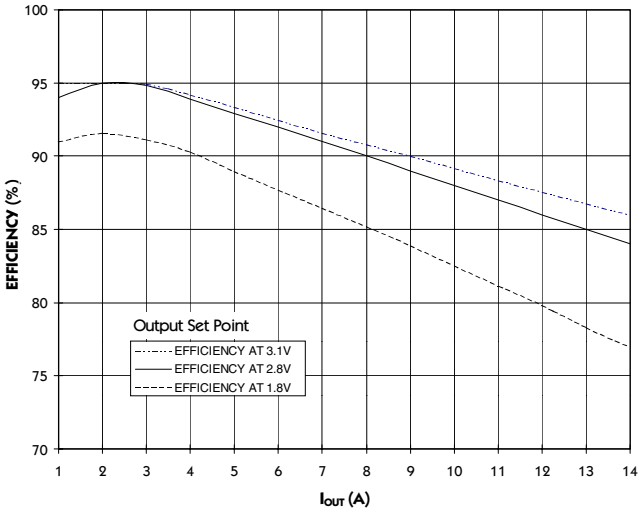


**FIGURE 3** — Efficiency Test Results: Synchronous Operation, $V_{IN}$ = 5V

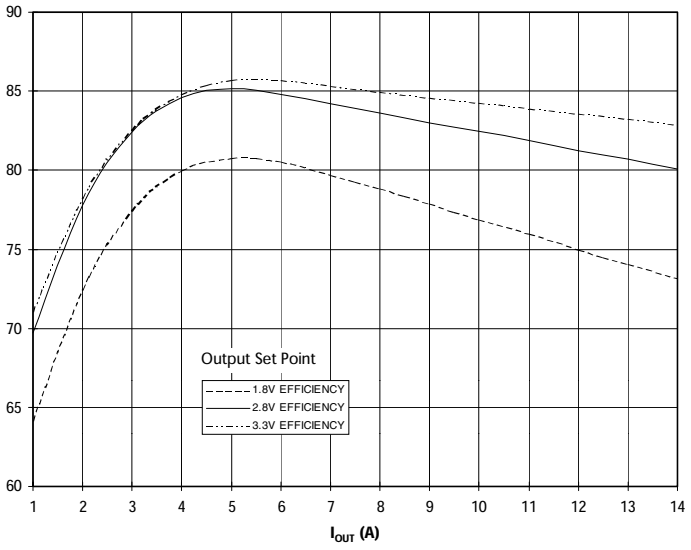


**FIGURE 4** — Efficiency Test Results: Synchronous Operation, $V_{IN}$ = 12V.

Note: Non-synchronous operation not recommended for 12V operation, due to power loss in Schottky diode.

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## BLOCK DIAGRAM

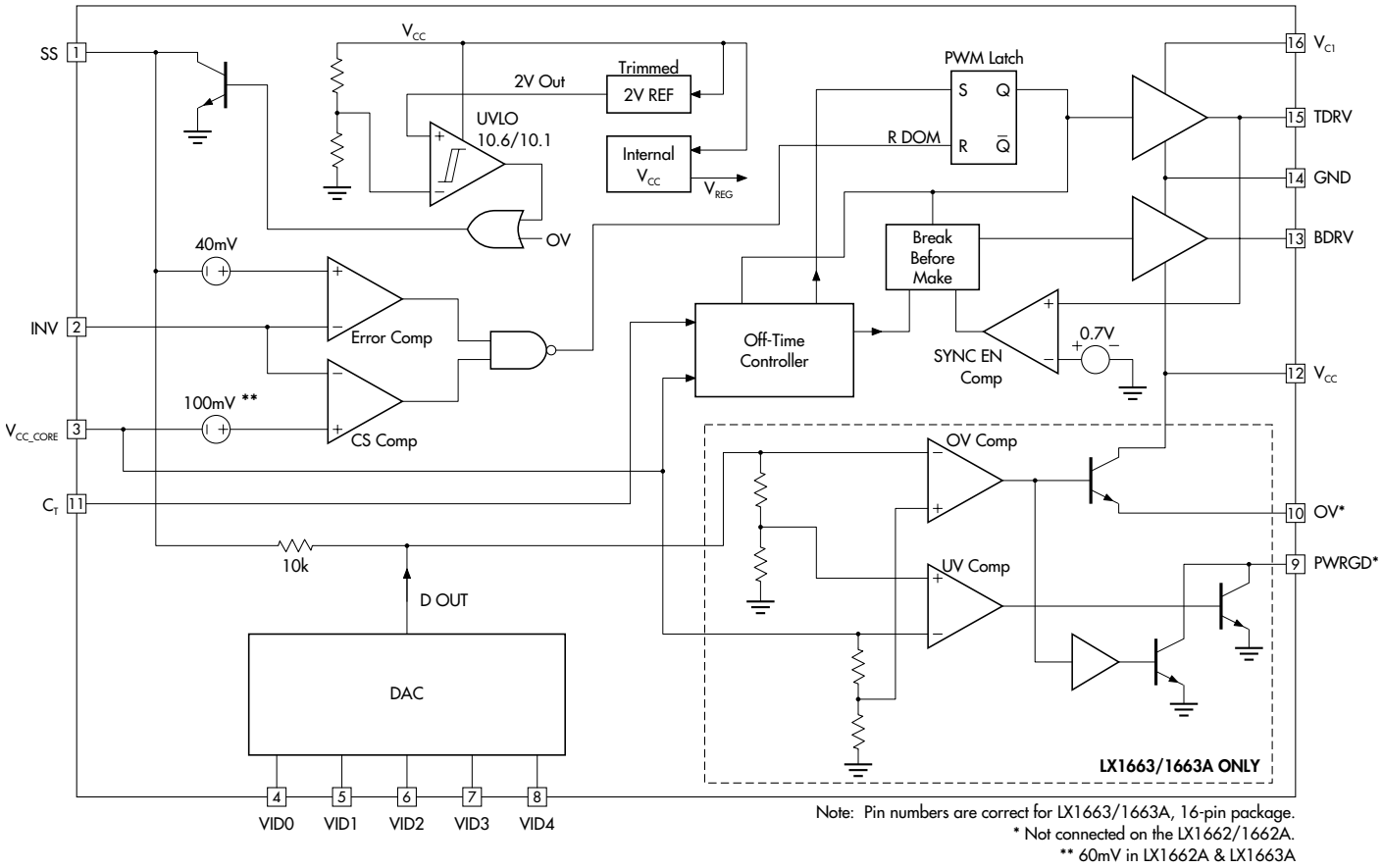


**FIGURE 5** — Block Diagram



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## FUNCTIONAL PIN DESCRIPTION

| Pin Name | LX1662 Pin # | LX1663 Pin # | Description |
|---|---|---|---|
| SS | 1 | 1 | Soft-Start pin, internally connected to the non-inverting input of the error comparator. |
| INV | 2 | 2 | Inverting input of the error comparator. |
| $V_{CC_CORE}$ | 3 | 3 | Output voltage. Connected to non-inverting input of the current-sense comparator. |
| VID0 | 4 | 4 | Voltage Identification pin (LSB) input used to set output voltage. |
| VID1 | 5 | 5 | Voltage Identification pin ($2^{nd}$ SB) input. |
| VID2 | 6 | 6 | Voltage Identification pin ($3^{rd}$ SB) input. |
| VID3 | 7 | 7 | Voltage Identification pin ($4^{th}$ SB) input. |
| VID4 | 8 | 8 | Voltage Identification pin (MSB) input. This pin is also the range select pin — when low (CLOSED), output voltage is set to between 1.30 and 2.05V in 0.05V increments. When high (OPEN), output is adjusted from 2.0 to 3.5V in 0.1V increments. |
| PWRGD | N.C. | 9 | Open collector output pulls low when the output voltage is out of limits. |
| OV | N.C. | 10 | SCR driver goes high when the processor's supply is over specified voltage limits. |
| $C_T$ | 9 | 11 | The off-time is programmed by connecting a timing capacitor to this pin. |
| $V_{CC}$ | 10 | 12 | This is the (12V) supply to the IC, as well as gate drive to the bottom FET. |
| BDRV | 11 | 13 | This is the gate drive to the bottom FET. Leave open in non-synchronous operation (when bottom FET is replaced by a Schottky diode). |
| GND | 12 | 14 | Both power and signal ground of the device. |
| TDRV | 13 | 15 | Gate drive for top MOSFET. |
| $V_{C1}$ | 14 | 16 | This pin is a separate power supply input for the top drive. Can be connected to a charge pump when only 12V is available. |

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## THEORY OF OPERATION

### IC OPERATION

Referring to the block diagram and typical application circuit, the output turns ON the top MOSFET, allowing the inductor current to increase. At the error comparator threshold, the PWM latch is reset, the top MOSFET turns OFF and the synchronous MOSFET turns ON. The OFF-time capacitor $C_T$ is now allowed to discharge. At the valley voltage, the synchronous MOSFET turns OFF and the top MOSFET turns on. A special break-before-make circuit prevents simultaneous conduction of the two MOSFETs.

The $V_{CC_CORE}$ pin is offset by +40mV to enhance transient response. The INV pin is connected to the positive side of the current sense resistor, so the controller regulates the positive side of the sense resistor. At light loads, the output voltage will be regulated above the nominal setpoint voltage. At heavy loads, the output voltage will drop below the nominal setpoint voltage. To minimize frequency variation with varying output voltage, the OFF-time is modulated as a function of the voltage at the $V_{CC_CORE}$ pin.

### ERROR VOLTAGE COMPARATOR

The error voltage comparator compares the voltage at the positive side of the sense resistor to the set voltage plus 40mV. An external filter is recommended for high-frequency noise.

### CURRENT LIMIT

Current limiting is done by sensing the inductor current. Exceeding the current sense threshold turns the output drive OFF and latches it OFF until the PWM latch Set input goes high again. See Current Limit Section in "Using The LX1662/63 Devices" later in this data sheet.

### OFF-TIME CONTROL TIMING SECTION

The timing capacitor $C_T$ allows programming of the OFF-time. The timing capacitor is quickly charged during the ON time of the top MOSFET and allowed to discharge when the top MOSFET is OFF. In order to minimize frequency variations while providing different supply voltages, the discharge current is modulated by the voltage at the $V_{CC_CORE}$ pin. The OFF-time is inversely proportional to the $V_{CC_CORE}$ voltage.

### UNDER VOLTAGE LOCKOUT SECTION

The purpose of the UVLO is to keep the output drive off until the input voltage reaches the start-up threshold. At voltages below the start-up voltage, the UVLO comparator disables the internal biasing, and turns off the output drives, and the SS (Soft-Start) pin is pulled low.

### SYNCHRONOUS CONTROL SECTION

The synchronous control section incorporates a unique break-before-make function to ensure that the primary switch and the synchronous switch are not turned on at the same time. Approximately 100 nanoseconds of deadtime is provided by the break-before-make circuitry to protect the MOSFET switches.

### PROGRAMMING THE OUTPUT VOLTAGE

The output voltage is set by means of a 5-bit digital Voltage Identification (VID) word (See Table 1). The VID code may be incorporated into the package of the processor or the output voltage can be set by means of a DIP switch or jumpers. For a low or '0' signal, connect the VID pin to ground (DIP switch ON/CLOSED); for a high or '1' signal, leave the VID pin open (DIP switch OFF/OPEN).

The five VID pins on the LX166x series are designed to interface directly with a Pentium Pro or Pentium II processor. Therefore, all inputs are expected to be either ground or floating. Any floating input will be pulled high by internal connections. If using a Socket 7 processor, or other load, the VID code can be set directly by connecting jumpers or DIP switches to the VID[0:4] pins.

The VID pins **are not designed to take TTL inputs, and should not be connected high.** Unpredictable output voltages may result. If the LX166x devices are to be connected to a logic circuit, such as BIOS, for programming of output voltage, they should be buffered using a CMOS gate with open-drain, such as a 74HC125 or 74C906.

### POWER GOOD SIGNAL (LX1663 only)

An open collector output is provided which presents high impedance when the output voltage is between 90% and 117% of the programmed VID voltage, measured at the SS pin. Outside this window the output presents a low impedance path to ground. The Power Good function also toggles low during OVP operation.

### OVER-VOLTAGE PROTECTION

The controller is inherently protected from an over-voltage condition due to its constant OFF-time architecture. However, should a failure occur at the power switch, an over-voltage drive pin is provided (on the LX1663 only) which can drive an external SCR crowbar ($Q_3$), and so blow a fuse ($F_1$). The fault condition must be removed and power recycled for the LX1663 to resume normal operation (See Figure 9).



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## APPLICATION INFORMATION

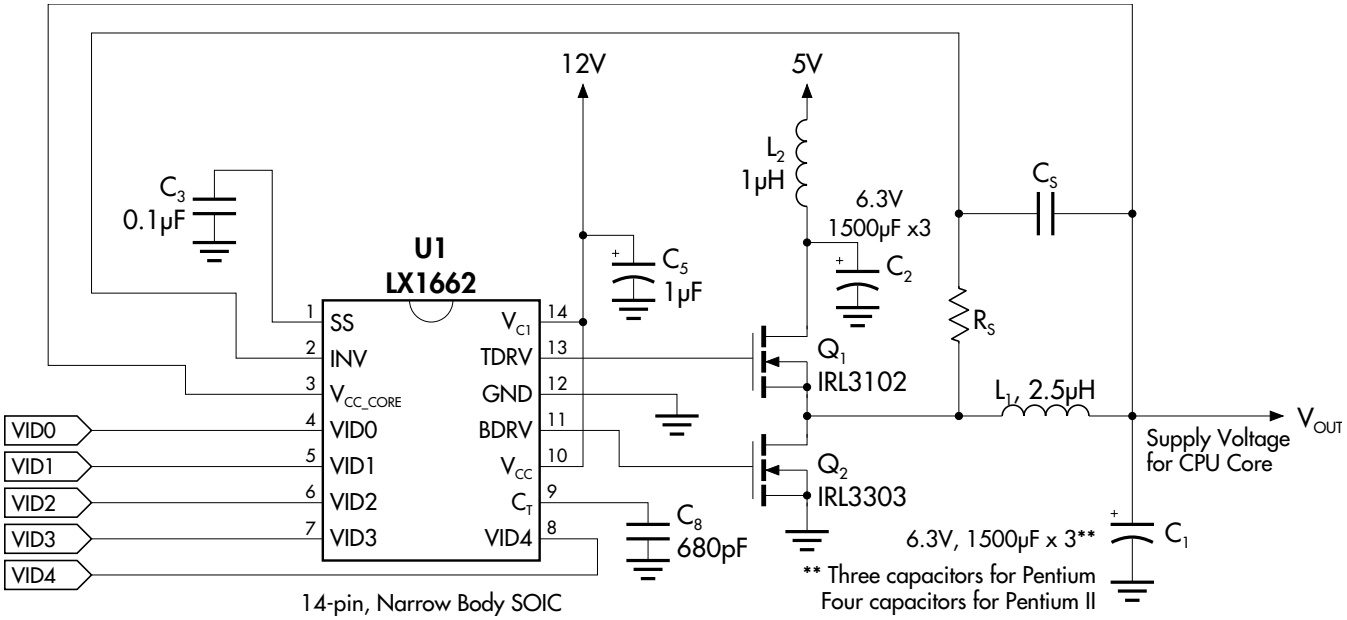


**FIGURE 6** — LX1662 In A Pentium / Pentium II Processor Single Chip Power Supply Controller Solution With Loss-Less Current Sensing (Synchronous)

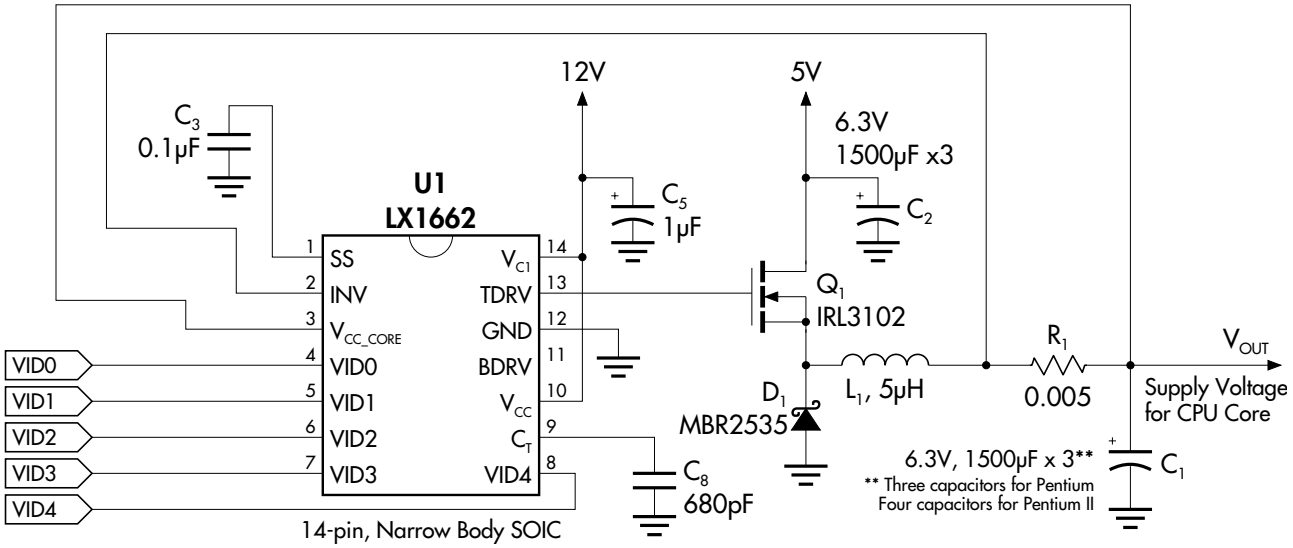


**FIGURE 7** — LX1662 In A Non-Synchronous Pentium / Socket 7 Power Supply Application

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## APPLICATION INFORMATION

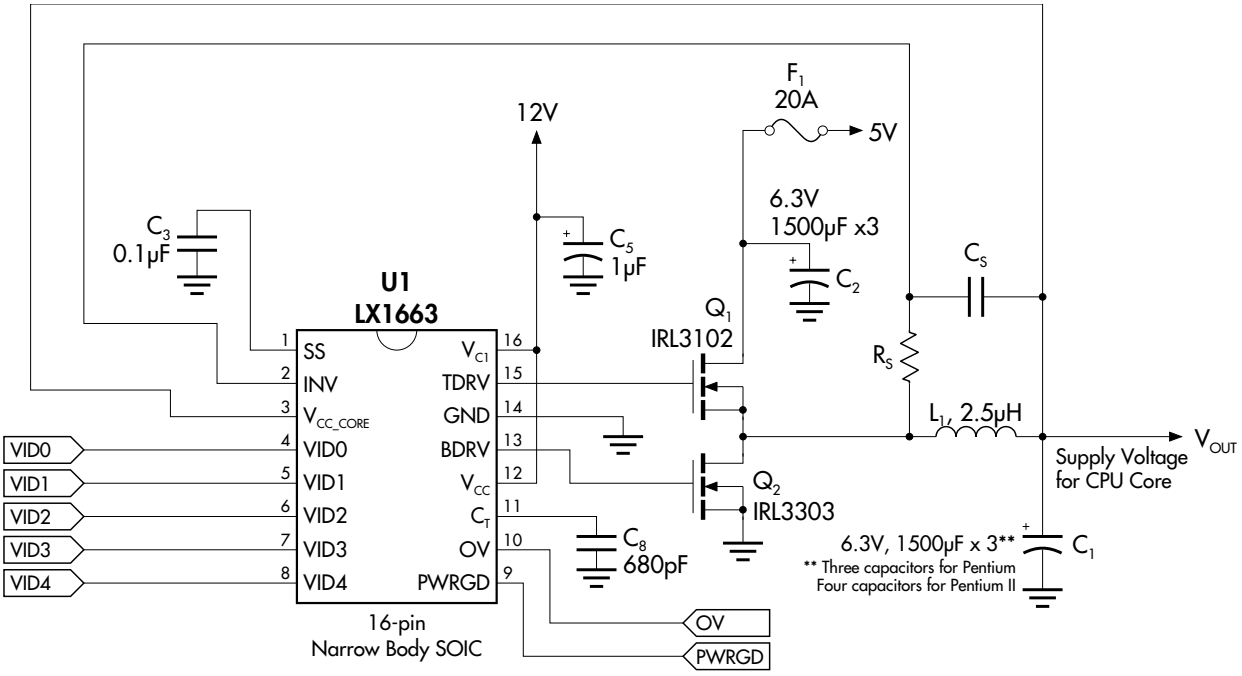


**FIGURE 8** — Pentium II Processor Application With OVP, Power Good And Loss-Less Current Sensing (Synchronous)

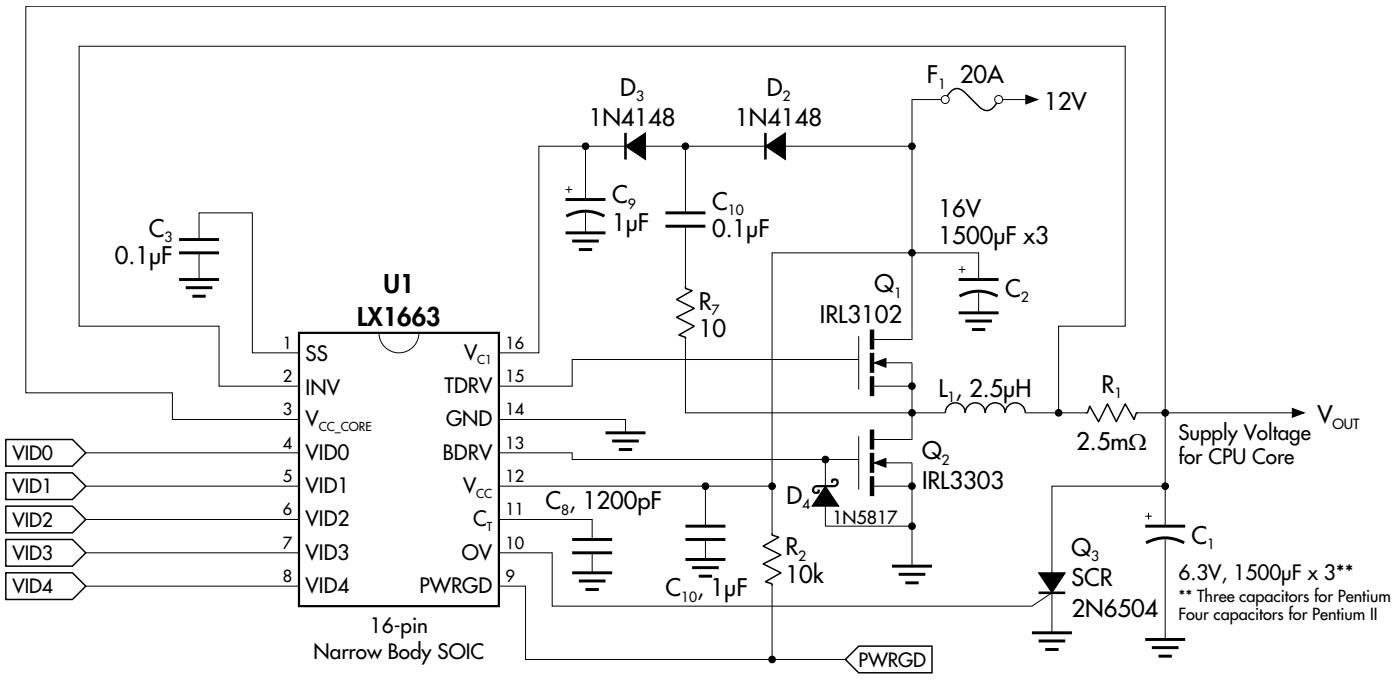


**FIGURE 9** — Full-Featured Pentium II Processor Supply With 12V Power Input



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## BILL OF MATERIALS

**LX1662 Bill of Materials** (Refer to Product Highlight)

| Ref | Description | Part Number / Manufacturer | Qty. |
|---|---|---|---|
| $C_2$ | 1500µF, 6.3V capacitor | MV-GX Sanyo | 2 |
| $C_1$ | 1500µF, 6.3V capacitor | MV-GX Sanyo | 4 |
| $C_8$ | 680pF | SMD Cap | 1 |
| $C_3$ | 0.1µF | SMD Cap | 1 |
| $C_5$ | 1µF, 16V | SMD Ceramic | 1 |
| $L_1$ | 5µF Inductor | HM0096832 BI | 1 |
| $L_2$ | 1µF Inductor | | 1 |
| $Q_1$ | MOSFET | IRL3102 International Rectifier or equivalent | 1 |
| $Q_2$ | MOSFET | IRL3303 International Rectifier or equivalent | 1 |
| $R_1$ | 2.5mΩ Sense Resistor (PCB trace) | | 1 |
| U1 | Controller IC | LX1662CD Linfinity | 1 |
| **Total** | | | **15** |

## USING THE LX1662/63 DEVICES

The LX1662/63 devices are very easy to design with, requiring only a few simple calculations to implement a given design. The following procedures and considerations should provide effective operation for virtually all applications. Refer to the **Application Information** section for component reference designators.

### TIMING CAPACITOR SELECTION

The frequency of operation of the LX166x is a function of duty cycle and OFF-time. The OFF-time is proportional to the timing capacitor (which is shown as $C_8$ in all application schematics in this data sheet), and is modulated to minimize frequency variations with duty cycle. The frequency is constant, during steady-state operation, due to the modulation of the OFF-time.

The timing capacitor ($C_T$) should be selected using the following equation:

$$C_T = \frac{(1 - V_{OUT}/V_{IN}) * I_{DIS}}{f_S(1.52 - 0.29 * V_{OUT})}$$

Where $I_{DIS}$ is fixed at 200µA and $f_S$ is the switching frequency (recommended to be around 200kHz for optimal operation and component selection).

When using a 5V input voltage, the switching frequency ($f_S$) can be approximated as follows:

$$C_T = 0.621 * \frac{I_{DIS}}{f_S}$$

Choosing a 680pF capacitor will result in an operating frequency of 183kHz at $V_{OUT}$ = 2.8V. When a 12V power input is used, he capacitor value must be changed (the optimal timing capacitor for 12V input will be in the range of 1000-1500pF).

### $L_1$ OUTPUT INDUCTOR SELECTION

The inductance value chosen determines the ripple current present at the output of the power supply. Size the inductance to allow a nominal ±10% swing above and below the nominal DC load current, using the equation $L = V_L * \Delta T/\Delta I$, where $\Delta T$ is the OFF-time, $V_L$ is the voltage across the inductor during the OFF-time, and $\Delta I$ is peak-to-peak ripple current in the inductor. Be sure to select a high-frequency core material which can handle the DC current, such as 3C8, which is sized for the correct power level. Typical inductance values can range from 2 to 10µH.

Note that ripple current will increase with a smaller inductor. Exceeding the ripple current rating of the capacitors could cause reliability problems.

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## USING THE LX1662/63 DEVICES

### INPUT INDUCTOR SELECTION

In order to cope with faster transient load changes, a smaller output inductor is needed. However, reducing the size of the output inductor will result in a higher ripple voltage on the input supply. This noise on the 5V rail can affect other loads, such as graphics cards. It is recommended that a smaller input inductor, $L_2$ (1 - 1.5µH), is used on the 5V rail to filter out the ripple. Ensure that this inductor has the same current rating as the output inductor.

### $C_1$ FILTER CAPACITOR SELECTION

The capacitors on the output of the PWM section are used to filter the output current ripple, as well as help during transient load conditions, and the capacitor bank should be sized to meet ripple and transient performance specifications.

When a transient (step) load current change occurs, the output voltage will have a step which equals the product of the Effective Series Resistance (ESR) of the capacitor and the current step (ΔI). when current increases from low (in sleep mode) to high, the output voltage will drop below its steady state value. In the advanced microprocessor power supply, the capacitor should usually be selected on the basis of its ESR value, rather than the capacitance or RMS current capability. Capacitors that satisfy the ESR requirement usually have a larger capacitance and current capability than needed for the application. The allowable ESR can be found by:

$$ESR * (I_{RIPPLE} + \Delta I) < V_{EX}$$

Where $V_{EX}$ is the allowable output voltage excursion in the transient and $I_{RIPPLE}$ is the inductor ripple current. Regulators such as the LX166x series, have adaptive output voltage positioning, which adds 40mV to the DC set-point voltage — $V_{EX}$ is therefore the difference between the low load voltage and the minimum dynamic voltage allowed for the microprocessor.

Ripple current is a function of the output inductor value ($L_{OUT}$), and can be approximated as follows:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{f_S * L_{OUT}} * \frac{V_{OUT}}{V_{IN}}$$

Where $f_S$ is the switching frequency.

Electrolytic capacitors can be used for the output filter capacitor bank, but are less stable with age than tantalum capacitors. As they age, their ESR degrades, reducing the system performance and increasing the risk of failure. It is recommended that multiple parallel capacitors are used so that, as ESR increases with age, overall performance will still meet the processor's requirements.

There is frequently strong pressure to use the least expensive components possible, however, this could lead to degraded long-term reliability, especially in the case of filter capacitors. Linfinity's demo boards use Sanyo MV-GX filter capacitors, which are aluminum electrolytic, and have demonstrated reliability. The Oscon series from Sanyo generally provides the very best performance in terms of long term ESR stability and general reliability, but at a substantial cost penalty. The MV-GX series provides excellent ESR performance, meeting all Intel transient specifications, at a reasonable cost. Beware of off-brand, very-low cost filter capacitors, which have been shown to degrade in both ESR and general electrolyte characteristics over time.

### CURRENT LIMIT

Current limiting occurs when a sensed voltage, proportional to load current, exceeds the current-sense comparator threshold value. The current can be sensed either by using a fixed sense resistor in series with the inductor to cause a voltage drop proportional to current, or by using a resistor and capacitor in parallel with the inductor to sense the voltage drop across the parasitic resistance of the inductor.

The LX166x family offers two different comparator thresholds. The LX1662 & 1663 have a threshold of 100mV, while the LX1662A and LX1663A have a threshold of 60mV. The 60mV threshold is better suited to higher current loads, such as a Pentium II or Deschutes processor.

#### *Sense Resistor*

The current sense resistor, $R_1$, is selected according to the formula:

$$R_1 = V_{TRIP} / I_{TRIP}$$

Where $V_{TRIP}$ is the current sense comparator threshold (100mV for LX1662/63 and 60mV for LX1662A/63A) and $I_{TRIP}$ is the desired current limit. Typical choices are shown below.

**TABLE 2 - Current Sense Resistor Selection Guide**

| Load | Sense Resistor Value | Recommended Controller |
|---|---|---|
| Pentium-Class Processor (<10A) | 5mΩ | LX1662 or LX1663 |
| Pentium II Class (>10A) | 2.5mΩ | LX1662A or LX1663A |

A smaller sense resistor will result in lower heat dissipation ($I^2R$) and also a smaller output voltage droop at higher currents.

There are several alternative types of sense resistor. The surface-mount metal "staple" form of resistor has the advantage of exposure to free air to dissipate heat and its value can be controlled very tightly. Its main drawback, however, is cost. An alternative is to construct the sense resistor using a copper PCB trace. Although the resistance cannot be controlled as tightly, the PCB trace is very low cost.



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## USING THE LX1662/63 DEVICES

**CURRENT LIMIT** (continued)

***PCB Sense Resistor***

A PCB sense resistor should be constructed as shown in Figure 10. By attaching directly to the large pads for the capacitor and inductor, heat is dissipated efficiently by the larger copper masses. Connect the current sense lines as shown to avoid any errors.

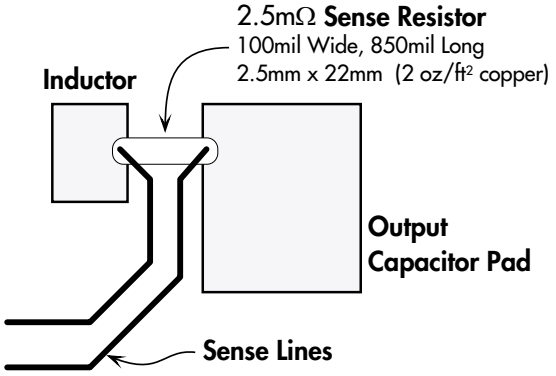


**FIGURE 10** — Sense Resistor Construction Diagram

Recommended sense resistor sizes are given in the following table:

**TABLE 3 - PCB Sense Resistor Selection Guide**

| Copper Weight | Copper Thickness | Desired Resistor Value | Dimensions (w x l) mm | inches |
|---|---|---|---|---|
| 2 oz/ft² | 68µm | 2.5mΩ | 2.5 x 22 | 0.1 x 0.85 |
| | | 5mΩ | 2.5 x 43 | 0.1 x 1.7 |

***Loss-Less Current Sensing Using Resistance of Inductor***

Any inductor has a parasitic resistance, $R_L$, which causes a DC voltage drop when current flows through the inductor. Figure 11 shows a sensor circuit comprising of a surface mount resistor, $R_S$, and capacitor, $C_S$, in parallel with the inductor, eliminating the current sense resistor.

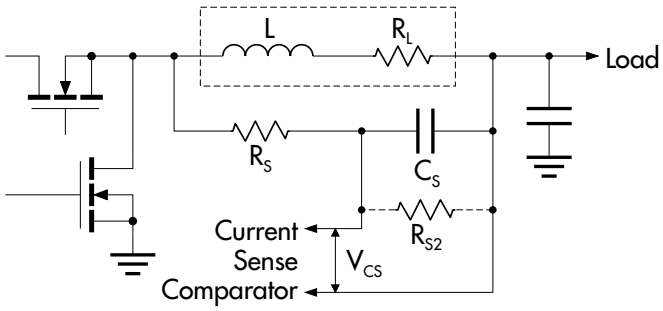


**FIGURE 11** — Current Sense Circuit

**CURRENT LIMIT** (continued)

The current flowing through the inductor is a triangle wave. If the sensor components are selected such that:

$$L/R_L = R_S * C_S$$

The voltage across the capacitor will be equal to the current flowing through the resistor, i.e.

$$V_{CS} = I_L R_L$$

Since $V_{CS}$ reflects the inductor current, by selecting the appropriate $R_S$ and $C_S$, $V_{CS}$ can be made to reach the comparator voltage (60mV for LX166xA or 100mV for the LX166x) at the desired trip current.

***Design Example***

*(Pentium II circuit, with a maximum static current of 14.2A)*

The gain of the sensor can be characterized as:

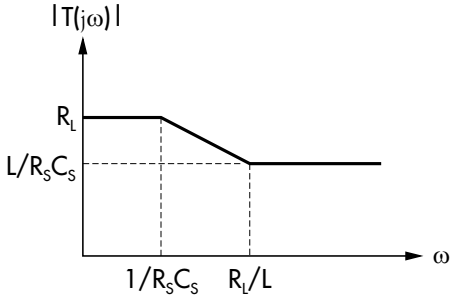


**FIGURE 12** — Sensor Gain

The dc/static tripping current $I_{trip,S}$ satisfies:

$$I_{trip,S} = \frac{V_{trip}}{R_L}$$

Select $L/R_SC_S \le R_L$ to have higher dynamic tripping current than the static one. The dynamic tripping current $I_{trip,d}$ satisfies:

$$I_{trip,d} = \frac{V_{trip}}{L/(R_S C_S)}$$

***General Guidelines for Selecting $R_S$, $C_S$, and $R_L$***

$$R_L = \frac{V_{trip}}{I_{trip,S}}$$ Select: $R_S \le 10\ k\Omega$

and $C_S$ according to: $$C_{S\,n} = \frac{L_n}{R_L R_S}$$

The above equation has taken into account the current-dependency of the inductance.

The test circuit (Figure 6) used the following parameters: $R_L$ = 3mΩ, $R_S$ = 9kΩ, $C_S$ = 0.1µF, and L is 2.5µH at 0A current.

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## USING THE LX1662/63 DEVICES

### CURRENT LIMIT (continued)

In cases where $R_L$ is so large that the trip point current would be lower than the desired short-circuit current limit, a resistor ($R_{S2}$) can be put in parallel with $C_S$, as shown in Figure 11. The selection of components is as follows:

$$\frac{R_{L\,(Required)}}{R_{L\,(Actual)}} = \frac{R_{S2}}{R_{S2} + R_S}$$

$$C_S = \frac{L}{R_{L\,(Actual)} * (R_{S2} // R_S)} = \frac{L}{R_{L\,(Actual)}} * \frac{R_S + R_{S2}}{R_{S2} * R_S}$$

Again, select ($R_{S2}$//$R_S$) < 10kΩ.

### FET SELECTION

To insure reliable operation, the operating junction temperature of the FET switches must be kept below certain limits. The Intel specification states that 115°C maximum junction temperature should be maintained with an ambient of 50°C. This is achieved by properly derating the part, and by adequate heat sinking. One of the most critical parameters for FET selection is the $R_{DS}$ ON resistance. This parameter directly contributes to the power dissipation of the FET devices, and thus impacts heat sink design, mechanical layout, and reliability. In general, the larger the current handling capability of the FET, the lower the $R_{DS}$ ON will be, since more die area is available.

**TABLE 4 - FET Selection Guide**

This table gives selection of suitable FETs from International Rectifier.

| Device | $R_{DS(ON)}$ @ 10V (mΩ) | $I_D$ @ $T_C$ = 100°C | Max. Break-down Voltage |
|---|---|---|---|
| IRL3803 | 6 | 83 | 30 |
| IRL22203N | 7 | 71 | 30 |
| IRL3103 | 14 | 40 | 30 |
| IRL3102 | 13 | 56 | 20 |
| IRL3303 | 26 | 24 | 30 |
| IRL2703 | 40 | 17 | 30 |

All devices in TO-220 package. For surface mount devices (TO-263 / $D^2$-Pak), add 'S' to part number, e.g. IRL3103S.

The recommended solution is to use IRL3102 for the high side and IRL3303 for the low side FET, for the best combination of cost and performance. Alternative FET's from any manufacturer could be used, provided they meet the same criteria for $R_{DS(ON)}$.

#### *Heat Dissipated In Upper MOSFET*

The heat dissipated in the top MOSFET will be:

$$P_D = (I^2 * R_{DS(ON)} * Duty\ Cycle) + (0.51 * V_{IN} * t_{SW} * f_S)$$

Where $t_{SW}$ is switching transition line for body diode (~100ns) and $f_S$ is the switching frequency.

### FET SELECTION (continued)

For the IRL3102 (13mΩ $R_{DS(ON)}$), converting 5V to 2.8V at 14A will result in typical heat dissipation of 1.48W.

#### *Synchronous Rectification – Lower MOSFET*

The lower pass element can be either a MOSFET or a Schottky diode. The use of a MOSFET (synchronous rectification) will result in higher efficiency, but at higher cost than using a Schottky diode (non-synchronous).

Power dissipated in the bottom MOSFET will be:

$$P_D = I^2 * R_{DS(ON)} * [1 - Duty\ Cycle] = 2.24W$$

[IRL3303 or 1.12W for the IRL3102]

#### *Catch Diode – Lower MOSFET*

A low-power Schottky diode, such as a 1N5817, is recommended to be connected between the gate and source of the lower MOSFET when operating from a 12V-power supply (see Figure 9). This will help protect the controller IC against latch-up due to the inductor voltage going negative. Although latch-up is unlikely, the use of such a catch diode will improve reliability and is highly recommended.

#### *Non-Synchronous Operation - Schottky Diode*

A typical Schottky diode, with a forward drop of 0.6V will dissipate 0.6∗ 14∗ [1 – 2.8/5] = 3.7W (compared to the 1.1 to 2.2W dissipated by a MOSFET under the same conditions). This power loss becomes much more significant at lower duty cycles – synchronous rectification is recommended especially when a 12V-power input is used. The use of a dual Schottky diode in a single TO-220 package (e.g. the MBR2535) helps improve thermal dissipation.

### MOSFET GATE BIAS

The power MOSFETs can be biased by one of two methods: charge pump or 12V supply connected to $V_{C1}$.

1) **Charge Pump (Bootstrap)**
When 12V is supplied to the drain of the MOSFET, as in Figure 9, the gate drive needs to be higher than 12V in order to turn the MOSFET on. Capacitor $C_{10}$ and diodes $D_2$ & $D_3$ are used as a charge pump voltage doubling circuit to raise the voltage of $V_{C1}$ so that the TDRV pin always provides a high enough voltage to turn on $Q_1$. The 12V supply must always be connected to $V_{CC}$ to provide power for the IC itself, as well as gate drive for the bottom MOSFET.

2) **12V Supply**
When 5V is supplied to the drain of $Q_1$, a 12V supply should be connected to both $V_{CC}$ and $V_{C1}$.



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## USING THE LX1662/63 DEVICES

### LAYOUT GUIDELINES - THERMAL DESIGN

A great deal of time and effort were spent optimizing the thermal design of the demo boards. Any user who intends to implement an embedded motherboard would be well advised to carefully read and follow these guidelines. If the FET switches have been carefully selected, external heatsinking is generally not required. However, this means that copper trace on the PC board must now be used. This is a potential trouble spot; as much copper area as possible must be dedicated to heatsinking the FET switches, and the diode as well if a non-synchronous solution is used.

In our VRM module, heatsink area was taken from internal ground and $V_{CC}$ planes which were actually split and connected with VIAS to the power device tabs. The TO-220 and TO-263 cases are well suited for this application, and are the preferred packages. Remember to remove any conformal coating from all exposed PC traces which are involved in heatsinking.

#### *General Notes*

As always, be sure to provide local capacitive decoupling close to the chip. Be sure use ground plane construction for all high-frequency work. Use low ESR capacitors where justified, but be alert for damping and ringing problems. High-frequency designs demand careful routing and layout, and may require several iterations to achieve desired performance levels.

#### *Power Traces*

To reduce power losses due to ohmic resistance, careful consideration should be given to the layout of traces that carry high currents. The main paths to consider are:

- Input power from 5V supply to drain of top MOSFET.
- Trace between top MOSFET and lower MOSFET or Schottky diode.
- Trace between lower MOSFET or Schottky diode and ground.
- Trace between source of top MOSFET and inductor, sense resistor and load.

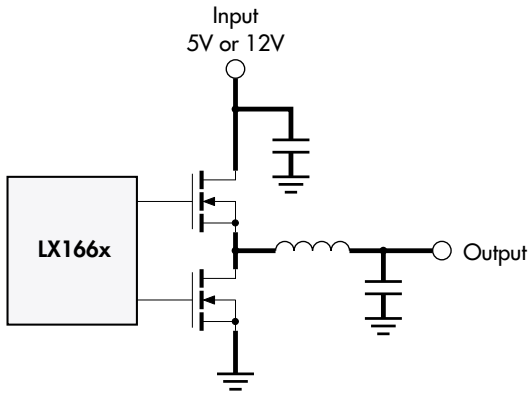


**FIGURE 13** — Power Traces

All of these traces should be made as wide and thick as possible, in order to minimize resistance and hence power losses. It is also recommended that, whenever possible, the ground, input and output power signals should be on separate planes (PCB layers). See Figure 13 – bold traces are power traces.

#### *$C_5$ Input Decoupling ($V_{CC}$) Capacitor*

Ensure that this 1µF capacitor is placed as close to the IC as possible to minimize the effects of noise on the device.

#### *Layout Assistance*

Please contact Linfinity's Applications Engineers for assistance with any layout or component selection issues. A Gerber file with layout for the most popular devices is available upon request.

Evaluation boards are also available upon request. Please check Linfinity's web site for further application notes.

## RELATED DEVICES

**LX1664/1665** - Dual Output PWM for µProcessor Applications
**LX1668** - Triple Output PWM for µProcessor Applications
**LX1553** - PWM for 5V - 3.3V Conversion

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