MT88L70

3 Volt Integrated DTMF Receiver

Data Sheet

August 2005

Features

- 2.7 - 3.6 volt operation
- Complete DTMF receiver
- Low power consumption
- Internal gain setting amplifier
- Adjustable guard time
- Central office quality
- Power-down mode
- Inhibit mode
- Functionally compatible with Zarlink's MT8870D

Applications

- Paging systems
- Repeater systems/mobile radio
- Credit card systems
- Remote control
- Personal computers
- Telephone answering machine

Ordering Information

MT88L70AE	18 Pin PDIP	Tubes
MT88L70AS	18 Pin SOIC	Tubes
MT88L70AN	20 Pin SSOP	Tubes
MT88L70ASR	18 Pin SOIC	Tape & Reel
MT88L70ANR	20 Pin SSOP	Tape & Reel
MT88L70AE1	18 Pin PDIP*	Tubes
MT88L70AN1	20 Pin SSOP*	Tubes
MT88L70ANR1	20 Pin SSOP*	Tape & Reel
MT88L70AS1	18 Pin SOIC*	Tubes
MT88L70ASR1	18 Pin SOIC*	Tape & Reel

* Pb Free Matte Tin

-40°C to +85°C

Description

The MT88L70 is a complete 3 Volt, DTMF receiver integrating both the bandsplit filter and digital decoder functions. The filter section uses switched capacitor techniques for high and low group filters; the decoder uses digital counting techniques to detect and decode all 16 DTMF tone-pairs into a 4-bit code. External component count is minimized by on chip provision of a differential input amplifier, clock oscillator and latched three-state bus interface.

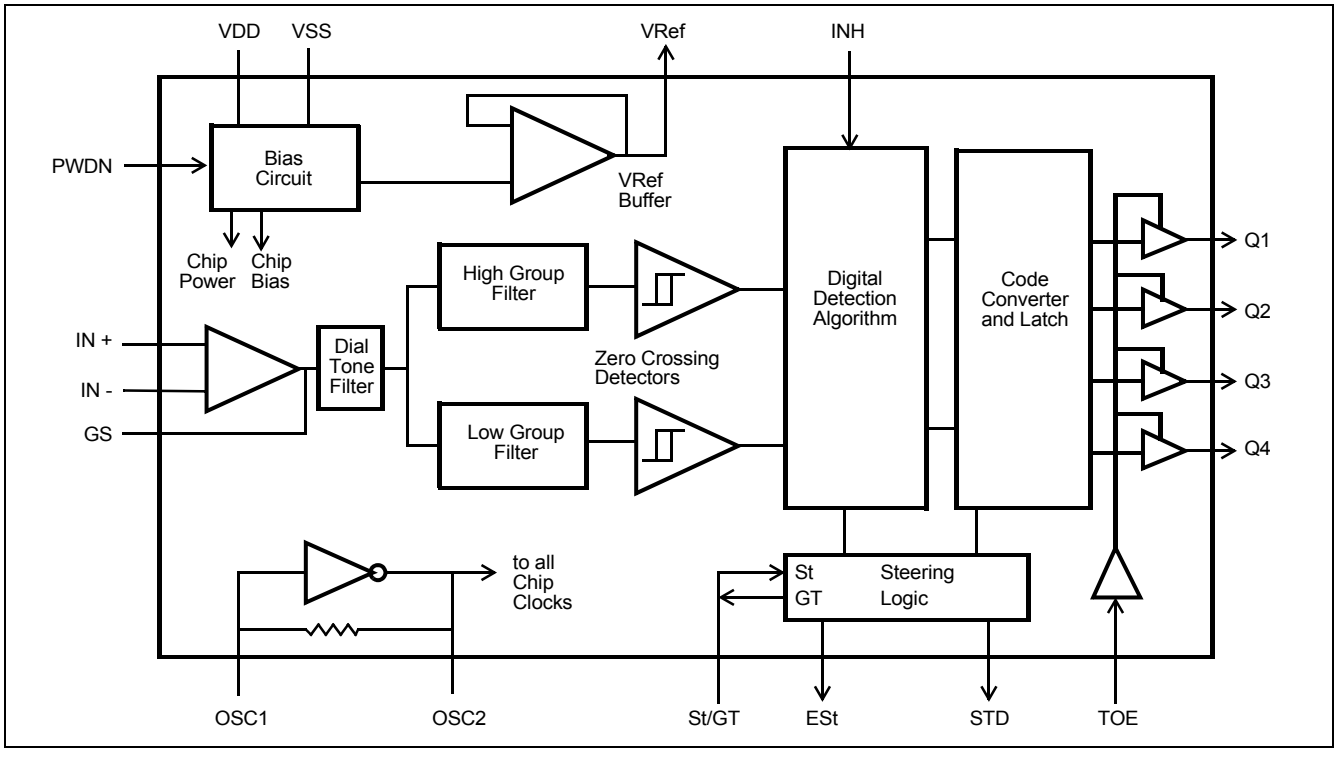

Figure 1 - Functional Block Diagram

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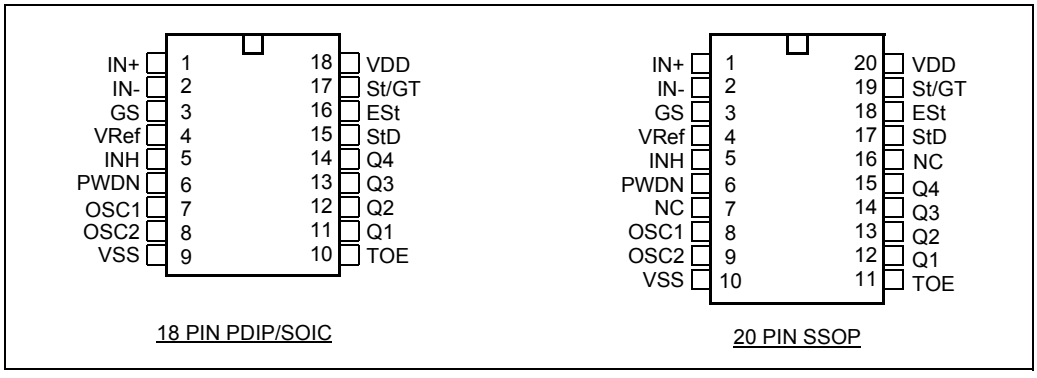


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
18	**20**		
1	1	IN+	**Non-Inverting Op-Amp (Input).**
2	2	IN-	**Inverting Op-Amp (Input)**.
3	3	GS	**Gain Select.** Gives access to output of front end differential amplifier for connection of feedback resistor.
4	4	V_{Ref}	**Reference Voltage (Output).** Nominally $V_{DD}/2$ is used to bias inputs at mid-rail (see Figure 5 and Figure 6).
5	5	INH	**Inhibit (Input).** Logic high inhibits the detection of tones representing characters A, B, C and D. This pin input is internally pulled down.
6	6	PWDN	**Power Down (Input).** Active high. Powers down the device and inhibits the oscillator. This pin input is internally pulled down.
7	8	OSC1	**Clock (Input)**.
8	9	OSC2	**Clock (Output)**. A 3.579545 MHz crystal connected between pins OSC1 and OSC2 completes the internal oscillator circuit.
9	10	V_{SS}	**Ground (Input)**. 0 V typical.
10	11	TOE	**Three State Output Enable (Input).** Logic high enables the outputs Q1-Q4. This pin is pulled up internally.
11-14	12-15	Q1-Q4	**Three State Data (Output).** When enabled by TOE, provide the code corresponding to the last valid tone-pair received (see Table 1). When TOE is logic low, the data outputs are high impedance.
15	17	StD	**Delayed Steering (Output).**Presents a logic high when a received tone-pair has been registered and the output latch updated; returns to logic low when the voltage on St/GT falls below $V_{TSt.}$
16	18	ESt	**Early Steering (Output).** Presents a logic high once the digital algorithm has detected a valid tone pair (signal condition). Any momentary loss of signal condition will cause ESt to return to a logic low.

Pin Description

Pin #		Name	Description
18	20		
17	19	St/GT	**Steering Input/Guard time (Output) Bidirectional.** A voltage greater than V_{TSt} detected at St causes the device to register the detected tone pair and update the output latch. A voltage less than V_{TSt} frees the device to accept a new tone pair. The GT output acts to reset the external steering time-constant; its state is a function of ESt and the voltage on St.
18	20	V_{DD}	**Positive power supply (Input)**. +3 V typical.
	7, 16	NC	No Connection.

Functional Description

The MT88L70 monolithic DTMF receiver offers small size, low power consumption and high performance, with 3 volt operation. Its architecture consists of a bandsplit filter section, which separates the high and low group tones, followed by a digital counting section which verifies the frequency and duration of the received tones before passing the corresponding code to the output bus.

Filter Section

Separation of the low-group and high group tones is achieved by applying the DTMF signal to the inputs of two sixth-order switched capacitor bandpass filters, the bandwidths of which correspond to the low and high group frequencies. The filter section also incorporates notches at 350 and 440 Hz for exceptional dial tone rejection. Each filter output is followed by a single order switched capacitor filter section which smooths the signals prior to limiting. Limiting is performed by high-gain comparators which are provided with hysteresis to prevent detection of unwanted low-level signals. The outputs of the comparators provide full rail logic swings at the frequencies of the incoming DTMF signals.

Decoder Section

Following the filter section is a decoder employing digital counting techniques to determine the frequencies of the incoming tones and to verify that they correspond to standard DTMF frequencies. A complex averaging algorithm protects against tone simulation by extraneous signals such as voice while providing tolerance to small frequency deviations and variations. This averaging algorithm has been developed to ensure an optimum combination of immunity to talk-off and tolerance to the presence of interfering frequencies (third tones) and noise. When the detector recognizes the presence of two valid tones (this is referred to as the “signal condition” in some industry specifications) the “Early Steering” (ESt) output will go to an active state. Any subsequent loss of signal condition will cause ESt to assume an inactive state (see “Steering Circuit”).

Steering Circuit

Before registration of a decoded tone pair, the receiver checks for a valid signal duration (referred to as character recognition condition). This check is performed by an external RC time constant driven by ESt. A logic high on ESt causes v_c (see Figure 3) to rise as the capacitor discharges. Provided signal condition is maintained (ESt remains high) for the validation period (t_{GTP}), v_c reaches the threshold (V_{TSt}) of the steering logic to register the tone pair, latching its corresponding 4-bit code (see Table 1) into the output latch. At this point the GT output is activated and drives v_c to V_{DD}. GT continues to drive high as long as ESt remains high. Finally, after a short delay to allow the output latch to settle, the delayed steering output flag (StD) goes high, signalling that a received tone pair has been registered. The contents of the output latch are made available on the 4-bit output bus by raising the three state control input (TOE) to a logic high. The steering circuit works in reverse to validate the interdigit pause between signals. Thus, as well as rejecting signals too short to be considered valid, the receiver will tolerate signal interruptions (dropout) too short to be considered a valid pause. This facility, together with the capability of selecting

the steering time constants externally, allows the designer to tailor performance to meet a wide variety of system requirements.

Digit	TOE	INH	ESt	Q_4	Q_3	Q_2	Q_1
ANY	L	X	H	Z	Z	Z	Z
1	H	X	H	0	0	0	1
2	H	X	H	0	0	1	0
3	H	X	H	0	0	1	1
4	H	X	H	0	1	0	0
5	H	X	H	0	1	0	1
6	H	X	H	0	1	1	0
7	H	X	H	0	1	1	1
8	H	X	H	1	0	0	0
9	H	X	H	1	0	0	1
0	H	X	H	1	0	1	0
*	H	X	H	1	0	1	1
#	H	X	H	1	1	0	0
A	H	L	H	1	1	0	1
B	H	L	H	1	1	1	0
C	H	L	H	1	1	1	1
D	H	L	H	0	0	0	0
A	H	H	L	undetected, the output code will remain the same as the previous detected code			
B	H	H	L				
C	H	H	L				
D	H	H	L				

Table 1 - Functional Decode Table

L=LOGIC LOW, H=LOGIC HIGH, Z=HIGH IMPEDANCE
X = DON'T CARE

Guard Time Adjustment

In many situations not requiring selection of tone duration and interdigital pause, the simple steering circuit shown in Figure 3 is applicable. Component values are chosen according to the formula:

$$t_{REC}=t_{DP}+t_{GTP}$$
$$t_{ID}=t_{DA}+t_{GTA}$$

The value of t_{DP} is a device parameter (see Figure 7) and t_{REC} is the minimum signal duration to be recognized by the receiver. A value for C of 0.1 μF is recommended for most applications, leaving R to be selected by the designer.

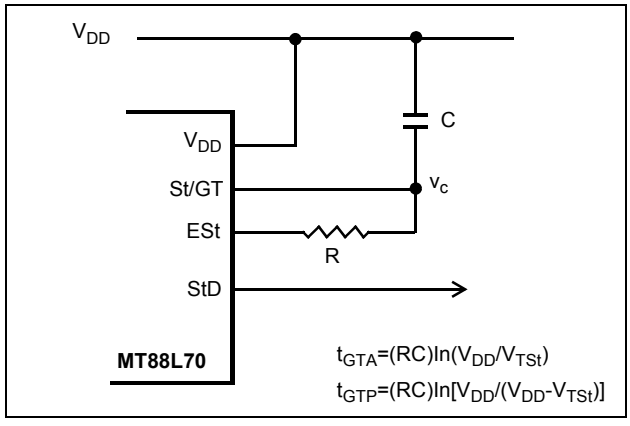


Figure 3 - Basic Steering Circuit

Different steering arrangements may be used to select independently the guard times for tone present (t_{GTP}) and tone absent (t_{GTA}). This may be necessary to meet system specifications which place both accept and reject limits on both tone duration and interdigital pause. Guard time adjustment also allows the designer to tailor system parameters such as talk off and noise immunity. Increasing t_{REC} improves talk-off performance since it reduces the probability that tones simulated by speech will maintain signal condition long enough to be registered. Alternatively, a relatively short t_{REC} with a long t_{DO} would be appropriate for extremely noisy environments where fast acquisition time and immunity to tone drop-outs are required. Design information for guard time adjustment is shown in Figure 4.

Power-down and Inhibit Mode

A logic high applied to pin 6 (PWDN) will power down the device to minimize the power consumption in a standby mode. It stops the oscillator and the functions of the filters.

Inhibit mode is enabled by a logic high input to the pin 5 (INH). It inhibits the detection of tones representing characters A, B, C, and D. The output code will remain the same as the previous detected code (see Table 1).

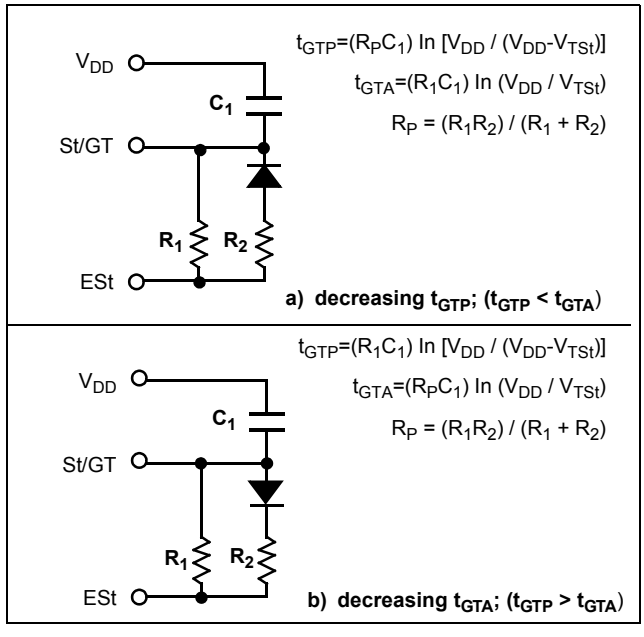
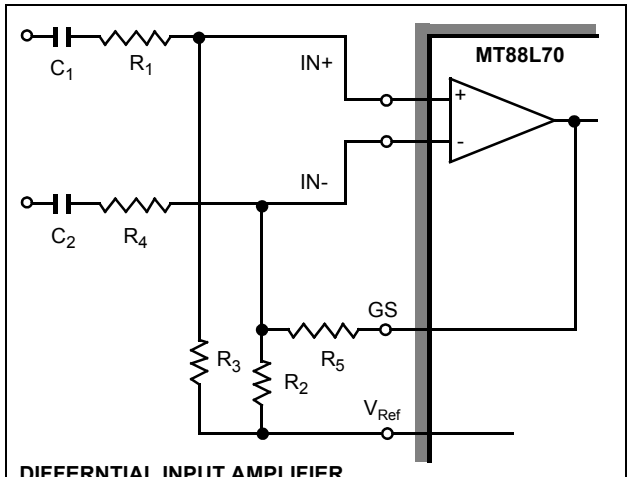


Figure 4 - Guard Time Adjustment

Differential Input Configuration

The input arrangement of the MT88L70 provides a differential-input operational amplifier as well as a bias source (V_{Ref}) which is used to bias the inputs at mid-rail. Provision is made for connection of a feedback resistor to the op-amp output (GS) for adjustment of gain. In a single-ended configuration, the input pins are connected as shown in Figure 6 with the op-amp connected for unity gain and V_{Ref} biasing the input at $1/2V_{DD}$. Figure 5 shows the differential configuration, which permits the adjustment of gain with the feedback resistor R_5.



DIFFERNTIAL INPUT AMPLIFIER

$C_1 = C_2 = 10$ nF
$R_1 = R_4 = R_5 = 100$ kΩ
$R_2 = 60$ kΩ, R_3, = 37.5 kΩ

All resistors are ± 1% tolerance.
All capacitors are ± 5% tolerance.

$$R_3 = \frac{R_2 R_5}{R_2 + R_5}$$

VOLTAGE GAIN (A_V diff) = $\frac{R5}{R1}$

INPUT IMPEDANCE

$$(Z_{INDIFF}) = 2\sqrt{R_1^2 + \left(\frac{1}{\omega C}\right)^2}$$

Figure 5 - Differential Input Configuration

Crystal Oscillator

The internal clock circuit is completed with the addition of an external 3.579545 MHz crystal and is connected as shown in Figure 6 (Single-ended Input Configuration).

Applications

A single-ended input configuration is shown in Figure 6. For applications with differential signal inputs the circuit shown in Figure 5 may be used.

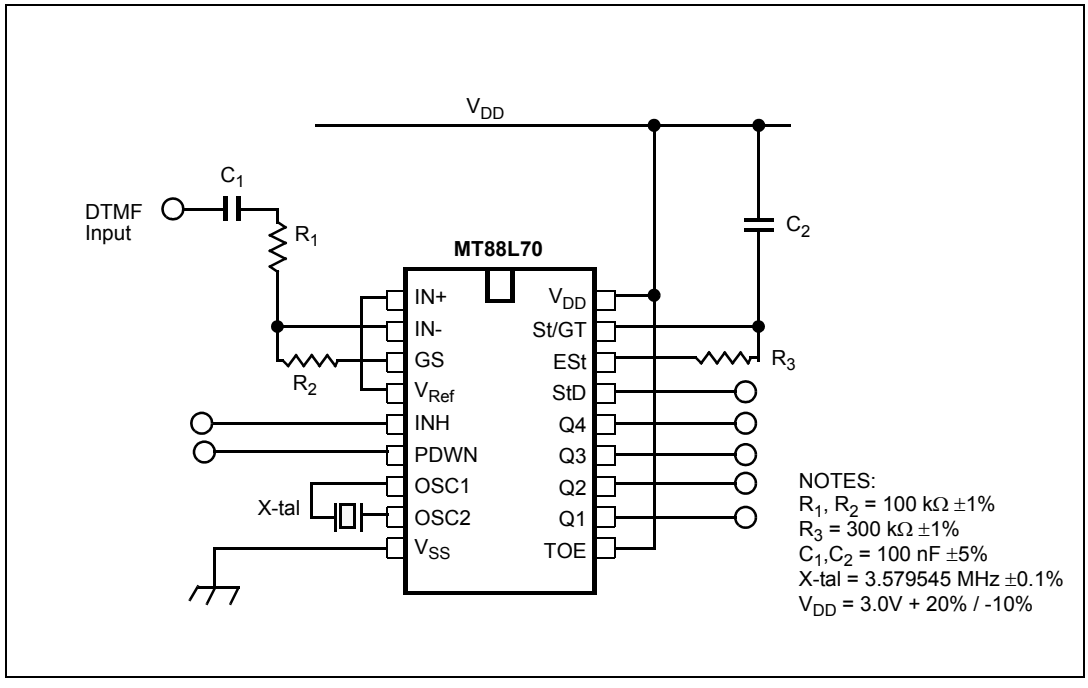


Figure 6 - Single-Ended Input Configuration

Absolute Maximum Ratings†

	Parameter	Symbol	Min.	Max.	Units
1	DC Power Supply Voltage	V_{DD}		7	V
2	Voltage on any pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Current at any pin (other than supply)	I_I		10	mA
4	Storage temperature	T_{STG}	-65	+150	°C
5	Package power dissipation	P_D		500	mW

† Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.
Derate above 75 °C at 16 mW / °C. All leads soldered to board.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Parameter	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	DC Power Supply Voltage	V_{DD}	2.7	3.0	3.6	V	
2	Operating Temperature	T_O	-40		+85	°C	
3	Crystal/Clock Frequency	fc		3.579545		MHz	
4	Crystal/Clock Freq.Tolerance	Δfc		±0.1		%	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - V_{DD} = 3.0 V+ 20%/-10%, V_{SS} = 0 V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	SUPPLY	Standby supply current	I_{DDQ}		1	10	µA	PWDN=V_{DD}
2		Operating supply current	I_{DD}		2.0	5.5	mA	
3		Power consumption	P_O		6		mW	f_c=3.579545 MHz
4	INPUTS	High level input	V_{IH}	2.1			V	V_{DD} = 3.0 V
5		Low level input voltage	V_{IL}			0.9	V	V_{DD} = 3.0 V
6		Input leakage current	I_{IH}/I_{IL}		0.05	5	µA	V_{IN} = V_{SS} or V_{DD}
7		Pull up (source) current	I_{SO}		4	15	µA	TOE (pin 10) = 0, V_{DD} = 3.0 V
8		Pull down (sink) current	I_{SI}		15	40	µA	INH = V_{DD}, PWDN = V_{DD}, V_{DD} = 3.0 V
9		Input impedance (IN+, IN-)	R_{IN}		10		MΩ	@ 1 kHz
10		Steering threshold voltage	V_{TSt}		0.465V_{DD}		V	

DC Electrical Characteristics - V_{DD} = 3.0 V+ 20%/-10%, V_{SS} = 0 V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
11	OUTPUTS	Low level output voltage	V_{OL}			V_{SS}+0.03	V	No load
12		High level output voltage	V_{OH}	V_{DD}-0.03			V	No load
13		Output low (sink) current	I_{OL}	1.5	8		mA	V_{OUT} = 0.4 V
14		Output high (source) current	I_{OH}	1.0	3.0		mA	V_{OUT} = 3.6 V, V_{DD} = 3.6 V
15		V_{Ref} output voltage	V_{Ref}		0.512V_{DD}		V	No load
16		V_{Ref} output resistance	R_{OR}		1		kΩ	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

Operating Characteristics - V_{DD} = 3.0 V+20%/-10%, V_{SS} = 0 V, -40°C ≤ T_O ≤ +85°C, unless otherwise stated.

Gain Setting Amplifier

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Input leakage current	I_{IN}			100	nA	$V_{SS} \le V_{IN} \le V_{DD}$
2	Input resistance	R_{IN}	10			MΩ	
3	Input offset voltage	V_{OS}			25	mV	
4	Power supply rejection	PSRR	50			dB	1 kHz
5	Common mode rejection	CMRR	40			dB	V_{SS} + 0.75 V ≤ V_{IN} ≤ V_{DD}-0.75 biased at V_{Ref} =1.5 V
6	DC open loop voltage gain	A_{VOL}	32			dB	
7	Unity gain bandwidth	f_C	0.30			MHz	
8	Output voltage swing	V_O		2.2		V_{pp}	Load ≥ 100 kΩ to V_{SS} @ GS
9	Maximum capacitive load (GS)	C_L			100	pF	
10	Resistive load (GS)	R_L			50	kΩ	
11	Common mode range	V_{CM}		1.5		V_{pp}	No Load

AC Electrical Characteristics - V_{DD} = 3.0 V +20%/-10%, V_{SS} = 0 V, -40°C ≤ T_O ≤ +85°C, using Test Circuit shown in Fig. 6.

		Characteristics	Sym	Min.	Typ‡	Max	Units	Notes*
1		Valid input signal levels (each tone of composite signal)		-34 15.4		-4.0 489	dBm mV_{RMS}	1,2,3,5,6,9 Min @ V_{DD}=3.6 V Max @ V_{DD}=2.7 V
2		Negative twist accept				8	dB	2,3,6,9,12
3		Positive twist accept				8	dB	2,3,6,9,12
4		Frequency deviation accept		±1.5% ± 2 Hz				2,3,5,9
5		Frequency deviation reject		±3.5%				2,3,5,9
6		Third zone tolerance			-16		dB	2,3,4,5,9,10
7		Noise tolerance			-12		dB	2,3,4,5,7,9,10
8		Dial zone tolerance			+22		dB	2,3,4,5,8,9,11

‡ Typical figures are at 25 °C and are for design aid only: not guaranteed and not subject to production testing.

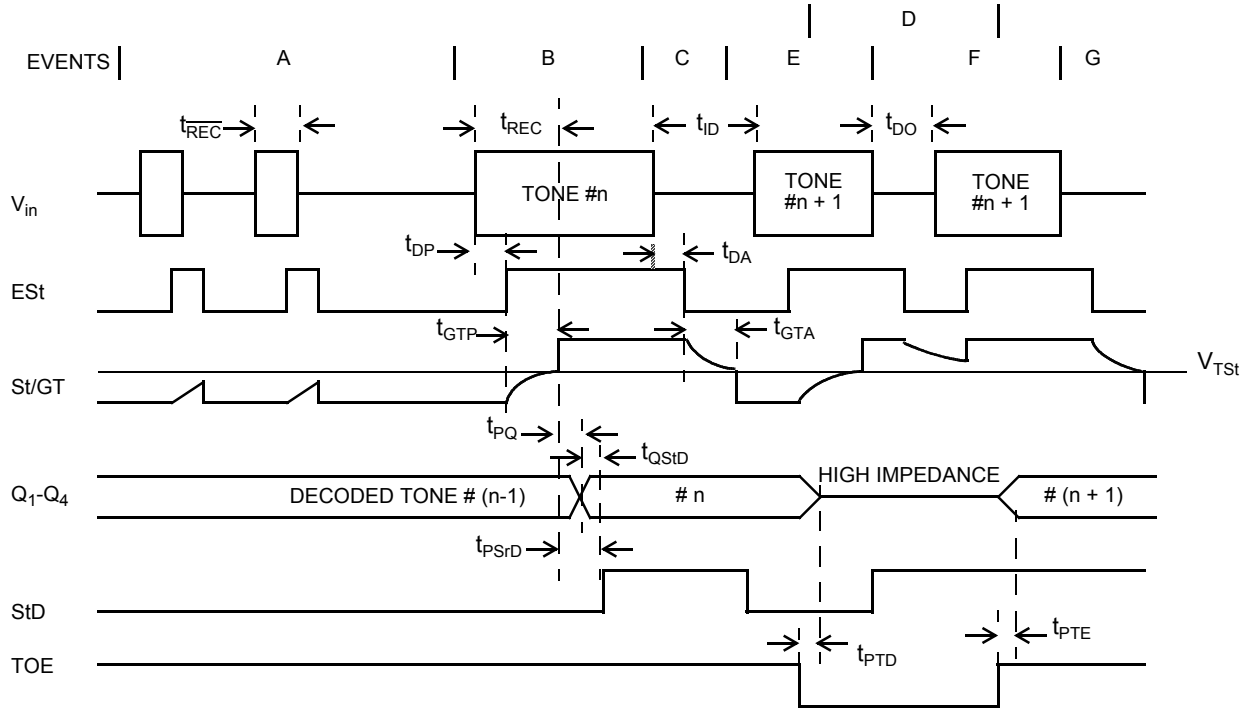
***NOTES**
1. dBm= decibels above or below a reference power of 1 mW into a 600 ohm load.
2. Digit sequence consists of all DTMF tones.
3. Tone duration= 40 ms, tone pause= 40 ms.
4. Signal condition consists of nominal DTMF frequencies.
5. Both tones in composite signal have an equal amplitude.
6. Tone pair is deviated by ±1.5%± 2 Hz.
7. Bandwidth limited (3 kHz) Gaussian noise.
8. The precise dial tone frequencies are (350 Hz and 440 Hz) ± 2%.
9. For an error rate of better than 1 in 10,000.
10. Referenced to lowest level frequency component in DTMF signal.
11. Referenced to the minimum valid accept level.
12. Guaranteed by design and characterization.

AC Electrical Characteristics - V_{DD} = 3.0 V+20%/-10%, V_{SS} = 0 V, -40°C ≤ To ≤ +85°C, using Test Circuit shown in Figure 6.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Conditions
1	TIMING	Tone present detect time	t_{DP}	5	11	14	ms	Note 1
2		Tone absent detect time	t_{DA}	0.5	4	8.5	ms	Note 1
3		Tone duration accept	t_{REC}			40	ms	Note 2
4		Tone duration reject	$t_{\overline{REC}}$	20			ms	Note 2
5		Interdigit pause accept	t_{ID}			40	ms	Note 2
6		Interdigit pause reject	t_{DO}	20			ms	Note 2
7	OUTPUTS	Propagation delay (St to Q)	t_{PQ}			11	µs	TOE=V_{DD}
8		Propagation delay (St to StD)	t_{PStD}			20	µs	TOE=V_{DD}
9		Output data set up (Q to StD)	t_{QStD}		5.0		µs	TOE=V_{DD}
10		Propagation delay (TOE to Q ENABLE)	t_{PTE}		50		ns	load of 10 kΩ, 50 pF
11		Propagation delay (TOE to Q DISABLE)	t_{PTD}		130		ns	load of 10 kΩ, 50 pF
12	PDWN	Power-up time	t_{PU}		30		ms	Note 3
13		Power-down time	t_{PD}		20		ms	
14	CLOCK	Crystal/clock frequency	f_C	3.5759	3.5795	3.5831	MHz	
15		Clock input rise time	t_{LHCL}			110	ns	Ext. clock
16		Clock input fall time	t_{HLCL}			110	ns	Ext. clock
17		Clock input duty cycle	DC_{CL}	40	50	60	%	Ext. clock
18		Capacitive load (OSC2)	C_{LO}			15	pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

***NOTES:**
1. Used for guard-time calculation purposes only and tested at -4 dBm.
2. These, user adjustable parameters, are not device specifications. The adjustable settings of these minimums and maximums are recommendations based upon network requirements.
3. With valid tone present at input, t_{PU} equals time from PDWN going low until ESt going high.



EXPLANATION OF EVENTS

A) TONE BURSTS DETECTED, TONE DURATION INVALID, OUTPUTS NOT UPDATED.

B) TONE #n DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS.

C) END OF TONE #n DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

D) OUTPUTS SWITCHED TO HIGH IMPEDANCE STATE.

E) TONE #n+1 DETECTED, TONE DURATION VALID, TONE DECODED AND LATCHED IN OUTPUTS (CURRENTLY HIGH IMPEDANCE).

F) ACCEPTABLE DROPOUT OF TONE #n+1, TONE ABSENT DURATION INVALID, OUTPUTS REMAIN LATCHED.

G) END OF TONE #n+1 DETECTED, TONE ABSENT DURATION VALID, OUTPUTS REMAIN LATCHED UNTIL NEXT VALID TONE.

EXPLANATION OF SYMBOLS

V_{in} DTMF COMPOSITE INPUT SIGNAL.

ESt EARLY STEERING OUTPUT. INDICATES DETECTION OF VALID TONE FREQUENCIES.

St/GT STEERING INPUT/GUARD TIME OUTPUT. DRIVES EXTERNAL RC TIMING CIRCUIT.

Q_1-Q_4 4-BIT DECODED TONE OUTPUT.

StD DELAYED STEERING OUTPUT. INDICATES THAT VALID FREQUENCIES HAVE BEEN PRESENT/ABSENT FOR THE REQUIRED GUARD TIME THUS CONSTITUTING A VALID SIGNAL.

TOE TONE OUTPUT ENABLE (INPUT). A LOW LEVEL SHIFTS Q_1-Q_4 TO ITS HIGH IMPEDANCE STATE.

$t_{\overline{REC}}$ MAXIMUM DTMF SIGNAL DURATION NOT DETECTED AS VALID.

t_{REC} MINIMUM DTMF SIGNAL DURATION REQUIRED FOR VALID RECOGNITION.

t_{ID} MINIMUM TIME BETWEEN VALID DTMF SIGNALS.

t_{DO} MAXIMUM ALLOWABLE DROP OUT DURING VALID DTMF SIGNAL.

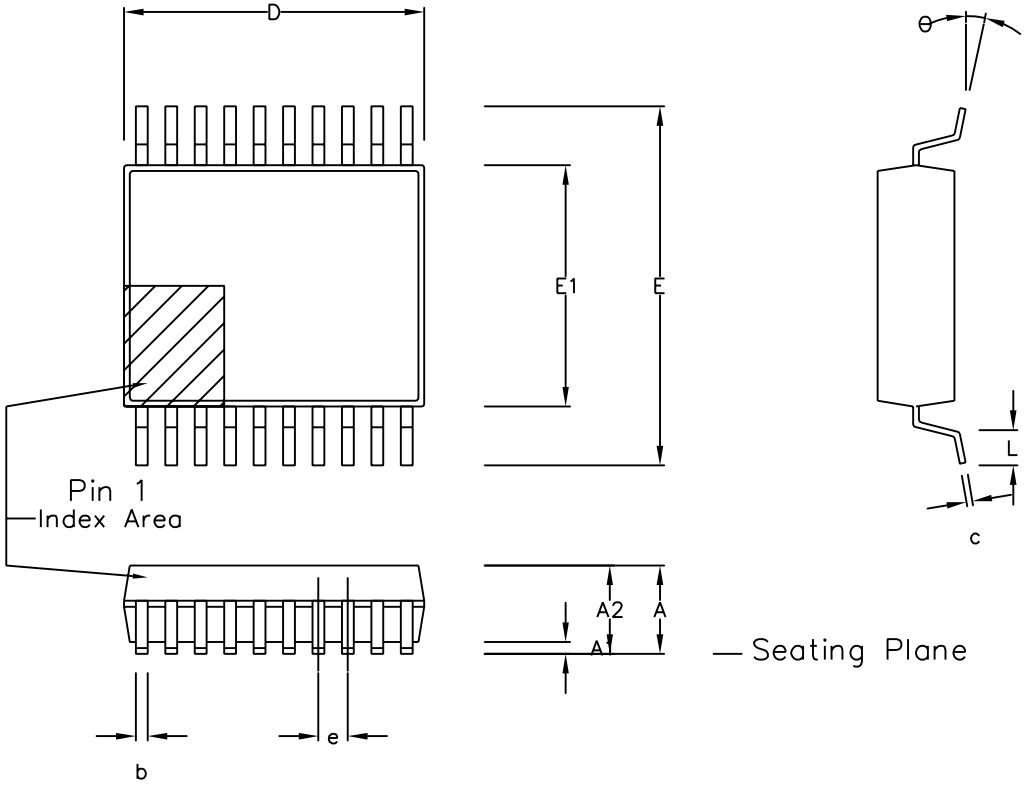
t_{DP} TIME TO DETECT THE PRESENCE OF VALID DTMF SIGNALS.

t_{DA} TIME TO DETECT THE ABSENCE OF VALID DTMF SIGNALS.

t_{GTP} GUARD TIME, TONE PRESENT.

t_{GTA} GUARD TIME, TONE ABSENT.

Figure 7 - Timing Diagram



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	1.70		2.00		0.067		0.079
A1	0.05		0.20		0.002		0.008
A2	1.65		1.85		0.065		0.073
D	6.90		7.50		0.272		0.295
E	7.40		8.20		0.291		0.323
E1	5.00		5.60		0.197		0.220
L	0.55		0.95		0.022		0.037
e	0.65 BSC.				0.026 BSC.		
b	0.22		0.38		0.009		0.015
c	0.09		0.25		0.004		0.010
θ	0°		8°		0°		8°
	Pin features						
N	20						
Conforms to JEDEC MO-150 AE Iss. B							

This drawing supersedes:-
418/ED/51481/002 (Swindon/Plymouth)

Notes:
1. A visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimension are in millimeters.
3. Dimensions D and E1 do not include mould flash or protusion. Mould flash or protusion shall not exceed 0.20 mm per side. D and E1 are maximum plastic body size dimensions including mould mismatch.
4. Dimension b does not include dambar protusion/intrusion. Allowable dambar protusion shall be 0.13 mm total in excess of b dimension. Dambar intrusion shall not reduce dimension b by more than 0.07 mm.

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ISSUE	1	2	3	
ACN	201933	205234	212477	
DATE	27Feb97	25Sep98	3Apr02	
APPRD.				

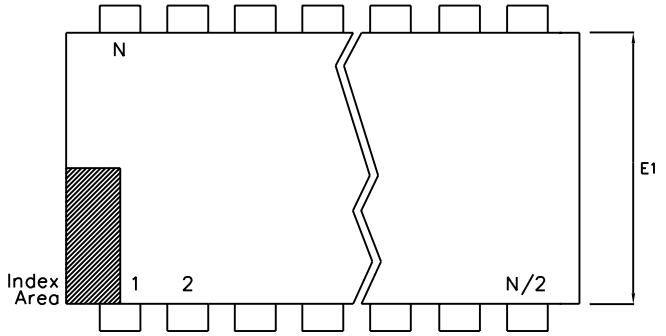
ZARLINK SEMICONDUCTOR

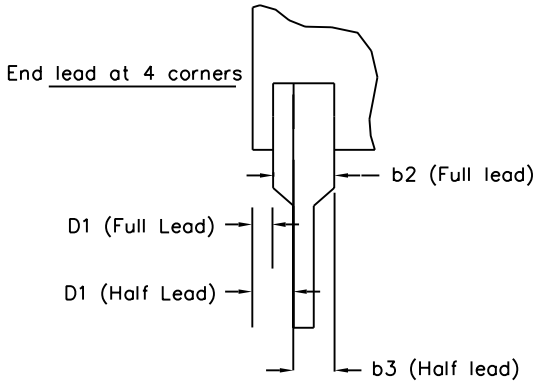
Previous package codes
NP / N

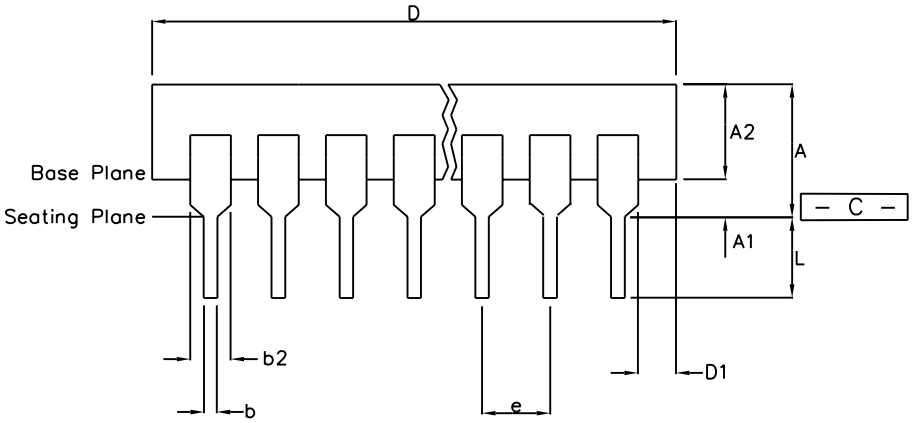
Package Code DD

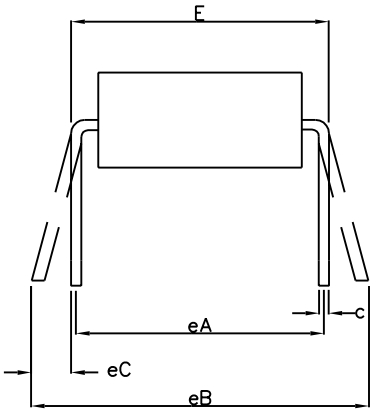
Package Outline for 20 lead SSOP (5.3mm Body Width)

GPD00294









	Min mm	Max mm	Min Inches	Max Inches
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
b3	n/a	n/a	n/a	n/a
c	0.20	0.36	0.008	0.014
D	22.35	23.37	0.880	0.920
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
eC	0.00	1.52	0.000	0.060
L	2.92	3.81	0.115	0.150
N	18		18	
Conforms to Jedec MS-001AC Issue D				

Notes:
1. Leadframe Material: Copper
2. Leadframe finish: Solder Plate
3. Dimensions D, D1 & E1 do not include mould flash or protrusions.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to datum – C –
5. Dimensions eB & eC are measured with the leads unconstrained
6. Controlling dimensions are Inches. Millimeter conversions are not necessarily exact.
7. N is the maximum of terminal positions.

This drawing supersedes: –
Plymouth/Swindon drawing # 418/ED/39502/004

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ISSUE	1	2		
ACN	202563	212483		
DATE	9Jun97	5Apr02		
APPRD.				

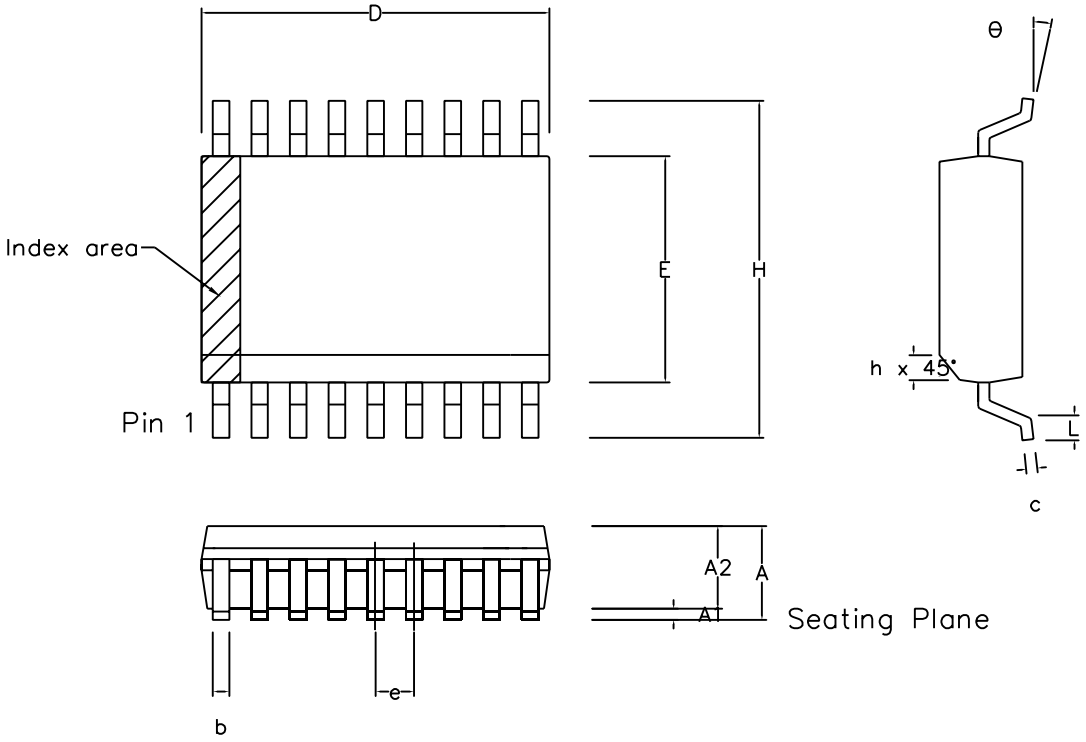
ZARLINK SEMICONDUCTOR

Previous package codes
DP / E

Package Code DA

Package Outline for
18 Lead PDIP

GPD00348



Symbol	Control Dimensions in millimetres				Altern. Dimensions in inches		
	MIN	Nominal	MAX		MIN	Nominal	MAX
A	2.35		2.65		0.093		0.104
A1	0.10		0.30		0.004		0.012
A2	2.25		2.35		0.089		0.092
D	11.35		11.75		0.447		0.463
H	10.00		10.65		0.394		0.419
E	7.40		7.60		0.291		0.299
L	0.40		1.27		0.016		0.050
e	1.27 BSC.				0.050 BSC.		
b	0.33		0.51		0.013		0.020
c	0.23		0.32		0.009		0.013
θ	0°		8°		0°		8°
h	0.25		0.75		0.010		0.029
	Pin features						
N	18						
Conforms to JEDEC MS-013AB Iss. C							

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in millimeters
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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ISSUE	1	2	3	
ACN	6746	201940	212432	
DATE	7Apr95	27Feb97	25Mar02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

MP / S

Package Code DC

Package Outline for 18 lead SOIC (0.300" Body Width)

GPD00014



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