Features

- Zarlink ST-BUS compatible
- 8-line x 32-channel inputs
- 8-line x 32-channel outputs
- 256 ports non-blocking switch
- Single power supply (+5 V)
- Low power consumption: 30 mW Typ.
- Microprocessor-control interface
- Three-state serial outputs

April 2011

Ordering Information

MT8980DP1	44 Pin PLCC*	Tubes
MT8980DE1	40 Pin PDIP*	Tubes
MT8980DPR1	44 Pin PLCC*	Tape & Reel

***Pb Free Matte Tin**

-40°C to +85°C

Description

This VLSI ISO-CMOS device is designed for switching PCM-encoded voice or data, under microprocessor control, in a modern digital exchange, PBX or Central Office. It provides simultaneous connections for up to 256 64 kbit/s channels. Each of the eight serial inputs and outputs consist of 32 64 kbit/s channels multiplexed to form a 2048 kbit/s ST-BUS stream. In addition, the MT8980 provides microprocessor read and write access to individual ST-BUS channels.

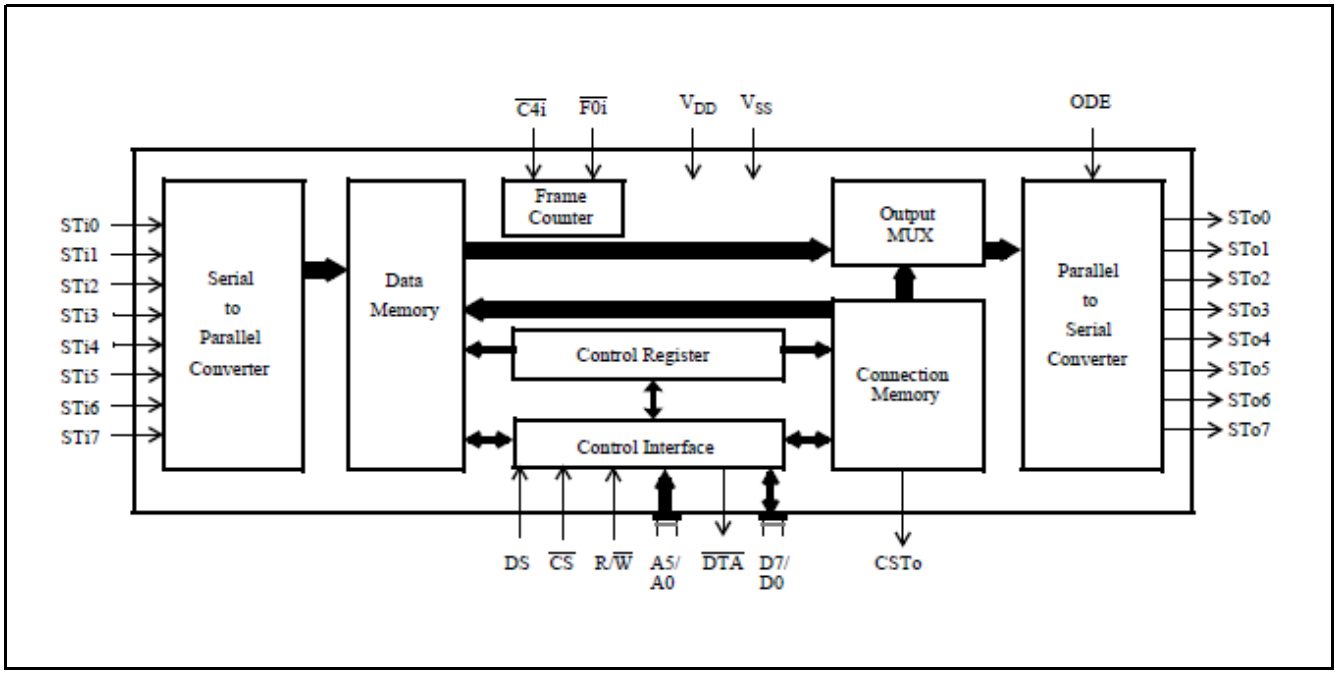

Figure 1 - Functional Block Diagram

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Change Summary

Changes from February 2005 Issue to April 2011 Issue.

Page	Item	Change
1	Ordering Information	Obsolete Leaded packages, only Pb Free packages are available.

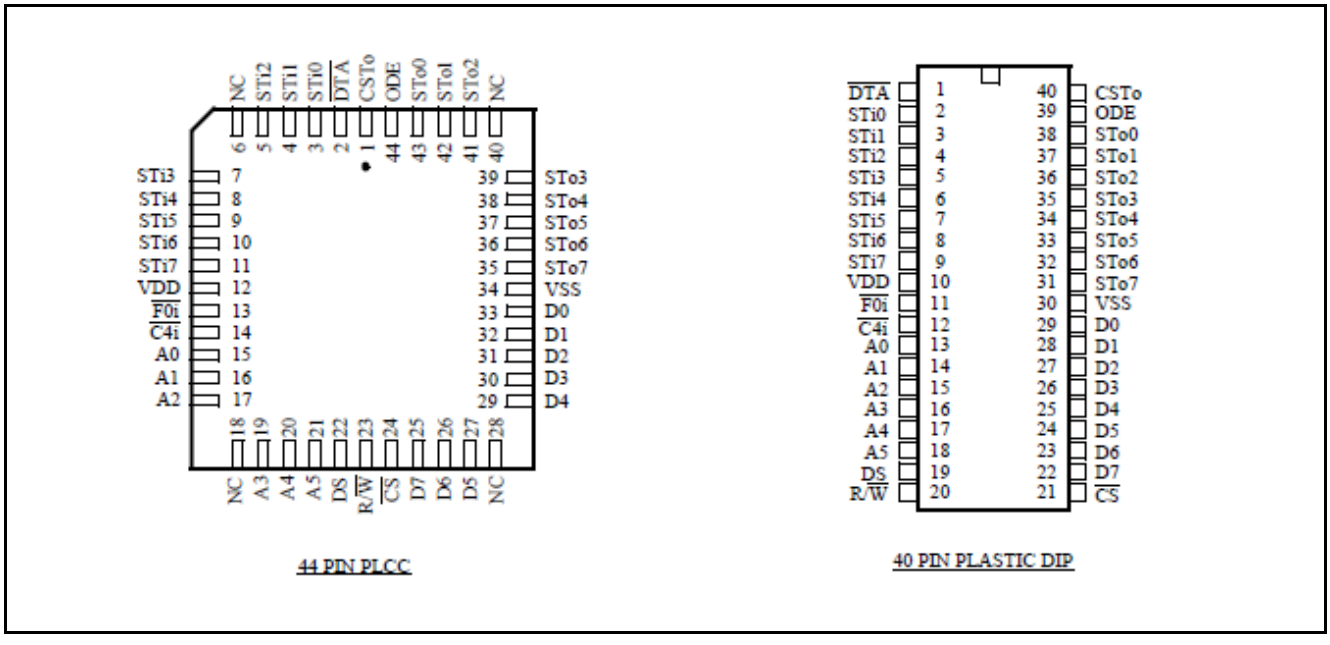


Figure 2 - Pin Connections

Pin Descripton

Pin #		Name	Description
40 DIP	44 PLCC		
1	2	$\overline{DTA}$	**Data Acknowledgement (Open Drain Output).** This is the data acknowledgement on the microprocessor interface. This pin is pulled low to signal that the chip has processed the data. A 909 Ω 1/4W, resistor is recommended to be used as a pullup.
2-4	3-5	STi0-STi2	**ST-BUS Input 0 to 2 (Inputs)**. These are the inputs for the 2048 kbit/s ST-BUS input streams.
5-9	7-11	STi3-STi7	**ST-BUS Input 3 to 7 (Inputs)**. These are the inputs for the 2048 kbit/s ST-BUS input streams.
10	12	V_{DD}	**Power Input**. Positive Supply.
11	13	$\overline{F0i}$	**Framing 0-Type (Input)**. This is the input for the frame synchronization pulse for the 2048 kbit/s ST-BUS streams. A low on this input causes the internal counter to reset on the next negative transition of $\overline{C4i}$.

Pin Descripton

Pin #		Name	Description
40 DIP	**44 PLCC**		
12	14	$\overline{C4i}$	**4.096 MHz Clock (Input)**. ST-BUS bit cell boundaries lie on the alternate falling edges of this clock.
13-15	15-17	A0-A2	**Address 0 to 2 (Inputs)**. These are the inputs for the address lines on the microprocessor interface.
16-18	19-21	A3-A5	**Address 3 to 5 (Inputs)**. These are the inputs for the address lines on the microprocessor interface.
19	22	DS	**Data Strobe (Input)**. This is the input for the active high data strobe on the microprocessor interface.
20	23	R/$\overline{W}$	**Read or Write (Input)**. This is the input for the read/write signal on the microprocessor interface - high for read, low for write.
21	24	$\overline{CS}$	**Chip Select (Input)**. This is the input for the active low chip select on the microprocessor interface.
22-24	25-27	D7-D5	**Data 7 to 5 (Three-state I/O Pins)**. These are the bidirectional data pins on the microprocessor interface.
25-29	29-33	D4-D0	**Data 4 to 0 (Three-state I/O Pins).** These are the bidirectional data pins on the microprocessor interface.
30	34	V_{SS}	**Power Input.** Negative Supply (Ground).
31-35	35-39	STo7-STo3	**ST-BUS Output 7 to 3 (Three-state Outputs).** These are the pins for the eight 2048 kbit/s ST-BUS output streams.
36-38	41-43	STo2-STo0	**ST-BUS Output 2 to 0 (Three-state Outputs).** These are the pins for the eight 2048 kbit/s ST-BUS output streams.
39	44	ODE	**Output Drive Enable (Input)**. If this input is held high, the STo0-STo7 output drivers function normally. If this input is low, the STo0-STo7 output drivers go into their high impedance state. **NB**: Even when ODE is high, channels on the STo0-STo7 outputs can go high impedance under software control.
40	1	CSTo	**Control ST-BUS Output (Complementary Output).** Each frame of 256 bits on this ST-BUS output contains the values of bit 1 in the 256 locations of the Connection Memory High.
	6, 18, 28, 40	NC	No Connection.

Functional Description

In recent years, there has been a trend in telephony towards digital switching, particularly in association with software control. Simultaneously, there has been a trend in system architectures towards distributed processing or multi-processor systems.

In accordance with these trends, Zarlink has devised the ST-BUS (Serial Telecom Bus). This bus architecture can be used both in software-controlled digital voice and data switching, and for interprocessor communications. The uses in switching and in interprocessor communications are completely integrated to allow for a simple general purpose architecture appropriate for the systems of the future.

The serial streams of the ST-BUS operate continuously at 2048 kbit/s and are arranged in 125 µs wide frames which contain 32 8-bit channels. Zarlink manufactures a number of devices which interface to the ST-BUS; a key device being the MT8980 chip.

The MT8980 can switch data from channels on ST-BUS inputs to channels on ST-BUS outputs, and simultaneously allows its controlling microprocessor to read channels on ST-BUS inputs or write to channels on ST-BUS outputs (Message Mode). To the microprocessor, the MT8980 looks like a memory peripheral. The microprocessor can write to the MT8980 to establish switched connections between input ST-BUS channels and output ST-BUS channels, or to transmit messages on output ST-BUS channels. By reading from the MT8980, the microprocessor can receive messages from ST-BUS input channels or check which switched connections have already been established.

By integrating both switching and interprocessor communications, the MT8980 allows systems to use distributed processing and to switch voice or data in an ST-BUS architecture.

Hardware Description

Serial data at 2048 kbit/s is received at the eight ST-BUS inputs (STi0 to STi7), and serial data is transmitted at the eight ST-BUS outputs (STo0 to STo7). Each serial input accepts 32 channels of digital data, each channel containing an 8-bit word which may represent a PCM-encoded analog/voice sample as provided by a codec (e.g., Zarlink's MT8964).

This serial input word is converted into parallel data and stored in the 256 X 8 Data Memory. Locations in the Data Memory are associated with particular channels on particular ST-BUS input streams. These locations can be read by the microprocessor which controls the chip.

Locations in the Connection Memory, which is split into high and low parts, are associated with particular ST-BUS output streams. When a channel is due to be transmitted on an ST-BUS output, the data for the channel can either be switched from an ST-BUS input or it can originate from the microprocessor. If the data is switched from an input, then the contents of the Connection Memory Low location associated with the output channel is used to address the Data Memory. This Data Memory address corresponds to the channel on the input ST-BUS stream on which the data for switching arrived. If the data for the output channel originates from the microprocessor (Message Mode), then the contents of the Connection Memory Low location associated with the output channel are output directly, and this data is output repetitively on the channel once every frame until the microprocessor intervenes.

The Connection Memory data is received, via the Control Interface, at D7 to D0. The Control Interface also receives address information at A5 to A0 and handles the microprocessor control signals $\overline{CS}$, $\overline{DTA}$, R/$\overline{W}$ and DS. There are two parts to any address in the Data Memory or Connection Memory. The higher order bits come from the Control Register, which may be written to or read from via the Control Interface. The lower order bits come from the address lines directly.

The Control Register also allows the chip to broadcast messages on all ST-BUS outputs (i.e., to put every channel into Message Mode), or to split the memory so that reads are from the Data Memory and writes are to the Connection Memory Low. The Connection Memory High determines whether individual output channels are in Message Mode, and allows individual output channels to go into a high-impedance state, which enables arrays of MT8980s to be constructed. It also controls the CSTo pin.

All ST-BUS timing is derived from the two signals $\overline{C4i}$ and $\overline{F0i}$.

A5	A4	A3	A2	A1	A0	HEX ADDRESS	LOCATION
0	X	X	X	X	X	00 - 1F	Control Register *
1	0	0	0	0	0	20	Channel 0†
1	0	0	0	0	1	21	Channel 1†
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•
1	1	1	1	1	1	3F	Channel 31†

* Writing to the Control Register is the only fast transaction.
† Memory and stream are specified by the contents of the Control Register.

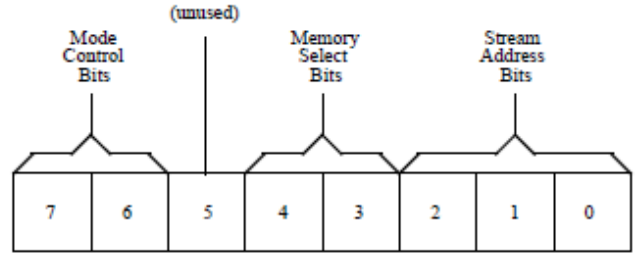
Figure 3 - Address Memory Map

Software Control

The address lines on the Control Interface give access to the Control Register directly or, depending on the contents of the Control Register, to the High or Low sections of the Connection Memory or to the Data Memory.

If address line A5 is low, then the Control Register is addressed regardless of the other address lines (see Fig. 3). If A5 is high, then the address lines A4-A0 select the memory location corresponding to channel 0-31 for the memory and stream selected in the Control Register.

The data in the Control Register consists of mode control bits, memory select bits, and stream address bits (see Fig. 4). The memory select bits allow the Connection Memory High or Low or the Data Memory to be chosen, and the stream address bits define one of the ST-BUS input or output streams.



BIT	NAME	DESCRIPTION
7	Split Memory	When 1, all subsequent reads are from the Data Memory and writes are to the Connection Memory Low, except when the Control Register is accessed again. When 0, the Memory Select bits specify the memory for subsequent operations. In either case, the Stream Address Bits select the subsection of the memory which is made available.
6	Message Mode	When 1, the contents of the Connection Memory Low are output on the Serial Output streams except when the ODE pin is low. When 0, the Connection Memory bits for each channel determine what is output.
5	(unused)	
4-3	Memory Select Bits	0-0 - Not to be used 0-1 - Data Memory (read only from the microprocessor port) 1-0 - Connection Memory Low 1-1 - Connection Memory High
2-0	Stream Address Bits	The number expressed in binary notation on these bits refers to the input or output ST-BUS stream which corresponds to the subsection of memory made accessible for subsequent operations.

Figure 4 - Control Register Bits

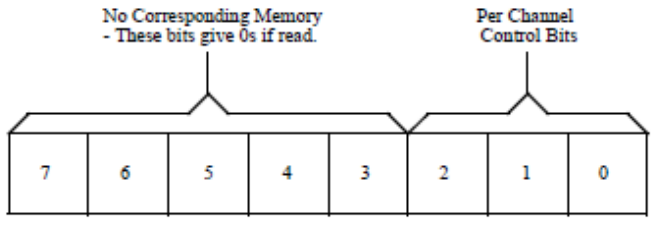
Bit 7 of the Control Register allows split memory operation - reads are from the Data Memory and writes are to the Connection Memory Low.

The other mode control bit, bit 6, puts every output channel on every output stream into active Message Mode; i.e., the contents of the Connection Memory Low are output on the ST-BUS output streams once every frame unless the ODE pin is low. In this mode the chip behaves as if bits 2 and 0 of every Connection Memory High location were 1, regardless of the actual values.

If bit 6 of the Control Register is 0, then bits 2 and 0 of each Connection Memory High location function normally (see Fig. 5). If bit 2 is 1, the associated ST-BUS output channel is in Message Mode; i.e., the byte in the corresponding Connection Memory Low location is transmitted on the stream at that channel. Otherwise, one of the bytes received on the serial inputs is transmitted and the contents of the Connection Memory Low define the ST-BUS input stream and channel where the byte is to be found (see Fig. 6).

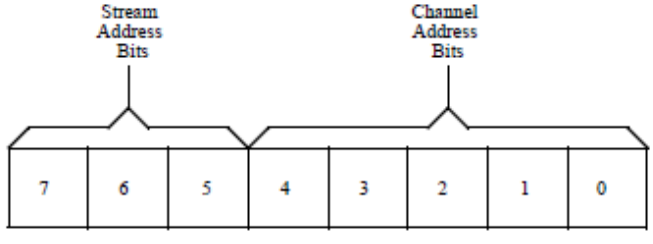
If the ODE pin is low, then all serial outputs are high-impedance. If it is high and bit 6 in the Control Register is 1, then all outputs are active. If the ODE pin is high and bit 6 in the Control Register is 0, then the bit 0 in the Connection Memory High location enables the output drivers for the corresponding individual ST-BUS output stream and channel. Bit 0=1 enables the driver and bit 0=0 disables it (see Fig. 5).

Bit 1 of each Connection Memory High location (see Fig. 5) is output on the CSTo pin once every frame. To allow for delay in any external control circuitry the bit is output one channel before the corresponding channel on the ST-BUS streams, and the bit for stream 0 is output first in the channel; e.g., bit 1's for channel 9 of streams 0-7 are output synchronously with ST-BUS channel 8 bits 7-0.



BIT	NAME	DESCRIPTION
2	Message Channel	When 1, the contents of the corresponding location in Connection Memory Low are output on the location's channel and stream. When 0, the contents of the corresponding location in Connection Memory Low act as an address for the Data Memory and so determine the source of the connection to the location's channel and stream.
1	CSTo Bit	This bit is output on the CSTo pin one channel early. The CSTo bit for stream 0 is output first.
0	Output Enable	If the ODE pin is high and bit 6 of the Control Register is 0, then this bit enables the output driver for the location's channel and stream. This allows individual channels on individual streams to be made high-impedance, allowing switching matrices to be constructed. A 1 enables the driver and a 0 disables it.

Figure 5 - Connection Memory High Bits



BIT	NAME	DESCRIPTION
7-5*	Stream Address Bits*	The number expressed in binary notation on these 3 bits is the number of the ST-BUS stream for the source of the connection. Bit 7 is the most significant bit. e.g., if bit 7 is 1, bit 6 is 0 and bit 5 is 0, then the source of the connection is a channel on STi4.
4-0*	Channel Address Bits*	The number expressed in binary notation on these 5 bits is the number of the channel which is the source of the connection (The ST-BUS stream where the channel lies is defined by bits 7, 6 and 5.). Bit 4 is the most significant bit. e.g., if bit 4 is 1, bit 3 is 0, bit 2 is 0, bit 1 is 1 and bit 0 is 1, then the source of the connection is channel 19.
*If bit 2 of the corresponding Connection High location is 1 or if bit 6 of the Control Register is 1, then these entire 8 bits are output on the channel and stream associated with this location. Otherwise, the bits are used as indicated to define the source of the connection which is output on the channel and stream associated with this location.		

Figure 6 - Connection Memory Low Bits

Applications

Use in a Simple Digital Switching System

Figs. 7 and 8 show how MT8980s can be used with MT8964s to form a simple digital switching system. Fig. 7 shows the interface between the MT8980s and the filter/codecs. Fig. 8 shows the position of these components in an example architecture.

The MT8964 filter/codec in Fig. 7 receives and transmits digitized voice signals on the ST-BUS input DR, and ST-BUS output D_X, respectively. These signals are routed to the ST-BUS inputs and outputs on the top MT8980, which is used as a digital speech switch.

The MT8964 is controlled by the ST-BUS input DC originating from the bottom MT8980, which generates the appropriate signals from an output channel in Message Mode. This architecture optimizes the messaging capability of the line circuit by building signalling logic, e.g., for on-off hook detection, which communicates on an ST-BUS output. This signalling ST-BUS output is monitored by a microprocessor (not shown) through an ST-BUS input on the bottom MT8980.

Fig. 8 shows how a simple digital switching system may be designed using the ST-BUS architecture. This is a private telephone network with 256 extensions which uses a single MT8980 as a speech switch and a second MT8980 for communication with the line interface circuits.

A larger digital switching system may be designed by cascading a number of MT8980s. Fig. 9 shows how four MT8980s may be arranged in a non-blocking configuration which can switch any channel on any of the ST-BUS inputs to any channel on the ST-BUS outputs.

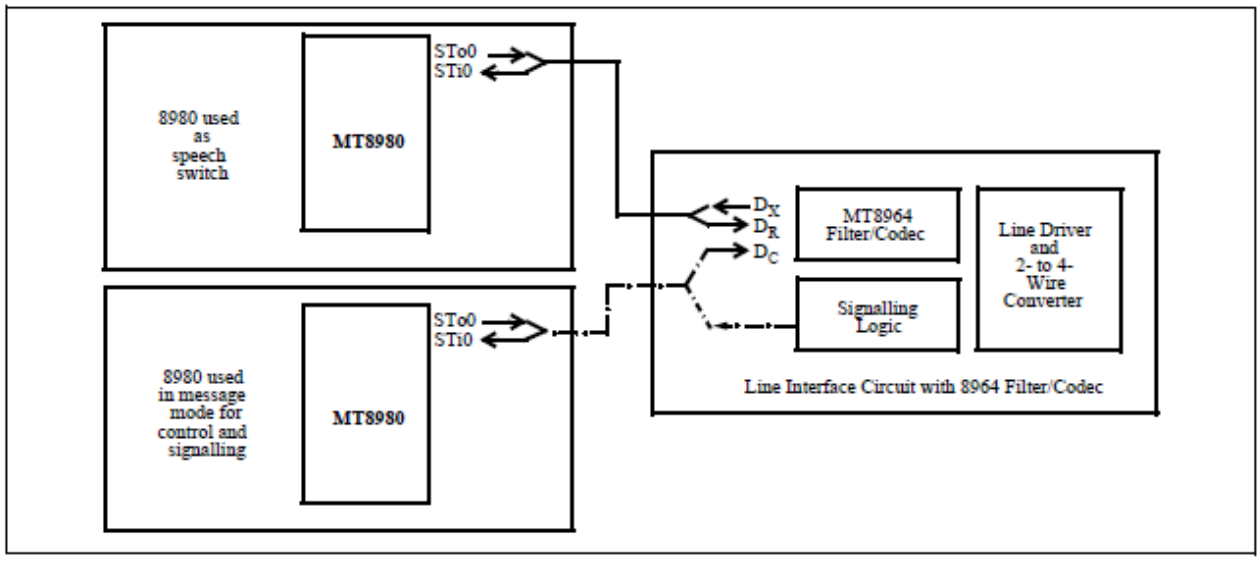


Figure 7 - Example of Typical Interface between 8980s and 8964s for Simple Digital Switching System

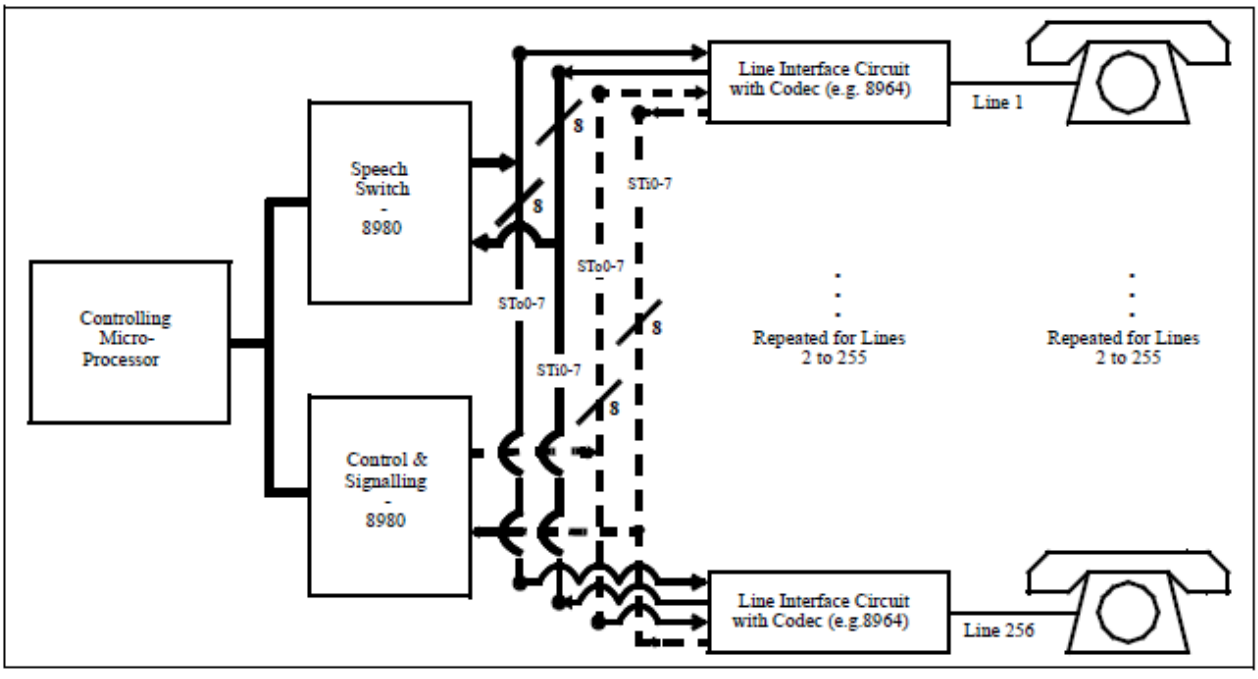


Figure 8 - Example Architecture of a Simple Digital Switching System

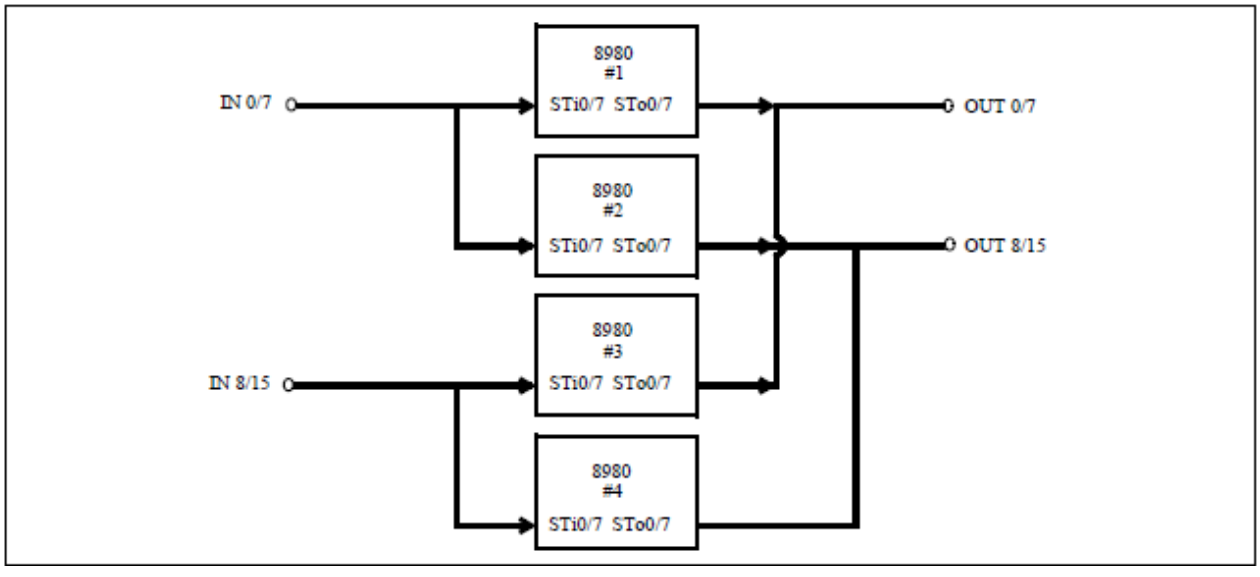


Figure 9 - Four 8980s Arranged in a Non-Blocking 16 x 16 Configuration

Application Circuit with 6802 Processor

Fig. 10 shows an example of a complete circuit which may be used to evaluate the chip.

For convenience, a 4 MHz crystal oscillator has been used rather than a 4.096 MHz clock, as both are within the limits of the chip's specifications. The RC delay used with the 393 counters ensures a sufficient hold time for the FP signal, but the values used may have to be changed if faster 393 counters become available.

The chip is shown as memory mapped into the MEK6802D3 system. Chip addresses 00-3F correspond to processor addresses 2000-203F. Delay through the address decoder requires the VMA signal to be used twice to remove glitches. The MEK6802D3 board uses a 10 KΩ pullup on the MR pin, which would have to be incorporated into the circuit if the board was replaced by a processor.

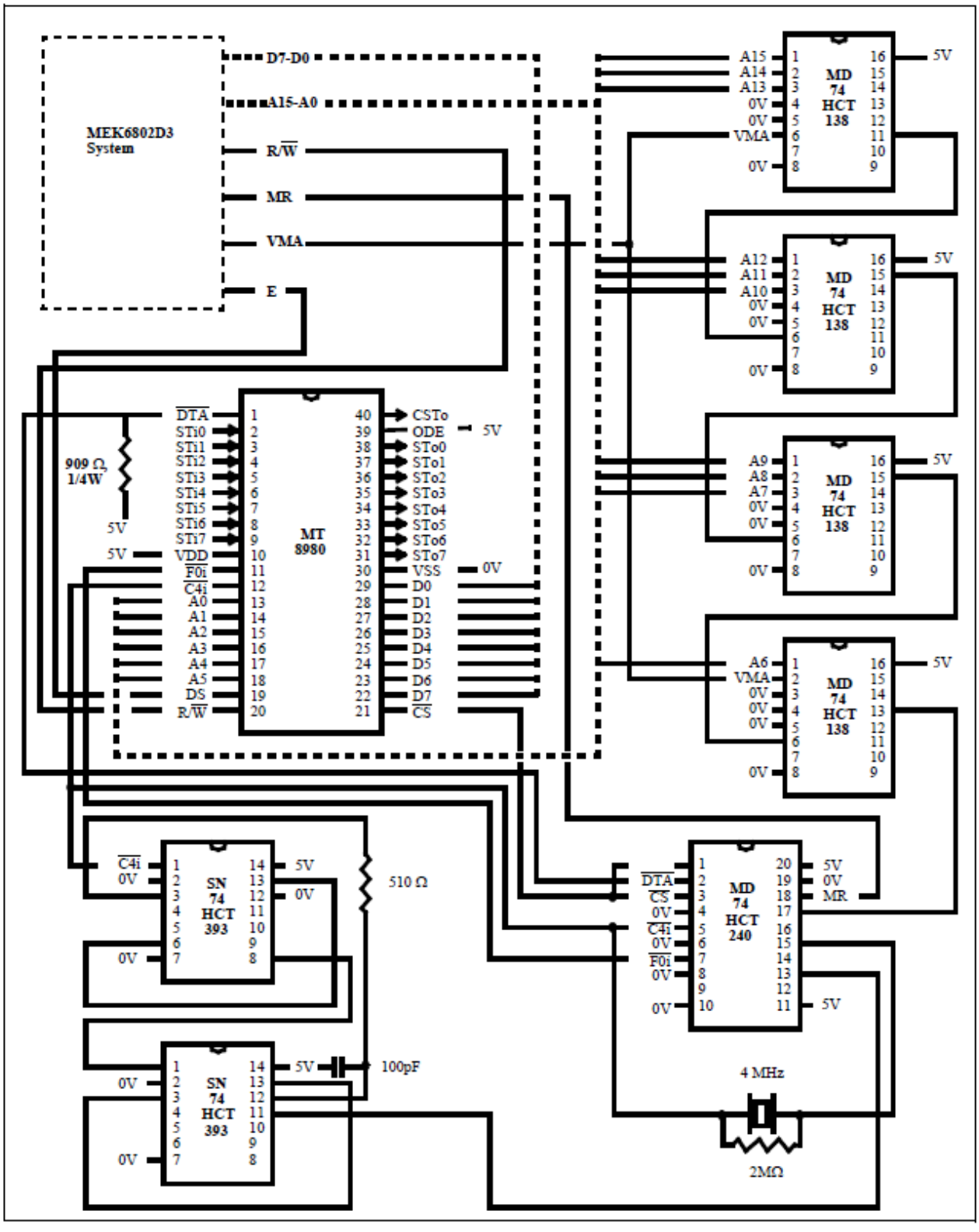


Figure 10 - Application Circuit with 6802

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	V_{DD} - V_{SS}		-0.3	7	V
2	Voltage on Digital Inputs	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Voltage on Digital Outputs	V_O	V_{SS}-0.3	V_{DD}+0.3	V
4	Current at Digital Outputs	I_O		40	mA
5	Storage Temperature	T_S	-65	+150	°C
6	Package Power Dissipation	P_D		2	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		+85	°C	
2	Positive Supply	V_{DD}	4.75		5.25	V	
3	Input Voltage	V_I	0		V_{DD}	V	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

DC Electrical Characteristics - Voltages are with respect to ground (VSS) unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡			
1	I	Supply Current	I_{DD}		6	10	mA	Outputs unloaded
2	N	Input High Voltage	V_{IH}	2.0			V	
3	P	Input Low Voltage	V_{IL}			0.8	V	
4	U	Input Leakage	I_{IL}			5	µA	V_I between V_{SS} and V_{DD}
5	S	Input Pin Capacitance	C_I		8		pF	
6	O	Output High Voltage	V_{OH}	2.4			V	I_{OH} = 10 mA
7	U	Output High Current	I_{OH}	10	15		mA	Sourcing. V_{OH}=2.4V
8	T	Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 5 mA
9	P	Output Low Current	I_{OL}	5	10		mA	Sinking. V_{OL} = 0.4V
10	U	High Impedance Leakage	I_{OZ}			5	µA	V_O between V_{SS} and V_{DD}
11	T S	Output Pin Capacitance	C_O		8		pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

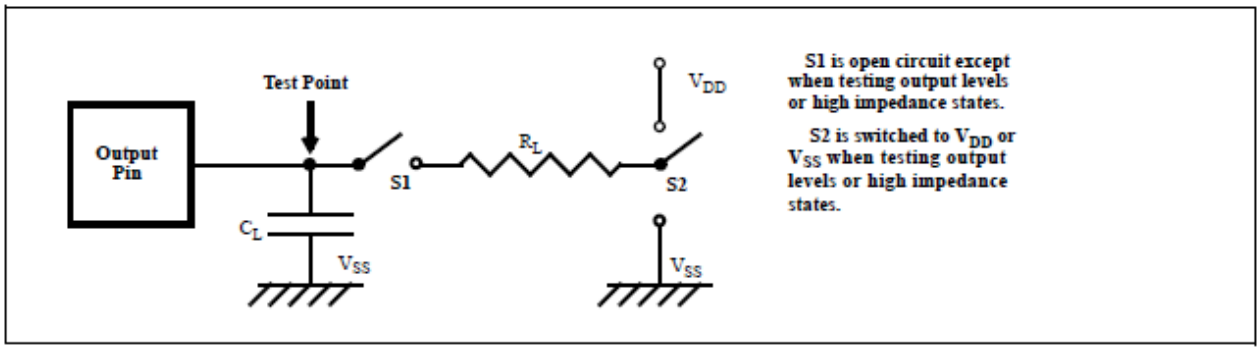


Figure 11 - Output Test Load

AC Electrical Characteristics† - Clock Timing (Figures 12 and 13)

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	INPUTS	Clock Period*	t_{CLK}	220	244	300	ns	
2		Clock Width High	t_{CH}	95	122	150	ns	
3		Clock Width Low	t_{CL}	110	122	150	ns	
4		Clock Transition Time	t_{CTT}		20		ns	
5		Frame Pulse Setup Time	t_{FPS}	20		200	ns	
6		Frame Pulse Hold Time	tFPH	0.020		50	µs	
7		Frame Pulse Width	t_{FPW}		244		ns	

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* Contents of Connection Memory are not lost if the clock stops, however, ST-BUS outputs go into the high impedance state.
NB: Frame Pulse is repeated every 512 cycles of $\overline{C4i}$.

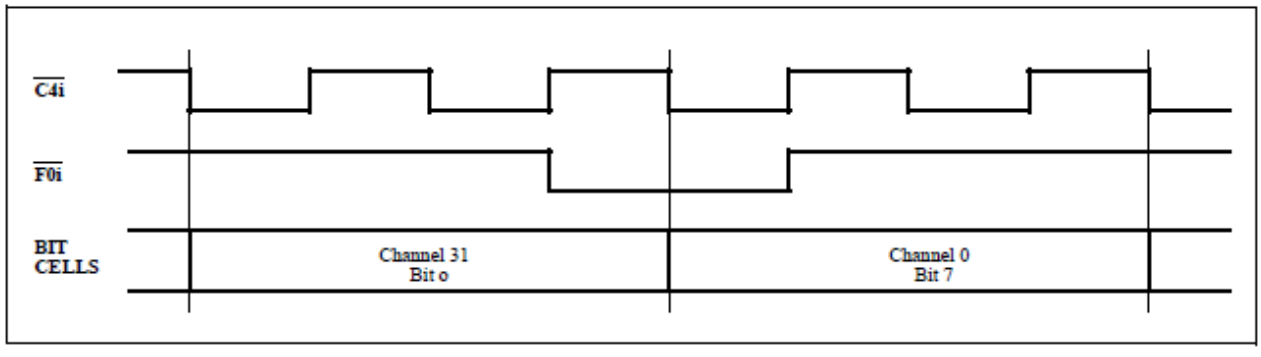


Figure 12 - Frame Alignment

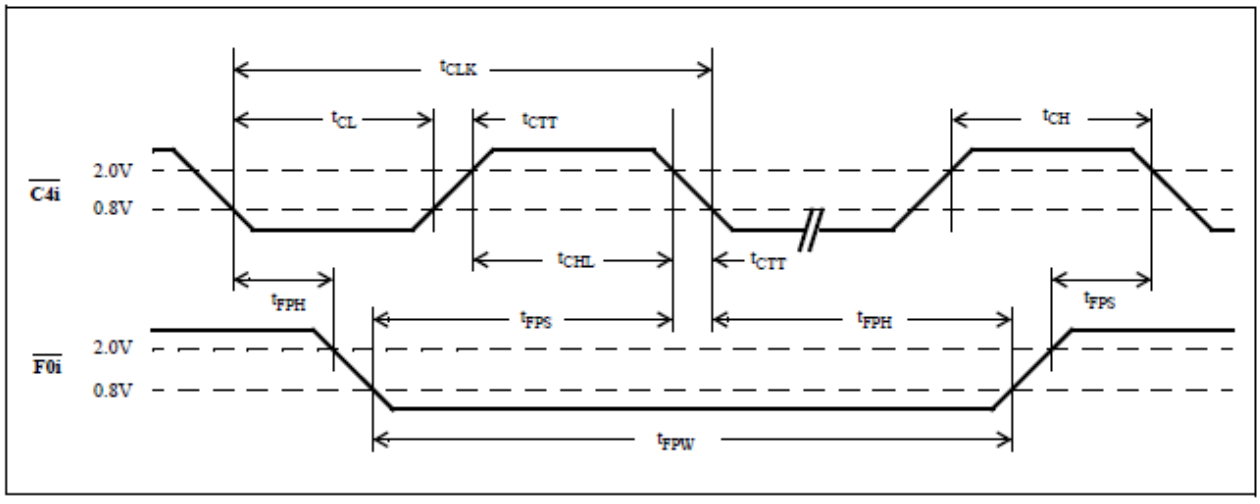


Figure 13 - Clock Timing

AC Electrical Characteristics† - Serial Streams (Figures 11, 14, 15 and 16)

		Characteristics	Sym.	Min.	Typ.‡	Max,	Units	Test Conditions
1	OUTPUTS	STo0/7 Delay - Active to High Z	t_{SAZ}	20	50	80	ns	R_L=1 KΩ*, C_L=150 pF
2		ISTo0/7 Delay - High Z to Active	t_{SZA}	25	60	125	ns	C_L=150 pF
3		STo0/7 Delay - Active to Active	t_{SAA}	30	65	125	ns	C_L=150 pF
4		STo0/7 Hold Time	t_{SOH}	25	45		ns	C_L=150 pF
5		Output Driver Enable Delay	t_{OED}		45	125	ns	R_L=1 KΩ*, C_L=150 pF
6		External Control Hold Time	t_{XCH}	0	50		ns	C_L=150 pF
7		External Control Delay	t_{XCD}		75	110	ns	C_L=150 pF
8	IN	Serial Input Setup Time	t_{SIS}		-40	-20	ns	
9		Serial Input Hold Time	t_{SIH}	90			ns	

† Timing is over recommended temperature & power supply voltages.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

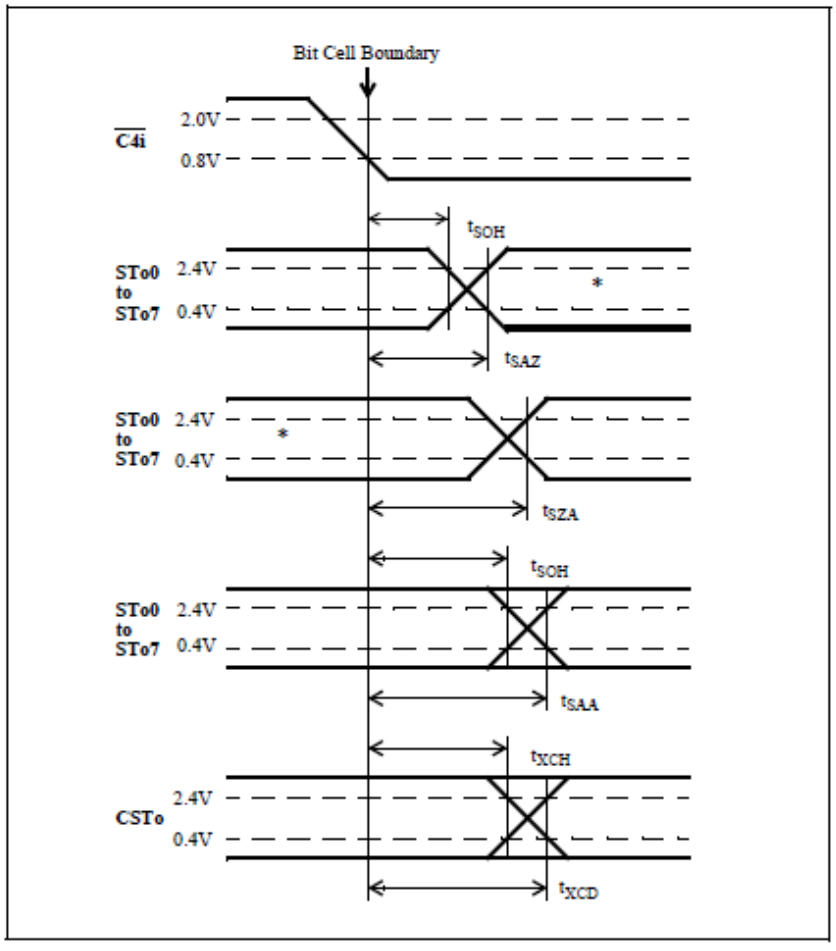


Figure 14 - Serial Outputs and External Control

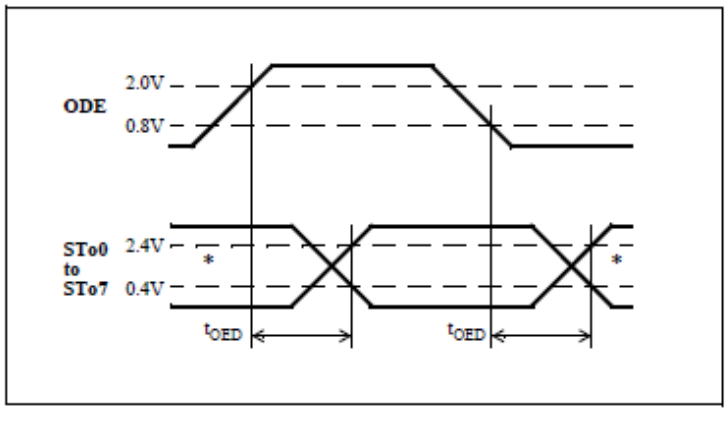


Figure 15 - Output Driver Enable

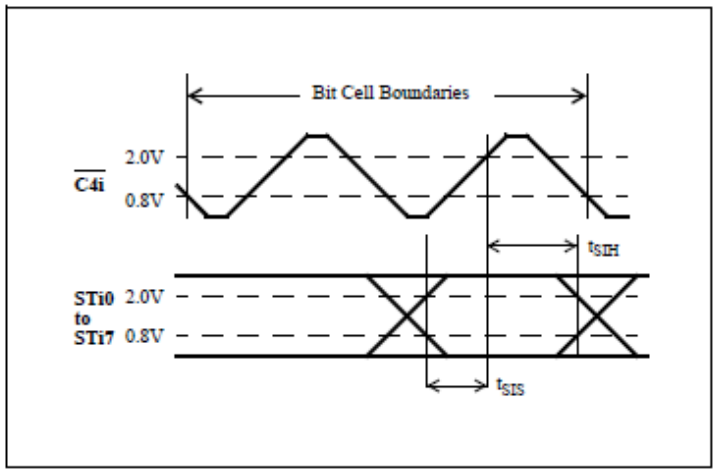


Figure 16 - Serial Inputs

AC Electrical Characteristics† - Processor Bus (Figures 11 and 17)

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	Chip Select Setup Time	t_{CSS}	20	0		ns	
2	Read/Write Setup Time	t_{RWS}	25	5		ns	
3	Address Setup Time	t_{ADS}	25	5		ns	
4	Acknowledgement Delay Fast	t_{AKD}		40	100	ns	C_L=150 pF
	Slow	t_{AKD}	2.7		7.2	cycles	$\overline{C4i}$ cycles[1]
5	Fast Write Data Setup Time	t_{FWS}	20			ns	
6	Slow Write Data Delay	t_{SWD}		2.0	1.7	cycles	$\overline{C4i}$ cycles[1]
7	Read Data Setup Time	t_{RDS}			0.5	cycles	$\overline{C4i}$ cycles[1], C_L= 150 pF
8	Data Hold Time Read	t_{DHT}	20			ns	R_L=1 KΩ*, C_L=150 pF
	Write	t_{DHT}	20	10		ns	
9	Read Data To High Impedance	t_{RDZ}		50	90	ns	R_L=1 KΩ*, C_L=150 pF
10	Chip Select Hold Time	t_{CSH}	0			ns	
11	Read/Write Hold Time	t_{RWH}	0			ns	
12	Address Hold Time	t_{ADH}	0			ns	
13	Acknowledgement Hold Time	t_{AKH}	10	60	80	ns	R_L=1 KΩ*, C_L=150 pF

† Timing is over recommended temperature & power supply voltages.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

Note 1. Processor accesses are dependent on the $\overline{C4i}$ clock, and so some timings are expressed as multiples of the $\overline{C4i}$ clock period.

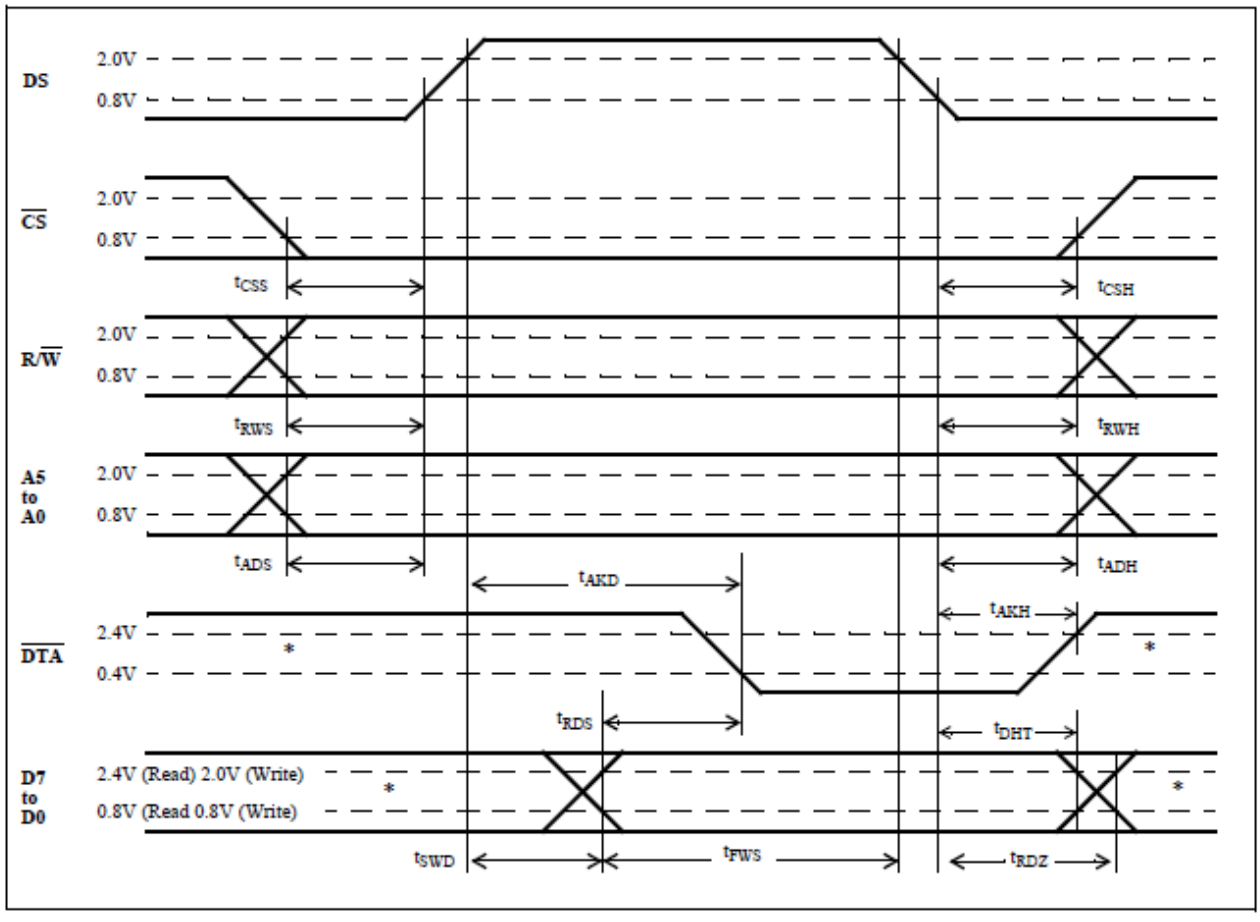
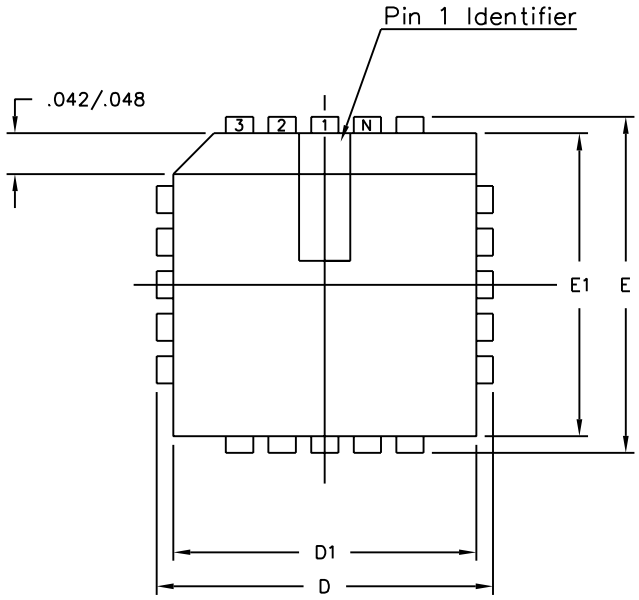
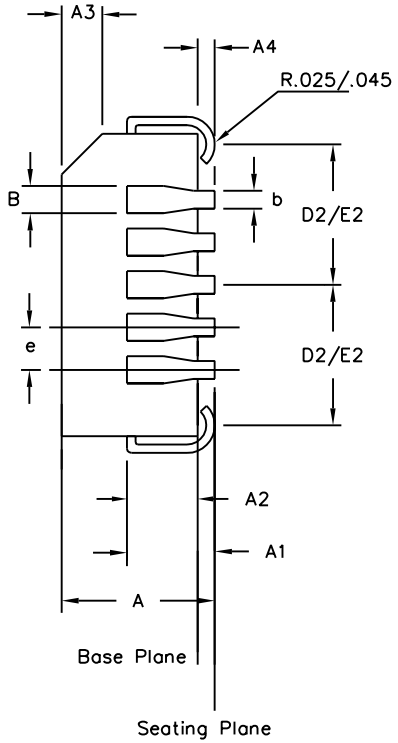


Figure 17 - Processor Bus





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.062	0.083	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	0.685	0.695	17.40	17.65
D1	0.650	0.656	16.51	16.66
D2	0.291	0.319	7.39	8.10
E	0.685	0.695	17.40	17.65
E1	0.650	0.656	16.51	16.66
E2	0.291	0.319	7.39	8.10
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	11			
NE	11			
N	44			
Note	Square			
Conforms to JEDEC MS-018AC Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

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ZARLINK SEMICONDUCTOR

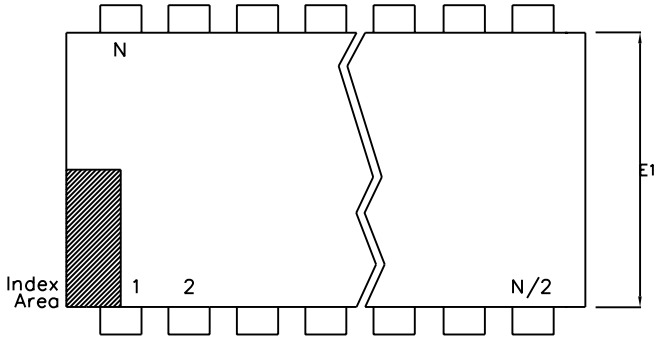
Previous package codes

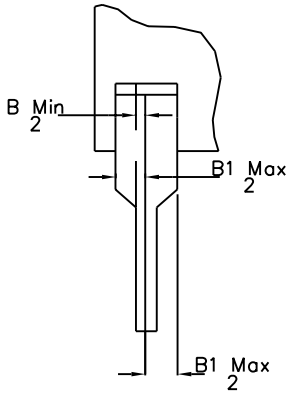
HP / P

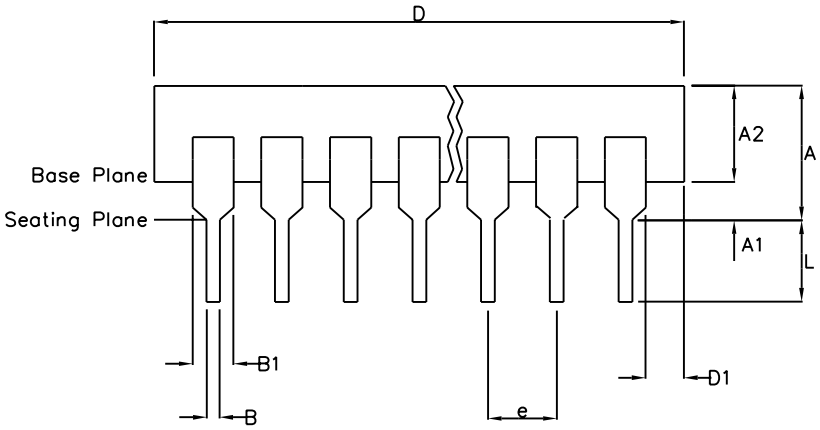
Package Code QA

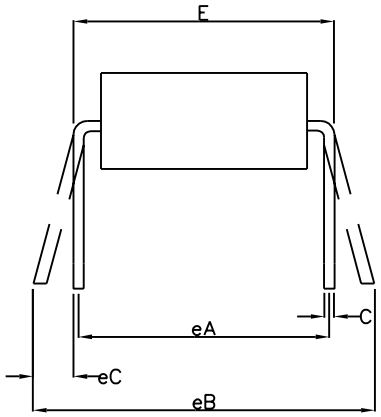
Package Outline for 44 lead PLCC

GPD00003









	Min mm	Max mm	Min Inches	Max Inches
A		6.35		0.250
A1	0.38		0.015	
A2	3.18	4.95	0.125	0.195
B	0.36	0.56	0.014	0.022
B1	0.76	1.78	0.030	0.070
C	0.20	0.38	0.008	0.015
D	50.29	53.21	1.980	2.095
D1	0.13		0.005	
E	15.24	15.88	0.600	0.625
E1	12.32	14.73	0.485	0.580
e	2.54 BSC		0.100 BSC	
eA	15.24 BSC		0.600 BSC	
eB		17.78		0.700
L	2.92	5.08	0.115	0.200
N	40		40	
Conforms to Jedec MS-011AC ISS.B				

Notes:
1. Controlling Dimensions are in inches
2. Dimension A, A1 and L are measured with the package seated in the Seating Plane
3. Dimensions D & E1 do not include mould flash or protrusions. Mould flash or protrusion shall not exceed 0.010 inch.
4. Dimensions E & eA are measured with leads constrained to be perpendicular to plane T.
5. Dimensions eB & eC are measured at the lead tips with the leads unconstrained; eC must be zero or greater.

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ZARLINK SEMICONDUCTOR

Previous package codes

DP / E

Package Code DA

Package Outline for 40 lead PDIP

GPD00073



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