PCA21125

SPI-bus Real-Time Clock and calendar

Rev. 2 — 25 November 2014 Product data sheet

1. General description

The PCA21125 is a CMOS[1] Real-Time Clock (RTC) and calendar optimized for low-power consumption and an operating temperature up to 125 °C. Data is transferred via a Serial Peripheral Interface (SPI-bus) with a maximum data rate of 6.0 Mbit/s. Alarm and timer functions are also available with the possibility to generate a wake-up signal on the interrupt pin.

For a selection of NXP Real-Time Clocks, see Table 46 on page 41

2. Features and benefits

- AEC Q100 compliant for automotive applications.
- Provides year, month, day, weekday, hours, minutes, and seconds based on 32.768 kHz quartz crystal
- Resolution: seconds to years
- Clock operating voltage: 1.3 V to 5.5 V
- Low supply current: typical 0.8 μA at T_{amb} = 25 °C
- 4-line SPI-bus with separate, but combinable data input and output
- Serial interface at V_{DD} = 1.6 V to 5.5 V
- 1 second or 1 minute interrupt output
- Freely programmable timer with interrupt capability
- Freely programmable alarm function with interrupt capability
- Integrated oscillator capacitor
- Internal Power-On Reset (POR)
- Open-drain interrupt pin

3. Applications

- Automotive time keeping
- Metering

1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 21.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
PCA21125T	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1

4.1 Ordering options

Table 2. Ordering options

Product type number	Orderable part number	Sales item (12NC)	Delivery form	IC revision
PCA21125T/Q900/1	PCA21125T/Q900/1,1	935290408118	tape and reel, 13 inch	1

5. Marking

Table 3. Marking codes

Type number	Marking code
PCA21125T/Q900/1	PC21125

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

6. Block diagram

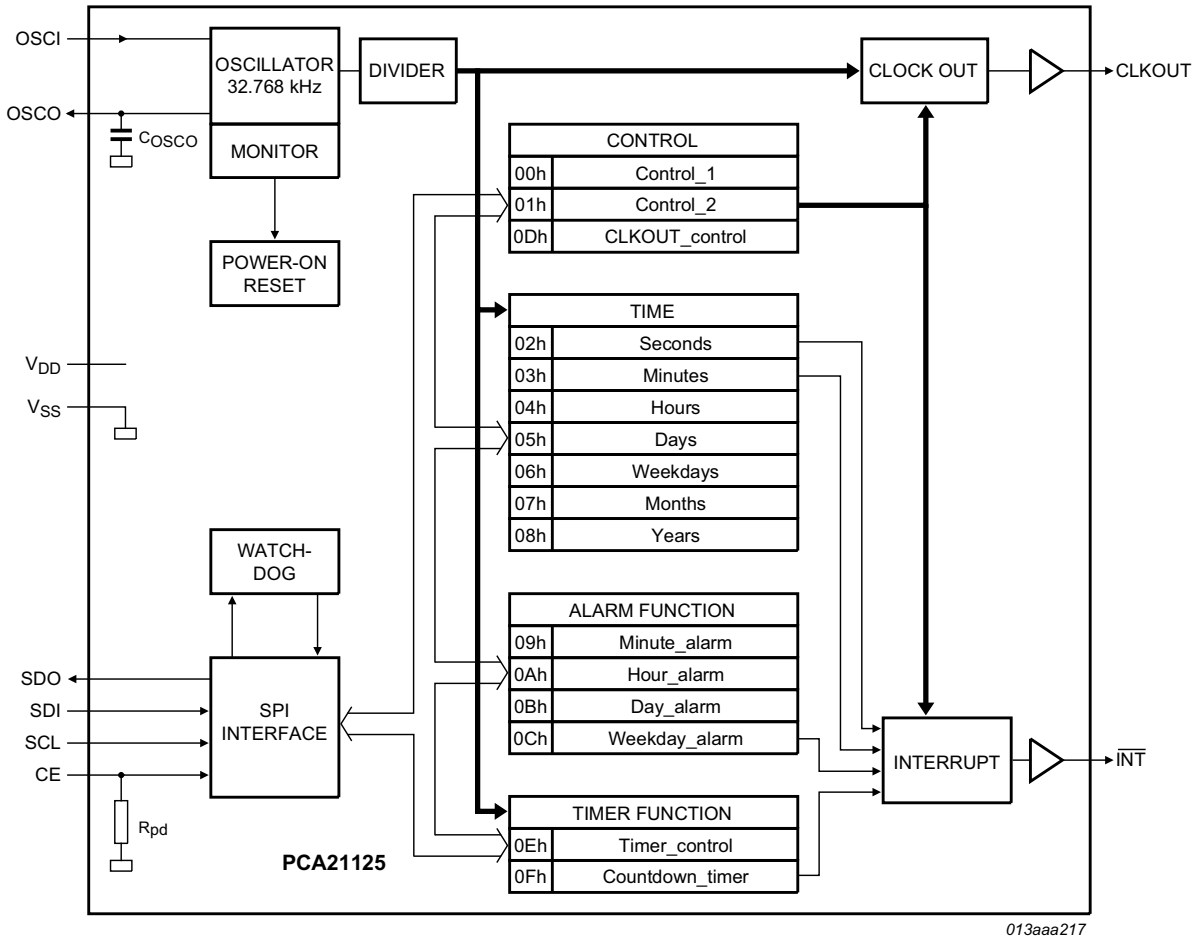


Fig 1. Block diagram of PCA21125

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

7. Pinning information

7.1 Pinning

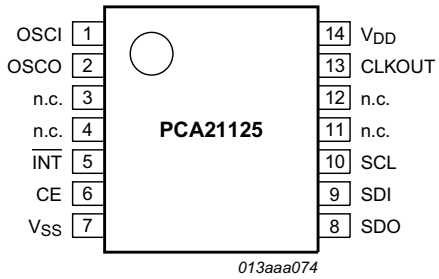


Fig 2. Pin configuration for TSSOP14

7.2 Pin description

Table 4. Pin description

Input or input/output pins must always be at a defined level (V_{SS} or V_{DD}) unless otherwise specified.

Symbol	Pin	Description
OSCI	1	oscillator input
OSCO	2	oscillator output
n.c.	3, 4	not connected; do not connect and do not use as feed through; connect to V_{DD} if floating pins are not allowed
$\overline{INT}$	5	interrupt output (open-drain; active LOW)
CE	6	chip enable input (active HIGH) with 200 kΩ pull-down resistor
V_{SS}	7	ground supply voltage
SDO	8	serial data output, push-pull
SDI	9	serial data input; might float when CE inactive
SCL	10	serial clock input; might float when CE inactive
n.c.	11, 12	not connected; do not connect and do not use as feed through; connect to V_{DD} if floating pins are not allowed
CLKOUT	13	clock output (open-drain)
V_{DD}	14	supply voltage

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

8. Functional description

The PCA21125 contains 16 8-bit registers with an auto-incrementing address register, an on-chip 32.768 kHz oscillator with one integrated capacitor, a frequency divider which provides the source clock for the RTC, a programmable clock output, and a 6 MHz SPI-bus.

All 16 registers are designed as addressable 8-bit parallel registers although not all bits are implemented:

- The first two registers at addresses 00h and 01h (Control_1 and Control_2) are used as control and status registers.
- Registers at addresses 02h to 08h (Seconds, Minutes, Hours, Days, Weekdays, Months, Years) are used as counters for the clock function. Seconds, minutes, hours, days, months, and years are all coded in Binary Coded Decimal (BCD) format. When one of the RTC registers is written or read, the contents of all counters are frozen. Therefore, faulty writing or reading of time and date during a carry condition is prevented.
- Registers at addresses 09h to 0Ch (Minute_alarm, Hour_alarm, Day_alarm, and Weekday_alarm) define the alarm condition.
- The register at address 0Dh (CLKOUT_control) defines the clock output mode.
- Registers at addresses 0Eh and 0Fh (Timer_control and Countdown_timer) are used for the countdown timer function. The countdown timer has four selectable source clocks allowing for countdown periods in the range from less than 1 ms to more than 4 hours (see Table 30). There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute. These are defined in register Control_2 (01h).

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

8.1 Register overview

The time, date, and alarm registers are encoded in BCD to simplify application use. Other registers are either bit-wise or standard binary.

Table 5. Register overview

Bits labeled - are not implemented and return logic 0 when read. Bit positions labeled N should always be written with logic 0. After reset, all registers are set according to Table 38 on page 26.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
Control and status registers									
00h	Control_1	EXT_TEST	N	STOP	N	POR_OVRD	12_24	N	N
01h	Control_2	MI	SI	MSF	TI_TP	AF	TF	AIE	TIE
Time and date registers									
02h	Seconds	RF	SECONDS (0 to 59)						
03h	Minutes	-	MINUTES (0 to 59)						
04h	Hours	-	-	AMPM	HOURS (1 to 12) in 12-hour mode				
		-	-	HOURS (0 to 23) in 24-hour mode					
05h	Days	-	-	DAYS (1 to 31)					
06h	Weekdays	-	-	-	-	-	WEEKDAYS (0 to 6)		
07h	Months	-	-	-	MONTHS (1 to 12)				
08h	Years	YEARS (0 to 99)							
Alarm registers									
09h	Minute_alarm	AEN_M	MINUTE_ALARM (0 to 59)						
0Ah	Hour_alarm	AEN_H	-	AMPM	HOUR_ALARM (1 to 12) in 12-hour mode				
			-	HOUR_ALARM (0 to 23) in 24-hour mode					
0Bh	Day_alarm	AEN_D	-	DAY_ALARM (1 to 31)					
0Ch	Weekday_alarm	AEN_W	-	-	-	-	WEEKDAY_ALARM (0 to 6)		
CLKOUT control register									
0Dh	CLKOUT_control	-	-	-	-	-	COF[2:0]		
Timer registers									
0Eh	Timer_control	TE	-	-	-	-	-	CTD[1:0]	
0Fh	Countdown_timer	T[7:0]							

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

8.2 Control and status registers

8.2.1 Register Control_1

Table 6. Control_1 - control and status register 1 (address 00h) bit description

Bit	Symbol	Value	Description	Reference
7	EXT_TEST	0[1]	normal mode	Section 8.8
		1	external clock test mode	
6	N	0	unused	-
5	STOP	0[1]	RTC source clock runs	Section 8.9
		1	RTC clock is stopped[2]	
4	N	0	unused	-
3	POR_OVRD	0	Power-On Reset Override facility is disabled; **Remark:** set logic 0 for normal operation	Section 8.10.1
		1[1]	Power-On Reset Override sequence reception enabled	
2	12_24	0[1]	24-hour mode selected	Table 11 and Table 19
		1	12-hour mode selected	
1 to 0	N	00	unused	-

[1] Default value.

[2] CLKOUT at 32.768 kHz, 16.384 kHz or 8.192 kHz is still available; divider chain flip-flops are asynchronously set logic 0.

8.2.2 Register Control_2

Table 7. Control_2 - control and status register 2 (address 01h) bit description

Bit	Symbol	Value	Description	Reference
7	MI	0[1]	minute interrupt disabled	Section 8.6.1
		1	minute interrupt enabled	
6	SI	0[1]	second interrupt disabled	Section 8.6.1
		1	second interrupt enabled	
5	MSF	0[1]	no minute or second interrupt generated	Section 8.6.1
		1	flag set when minute or second interrupt generated	
4	TI_TP	0[1]	interrupt pin follows TF and MSF (see Figure 9)	Section 8.6 et seq. and Section 8.7 et seq.
		1	interrupt pin generates a pulse	
3	AF	0[1]	no alarm interrupt generated	Section 8.4.5
		1	flag set when alarm triggered; **Remark:** flag must be cleared to clear interrupt	
2	TF	0[1]	no countdown timer interrupt generated	Section 8.6 et seq. and Section 8.7 et seq.
		1	flag set when countdown timer interrupt generated	
1	AIE	0[1]	no interrupt generated from alarm flag	Section 8.7.3
		1	interrupt generated when alarm flag set	
0	TIE	0[1]	no interrupt generated from countdown timer flag	Section 8.7
		1	interrupt generated when countdown timer flag set	

[1] Default value.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

8.3 Time and date registers

Most of these registers are coded in the Binary Coded Decimal (BCD) format. BCD is used to simplify application use. An example is shown for register Seconds in Table 9.

Loading these registers with values outside of the given range results in unpredictable time and date generation (see Figure 3 “Data flow of the time function”).

8.3.1 Register Seconds

Table 8. Seconds - seconds and clock integrity status register (address 02h) bit description

Bit	Symbol	Value	Description
7	RF	0	clock integrity is guaranteed
		1[1]	clock integrity is not guaranteed; chip reset has occurred since flag was last cleared
6 to 4	SECONDS	0 to 5	ten’s place
3 to 0		0 to 9	unit place

[1] Start-up value.

Table 9. Seconds coded in BCD format

Seconds value in decimal	Upper-digit (ten’s place)			Digit (unit place)			
	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	0	0	0	0	0	0	0
01	0	0	0	0	0	0	1
02	0	0	0	0	0	1	0
:	:	:	:	:	:	:	:
09	0	0	0	1	0	0	1
10	0	0	1	0	0	0	0
:	:	:	:	:	:	:	:
58	1	0	1	1	0	0	0
59	1	0	1	1	0	0	1

8.3.2 Register Minutes

Table 10. Minutes - minutes register (address 03h) bit description

Bit	Symbol	Value	Description
7	-	0	unused
6 to 4	MINUTES	0 to 5	ten’s place
3 to 0		0 to 9	unit place

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

8.3.3 Register Hours

Table 11. Hours - hours register (address 04h) bit description

Bit	Symbol	Value	Description
7 to 6	-	00	unused
12-hour mode[1]			
5	AMPM	0	indicates AM
		1	indicates PM
4	HOURS	0 to 1	ten's place
3 to 0		0 to 9	unit place
24-hour mode[1]			
5 to 4	HOURS	0 to 2	ten's place
3 to 0		0 to 9	unit place

[1] Hour mode is set by bit 12_24 in register Control_1 (see Table 6).

8.3.4 Register Days

Table 12. Days - days register (address 05h) bit description

Bit	Symbol	Value	Place value	Description
7 to 6	-	00	-	unused
5 to 4	DAYS[1]	0 to 3	ten's place	actual day coded in BCD format
3 to 0		0 to 9	unit place	

[1] The PCA21125 compensates for leap years by adding a 29th day to February if the year counter contains a value which is exactly divisible by 4, including the year 00.

8.3.5 Register Weekdays

Table 13. Weekdays - weekdays register (address 06h) bit description

Bit	Symbol	Value	Description
7 to 3	-	00000	unused
2 to 0	WEEKDAYS	0 to 6	actual weekday, values see Table 14

Table 14. Weekday assignments

Day[1]	Bit		
	2	**1**	**0**
Sunday	0	0	0
Monday	0	0	1
Tuesday	0	1	0
Wednesday	0	1	1
Thursday	1	0	0
Friday	1	0	1
Saturday	1	1	0

[1] Definition may be reassigned by the user.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

8.3.6 Register Months

Table 15. Months - months register (address 07h) bit description

Bit	Symbol	Value	Description
7 to 5	-	000	unused
4	MONTHS	0 to 1	ten's place
3 to 0		0 to 9	unit place

Table 16. Month assignments in BCD format

Month	Upper-digit (ten's place)	Digit (unit place)			
	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
January	0	0	0	0	1
February	0	0	0	1	0
March	0	0	0	1	1
April	0	0	1	0	0
May	0	0	1	0	1
June	0	0	1	1	0
July	0	0	1	1	1
August	0	1	0	0	0
September	0	1	0	0	1
October	1	0	0	0	0
November	1	0	0	0	1
December	1	0	0	1	0

8.3.7 Register Years

Table 17. Years - years register (08h) bit description

Bit	Symbol	Value	Place value	Description
7 to 4	YEARS	0 to 9	ten's place	actual year coded in BCD format
3 to 0		0 to 9	unit place	

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

8.3.8 Setting and reading the time

Figure 3 shows the data flow and data dependencies starting from the 1 Hz clock tick.

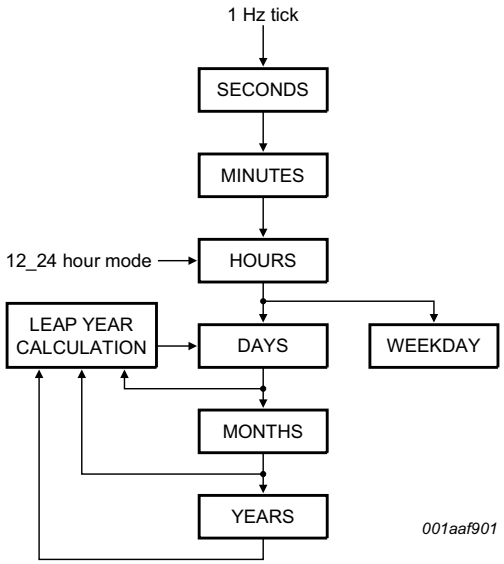


Fig 3. Data flow of the time function

During read/write operations, the time counting circuits (memory locations 02h through 08h) are blocked.

This prevents

- Faulty reading of the clock and calendar during a carry condition
- Incrementing the time registers during the read cycle

After this read/write access is completed, the time circuit is released again and any pending request to increment the time counters that occurred during the read/write access is serviced. A maximum of 1 request can be stored; therefore, all accesses must be completed within 1 second (see Figure 4).

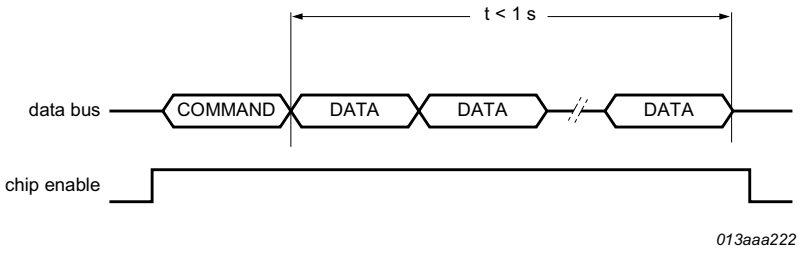


Fig 4. Access time for read/write operations

As a consequence of this method, it is very important to make a read or write access in one go, that is, setting or reading seconds through to years should be made in one single access. Failing to comply with this method could result in the time becoming corrupted.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

As an example, if the time (seconds through to hours) is set in one access and then in a second access the date is set, it is possible that the time may increment between the two accesses. A similar problem exists when reading. A roll-over may occur between reads thus giving the minutes from one moment and the hours from the next. Therefore it is advised to read all time and date registers in one access.

8.4 Alarm registers

When one or several alarm registers are loaded with a valid minute, hour, day, or weekday value and its corresponding alarm enable bit (AEN_X) is logic 0, then that information is compared with the current minute, hour, day, and weekday value.

8.4.1 Register Minute_alarm

Table 18. Minute_alarm - minute alarm register (address 09h) bit description

Bit	Symbol	Value	Place value	Description
7	AEN_M	0	-	minute alarm is enabled
		1[1]	-	minute alarm is disabled
6 to 4	MINUTE_ALARM	0 to 5	ten's place	minute alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.4.2 Register Hour_alarm

Table 19. Hour_alarm - hour alarm register (address 0Ah) bit description

Bit	Symbol	Value	Description
7	AEN_H	0	hour alarm is enabled
		1[1]	hour alarm is disabled
6	-	0	unused
12-hour mode[2]			
5	AMPM	0	indicates AM
		1	indicates PM
4	HOUR_ALARM	0 to 1	ten's place
3 to 0		0 to 9	unit place
24-hour mode[2]			
5 to 4	HOURS	0 to 2	ten's place
3 to 0		0 to 9	unit place

[1] Default value.

[2] Hour mode is set by bit 12_24 in register Control_1 (see Table 6).

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

8.4.3 Register Day_alarm

Table 20. Day_alarm - day alarm register (address 0Bh) bit description

Bit	Symbol	Value	Place value	Description
7	AEN_D	0	-	day alarm is enabled
		1[1]	-	day alarm is disabled
6	-	0	-	unused
5 to 4	DAY_ALARM	0 to 3	ten's place	day alarm information coded in BCD format
3 to 0		0 to 9	unit place	

[1] Default value.

8.4.4 Register Weekday_alarm

Table 21. Weekday_alarm - weekday alarm register (address 0Ch) bit description

Bit	Symbol	Value	Description
7	AEN_W	0	weekday alarm is enabled
		1[1]	weekday alarm is disabled
6 to 3	-	0000	unused
2 to 0	WEEKDAY_ALARM	0 to 6	weekday alarm information coded in BCD format

[1] Default value.

8.4.5 Alarm flag

By clearing the MSB, AEN_X (Alarm Enable), of one or more of the alarm registers the corresponding alarm condition(s) are active. When an alarm occurs, AF (register Control_2, see Table 7) is set logic 1. The asserted AF can be used to generate an interrupt ($\overline{INT}$). The AF is cleared by command.

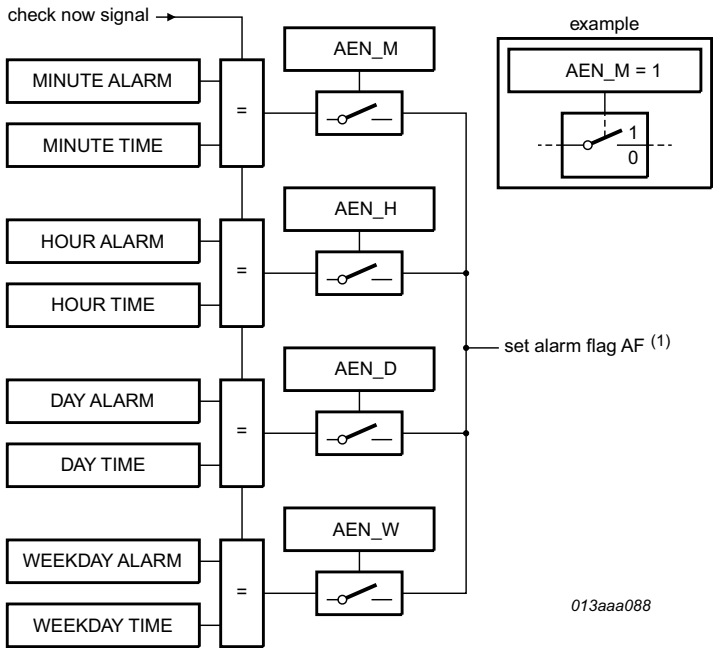


Fig 5. Alarm function block diagram

All information provided in this document is subject to legal disclaimers.

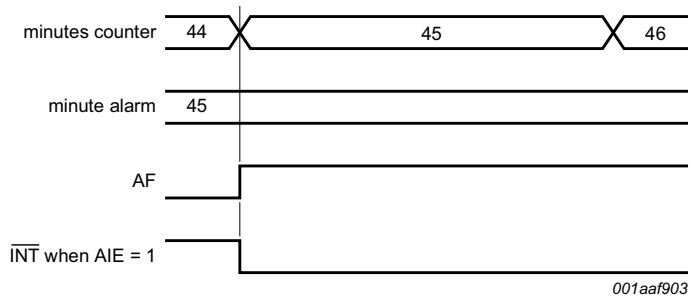
© NXP Semiconductors N.V. 2014. All rights reserved.

The registers at addresses 09h through 0Ch contain alarm information. When one or more of these registers is loaded with minute, hour, day, or weekday, and its corresponding Alarm Enable bit (AEN_X) is logic 0, then that information is compared with the current minute, hour, day, and weekday. When all enabled comparisons first match, the Alarm Flag (AF) is set logic 1.

The generation of interrupts from the alarm function is controlled via bit AIE (register Control_2, see Table 7). If bit AIE is enabled, the $\overline{INT}$ pin follows the condition of bit AF. AF remains set until cleared by the interface. Once AF has been cleared, it is only set again when the time increments to match the alarm condition once more. Alarm registers which have their AEN_X bit logic 1 are ignored.

Generation of interrupts from the alarm function is described in Section 8.7.3.

Figure 6, Table 22 and Table 23 show an example for clearing bit AF, but leaving bit MSF and bit TF unaffected. The flags are cleared by a write command, therefore bits 7, 6, 4, 1 and 0 must be written with their previous values. Repeatedly rewriting these bits has no influence on the functional behavior.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 6. Alarm flag timing

To prevent the timer flags being overwritten while clearing bit AF, logic AND is performed during a write access. A flag is cleared by writing logic 0 while a flag is not cleared by writing logic 1. Writing logic 1 results in the flag value remaining unchanged.

Table 22. Flag location in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	MSF	-	AF	TF	-	-

Table 23 shows what instruction must be sent to clear bit AF. In this example, bit MSF and bit TF are unaffected.

Table 23. Example to clear only AF (bit 3) in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	1	-	0	1	-	-

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

8.5 Register CLKOUT_control and clock output

A programmable square wave is available at pin CLKOUT. Operation is controlled by control bits COF[2:0] in register CLKOUT_control (0Dh); see Table 24. Frequencies of 32.768 kHz (default) down to 1 Hz can be generated for use as a system clock, microcontroller clock, input to a charge pump, or for calibration of the oscillator.

Table 24. CLKOUT_control - CLKOUT control register (address 0Dh) bit description

Bit	Symbol	Value	Description
7 to 3	-	00000	unused
2 to 0	COF[2:0]	see Table 25	frequency output at pin CLKOUT

Pin CLKOUT is an open-drain output and enabled at power-on. When disabled the output is LOW.

The duty cycle of the selected clock is not controlled, but due to the nature of the clock generation, all clock frequencies, except 32.768 kHz, have a duty cycle of 50 : 50.

The stop function can also affect the CLKOUT signal, depending on the selected frequency. When STOP is active, the CLKOUT pin generates a continuous LOW for those frequencies that can be stopped. For more details, see Section 8.9.

Table 25. CLKOUT frequency selection

Bits COF[2:0]	CLKOUT frequency (Hz)	Typical duty cycle[1] (%)	Effect of STOP
000[2]	32768	60 : 40 to 40 : 60	no effect
001	16384	50 : 50	no effect
010	8192	50 : 50	no effect
011	4096	50 : 50	CLKOUT = LOW
100	2048	50 : 50	CLKOUT = LOW
101	1024	50 : 50	CLKOUT = LOW
110	1	50 : 50	CLKOUT = LOW
111	CLKOUT = LOW		

[1] Duty cycle definition: HIGH-level time (%) : LOW-level time (%).

[2] Default value.

8.6 Timer registers

The countdown timer has four selectable source clocks allowing for countdown periods in the range from less than 1 ms to more than 4 hours (see Table 30). There are also two pre-defined timers which can be used to generate an interrupt once per second or once per minute.

Registers Control_2 (01h), Timer_control (0Eh), and Countdown_timer (0Fh) are used to control the timer function and output.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 26. Timer_control - timer control register (address 0Eh) bit description

Bit	Symbol	Value	Description	Reference
7	TE	0[1]	countdown timer is disabled	Section 8.6.2
		1	countdown timer is enabled	
6 to 2	-	00000	unused	
1 to 0	CTD[1:0]	00	4.096 kHz countdown timer source clock	
		01	64 Hz countdown timer source clock	
		10	1 Hz countdown timer source clock	
		11[1]	$^1/_{60}$ Hz countdown timer source clock	

[1] Default value.

Table 27. Countdown_timer - countdown timer register (address 0Fh) bit description

Bit	Symbol	Value	Description	Reference
7 to 0	T[7:0]	0h to FFh	countdown timer value[1]	Section 8.6.2

[1] Countdown period in seconds: $CountdownPeriod = \frac{T}{SourceClockFrequency}$ where T is the countdown value.

8.6.1 Second and minute interrupt

The second and minute interrupts (bits SI and MI) are pre-defined timers for generating periodic interrupts. The timers can be enabled independently of one another, however a minute interrupt enabled on top of a second interrupt is not distinguishable since it occurs at the same time; see Figure 7.

The minute and second flag (MSF) is set logic 1 when either the seconds or the minutes counter increments according to the currently enabled interrupt. The flag can be read and cleared by the interface. The status of bit MSF does not affect the $\overline{INT}$ pulse generation. If the MSF flag is not cleared prior to the next coming interrupt period, an $\overline{INT}$ pulse will still be generated.

Table 28. Effect of bits MI and SI on $\overline{INT}$ generation

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	no interrupt generated
1	0	an interrupt once per minute
0	1	an interrupt once per second
1	1	an interrupt once per second

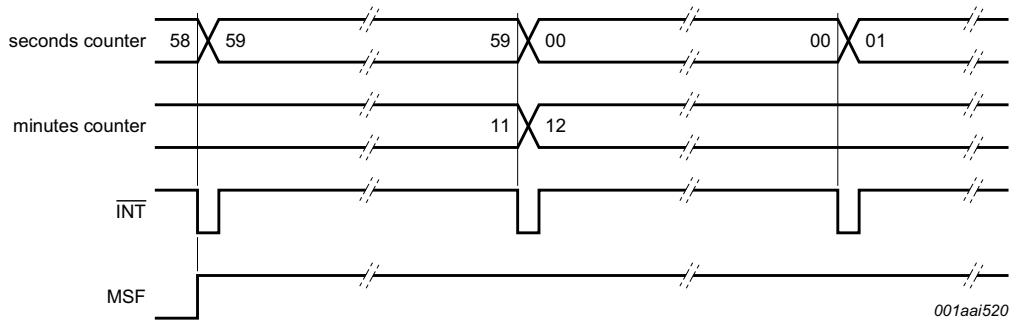
Table 29. Effect of bits MI and SI on bit MSF

Minute interrupt (bit MI)	Second interrupt (bit SI)	Result
0	0	MSF never set
1	0	MSF set when **minutes** counter increments[1]
0	1	MSF set when **seconds** counter increments
1	1	MSF set when **seconds** counter increments

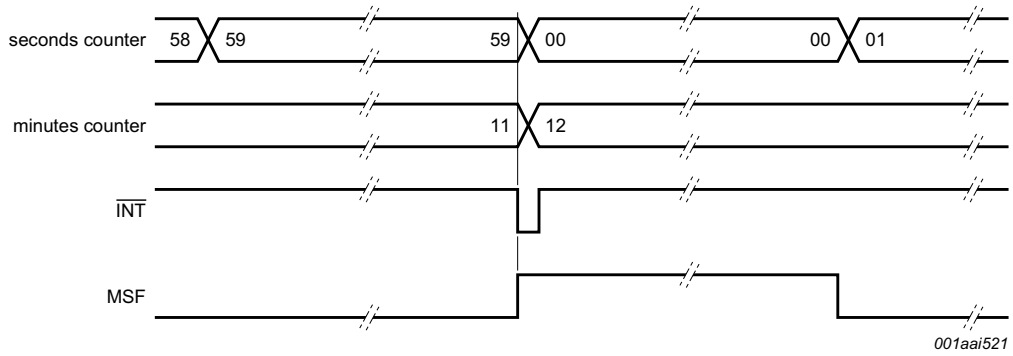
[1] If bit MI = 1 and bit SI = 0, bit MSF is cleared automatically after 1 second.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.



a. $\overline{INT}$ and MSF when SI enabled (MSF flag not cleared after an interrupt)



b. $\overline{INT}$ and MSF when only MI enabled

Bit TI_TP is set logic 1 resulting in $^1/_{64}$ Hz wide interrupt pulse.

Fig 7. $\overline{INT}$ example for bits SI and MI

The purpose of the flag is to allow the controlling system to interrogate the PCA21125 and identify the source of the interrupt such as the minute/second or countdown timer.

8.6.2 Countdown timer function

The 8-bit countdown timer at address 0Fh is controlled by the timer control register at address 0Eh. The timer control register determines one of 4 source clock frequencies for the timer (4.096 kHz, 64 Hz, 1 Hz, or $^1/_{60}$ Hz) and enables or disables the timer.

Table 30. CTD[1:0] for timer frequency selection and countdown timer durations

CTD[1:0]	Timer source clock frequency	Delay	
		Minimum timer duration T = 1	Maximum timer duration T = 255
00	4.096 kHz	244 µs	62.256 ms
01	64 Hz	15.625 ms	3.984 s
10	1 Hz	1 s	255 s
11	$^1/_{60}$ Hz	60 s[1]	4 h 15 min

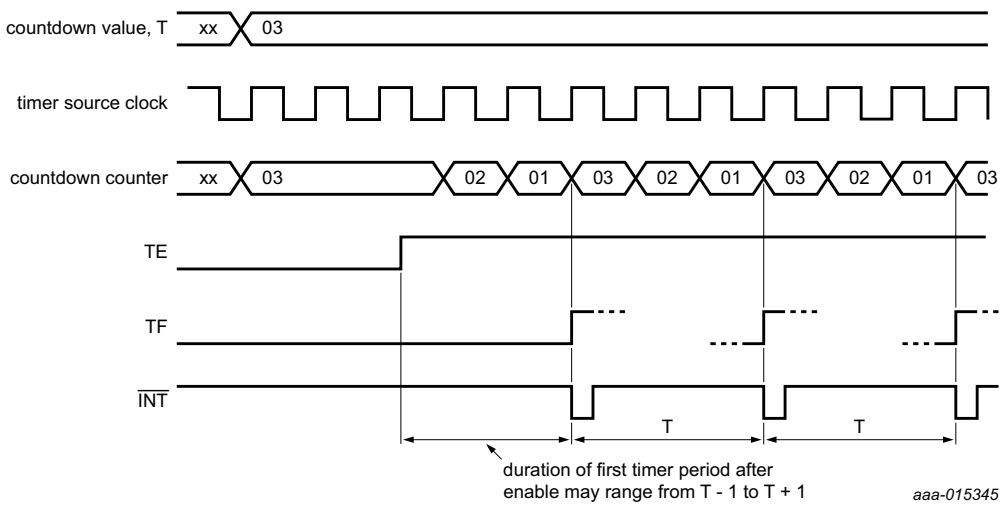
[1] When not in use, CTD[1:0] must be set to $^1/_{60}$ Hz for power saving.

Remark: Note that all timings which are generated from the 32.768 kHz oscillator are based on the assumption that there is 0 ppm deviation. Deviation in oscillator frequency results in a corresponding deviation in timings. This is not applicable to interface timing.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

The timer counts down from a software-loaded 8-bit binary value T. Loading the counter with 0 effectively stops the timer. Values from 1 to 255 are valid. When the counter reaches 1, the countdown timer flag (bit TF in register Control_2, see Table 7) will be set and the counter automatically reloads and starts the next timer period. Reading the timer returns the current value of the countdown counter; see Figure 8.



In the example, it is assumed that the timer flag is cleared before the next countdown period expires and that the $\overline{INT}$ is set to pulsed mode.

Fig 8. General countdown timer behavior

If a new value of T is written before the end of the current timer period, then this new value takes immediate effect. It is not recommended to change T without first disabling the counter (by setting bit TE = 0). The update of T is asynchronous with the timer clock, therefore changing it without setting bit TE = 0 results in a corrupted value loaded into the countdown counter which results in an undetermined countdown period for the first period. The countdown value T will however be correctly stored and correctly loaded on subsequent timer periods.

When the countdown timer flag is set, an interrupt signal on $\overline{INT}$ is generated, if this mode is enabled. See Section 8.7.2 for details on how the interrupt can be controlled.

When starting the timer for the first time, the first period has an uncertainty which is a result of the enable instruction being generated from the interface clock which is asynchronous with the timer source clock. Subsequent timer periods have no such delay. The amount of delay for the first timer period depends on the chosen source clock; see Table 31.

Table 31. First period delay for timer counter value T

Timer source clock	Minimum timer period	Maximum timer period
4.096 kHz	T	T + 1
64 Hz	T	T + 1
1 Hz	(T – 1) + $\frac{1}{64}$ Hz	T + $\frac{1}{64}$ Hz
$\frac{1}{60}$ Hz	(T – 1) + $\frac{1}{64}$ Hz	T + $\frac{1}{64}$ Hz

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

At the end of every countdown, the timer sets the countdown timer flag (bit TF). Bit TF can only be cleared by command. The asserted bit TF can be used to generate an interrupt ($\overline{INT}$). The interrupt can be generated as a pulsed signal every countdown period or as a permanently active signal which follows the condition of bit TF. Bit TI_TP is used to control this mode selection and the interrupt output can be disabled with bit TIE.

For accurate read back of the count down value, it is recommended to read the register twice and check for consistent results, since it is not possible to freeze the countdown timer counter during read back.

8.6.3 Timer flags

When a minute or second interrupt occurs, bit MSF (register Control_2, see Table 7) is set logic 1. Similarly, at the end of a timer countdown bit TF is set logic 1. These bits maintain their value until overwritten by command. If both countdown timer and minute/second interrupts are required in the application, the source of the interrupt can be determined by reading these bits. To prevent one flag being overwritten while clearing another, a logic AND is performed during a write access. A flag is cleared by writing logic 0 while a flag is not cleared by writing logic 1. Writing logic 1 results in the flag value remaining unchanged.

Three examples are given for clearing the flags. Flags MSF and TF are cleared by a write command, therefore bits 7, 6, 4, 1, and 0 must be written with their previous values. Repeatedly rewriting these bits has no influence on the functional behavior.

Table 32. Flag location in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	MSF	-	AF	TF	-	-

Table 33, Table 34, and Table 35 show what instruction must be sent to clear the appropriate flag.

Table 33. Example to clear only TF (bit 2) in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	1	-	1	0	-	-

Table 34. Example to clear only MSF (bit 5) in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	0	-	1	1	-	-

Table 35. Example to clear both TF and MSF (bits 2 and 5) in register Control_2

Register	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Control_2	-	-	0	-	1	0	-	-

Clearing the alarm flag (bit AF) operates in the same way; see Section 8.4.5.

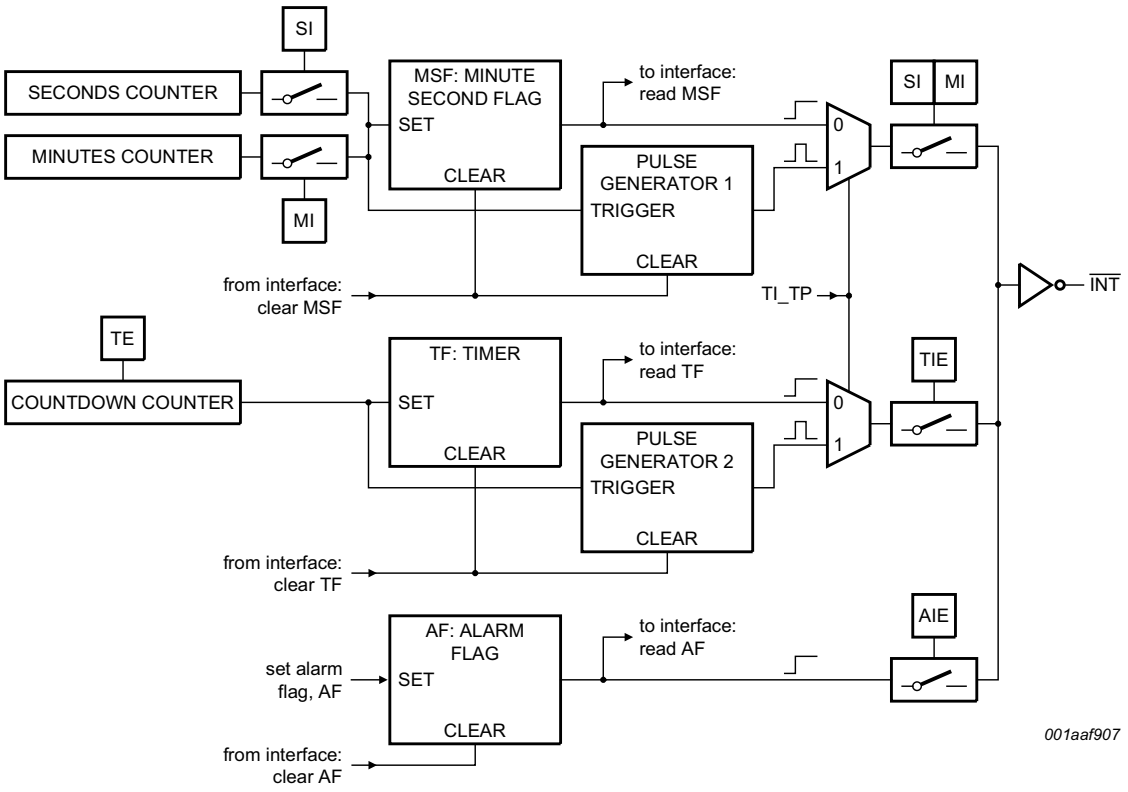
All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

8.7 Interrupt output

An active LOW interrupt signal is available at pin $\overline{INT}$. Operation is controlled via the bits of register Control_2. Interrupts can be sourced from three places: second/minute timer, countdown timer, and alarm function.

Bit TI_TP configures the timer generated interrupts to be either a pulse or to follow the status of the interrupt flags (bits TF and MSF).



When bits SI, MI, TIE and AIE are all disabled, pin $\overline{INT}$ remains high-impedance.

Fig 9. Interrupt scheme

Remark: Note that the interrupts from the three groups are wired-OR, meaning they will mask one another; see Figure 9.

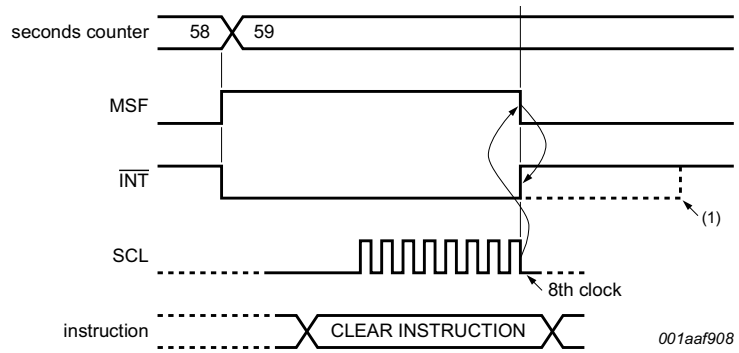
8.7.1 Minute and second interrupts

The pulse generator for the minute/second interrupt operates from an internal 64 Hz clock and consequently generates a pulse of $1/_{64}$ second duration.

If the MSF flag is clear before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced, i.e., the system does not have to wait for the completion of the pulse before continuing; see Figure 10. Instructions for clearing MSF are given in Section 8.6.3.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.



(1) Indicates normal duration of $\overline{INT}$ pulse (bit TI_TP = 1).

Fig 10. Example of shortening the $\overline{INT}$ pulse by clearing the MSF flag

The timing shown for clearing bit MSF in Figure 10 is also valid for the non-pulsed interrupt mode, i.e., when bit TI_TP = 0, where the pulse can be shortened by setting both bits MI and SI logic 0.

8.7.2 Countdown timer interrupts

Generation of interrupts from the countdown timer is controlled via bit TIE (register Control_2, see Table 7).

The pulse generator for the countdown timer interrupt also uses an internal clock which is dependent on the selected source clock for the countdown timer and on the countdown value T. As a consequence, the width of the interrupt pulse varies; see Table 36.

Table 36. $\overline{INT}$ operation (bit TI_TP = 1)

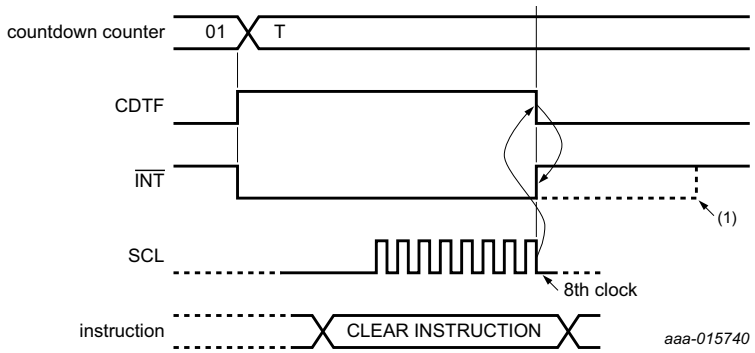
Source clock (Hz)	$\overline{INT}$ period (s)	
	T = 1[1]	T > 1
4096	$1/8192$	$1/4096$
64	$1/128$	$1/64$
1	$1/64$	$1/64$
$1/60$	$1/64$	$1/64$

[1] T = loaded countdown value. Timer stopped when T = 0.

If the TF flag is cleared before the end of the $\overline{INT}$ pulse, then the $\overline{INT}$ pulse is shortened. This allows the source of a system interrupt to be cleared immediately it is serviced, i.e., the system does not have to wait for the completion of the pulse before continuing; see Figure 11. Instructions for clearing TF are given in Section 8.6.3.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.



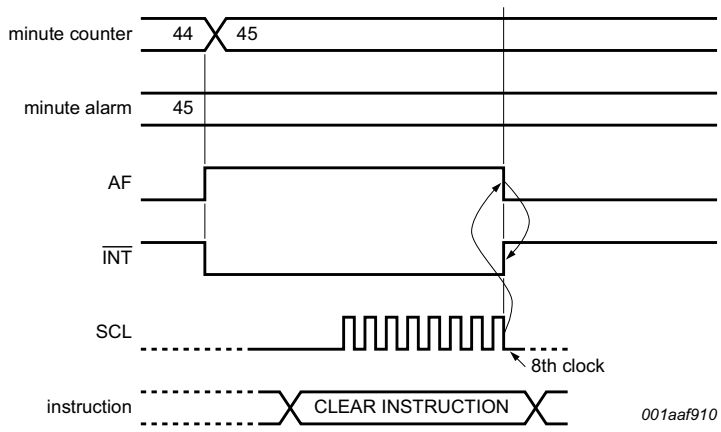
(1) Indicates normal duration of INT pulse (bit TI_TP = 1).

Fig 11. Example of shortening the INT pulse by clearing the TF flag

The timing shown for clearing bit TF in Figure 11 is also valid for the non-pulsed interrupt mode, i.e., when bit TI_TP = 0, where the pulse can be shortened by setting bit TIE = 0.

8.7.3 Alarm interrupts

Generation of interrupts from the alarm function is controlled via bit AIE (register Control_2, see Table 7). If bit AIE is enabled, the INT pin follows the status of bit AF. Clearing bit AF immediately clears INT. No pulse generation is possible for alarm interrupts; see Figure 12.



Example where only the minute alarm is used and no other interrupts are enabled.

Fig 12. AF timing

8.8 External clock test mode

A test mode is available which allows for on-board testing. In this mode, it is possible to set up test conditions and control the operation of the RTC.

The test mode is entered by setting the EXT_TEST bit in register Control_1 (see Table 6). The CLKOUT pin then becomes an input. The test mode replaces the internal signal with the signal applied to pin CLKOUT.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

The signal applied to pin CLKOUT should have a minimum pulse width of 300 ns and a maximum period of 1000 ns. The internal clock, now sourced from pin CLKOUT, is divided down to 1 Hz by a 2^6 divide chain called a prescaler; see Section 8.9. The prescaler can be set into a known state by using the STOP bit. When the STOP bit is set, the prescaler is reset to 0. (STOP must be cleared before the prescaler can operate again.)

From a stop condition, the first 1 second increment will take place after 32 positive edges on pin CLKOUT. Thereafter, every 64 positive edges cause a 1 second increment.

Remark: Entry into test mode is not synchronized to the internal 64 Hz clock. When entering the test mode, no assumption as to the state of the prescaler can be made.

Operation example:

1. Set EXT_TEST test mode (register Control_1, bit EXT_TEST = 1).
2. Set STOP (register Control_1, bit STOP = 1).
3. Clear STOP (register Control_1, bit STOP = 0).
4. Set time registers to desired value.
5. Apply 32 clock pulses to pin CLKOUT.
6. Read time registers to see the first change.
7. Apply 64 clock pulses to pin CLKOUT.
8. Read time registers to see the second change.

Repeat steps 7 and 8 for additional increments.

8.9 STOP bit function

The STOP bit function (register Control_1, see Table 6) allows the accurate starting of the time circuits. The STOP bit function causes the upper part of the prescaler (F_2 to F_{14}) to be held at reset, thus no 1 Hz ticks are generated. The time circuits can then be set and do not increment until STOP is released; see Figure 13. STOP does not affect the output of 32.768 kHz, 16.384 kHz, or 8.192 kHz; see Section 8.5.

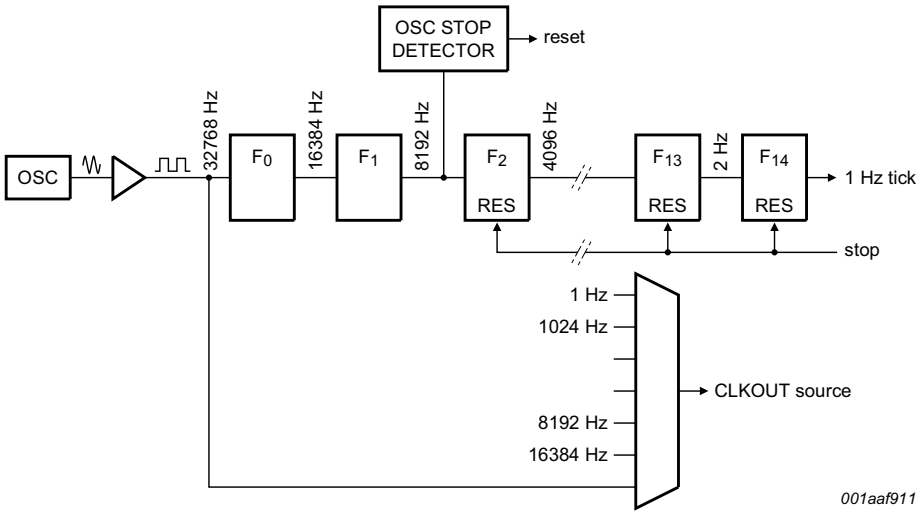


Fig 13. STOP bit functional diagram

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

The lower two stages of the prescaler (F_0 and F_1) are not reset and because the SPI-bus is asynchronous to the crystal oscillator, the accuracy of restarting the time circuits is between 0 and one 8.192 kHz cycle; see Figure 14. The first increment of the time circuits is between 0.499878 s and 0.500000 s after STOP is released. The uncertainty is caused by prescaler bits F0 and F1 not being reset; see Table 37.

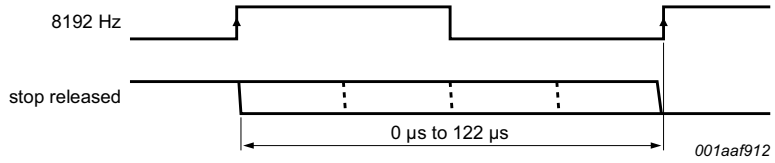
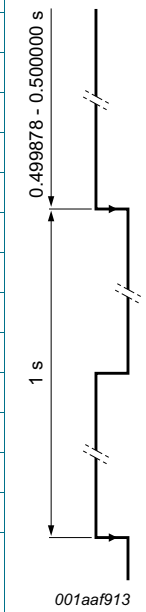


Fig 14. STOP bit release timing

Table 37. Example: first increment of time circuits after STOP release

Bit STOP	Prescaler bits	1 Hz tick	Time	Comment
	F_0F_1-F_2 to F_{14}[1]		hh:mm:ss	
Clock is running normally				
0	01-0 0001 1101 0100		12:45:12	prescaler counting normally
STOP is activated by user. F0F1 are not reset and values cannot be predicted externally				
1	XX-0 0000 0000 0000		12:45:12	prescaler is reset; time circuits are frozen
New time is set by user				
1	XX-0 0000 0000 0000		08:00:00	prescaler is reset; time circuits are frozen
STOP is released by user				
0	XX-0 0000 0000 0000		08:00:00	prescaler is now running
	XX-1 0000 0000 0000		08:00:00	-
	XX-0 1000 0000 0000		08:00:00	-
	XX-1 1000 0000 0000		08:00:00	-
	:		:	:
	11-1 1111 1111 1110		08:00:00	-
	00-0 0000 0000 0001		08:00:01	0 to 1 transition of F14 increments the time circuits
	10-0 0000 0000 0001		08:00:01	-
	:		:	:
	11-1 1111 1111 1111		08:00:01	-
	00-0 0000 0000 0000		08:00:01	-
	10-0 0000 0000 0000		08:00:01	-
	:		:	:
	11-1 1111 1111 1110		08:00:01	-
	00-0 0000 0000 0001		08:00:02	0 to 1 transition of F14 increments the time circuits

[1] F_0 is clocked at 32.768 kHz.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

8.10 Reset

The PCA21125 includes an internal reset circuit which is active whenever the oscillator is stopped; see Figure 15. The oscillator can be stopped, for example, by connecting one of the oscillator pins OSCI or OSCO to ground.

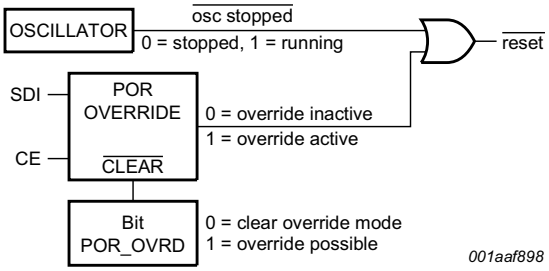


Fig 15. Reset system

The oscillator is considered to be stopped during the time between power-on and stable crystal resonance; see Figure 16. This time can be in the range of 200 ms to 2 s depending on crystal type, temperature and supply voltage. Whenever an internal reset occurs, the reset flag RF (register Seconds, see Table 8) is set.

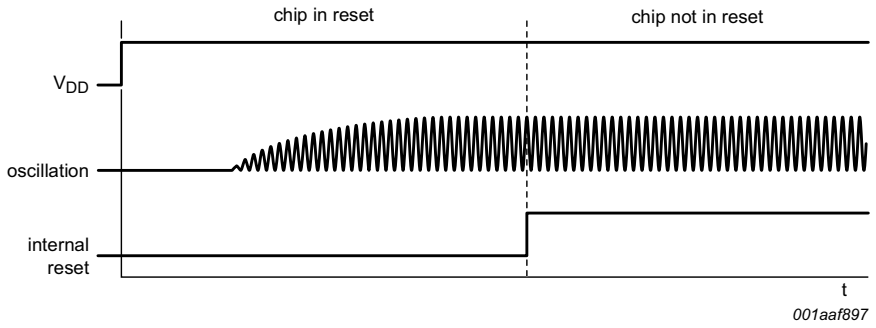


Fig 16. Power-On Reset (POR)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 38. Register reset values

Bits labeled - are not implemented and return logic 0 when read. Bits labeled X are undefined at power-on and unchanged by subsequent resets.

Address	Register name	Bit							
		7	6	5	4	3	2	1	0
00h	Control_1	0	0	0	-	1	0	-	-
01h	Control_2	0	0	0	0	0	0	0	0
02h	Seconds	1	X	X	X	X	X	X	X
03h	Minutes	-	X	X	X	X	X	X	X
04h	Hours	-	-	X	X	X	X	X	X
05h	Days	-	-	X	X	X	X	X	X
06h	Weekdays	-	-	-	-	-	X	X	X
07h	Months	-	-	-	X	X	X	X	X
08h	Years	X	X	X	X	X	X	X	X
09h	Minute_alarm	1	X	X	X	X	X	X	X
0Ah	Hour_alarm	1	-	X	X	X	X	X	X
0Bh	Day_alarm	1	-	X	X	X	X	X	X
0Ch	Weekday_alarm	1	-	-	-	-	X	X	X
0Dh	CLKOUT_control	-	-	-	-	-	0	0	0
0Eh	Timer_control	0	-	-	-	-	-	1	1
0Fh	Countdown_timer	X	X	X	X	X	X	X	X

After reset, the following mode is entered:

- 32.768 kHz on pin CLKOUT active
- POR override available to be set
- 24-hour mode is selected

The SPI-bus is initialized whenever the chip enable pin CE is inactive (LOW).

8.10.1 POR override

The Power-On Reset (POR) duration is directly related to the crystal oscillator start-up time. Due to the long start-up times experienced by these types of circuits, a mechanism has been built in to disable the POR and hence speed up the on-board test of the device.

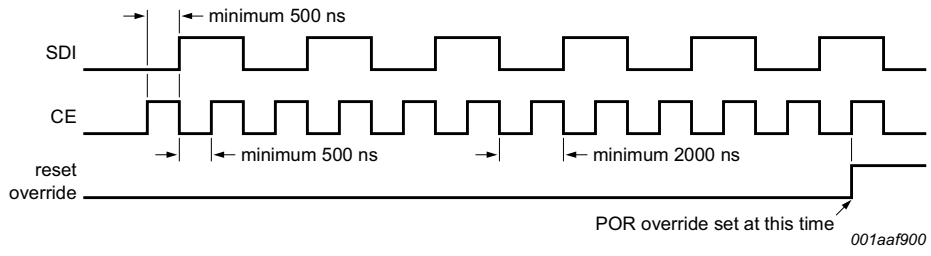


Fig 17. POR override sequence

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

The setting of this mode requires that bit POR_OVRD (register Control_1, see Table 6) be set logic 1 and that the signals at the SPI-bus pins SDI and CE are toggled as illustrated in Figure 17. All timings are required minimums.

Once the override mode has been entered, the device immediately stops being reset and set-up operation can commence, i.e., entry into the external clock test mode via the SPI-bus access. The override mode can be cleared by writing logic 0 to bit POR_OVRD. Bit POR_OVRD must be set logic 1 before a re-entry into the override mode is possible. Setting bit POR_OVRD logic 0 during normal operation has no effect except to prevent accidental entry into the POR override mode. This is the recommended setting.

8.11 4-line SPI-bus

Data transfer to and from the device is made via a 4-line SPI-bus; see Table 39.

Table 39. Serial interface

Pin	Function	Description
CE	chip enable input	when HIGH, data transfer is active when LOW, data transfer is inactive; the interface is reset; pull-down resistor included; active input can be higher than V_{DD}, but must not be wired HIGH permanently
SCL	serial clock input	when pin CE = LOW, this input might float; input can be higher than V_{DD}
SDI	serial data input	when pin CE = LOW, this input might float; input can be higher than V_{DD}; input data is sampled on the rising edge of SCL
SDO	serial data output	push-pull output; drives from V_{SS} to V_{DD}; output data is changed on the falling edge of SCL

The data lines for input and output are split. The data input and output lines can be connected together to facilitate a bidirectional data bus (see Figure 18).

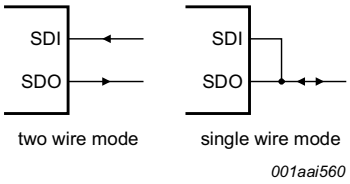


Fig 18. SDI, SDO configurations

The chip enable signal is used to identify the transmitted data. Each data transfer is a byte, with the Most Significant Bit (MSB) sent first; see Figure 19.

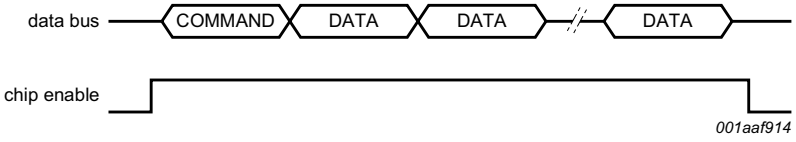


Fig 19. Data transfer overview

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

The transmission is initiated by an active HIGH chip enable signal CE and terminated by an inactive LOW signal. The first byte transmitted is the command byte (see Table 40 and Figure 20). Subsequent bytes are either data to be written or data to be read. Data is captured on the rising edge of the clock and transferred internally on the falling edge.

The command byte defines the address of the first register to be accessed and the read/write mode. The address counter will auto increment after every access and will reset to zero after the last valid register is accessed. The read/write bit (R/$\overline{W}$) defines if the following bytes are read or write information.

Table 40. Command byte definition

Bit	Symbol	Value	Description
7	R/$\overline{W}$		data read or data write selection
		0	write data
		1	read data
6 to 4	SA	001	subaddress; other codes cause the device to ignore data transfer
3 to 0	RA	00h to 0Fh	register address

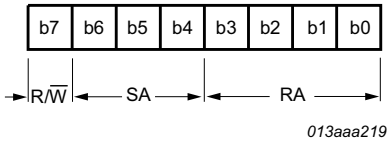


Fig 20. Command byte

In Figure 21, the register Seconds is set to 45 seconds and the register Minutes to 10 minutes.

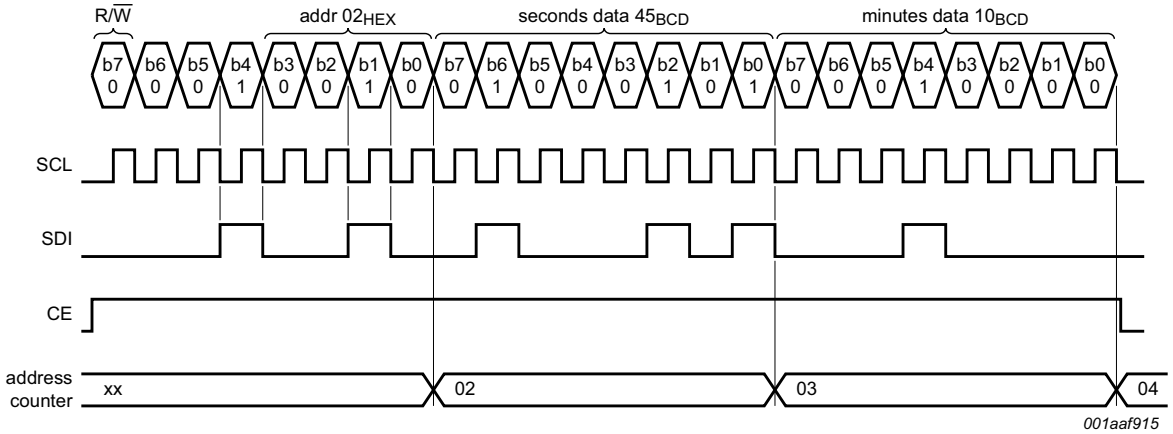


Fig 21. Serial bus write example

In Figure 22, the Months and Years registers are read. In this example, pins SDI and SDO are not connected together.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

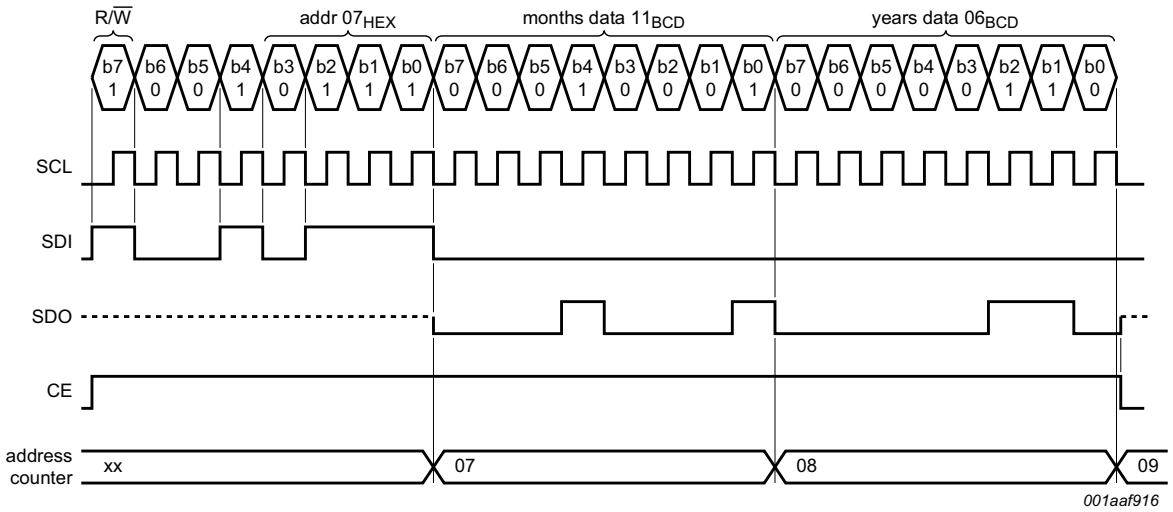
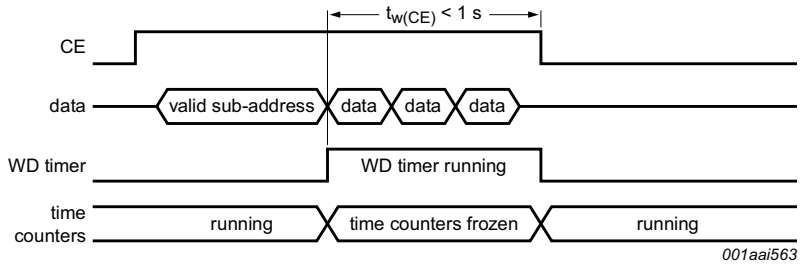


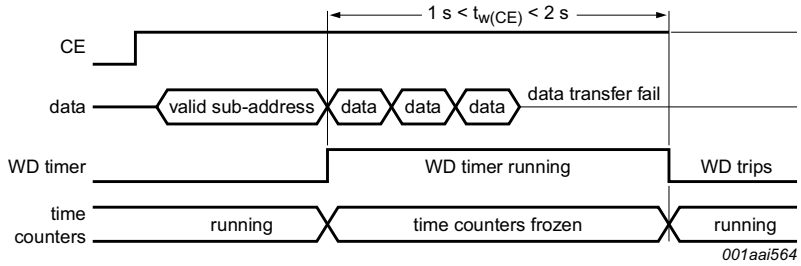
Fig 22. Serial bus read example

8.11.1 Interface watchdog timer

During read/write operations, the time counting circuits are frozen. To prevent a situation where the accessing device becomes locked and does not clear the interface by setting pin CE LOW, the PCA21125 has a built-in watchdog timer. Should the interface be active for more than 1 s from the time a valid subaddress is transmitted, then the PCA21125 will automatically clear the interface and allow the time counting circuits to continue counting. CE must return LOW once more before a new data transfer can be executed.



a. Correct data transfer: read or write



b. Incorrect data transfer; read or write

Fig 23. Interface watchdog timer

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

The watchdog is implemented to prevent the excessive loss of time due to interface access failure, e.g., if main power is removed from a battery backed-up system during an interface access.

Each time the watchdog period is exceeded, 1 s is lost from the time counters. The watchdog will trigger between 1 s and 2 s after receiving a valid subaddress.

9. Internal circuitry

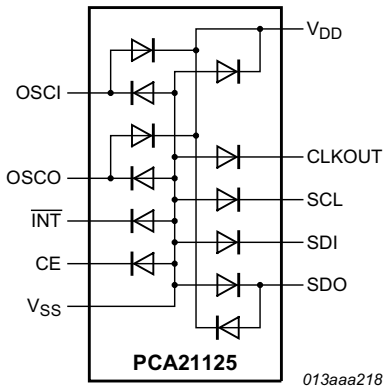


Fig 24. Device diode protection diagram

10. Safety notes

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

11. Limiting values

Table 41. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		–0.5	+6.5	V
I_{DD}	supply current		–50	+50	mA
V_I	input voltage		–0.5	+6.5	V
V_O	output voltage		–0.5	+6.5	V
I_I	input current		–10	+10	mA
I_O	output current		–10	+10	mA
P_{tot}	total power dissipation		-	300	mW
T_{amb}	ambient temperature	operating device	–40	+125	°C
V_{ESD}	electrostatic discharge voltage	HBM [1]	-	±3500	V
		MM [2]	-	±200	V
		CDM [3]	-	±1500	V
I_{lu}	latch-up current	[4]	-	100	mA
T_{stg}	storage temperature	[5]	–65	+150	°C

[1] Pass level; Human Body Model (HBM) according to Ref. 5 “JESD22-A114”.

[2] Pass level; Machine Model (MM), according to Ref. 6 “JESD22-A115”.

[3] Pass level; Charged-Device Model (CDM), according to Ref. 7 “JESD22-C101”.

[4] Pass level; latch-up testing, according to Ref. 8 “JESD78” at maximum ambient temperature ($T_{amb(max)}$ = +125 °C).

[5] According to the store and transport requirements (see Ref. 11 “UM10569”) the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

12. Static characteristics

Table 42. Static characteristics

V_{DD} = 1.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +125 °C; f_{osc} = 32.768 kHz; quartz R_s = 60 kΩ; C_L = 12.5 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply: pin V_{DD}						
V_{DD}	supply voltage	SPI-bus inactive; for clock data integrity [1]	1.3	-	5.5	V
		SPI-bus active	1.6	-	5.5	V
I_{DD}	supply current	SPI-bus active				
		f_{SCL} = 6.0 MHz	-	-	500	µA
		f_{SCL} = 1.0 MHz	-	-	100	µA
		SPI-bus inactive; CLKOUT disabled; V_{DD} = 2.0 V to 5.0 V [2]				
		T_{amb} = 25 °C	-	820	-	nA
		T_{amb} = −40 °C to +125 °C	-	1140	3300	nA
		SPI-bus inactive (f_{SCL} = 0 Hz); CLKOUT enabled at 32 kHz				
		T_{amb} = 25 °C				
		V_{DD} = 5.0 V	-	1220	-	nA
		V_{DD} = 3.0 V	-	940	-	nA
		V_{DD} = 2.0 V	-	810	-	nA
		T_{amb} = −40 °C to +125 °C				
		V_{DD} = 5.0 V	-	-	4000	nA
		V_{DD} = 3.0 V	-	-	2400	nA
		V_{DD} = 2.0 V	-	-	1900	nA
Inputs						
V_I	input voltage	pin OSCI	−0.5	-	V_{DD} + 0.5	V
		pins CE, SDI, SCL	−0.5	-	+5.5	V
V_{IL}	LOW-level input voltage		V_{SS}	-	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	-	V_{DD}	V
I_L	leakage current	V_I = V_{DD} or V_{SS}; on pins SDI, SCL and CLKOUT	−1	0	+1	µA
C_I	input capacitance	[3]	-	-	7	pF
R_{pd}	pull-down resistance	pin CE	-	240	550	kΩ
Outputs						
V_O	output voltage	pins OSCO and SDO	-	-	V_{DD} + 0.5	V
		pins CLKOUT and $\overline{INT}$; refers to external pull-up voltage	-	-	5.5	V
V_{OH}	HIGH-level output voltage	pin SDO	0.8V_{DD}	-	V_{DD}	V

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 42. Static characteristics *...continued*

V_{DD} = 1.3 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +125 °C; f_{osc} = 32.768 kHz; quartz R_s = 60 kΩ; C_L = 12.5 pF; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-level output voltage	pin SDO	V_{SS}	-	$0.2V_{DD}$	V
		pins CLKOUT and $\overline{INT}$; V_{DD} = 5 V; I_{OL} = −1.5 mA	V_{SS}	-	0.4	V
I_{OH}	HIGH-level output current	output source current; pin SDO; V_{OH} = 4.6 V; V_{DD} = 5 V	1.5	-	-	mA
I_{OL}	LOW-level output current	output sink current; pins $\overline{INT}$, SDO and CLKOUT; V_{OL} = 0.4 V; V_{DD} = 5 V	1.5	-	-	mA
I_{LO}	output leakage current	$V_O = V_{DD}$ or V_{SS}	−1	0	+1	µA
C_{ext}	external capacitance	[4]	-	25	-	pF
C_{OSCO}	capacitance on pin OSCO	[4]	-	25	-	pF

[1] For reliable oscillator start at power-up: $V_{DD} = V_{DD(min)} + 0.3$ V.

[2] Timer source clock = $\frac{1}{60}$ Hz; voltage on pins CE, SDI and SCL at V_{DD} or V_{SS}.

[3] Implicit by design.

[4] C_L is a calculation of C_{ext} and C_{OSCO} in series: $C_L = \frac{(C_{ext} \cdot C_{OSCO})}{(C_{ext} + C_{OSCO})}$.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

13. Dynamic characteristics

Table 43. Dynamic characteristics

V_{DD} = 1.6 V to 5.5 V; V_{SS} = 0 V; T_{amb} = −40 °C to +125 °C; all timing values are valid within the operating supply voltage at ambient temperature and referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

Symbol	Parameter	Conditions	V_{DD} = 1.6 V		V_{DD} = 2.7 V		V_{DD} = 4.5 V		V_{DD} = 5.5 V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Pin SCL											
$f_{clk(SCL)}$	SCL clock frequency		-	1.5	-	4.0	-	5.00	-	6.25	MHz
t_{SCL}	SCL time		660	-	250	-	200	-	160	-	ns
$t_{clk(H)}$	clock HIGH time		320	-	120	-	100	-	70	-	ns
$t_{clk(L)}$	clock LOW time		320	-	130	-	100	-	90	-	ns
t_r	rise time	for SCL signal	-	100	-	100	-	100	-	100	ns
t_f	fall time	for SCL signal	-	100	-	100	-	100	-	100	ns
Pin CE											
$t_{su(CE)}$	CE set-up time		30	-	30	-	30	-	30	-	ns
$t_{h(CE)}$	CE hold time		100	-	60	-	40	-	30	-	ns
$t_{rec(CE)}$	CE recovery time		100	-	100	-	100	-	100	-	ns
$t_{w(CE)}$	CE pulse width		-	0.99	-	0.99	-	0.99	-	0.99	s
Pin SDI											
t_{su}	set-up time		25	-	15	-	15	-	10	-	ns
t_h	hold time		100	-	60	-	40	-	30	-	ns
Pin SDO											
$t_{d(R)SDO}$	SDO read delay time	bus load = 85 pF	-	320	-	130	-	100	-	90	ns
$t_{dis(SDO)}$	SDO disable time	no load value [1]	-	50	-	30	-	30	-	25	ns
$t_{t(SDI-SDO)}$	transition time from SDI to SDO	to avoid bus conflict	0	-	0	-	0	-	0	-	ns

[1] Bus is held up by bus capacitance; use RC time constant with application values.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

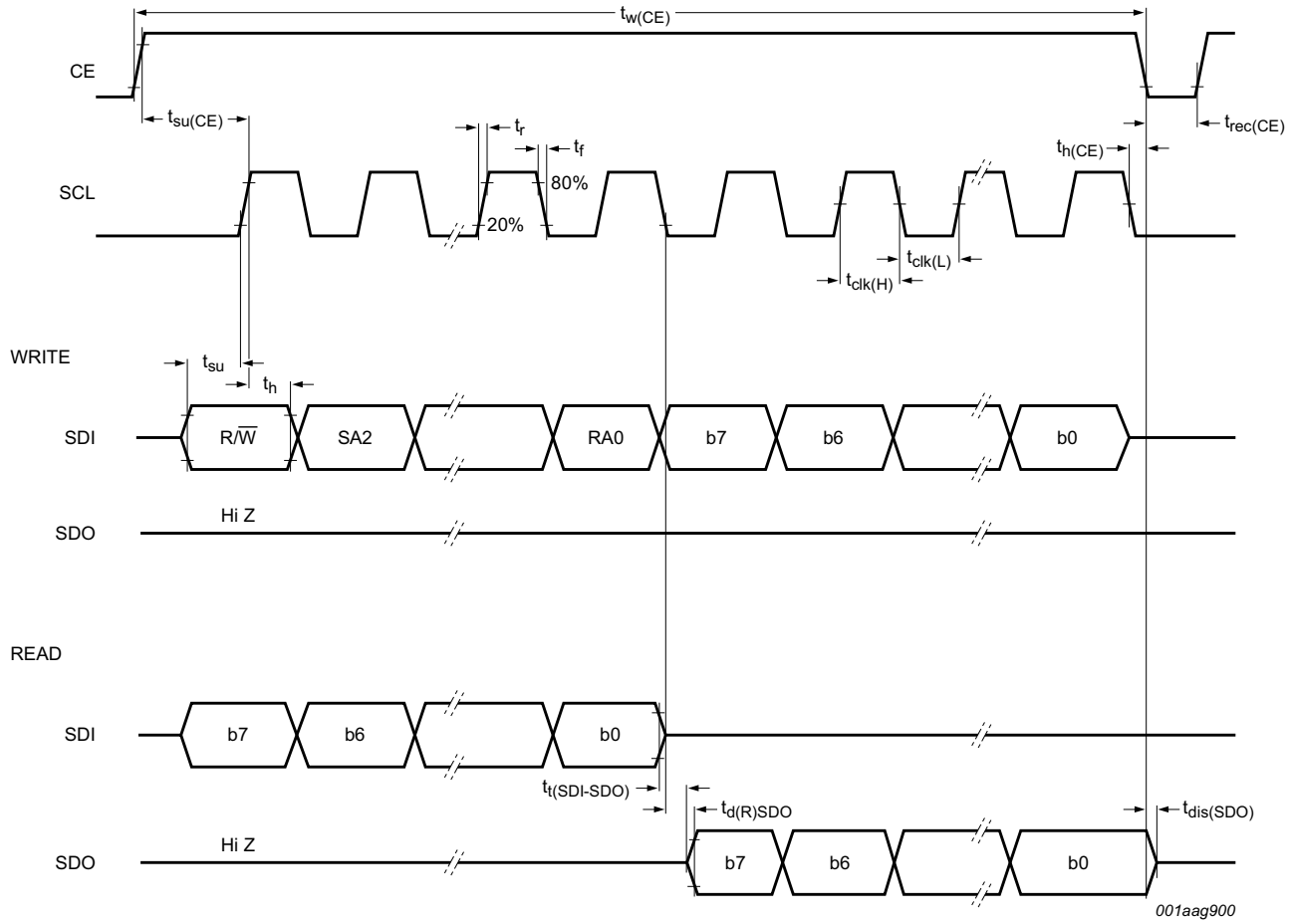


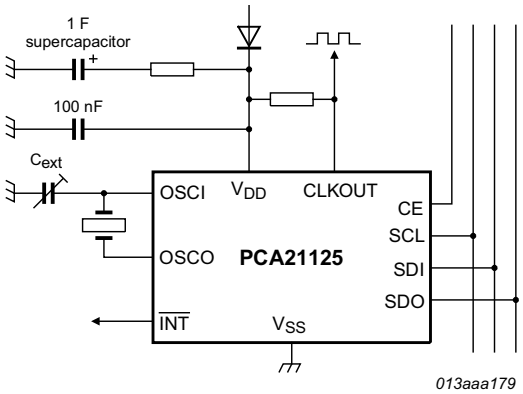
Fig 25. SPI interface timing

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

14. Application information

14.1 Application diagram



The 1 farad capacitor is used as a standby and back-up supply. With the RTC in its minimum power configuration, i.e., timer off and CLKOUT off, the RTC can operate for several weeks.

Fig 26. Application diagram

14.2 Quartz frequency adjustment

1. Method 1: fixed OSCI capacitor

   A fixed capacitor can be used whose value can be determined by evaluating the average capacitance necessary for the application layout; see Figure 26. The frequency is best measured via the 32.768 kHz signal at pin CLKOUT available after power-on. The frequency tolerance depends on the quartz crystal tolerance, the capacitor tolerance and the device-to-device tolerance (on average $\pm 5 \times 10^{-6}$). An average deviation of ± 5 minutes per year can easily be achieved.

2. Method 2: OSCI trimmer

   Fast setting of a trimmer is possible using the 32.768 kHz signal at pin CLKOUT available after power-on.

3. Method 3: OSCO output

   Direct measurement of OSCO output (accounting for test probe capacitance).

15. Test information

15.1 Quality information

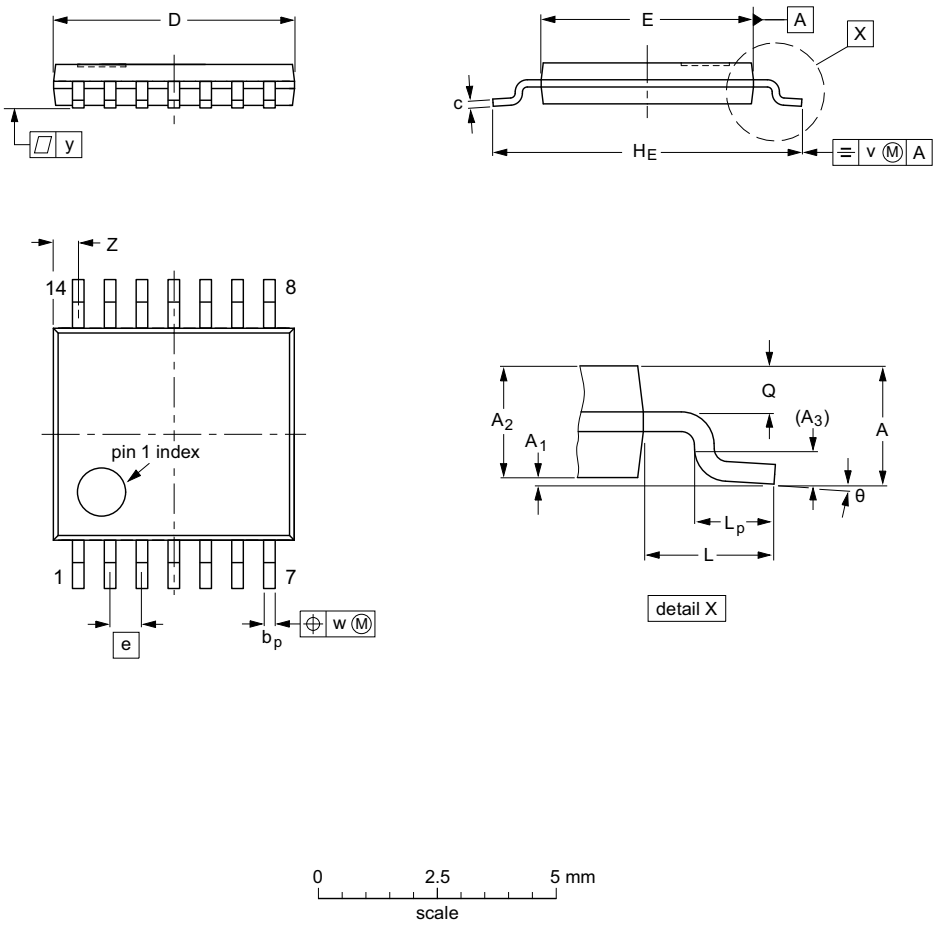
This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

16. Package outline

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm **SOT402-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.72 0.38	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT402-1		MO-153				~~99-12-27~~ 03-02-18

Fig 27. Package outline SOT402-1 (TSSOP14)

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

17. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling Metal-Oxide Semiconductor (MOS) devices ensure that all normal precautions are taken as described in *JESD625-A*, *IEC 61340-5* or equivalent standards.

18. Packing information

18.1 Tape and reel information

For tape and reel packing information, see Ref. 10 “SOT402-1_118” on page 43.

19. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 “Surface mount reflow soldering description”*.

19.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

19.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

19.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

19.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 28) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 44 and 45

Table 44. SnPb eutectic process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 45. Lead-free process (from J-STD-020D)

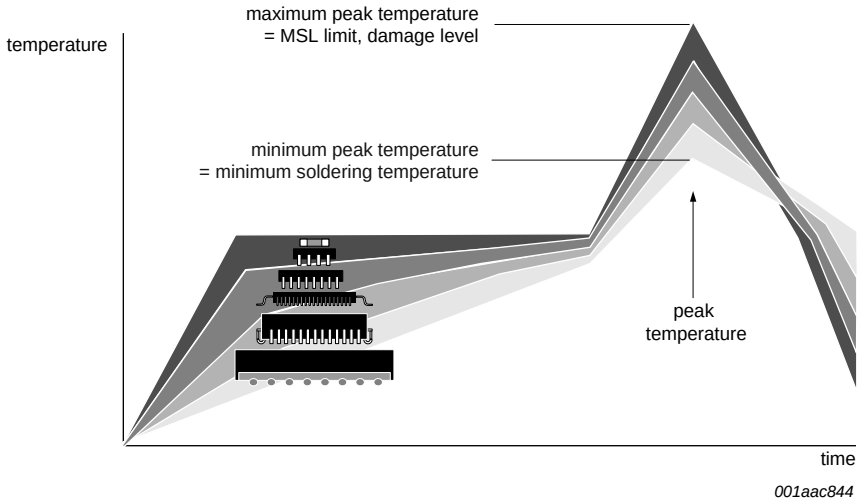
Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 28.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.



MSL: Moisture Sensitivity Level

Fig 28. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

20. Appendix

20.1 Real-Time Clock selection

Table 46. Selection of Real-Time Clocks

Type name	Alarm, Timer, Watchdog	Interrupt output	Interface	I_{DD}, typical (nA)	Battery backup	Timestamp, tamper input	AEC-Q100 compliant	Special features	Packages
PCF8563	X	1	I^2C	250	-	-	-	-	SO8, TSSOP8, HVSON10
PCF8564A	X	1	I^2C	250	-	-	-	integrated oscillator caps	WLCSP
PCA8565	X	1	I^2C	600	-	-	grade 1	high robustness, T_{amb}= −40 °C to 125 °C	TSSOP8, HVSON10
PCA8565A	X	1	I^2C	600	-	-	-	integrated oscillator caps, T_{amb}= −40 °C to 125 °C	WLCSP
PCF85063	-	1	I^2C	220	-	-	-	basic functions only, no alarm	HXSON8
PCF85063A	X	1	I^2C	220	-	-	-	tiny package	SO8, DFN2626-10
PCF85063B	X	1	SPI	220	-	-	-	tiny package	DFN2626-10
PCF85263A	X	2	I^2C	230	X	X	-	time stamp, battery backup, stopwatch $^1/_{100}$ s	SO8, TSSOP10, TSSOP8, DFN2626-10
PCF85263B	X	2	SPI	230	X	X	-	time stamp, battery backup, stopwatch $^1/_{100}$s	TSSOP10, DFN2626-10
PCF85363A	X	2	I^2C	230	X	X	-	time stamp, battery backup, stopwatch $^1/_{100}$s, 64 Byte RAM	TSSOP10, DFN2626-10
PCF85363B	X	2	SPI	230	X	X	-	time stamp, battery backup, stopwatch $^1/_{100}$s, 64 Byte RAM	TSSOP10, DFN2626-10
PCF8523	X	2	I^2C	150	X	-	-	lowest power 150 nA in operation, FM+ 1 MHz	SO8, HVSON8, TSSOP14, WLCSP
PCF2123	X	1	SPI	100	-	-	-	lowest power 100 nA in operation	TSSOP14, HVQFN16
PCF2127	X	1	I^2C and SPI	500	X	X	-	temperature compensated, quartz built in, calibrated, 512 Byte RAM	SO16

PCA21125

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

Table 46. Selection of Real-Time Clocks *...continued*

Type name	Alarm, Timer, Watchdog	Interrupt output	Interface	I_{DD}, typical (nA)	Battery backup	Timestamp, tamper input	AEC-Q100 compliant	Special features	Packages
PCF2127A	X	1	I^2C and SPI	500	X	X	-	temperature compensated, quartz built in, calibrated, 512 Byte RAM	SO20
PCF2129	X	1	I^2C and SPI	500	X	X	-	temperature compensated, quartz built in, calibrated	SO16
PCF2129A	X	1	I^2C and SPI	500	X	X	-	temperature compensated, quartz built in, calibrated	SO20
PCA2129	X	1	I^2C and SPI	500	X	X	grade 3	temperature compensated, quartz built in, calibrated	SO16
PCA21125	X	1	SPI	820	-	-	grade 1	high robustness, T_{amb}= −40 °C to 125 °C	TSSOP14

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

21. Abbreviations

Table 47. Abbreviations

Acronym	Description
AEC	Automotive Electronics Council
AM	Ante Meridiem
BCD	Binary Coded Decimal
CDM	Charged-Device Model
CMOS	Complementary Metal Oxide Semiconductor
HBM	Human Body Model
IC	Integrated Circuit
MM	Machine Model
MOS	Metal Oxide Semiconductor
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
PM	Post Meridiem
POR	Power-On Reset
RC	Resistance-Capacitance
RTC	Real-Time Clock
SMD	Surface Mount Device
SPI	Serial Peripheral Interface

22. References

[1] **AN10365 —** Surface mount reflow soldering description

[2] **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[3] **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[4] **IPC/JEDEC J-STD-020D —** Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

[5] **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[6] **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[7] **JESD22-C101 —** Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

[8] **JESD78 —** IC Latch-Up Test

[9] **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10] **SOT402-1_118 —** TSSOP14; Reel pack; SMD, 13", packing information

[11] **UM10569 —** Store and transport requirements

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

23. Revision history

Table 48. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA21125 v.2	20141125	Product data sheet	-	PCA21125 v.1
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Corrected delay time of first increment of the time circuits • Added C_{OSCO} value in Table 42 • Added Section 18.1 and Section 20.1 • Fixed typos			
PCA21125 v.1	20091116	Product data sheet	-	-

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

24. Legal information

24.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

24.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

24.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

24.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

25. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

26. Tables

Table 1. Ordering information 2
Table 2. Ordering options 2
Table 3. Marking codes 2
Table 4. Pin description 4
Table 5. Register overview 6
Table 6. Control_1 - control and status register 1 (address 00h) bit description 7
Table 7. Control_2 - control and status register 2 (address 01h) bit description 7
Table 8. Seconds - seconds and clock integrity status register (address 02h) bit description 8
Table 9. Seconds coded in BCD format 8
Table 10. Minutes - minutes register (address 03h) bit description 8
Table 11. Hours - hours register (address 04h) bit description 9
Table 12. Days - days register (address 05h) bit description 9
Table 13. Weekdays - weekdays register (address 06h) bit description 9
Table 14. Weekday assignments 9
Table 15. Months - months register (address 07h) bit description 10
Table 16. Month assignments in BCD format 10
Table 17. Years - years register (08h) bit description 10
Table 18. Minute_alarm - minute alarm register (address 09h) bit description 12
Table 19. Hour_alarm - hour alarm register (address 0Ah) bit description 12
Table 20. Day_alarm - day alarm register (address 0Bh) bit description 13
Table 21. Weekday_alarm - weekday alarm register (address 0Ch) bit description 13
Table 22. Flag location in register Control_2 14
Table 23. Example to clear only AF (bit 3) in register Control_2 14
Table 24. CLKOUT_control - CLKOUT control register (address 0Dh) bit description 15
Table 25. CLKOUT frequency selection 15
Table 26. Timer_control - timer control register (address 0Eh) bit description 16
Table 27. Countdown_timer - countdown timer register (address 0Fh) bit description 16
Table 28. Effect of bits MI and SI on $\overline{INT}$ generation 16
Table 29. Effect of bits MI and SI on bit MSF 16
Table 30. CTD[1:0] for timer frequency selection and countdown timer durations 17
Table 31. First period delay for timer counter value T . . . 18
Table 32. Flag location in register Control_2 19
Table 33. Example to clear only TF (bit 2) in register Control_2 19
Table 34. Example to clear only MSF (bit 5) in register Control_2 19
Table 35. Example to clear both TF and MSF (bits 2 and 5) in register Control_2 19
Table 36. $\overline{INT}$ operation (bit TI_TP = 1) 21
Table 37. Example: first increment of time circuits after STOP release 24
Table 38. Register reset values 26
Table 39. Serial interface 27
Table 40. Command byte definition 28
Table 41. Limiting values 31
Table 42. Static characteristics 32
Table 43. Dynamic characteristics 34
Table 44. SnPb eutectic process (from J-STD-020D) . . . 39
Table 45. Lead-free process (from J-STD-020D) 39
Table 46. Selection of Real-Time Clocks 41
Table 47. Abbreviations 43
Table 48. Revision history 44

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

27. Figures

Fig 1. Block diagram of PCA21125 3
Fig 2. Pin configuration for TSSOP14 4
Fig 3. Data flow of the time function. 11
Fig 4. Access time for read/write operations 11
Fig 5. Alarm function block diagram. 13
Fig 6. Alarm flag timing 14
Fig 7. INT example for bits SI and MI 17
Fig 8. General countdown timer behavior 18
Fig 9. Interrupt scheme 20
Fig 10. Example of shortening the INT pulse by clearing the MSF flag 21
Fig 11. Example of shortening the INT pulse by clearing the TF flag 22
Fig 12. AF timing 22
Fig 13. STOP bit functional diagram 23
Fig 14. STOP bit release timing 24
Fig 15. Reset system 25
Fig 16. Power-On Reset (POR) 25
Fig 17. POR override sequence 26
Fig 18. SDI, SDO configurations 27
Fig 19. Data transfer overview 27
Fig 20. Command byte 28
Fig 21. Serial bus write example 28
Fig 22. Serial bus read example 29
Fig 23. Interface watchdog timer 29
Fig 24. Device diode protection diagram 30
Fig 25. SPI interface timing 35
Fig 26. Application diagram 36
Fig 27. Package outline SOT402-1 (TSSOP14) 37
Fig 28. Temperature profiles for large and small components 40

All information provided in this document is subject to legal disclaimers.

© NXP Semiconductors N.V. 2014. All rights reserved.

28. Contents

1 General description 1
2 Features and benefits 1
3 Applications 1
4 Ordering information 2
4.1 Ordering options 2
5 Marking 2
6 Block diagram 3
7 Pinning information 4
7.1 Pinning 4
7.2 Pin description 4
8 Functional description 5
8.1 Register overview 6
8.2 Control and status registers 7
8.2.1 Register Control_1 7
8.2.2 Register Control_2 7
8.3 Time and date registers 8
8.3.1 Register Seconds 8
8.3.2 Register Minutes 8
8.3.3 Register Hours 9
8.3.4 Register Days 9
8.3.5 Register Weekdays 9
8.3.6 Register Months 10
8.3.7 Register Years 10
8.3.8 Setting and reading the time 11
8.4 Alarm registers 12
8.4.1 Register Minute_alarm 12
8.4.2 Register Hour_alarm 12
8.4.3 Register Day_alarm 13
8.4.4 Register Weekday_alarm 13
8.4.5 Alarm flag 13
8.5 Register CLKOUT_control and clock output . . 15
8.6 Timer registers 15
8.6.1 Second and minute interrupt 16
8.6.2 Countdown timer function 17
8.6.3 Timer flags 19
8.7 Interrupt output 20
8.7.1 Minute and second interrupts 20
8.7.2 Countdown timer interrupts 21
8.7.3 Alarm interrupts 22
8.8 External clock test mode 22
8.9 STOP bit function 23
8.10 Reset 25
8.10.1 POR override 26
8.11 4-line SPI-bus 27
8.11.1 Interface watchdog timer 29
9 Internal circuitry 30
10 Safety notes 30
11 Limiting values 31
12 Static characteristics 32
13 Dynamic characteristics 34
14 Application information 36
14.1 Application diagram 36
14.2 Quartz frequency adjustment 36
15 Test information 36
15.1 Quality information 36
16 Package outline 37
17 Handling information 38
18 Packing information 38
18.1 Tape and reel information 38
19 Soldering of SMD packages 38
19.1 Introduction to soldering 38
19.2 Wave and reflow soldering 38
19.3 Wave soldering 39
19.4 Reflow soldering 39
20 Appendix 41
20.1 Real-Time Clock selection 41
21 Abbreviations 43
22 References 43
23 Revision history 44
24 Legal information 45
24.1 Data sheet status 45
24.2 Definitions 45
24.3 Disclaimers 45
24.4 Trademarks 46
25 Contact information 46
26 Tables 47
27 Figures 48
28 Contents 49

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP Semiconductors N.V. 2014. All rights reserved.

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 25 November 2014
Document identifier: PCA21125