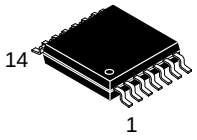
Hex Schmitt Inverter

74VHC14



TSSOP−14 WB
CASE 948G

General Description

The VHC14 is an advanced high speed CMOS Hex Schmitt Inverter fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. Pin configuration and function are the same as the VHC04 but the inputs have hysteresis between the positive−going and negative−going input thresholds, which are capable of transforming slowly changing input signals into sharply defined, jitter−free output signals, thus providing greater noise margin than conventional inverters.

An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: t_{PD} = 5.5 ns (Typ.) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 2 μA (Max.) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is Provided on All Inputs
- Low Noise: V_{OLP} = 0.8 V (Max.)
- Pin and Function Compatible with 74HC14
- Pb−Free, Halogen Free/BFR Free and RoHS Compliant

Logic Symbol

IEEE/IEC

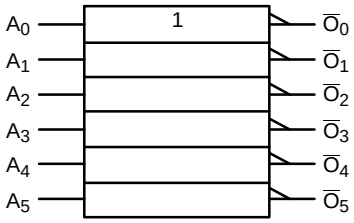
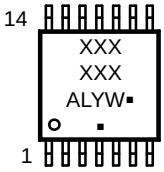


Figure 1. Logic Symbol

TRUTH TABLE

A	O
L	H
H	L

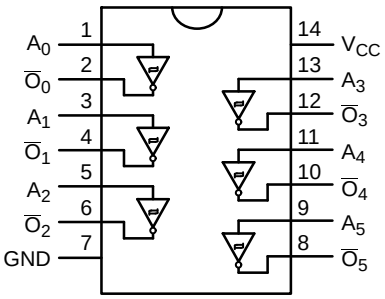
MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



PIN DESCRIPTION

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	−0.5 to +6.5	V
V_{IN}	DC Input Voltage	−0.5 to +6.5	V
V_{OUT}	DC Output Voltage Active Mode (High or Low State) Tristate Mode (Note 1) Power−Off Mode (V_{CC} = 0 V)	 −0.5 to V_{CC} + 0.5 −0.5 to +6.5 −0.5 to +6.5	V
I_{IN}	DC Input Current, Per Pin	±20	mA
I_{OUT}	DC Output Current, Per Pin	±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	±50	mA
I_{IK}	Input Clamp Current	−20	mA
I_{OK}	Output Clamp Current	±20	mA
T_{STG}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 s	260	°C
T_J	Junction Temperature Under Bias	+150	°C
θ_{JA}	Thermal Resistance (Note 2)	150	°C/W
P_D	Power Dissipation in Still Air at 25°C	833	mW
V_{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	 2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage	2.0	5.5	V
V_{IN}	DC Input Voltage (Note 4)	0	5.5	V
V_{OUT}	DC Output Voltage (Note 4) Active Mode (High or Low State) Tristate Mode Power−Off Mode (V_{CC} = 0 V)	 0 0 0	 V_{CC} 5.5 5.5	V
T_A	Operating Temperature	−40	+85	°C
t_r, t_f	Input Rise or Fall Rate	0	No Limit	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = 25°C			T_A = −40°C to +85°C		Unit
					Min	Typ	Max	Min	Max	
V_P	Positive Threshold Voltage	3.0			–	–	2.20	–	2.20	V
		4.5			–	–	3.15	–	3.15	
		5.5			–	–	3.85	–	3.85	
V_N	Negative Threshold Voltage	3.0			0.90	–	–	0.90	–	V
		4.5			1.35	–	–	1.35	–	
		5.5			1.65	–	–	1.65	–	
V_H	Hysteresis Voltage	3.0			0.30	–	1.20	0.30	1.20	V
		4.5			0.40	–	1.40	0.40	1.40	
		5.5			0.50	–	1.60	0.50	1.60	
V_{OH}	HIGH Level Output Voltage	2.0	V_{IN} = V_{IL}	I_{OH} = −50 μA	1.9	2.0	–	1.9	–	V
		3.0			2.9	3.0	–	2.9	–	
		4.5			4.4	4.5	–	4.4	–	
		3.0		I_{OH} = −4 mA	2.58	–	–	2.48	–	
		4.5		I_{OH} = −8 mA	3.94	–	–	3.80	–	
V_{OL}	LOW Level Output Voltage	2.0	V_{IN} = V_{IH}	I_{OL} = 50 μA	–	0.0	0.1	–	0.1	V
		3.0			–	0.0	0.1	–	0.1	
		4.5			–	0.0	0.1	–	0.1	
		3.0		I_{OL} = 4 mA	–	–	0.36	–	0.44	
		4.5		I_{OL} = 8 mA	–	–	0.36	–	0.44	
I_{IN}	Input Leakage Current	0−5.5	V_{IN} = 5.5 V or GND		–	–	±0.1	–	±1.0	μA
I_{CC}	Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND		–	–	2.0	–	20.0	μA

NOISE CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C		Unit
				Typ	Max	
V_{OLP}	Quiet Output Maximum Dynamic V_{OL}	5.0	C_L = 50 pF	0.4	0.8	V
V_{OLV}	Quiet Output Minimum Dynamic V_{OL}	5.0	C_L = 50 pF	–0.4	0.8	V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage	5.0	C_L = 50 pF	–	3.5	V
V_{ILD}	Maximum LOW Level Dynamic Input Voltage	5.0	C_L = 50 pF	–	1.5	V

5. Parameter guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C			T_A = −40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Time	3.3 ±0.3	C_L = 15 pF	–	8.3	12.8	1.0	15.0	ns
			C_L = 50 pF	–	10.8	16.3	1.0	18.5	
		5.0 ±0.5	C_L = 15 pF	–	5.5	8.6	1.0	10.0	ns
			C_L = 50 pF	–	7.0	10.6	1.0	12.0	
C_{IN}	Input Capacitance		V_{CC} = Open	–	4	10	–	10	pF
C_{PD}	Power Dissipation Capacitance		(Note 6)	–	21	–	–	–	pF

6. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (Opr) = $C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$ / 6 (per Gate)

ORDERING INFORMATION

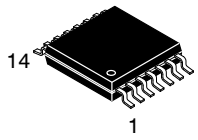
Device Order Number	Top Marking	Package Type	Shipping†
74VHC14MTCX	VHC 14	TSSOP−14 WB (Pb−Free, Halide Free)	2,500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

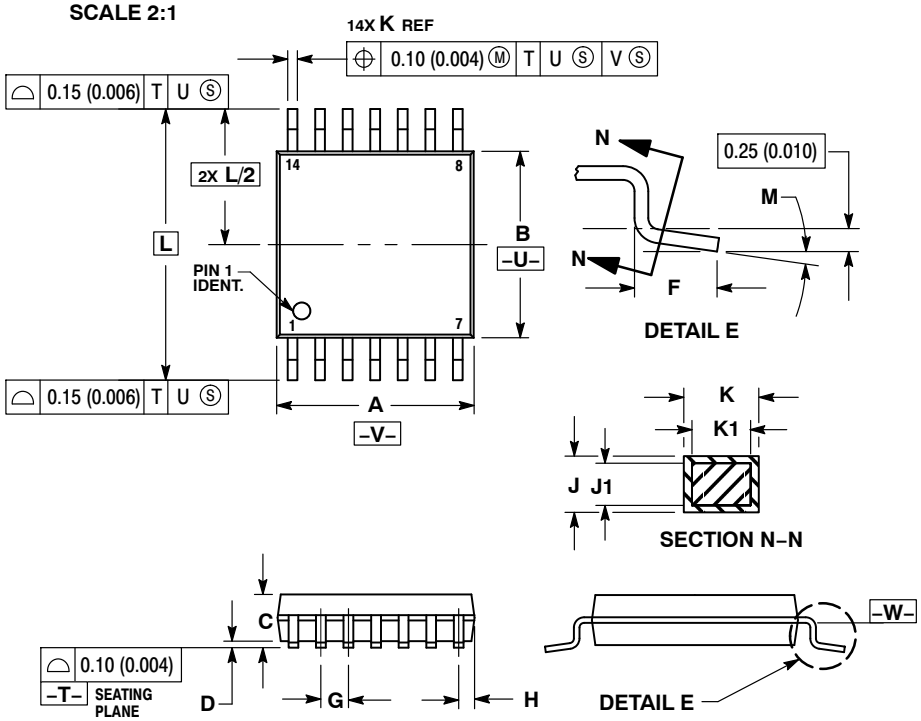
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016



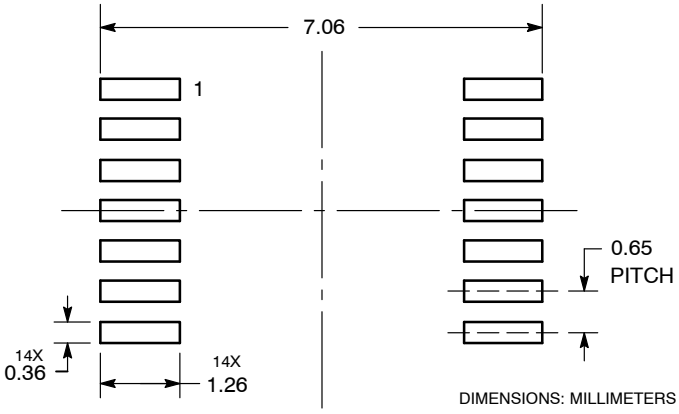
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

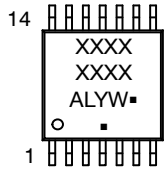
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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