ADT7467

dbCOOL Remote Thermal Monitor and Fan Controller

The ADT7467 dbCOOL controller is a thermal monitor and multiple PWM fan controller for noise-sensitive or power-sensitive applications requiring active system cooling. The ADT7467 can drive a fan using either a low or high frequency drive signal, monitor the temperature of up to two remote sensor diodes plus its own internal temperature, and measure and control the speed of up to four fans so that they operate at the lowest possible speed for minimum acoustic noise.

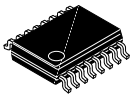
The automatic fan speed control loop optimizes fan speed for a given temperature. A unique dynamic T_{MIN} control mode enables the system thermals/acoustics to be intelligently managed. The effectiveness of the system's thermal solution can be monitored using the $\overline{\text{THERM}}$ input. The ADT7467 also provides critical thermal protection to the system using the bidirectional $\overline{\text{THERM}}$ pin as an output to prevent system or component overheating.

Features

- Controls and Monitors up to 4 Fans
- High and Low Frequency Fan Drive Signal
- 1 On-chip and 2 Remote Temperature Sensors
- Series Resistance Cancellation on the Remote Channel
- Extended Temperature Measurement Range, up to 191°C
- Dynamic T_{MIN} Control Mode Intelligently Optimizes System Acoustics
- Automatic Fan Speed Control Mode Manages System Cooling based on Measured Temperature
- Enhanced Acoustic Mode Dramatically Reduces User Perception of Changing Fan Speeds
- Thermal Protection Feature via $\overline{\text{THERM}}$ Output
- Monitors Performance Impact of Intel® Pentium® 4 Processor
- Thermal Control Circuit via $\overline{\text{THERM}}$ Input
- 2-wire, 3-wire, and 4-wire Fan Speed Measurement
- Limit Comparison of All Monitored Values
- Meets SMBus 2.0 Electrical Specifications (Fully SMBus 1.1 Compliant)
- This Device is Pb-Free and is RoHS Compliant*
- Halide-Free Packages are Available

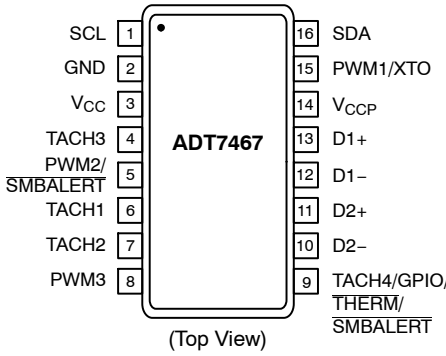
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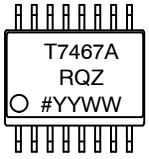
QSOP−16
CASE 492

PIN ASSIGNMENT



(Top View)

MARKING DIAGRAM



T7467ARQZ	= Specific Device Code
#	= Pb-Free Package
YY	= Date Code
WW	= Work Week

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 70 of this data sheet.

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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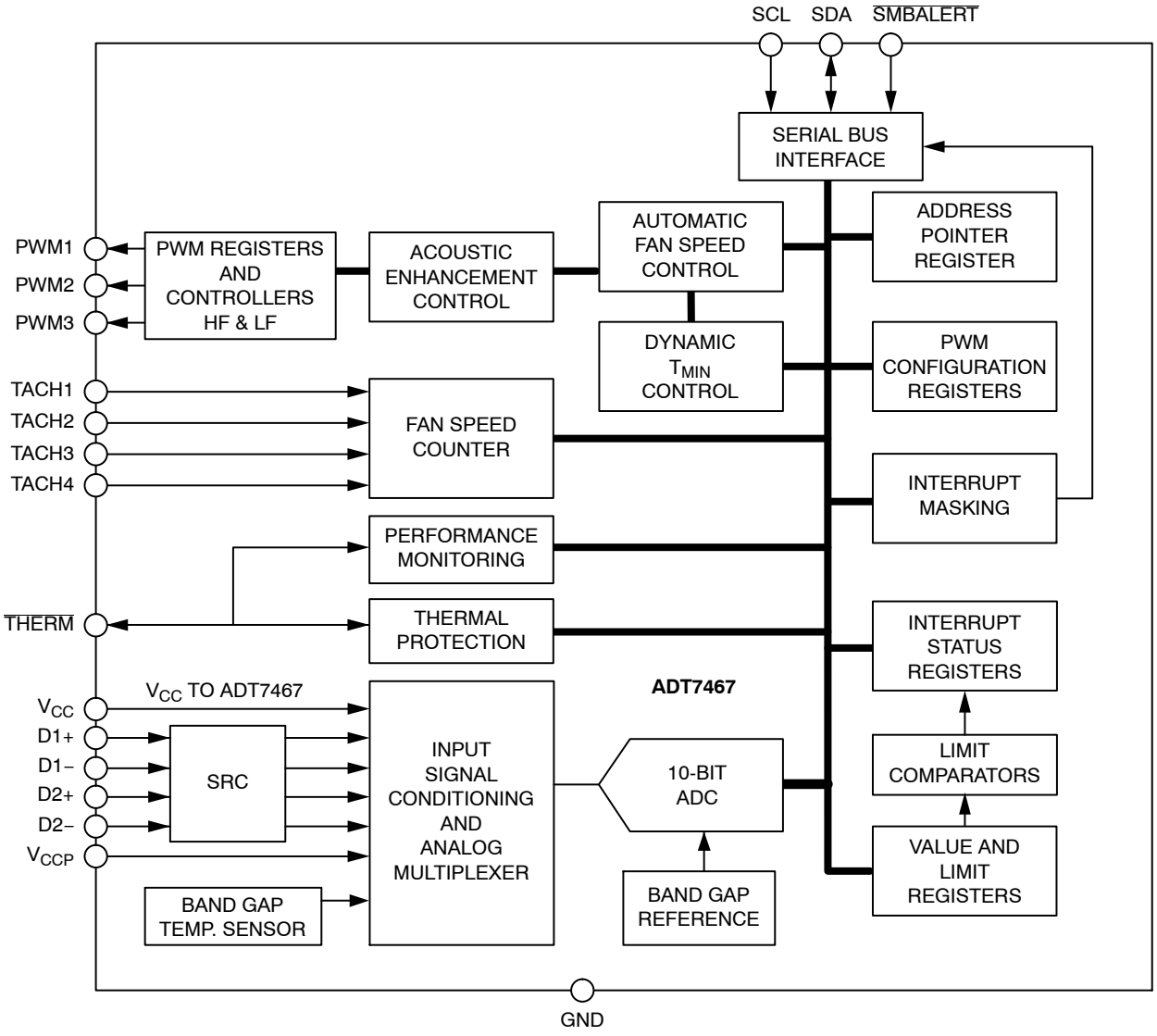


Figure 1. Functional Block Diagram

Table 1. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V_{CC})	5.5	V
Voltage on Any Input or Output Pin	−0.3 to +6.5	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature ($T_{J\ MAX}$)	150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature, Soldering IR Reflow Peak Temperature For Pb-Free Models Lead Temperature (Soldering, 10 sec)	 220 260 300	°C
ESD Rating	1,000	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

WARNING: Electrostatic Sensitive Device − Do not open packages or handle except at a static-free workstation.

Table 2. PIN FUNCTION DESCRIPTIONS

Pin No.	Mnemonic	Description
1	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pull-up.
2	GND	Ground Pin for the ADT7467.
3	V_{CC}	Power Supply. Can be powered by 3.3 V standby if monitoring in low power states is required. V_{CC} is also monitored through this pin. The ADT7467 can also be powered from a 5 V supply. Setting Bit 7 of Configuration Register 1 (0x40) rescales the V_{CC} input attenuators to correctly measure a 5 V supply.
4	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3. Can be reconfigured as an analog input (AIN3) to measure the speed of 2-wire fans (low frequency mode only).
5	PWM2 $\overline{\text{SMBALERT}}$	Digital Output (Open Drain). Requires 10 kΩ typical pull-up. Pulse width modulated output to control the speed of Fan 2. Can be configured as a high or low frequency drive. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
6	TACH1	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 1. Can be reconfigured as an analog input (AIN1) to measure the speed of 2-wire fans (low frequency mode only).
7	TACH2	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 2. Can be reconfigured as an analog input (AIN2) to measure the speed of 2-wire fans (low frequency mode only).
8	PWM3	Digital I/O (Open Drain). Pulse width modulated output to control the speed of Fan 3 and Fan 4. Requires 10 kΩ typical pull-up. Can be configured as a high or low frequency drive.
9	TACH4 GPIO $\overline{\text{THERM}}$ $\overline{\text{SMBALERT}}$	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 4. Can be reconfigured as an analog input (AIN4) to measure the speed of 2-wire fans (low frequency mode only). General-Purpose Open-Drain Digital I/O. Alternatively, the pin can be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin, which can be used to time and monitor assertions on the $\overline{\text{THERM}}$ input. For example, the pin can be connected to the $\overline{\text{PROCHOT}}$ output of an Intel® Pentium® 4 processor or to the output of a trip point temperature sensor. This pin can be used as an output to signal overtemperature conditions. Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out-of-limit conditions.
10	D2−	Cathode Connection to Second Thermal Diode.
11	D2+	Anode Connection to Second Thermal Diode.
12	D1−	Cathode Connection to First Thermal Diode.
13	D1+	Anode Connection to First Thermal Diode.
14	V_{CCP}	Analog Input. Monitors processor core voltage (0 V to 3 V).
15	PWM1 XTO	Digital Output (Open Drain). Pulse width modulated output to control the speed of Fan 1. Requires 10 kΩ typical pull-up. Also functions as the output from the XNOR tree in XNOR test mode.
16	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires 10 kΩ typical pull-up.

Table 3. ELECTRICAL SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Note 1)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY					
Supply Voltage		3.0	3.3	5.5	V
Supply Current, I_{CC}	Interface Inactive, ADC Active Standby Mode	– –	– –	3 20	mA μA
TEMPERATURE-TO-DIGITAL CONVERTER					
Local Sensor Accuracy	0°C ≤ T_A ≤ 70°C −40°C ≤ T_A ≤ +100°C −40°C ≤ T_A ≤ +120°C	– −3.5 −4	– – –	±1.5 +2 +2	°C
Resolution		–	0.25	–	°C
Remote Diode Sensor Accuracy	0°C ≤ T_A ≤ 70°C; 0°C ≤ T_D ≤ 120°C 0°C ≤ T_A ≤ 105°C; 0°C ≤ T_D ≤ 120°C −40°C ≤ T_A ≤ +120°C; 0°C ≤ T_D ≤ +120°C	– −3.5 −4.5	±0.5 – –	±1.5 +2 +2	°C
Resolution		–	0.25	–	°C
Remote Sensor Source Current	First Current Second Current Third Current	– – –	6 36 96	– – –	μA
ANALOG-TO-DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error (TUE)		–	–	±1.5	%
Differential Nonlinearity (DNL)	8 Bits	–	–	±1	LSB
Power Supply Sensitivity		–	±0.1	–	%/V
Conversion Time (Voltage Input)	Averaging Enabled	–	11	–	ms
Conversion Time (Local Temperature)	Averaging Enabled	–	12	–	ms
Conversion Time (Remote Temperature)	Averaging Enabled	–	38	–	ms
Total Monitoring Cycle Time	Averaging Enabled Averaging Disabled	– –	145 19	– –	ms
Input Resistance	For V_{CC} Channel For All Channels other than V_{CC}	40 80	80 140	100 200	kΩ
FAN RPM-TO-DIGITAL CONVERTER					
Accuracy	0°C ≤ T_A ≤ 70°C, 3.3 V −40°C ≤ T_A ≤ +120°C, 3.3 V −40°C ≤ T_A ≤ +120°C, 5.5 V	– – –	– – –	±5 ±7 ±10	%
Full-scale Count		–	–	65,535	
Nominal Input RPM	Fan Count = 0xBFFF Fan Count = 0x3FFF Fan Count = 0x0438 Fan Count = 0x021C	– – – –	109 329 5000 10,000	– – – –	RPM
Internal Clock Frequency	0°C ≤ T_A ≤ 70°C, V_{CC} = 3.3 V −40°C ≤ T_A ≤ +120°C, V_{CC} = 3.3 V	85.5 83.7	90 90	94.5 96.3	kHz
Internal Clock Frequency	−40°C ≤ T_A ≤ +120°C, V_{CC} = 5.5 V	81	90	99	kHz
OPEN-DRAIN DIGITAL OUTPUTS, PWM1 to PWM3, XTO					
Current Sink, I_{OL}		–	–	8.0	mA
Output Low Voltage, V_{OL}	I_{OUT} = −8.0 mA, V_{CC} = 3.3 V	–	–	0.4	V
High Level Output Current, I_{OH}	V_{OUT} = V_{CC}	–	0.1	1.0	μA
OPEN-DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}	I_{OUT} = −4.0 mA, V_{CC} = 3.3 V	–	–	0.4	V
High Level Output Current, I_{OH}	V_{OUT} = V_{CC}	–	0.1	1.0	μA

Table 3. ELECTRICAL SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted.) (Note 1)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
SMBus DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}		2.0	–	–	V
Input Low Voltage, V_{IL}		–	–	0.4	V
Hysteresis		–	500	–	mV
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)					
Input High Voltage, V_{IH}	Maximum Input Voltage	2.0 –	– –	– 5.5	V
Input Low Voltage, V_{IL}	Minimum Input Voltage	– –0.3	– –	0.8 –	V
Hysteresis		–	0.5	–	V p–p
DIGITAL INPUT LOGIC LEVELS ($\overline{THERM}$) ADTL+					
Input High Voltage, V_{IH}		–	0.75 × V_{CCP}	–	V
Input Low Voltage, V_{IL}		–	–	0.4	V
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	$V_{IN} = V_{CC}$	–1	–	–	μA
Input Low Current, I_{IL}	$V_{IN} = 0$	–	–	1	μA
Input Capacitance, C_{IN}		–	5	–	pF
SERIAL BUS TIMING					
Clock Frequency, f_{SCLK}		10	–	400	kHz
Glitch Immunity, t_{SW}		–	–	50	ns
Bus Free Time, t_{BUF}		4.7	–	–	μs
Start Setup Time, $t_{SU;\ STA}$		4.7	–	–	μs
Start Hold Time, $t_{HD;\ STA}$		4.0	–	–	μs
SCL Low Time, t_{LOW}		4.7	–	–	μs
SCL High Time, t_{HIGH}		4.0	–	50	μs
SCL, SDA Rise Time, t_r		–	–	1000	ns
SCL, SDA Fall Time, t_f		–	–	300	μs
Data Setup Time, $t_{SU;\ DAT}$		250	–	–	ns
Data Hold Time, $t_{HD;\ DAT}$		300	–	–	ns
Detect Clock Low Timeout, $t_{TIMEOUT}$	Can be Optionally Disabled	15	–	35	ms

1. All voltages are measured with respect to GND, unless otherwise specified. Typicals are at $T_A = 25°C$ and represent the most likely parametric norm. Logic inputs accept input high voltages up to V_{MAX} even when the device is operating down to V_{MIN}. Timing specifications are tested at logic levels of $V_{IL} = 0.8$ V for a falling edge and $V_{IH} = 2.0$ V for a rising edge. SMBus timing specifications are guaranteed by design and are not production tested.

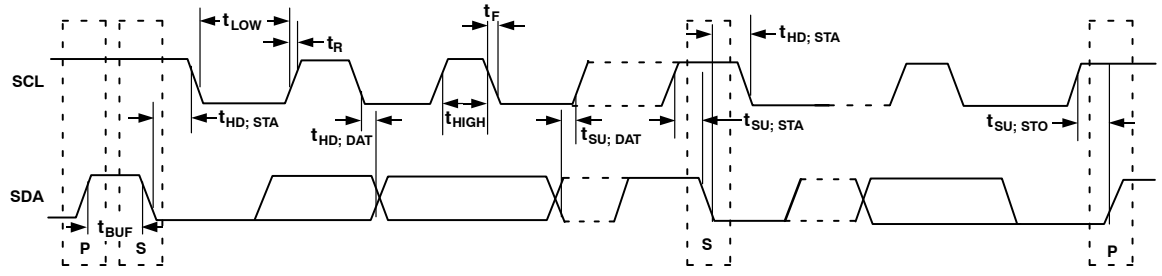


Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

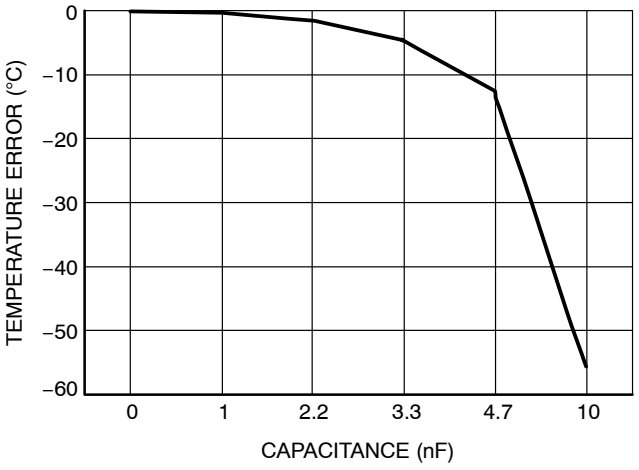


Figure 3. Temperature Error vs. Capacitance Between D+ and D−

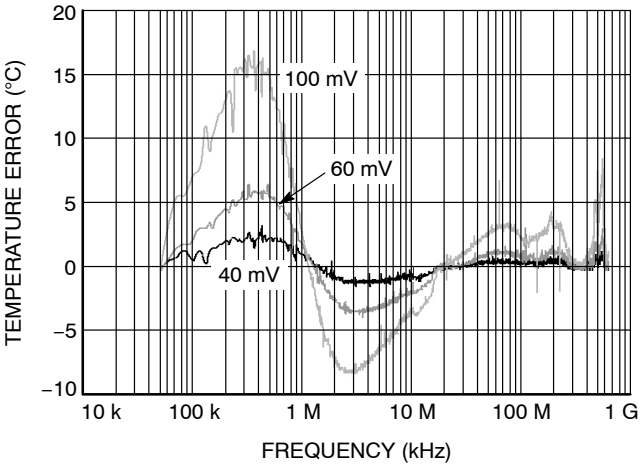


Figure 4. Remote Temperature Error vs. Common-Mode Noise Frequency

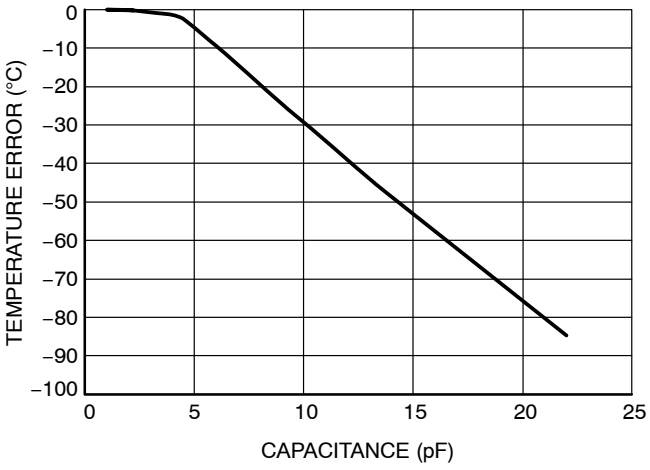


Figure 5. External Temperature Error vs. Capacitance Between D+ and D−

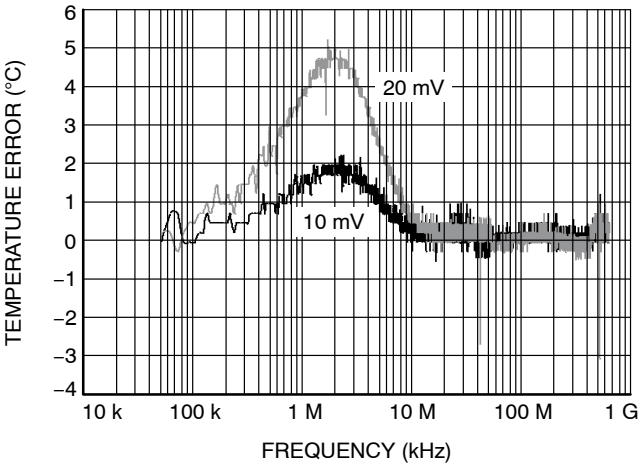


Figure 6. Remote Temperature Error vs. Differential Mode Noise Frequency

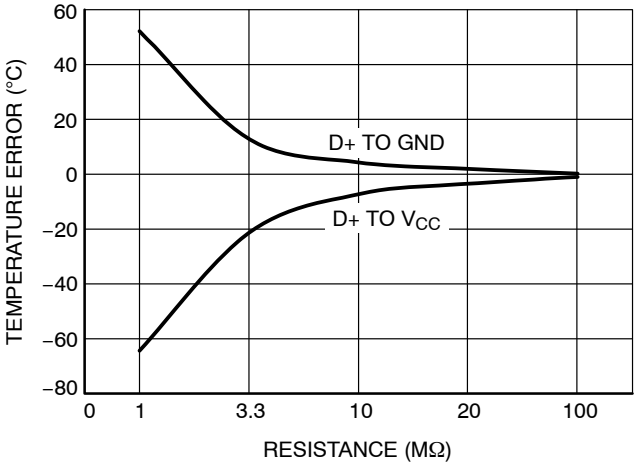


Figure 7. Temperature Error vs. PCB Resistance

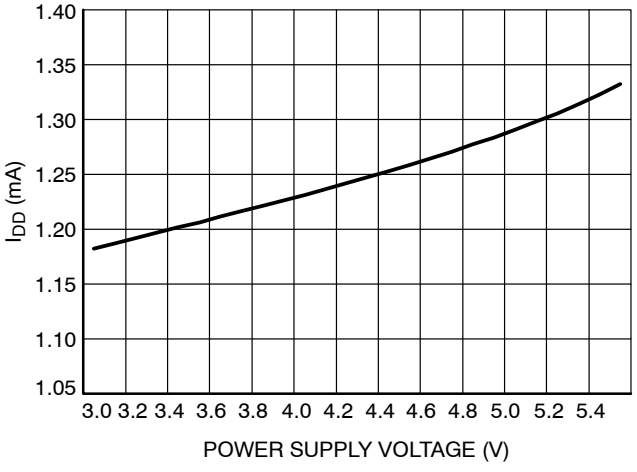


Figure 8. Normal I_{DD} vs. Power Supply

TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

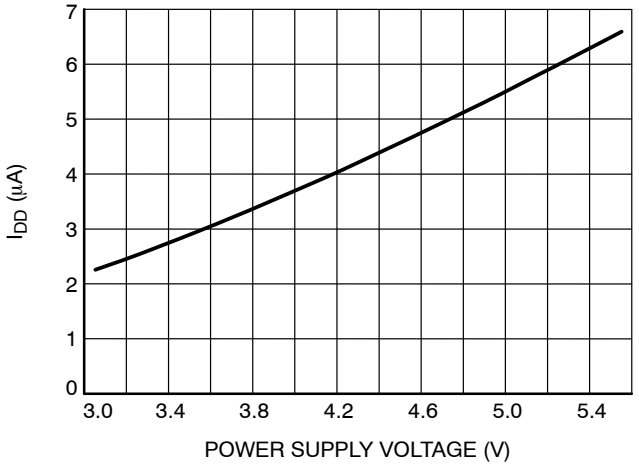


Figure 9. Shutdown I_{DD} vs. Power Supply

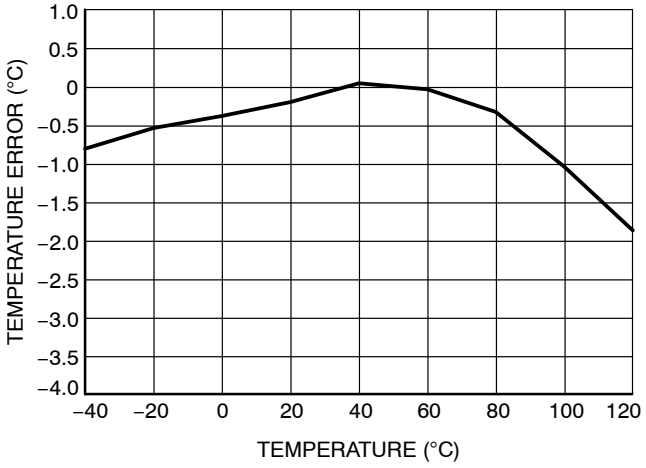


Figure 10. Internal Temperature Error vs. Temperature

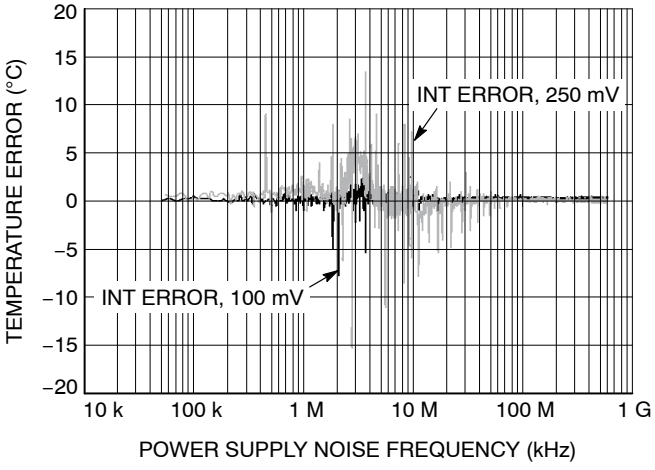


Figure 11. Internal Temperature Error vs. Power Supply Noise Frequency

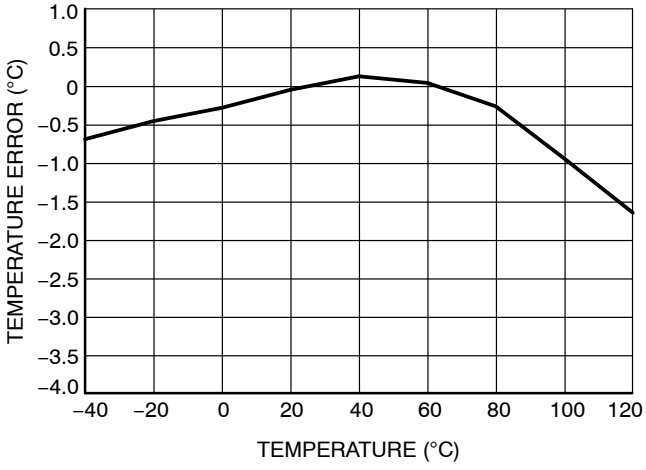


Figure 12. Remote Temperature Error vs. Temperature

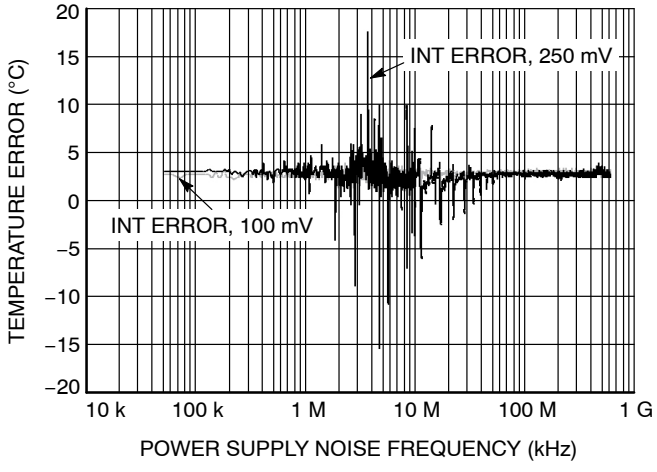


Figure 13. Remote Temperature Error vs. Power Supply Noise Frequency

Product Description

The ADT7467 is a complete thermal monitor and multiple fan controller for systems requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 16) and an input line for the serial clock (Pin 1). All control and programming functions for the ADT7467 are performed over the serial bus. In addition, one of two pins can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out-of-limit conditions.

Comparison between ADT7460 and ADT7467

The ADT7467 is an upgrade from the ADT7460. The ADT7467 and ADT7460 are almost pin and register map compatible. The ADT7467 and ADT7460 have the following differences:

1. On the ADT7467, the PWM drive signals can be configured as either high frequency or low frequency drives. The low frequency option is programmable between 10 Hz and 100 Hz. The high frequency option is 22.5 kHz. On the ADT7460, only the low frequency option is available.
2. Once V_{CC} and V_{CCP} are powered up, monitoring of temperature and fan speeds is enabled on the ADT7467. If V_{CCP} is never powered up, monitoring is enabled when the first SMBus transaction with the ADT7467 is complete. On the ADT7460, the STRT bit in Configuration Register 1 must be set to enable monitoring.
3. The fans are switched off by default upon power-up of the ADT7467. On the ADT7460, the fans run at full speed upon power-up.
   Fail-safe cooling is provided on the ADT7467. If the measured temperature exceeds the $\overline{\text{THERM}}$ limit (100°C), the fans run at full speed.
   Fail-safe cooling is also provided 4.6 sec after V_{CCP} is powered up. The fans operate at full speed if the ADT7467 has not been addressed via the SMBus within 4.6 sec of when the V_{CCP} is powered up. This protects the system in the event that the SMBus fails. The ADT7467 can be programmed at any time, and it behaves as programmed. If V_{CCP} is never powered up, fail-safe cooling is effectively disabled. If V_{CCP} is disabled, writing to the ADT7467 at any time causes the ADT7467 to operate normally.
4. Series resistance cancellation (SRC) is provided on the remote temperature channels on the ADT7467, but not on the ADT7460. SRC automatically cancels linear offset introduced by a series resistance between the thermal diode and the sensor.
5. The ADT7467 has an extended temperature measurement range. The measurement range goes from −64°C to +191°C. On the ADT7460, the measurement range is from −127°C to +127°C. This means that the ADT7467 can measure higher temperatures. The ADT7467 also includes the ADT7460 temperature range; the temperature measurement range can be switched by setting Bit 0 of Configuration Register 5.
6. The ADT7467 maximum fan speed (% duty cycle) in the automatic fan speed control loop can be programmed. The maximum fan speed is 100% duty cycle on the ADT7460 and is not programmable.
7. The offset register in the ADT7467 is programmable up to ±64°C with 0.50°C resolution. The offset register of the ADT7460 is programmable up to ±32°C with 0.25°C resolution.
8. V_{CCP} is monitored on Pin 14 of the ADT7467 and can be used to set the threshold for $\overline{\text{THERM}}$ ($\overline{\text{PROCHOT}}$) (2/3 of V_{CCP}). 2.5 V is monitored on Pin 14 of the ADT7460. The threshold for $\overline{\text{THERM}}$ ($\overline{\text{PROCHOT}}$) is set at V_{IH} = 1.7 V and V_{IL} = 0.8 V on the ADT7460.
9. On the ADT7460, Pin 14 could be reconfigured as $\overline{\text{SMBALERT}}$. This is not available on the ADT7467. $\overline{\text{SMBALERT}}$ can be enabled instead on Pin 9.
10. A GPIO can also be made available on Pin 9 on the ADT7467. This is not available on the ADT7460. Set the GPIO polarity and direction in Configuration Register 5. The GPIO status bit is Bit 5 of Status Register 2 (it is shared with TACH4 and $\overline{\text{THERM}}$ because only one can be enabled at a time).
11. The ADT7460 has three possible SMBus addresses, which are selectable using the address select and address enable pins. The ADT7467 has one SMBus address available at Address 0x2E.

Due to the inclusion of extra functionality, the register map has changed, including an additional configuration register, Configuration Register 5 at Address 0x7C.

Configuration Register 5

Bit 0: If Bit 0 is set to 1, the ADT7467, in terms of temperature, is backward compatible with the ADT7460. Measurements, including T_{MIN} calibration circuit and fan control, work in the range −127°C to +127°C. In addition, care should be taken in reprogramming the temperature limits (T_{MIN}, operating point, $\overline{\text{THERM}}$) to their desired twos complement value, because the power-on default for them is at Offset 64. The extended temperature range is −64°C to 191°C. The default is 1, which is in the −64°C to +191°C temperature range.

Bit 1 = 0 is the high frequency (22.5 kHz) fan drive signal.

Bit 1 = 1 switches the fan drive to low frequency PWM, programmable between 10 Hz and 100 Hz, the same as the ADT7460. The default is 0, or HF PWM.

Bit 2 sets the direction for the GPIO: 0 = input, 1 = output. Bit 3 sets the GPIO polarity: 0 = active low, 1 = active high.

Setting the Functionality of Pin 9

Pin 9 on the ADT7467 has four possible functions: $\overline{\text{SMBALERT}}$, $\overline{\text{THERM}}$, GPIO, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D.

Table 4. PIN 9 SETTINGS

Bit 1	Bit 0	Function
0	0	TACH4
0	1	$\overline{\text{THERM}}$
1	0	$\overline{\text{SMBALERT}}$
1	1	GPIO

Recommended Implementation

Configuring the ADT7467 as in Figure NO TAG allows the system designer to use the following features:

- Two PWM Outputs for Fan Control of Up to Three Fans (The Front and Rear Chassis Fans are Connected in Parallel)
- Three TACH Fan Speed Measurement Inputs
- V_{CC} Measured Internally through Pin 3
- CPU Temperature Measured Using the Remote 1 Temperature Channel
- Ambient Temperature Measured through the Remote 2 Temperature Channel
- Bidirectional $\overline{\text{THERM}}$ Pin. This Feature Allows Intel® Pentium® 4 $\overline{\text{PROCHOT}}$ Monitoring and Can Function as an Overtemperature $\overline{\text{THERM}}$ Output. Alternatively, it Can be Programmed as an $\overline{\text{SMBALERT}}$ System Interrupt Output

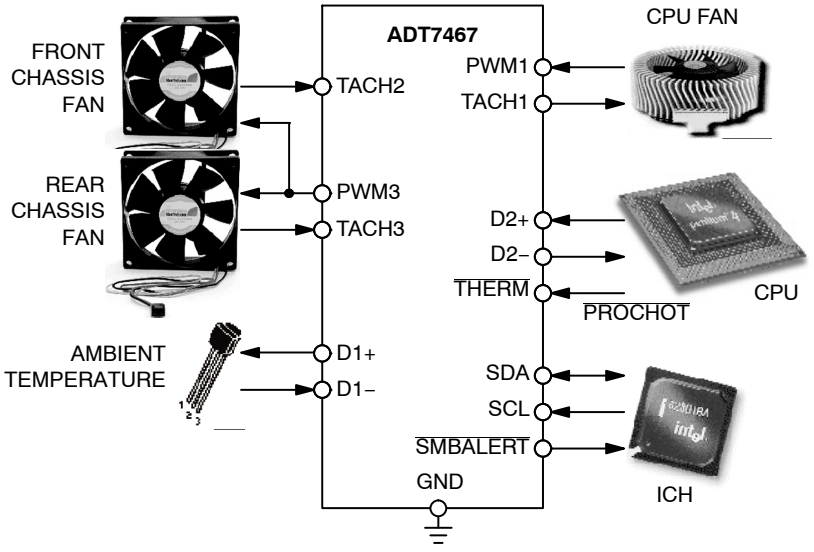


Figure 14. ADT7467 Implementation

Serial Bus Interface

On PCs and servers, control of the ADT7467 is carried out using the serial system management bus (SMBus). The ADT7467 is connected to this bus as a slave device under the control of a master controller, which is usually (but not necessarily) the ICH.

The ADT7467 has a fixed 7-bit serial bus address of 0101110 or 0x2E. The read/write bit must be added to get the 8-bit address (01011100 or 0x5C). Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition might be interpreted as a stop signal when the clock is high. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is only limited by what the master and slave devices can handle.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the 10th clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse. This is known as a no acknowledge. The master then takes the data line low during the low period before the 10th clock pulse, and then high during the 10th clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation. It is not possible to mix a read and a write in one operation, however, because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the ADT7467, write operations contain either one or two bytes, and read operations contain one byte. To write data to a device data register or read data from it, the address pointer register must first be set. The first byte of a write operation always contains an address, which is stored in the address pointer register, and the second byte, if there is a second byte, is written to the register selected by the address pointer register.

This write operation is illustrated in Figure 15. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register, and the second data byte is the data written to that internal data register.

When reading data from a register, there are two possibilities:

1. If the address pointer register value of the ADT7467 is unknown or not the desired value, it must be set to the correct value before data can be read from the desired data register. This is achieved by writing a data byte containing the register address to the ADT7467. This is shown in Figure 16. A read operation is then performed consisting of the serial bus address and the R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register. This is shown in Figure 17.
2. If the address pointer register is known to be at the desired address, data can be read from the corresponding data register without first writing to the address pointer register, as shown in Figure 17.

If the address pointer register is already at the correct value, it is possible to read a data byte from the data register without first writing to the address pointer register. However, it is not possible to write data to a register without writing to the address pointer register, because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the ADT7467 also supports the read byte protocol. (See the Intel *System Management Bus Specifications Rev. 2* for more information.)

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

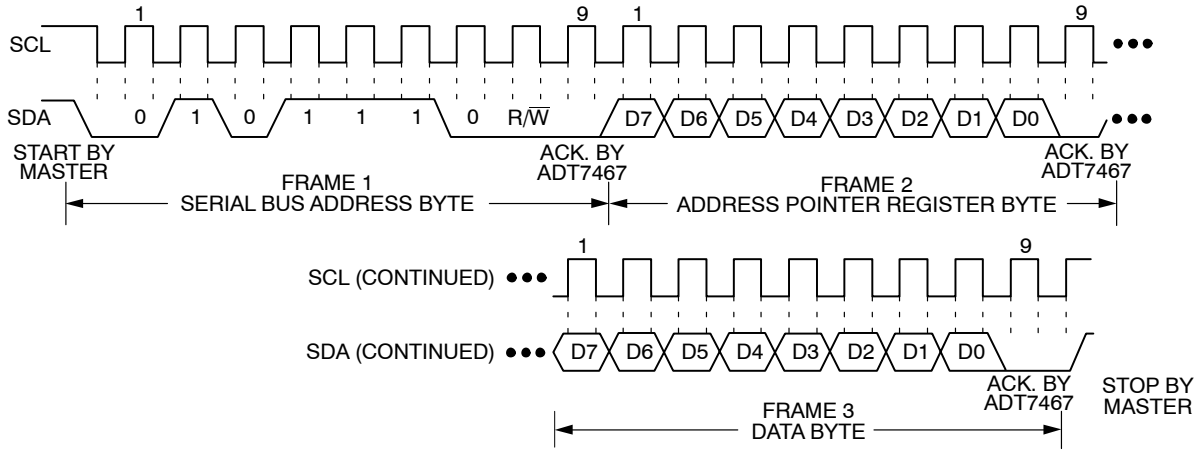


Figure 15. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

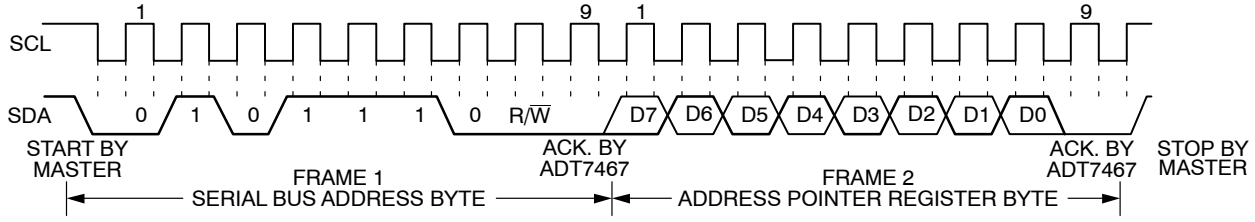


Figure 16. Writing to the Address Pointer Register Only

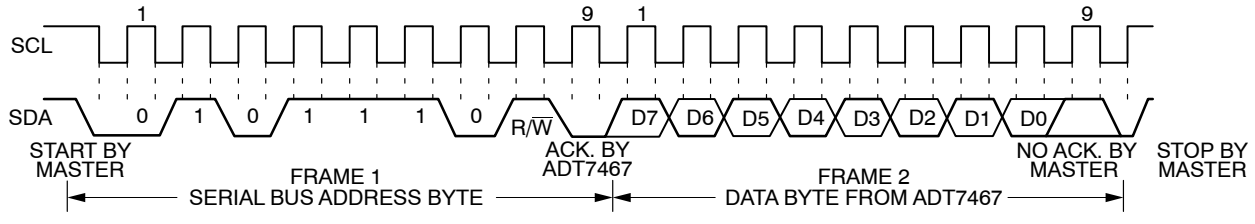


Figure 17. Reading Data from a Previously Selected Register

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the ADT7467 are discussed here. The following abbreviations are used in Figure 18 through Figure 20:

S = start
P = stop
R = read
W = write
A = acknowledge
$\overline{A}$ = no acknowledge

The ADT7467 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a command code.
5. The slave asserts an acknowledge on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

For the ADT7467, the send byte protocol is used to write a register address to RAM for a subsequent single byte read from the same address. This operation is illustrated in Figure 18.

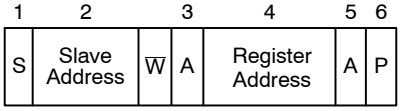


Figure 18. Setting a Register Address for Subsequent Read

If the master is required to read data from the register directly after setting up the address, it can assert a repeat start condition immediately after the final acknowledge and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the write bit (low).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master sends a command code.
5. The slave asserts an acknowledge on SDA.
6. The master sends a data byte.
7. The slave asserts an acknowledge on SDA.
8. The master asserts a stop condition on SDA to end the transaction.

This operation is illustrated in Figure 19.

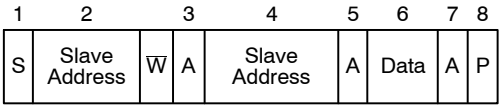


Figure 19. Single Byte Write to a Register

Read Operations

The ADT7467 uses the following SMBus read protocols.

Receive Byte

This operation is useful when repeatedly reading a single register. The register address must have been set up previously. In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7-bit slave address followed by the read bit (high).
3. The addressed slave device asserts an acknowledge on SDA.
4. The master receives a data byte.
5. The master asserts a no acknowledge on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the ADT7467, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation. This operation is illustrated in Figure 20.

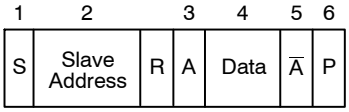


Figure 20. Single Byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as either an interrupt output or an $\overline{\text{SMBALERT}}$. One or more outputs can be connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following procedure occurs:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This is a general call address that must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of the

device is now known and can be interrogated in the usual way.

4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the ADT7467 has responded to the alert response address, the master must read the status registers. The $\overline{\text{SMBALERT}}$ is cleared only if the error condition is absent.

SMBus Timeout

The ADT7467 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the ADT7467 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus in anticipation of receiving data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Configuration Register 1 (0x40)

<6> TODIS = 0, SMBus timeout enabled (default)

<6> TODIS = 1, SMBus timeout disabled

Analog-to-Digital Converter

All analog inputs are multiplexed into the on-chip, successive approximation, analog-to-digital converter, which has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the input has built-in attenuators to allow measurement of V_{CCP} without any external components. To allow for the tolerance of the supply voltage, the ADC produces an output of 3/4 full scale (decimal 768 or 300 hexadecimal) for the nominal input voltage and, therefore, has adequate headroom to deal with overvoltages.

Voltage Measurement Input

The ADT7467 has one external voltage measurement channel. It can also measure its own supply voltage, V_{CC}. Pin 14 can measure V_{CCP}. The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 3). Setting Bit 7 of Configuration Register 1 (0x40) allows a 5 V supply to power the ADT7467 and be measured without overranging the V_{CC} measurement channel. The V_{CCP} input can be used to monitor a chipset supply voltage in computer systems.

Input Circuitry

The internal structure for the V_{CCP} analog input is shown in Figure 21. The input circuit consists of an input protection diode, an attenuator, and a capacitor to form a first-order low-pass filter that gives the input immunity to high frequency noise.

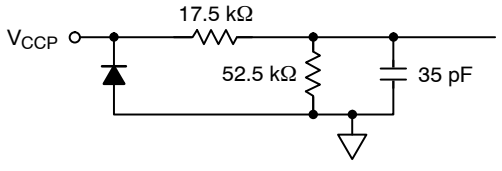


Figure 21. Structure of Analog Inputs

Voltage Measurement Registers

Register 0x21 V_{CCP} reading = 0x00 default

Register 0x22 V_{CC} reading = 0x00 default

V_{CCP} Limit Registers

Associated with the V_{CCP} and V_{CC} measurement channels is a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Register 0x46 V_{CCP} low limit = 0x00 default

Register 0x47 V_{CCP} high limit = 0xFF default

Register 0x48 V_{CC} low limit = 0x00 default

Register 0x49 V_{CC} high limit = 0xFF default

Table 6 shows the input ranges of the analog inputs and output codes of the 10-bit ADC.

When the ADC is running, it samples and converts a voltage input in 0.7 ms and averages 16 conversions to reduce noise; a measurement takes nominally 11 ms.

Additional ADC Functions for Voltage Measurements

A number of other functions are available on the ADT7467 to offer the system designer increased flexibility.

Turn-off Averaging

For each voltage measurement read from a value register, 16 readings are made internally, the results of which are averaged and then placed into the value register. For instances where faster conversions are needed, setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. This produces a reading that is 16 times faster (0.7 ms), but the reading may be noisier.

Bypass Voltage Input Attenuator

Setting Bit 5 of Configuration Register 2 (0x73) removes the attenuation circuitry from the V_{CCP} input. This allows the user to directly connect external sensors or to rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single-channel ADC Conversion

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7467 into single−channel ADC conversion mode. In this mode, the ADT7467 can be made to read a single voltage channel only. If the internal ADT7467 clock is used, the selected input is read every 0.7 ms. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 5. PROGRAMMING SINGLE-CHANNEL ADC MODE

Bits <7:5>, Register 0x55	Channel Selected
001	V_{CCP}
010	V_{CC}
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

Configuration Register 2 (0x73)

<4> = 1, Averaging Off

<5> = 1, Bypass Input Attenuators

<6> = 1, Single-channel Conversion Mode

TACH1 Minimum High Byte (0x55)

<7:5> Selects ADC Channel for Single-channel Convert Mode

Table 6. 10-BIT ANALOG-TO-DIGITAL OUTPUT CODE VS. V_{IN}

Input Voltage			A/D Output	
V_{CC} (5 V_{IN})	V_{CC} (3.3 V_{IN})	V_{CCP}	Decimal	Binary (10 Bits)
<0.0065	<0.0042	<0.00293	0	00000000 00
0.0065 to 0.0130	0.0042 to 0.0085	0.0293 to 0.0058	1	00000000 01
0.0130 to 0.0195	0.0085 to 0.0128	0.0058 to 0.0087	2	00000000 10
0.0195 to 0.0260	0.0128 to 0.0171	0.0087 to 0.0117	3	00000000 11
0.0260 to 0.0325	0.0171 to 0.0214	0.0117 to 0.0146	4	00000001 00
0.0325 to 0.0390	0.0214 to 0.0257	0.0146 to 0.0175	5	00000001 01
0.0390 to 0.0455	0.0257 to 0.0300	0.0175 to 0.0205	6	00000001 10
0.0455 to 0.0521	0.0300 to 0.0343	0.0205 to 0.0234	7	00000001 11
0.0521 to 0.0586	0.0343 to 0.0386	0.0234 to 0.0263	8	00000010 00
			…	
1.6675 to 1.6740	1.100 to 1.1042	0.7500 to 0.7529	256 (1/4 scale)	01000000 00
			…	
3.330 to 3.3415	2.200 to 2.2042	1.5000 to 1.5029	512 (1/2 scale)	10000000 00
			…	
5.0025 to 5.0090	3.300 to 3.3042	2.2500 to 2.2529	768 (3/4 scale)	11000000 00
			…	
6.5983 to 6.6048	4.3527 to 4.3570	2.9677 to 2.9707	1013	11111101 01
6.6048 to 6.6113	4.3570 to 4.3613	2.9707 to 2.9736	1014	11111101 10
6.6113 to 6.6178	4.3613 to 4.3656	2.9736 to 2.9765	1015	11111101 11
6.6178 to 6.6244	4.3656 to 4.3699	2.9765 to 2.9794	1016	11111110 00
6.6244 to 6.6309	4.3699 to 4.3742	2.9794 to 2.9824	1017	11111110 01
6.6309 to 6.6374	4.3742 to 4.3785	2.9824 to 2.9853	1018	11111110 10
6.6374 to 6.4390	4.3785 to 4.3828	2.9853 to 2.9882	1019	11111110 11
6.6439 to 6.6504	4.3828 to 4.3871	2.9882 to 2.9912	1020	11111111 00
6.6504 to 6.6569	4.3871 to 4.3914	2.9912 to 2.9941	1021	11111111 01
6.6569 to 6.6634	4.3914 to 4.3957	2.9941 to 2.9970	1022	11111111 10
>6.6634	>4.3957	>2.9970	1023	11111111 11

Temperature Measurement

A simple method of measuring temperature is to exploit the negative temperature coefficient of a diode, measuring the base-emitter voltage (V_{BE}) of a transistor operated at constant current. Unfortunately, this technique requires calibration to null the effect of the absolute value of V_{BE}, which varies from each device.

The technique used in the ADT7467 is to measure the change in V_{BE} when the device is operated at three currents. Previous devices have used only two operating currents, but the use of a third current allows automatic cancellation of resistances in series with the external temperature sensor.

Figure 23 shows the input signal conditioning used to measure the output of an external temperature sensor. This figure shows the external sensor as a substrate transistor, but it could equally be a discrete transistor. If a discrete transistor is used, the collector is not grounded and should be linked to the base. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D− input. C1 can optionally be added as a noise filter (the recommended maximum value is 1,000 pF). However, a better option in noisy environments is to add a filter as described in the Noise Filtering section.

Local Temperature Measurement

The ADT7467 contains an on-chip band gap temperature sensor whose output is digitized by the on-chip 10-bit ADC. The 8-bit MSB temperature data is stored in the local temperature register (Address 0x26). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Table 7 and Table 8. Theoretically, the temperature sensor and ADC can measure temperatures from −128°C to +127°C (or −64°C to +191°C in the extended temperature range) with a resolution of 0.25°C. However, this exceeds the operating temperature range of the device, preventing local temperature measurements outside the ADT7467 operating temperature range.

Remote Temperature Measurement

The ADT7467 can measure the temperature of two remote diode sensors or diode-connected transistors connected to Pin 10 and Pin 11 or to Pin 12 and Pin 13.

The forward voltage of a diode or diode-connected transistor operated at a constant current exhibits a negative temperature coefficient of about −2 mV/°C. Unfortunately, the absolute value of V_{BE} varies from each device and thus requires individual calibration; therefore, the technique is unsuitable for mass production. The technique used in the ADT7467 is to measure the change in V_{BE} when the device is operated at three currents. This is given by:

$$\Delta V_{BE} = kT/q \times \ln(N) \quad \text{(eq. 1)}$$

where:

k is Boltzmann's constant.
q is the charge on the carrier.
T is the absolute temperature in Kelvins.
N is the ratio of the two currents.

Figure 22 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor provided for temperature monitoring on some microprocessors. It could also be a discrete transistor such as a 2N3904/2N3906.

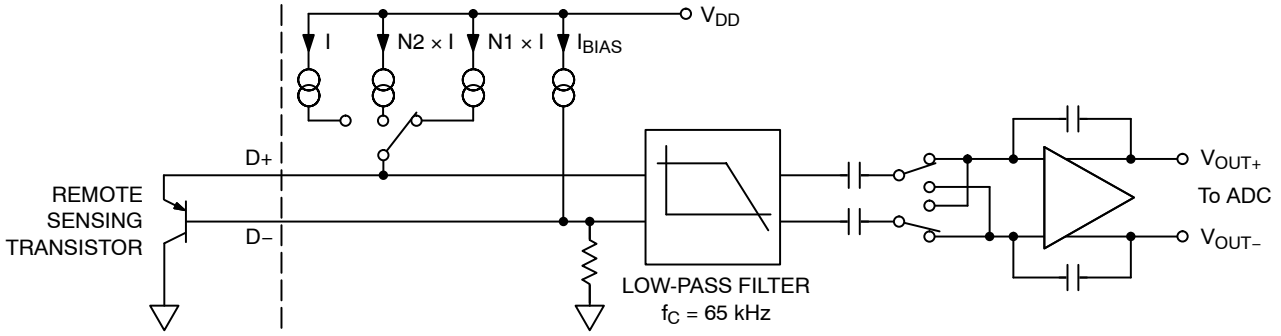


Figure 22. Signal Conditioning for Remote Diode Temperature Sensors

If a discrete transistor is used, the collector is not grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D− input and the emitter is connected to the D+ input. If an NPN transistor is used, the emitter is connected to the D− input and the base is connected to the D+ input. Figure 24 and Figure 25 show how to connect the ADT7467 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D− input.

To measure ΔV_{BE}, the operating current through the sensor is switched among three related currents. Shown in Figure 22, N1 × I and N2 × I are different multiples of the current I. The currents through the temperature diode are switched between I and N1 × I, resulting in ΔV_{BE1}; then

they are switched between I and N2 × I, resulting in ΔV_{BE2}. The temperature can then be calculated using the two ΔV_{BE} measurements. This method can also cancel the effect of series resistance on the temperature measurement.

The resulting ΔV_{BE} waveforms are passed through a 65 kHz low-pass filter to remove noise and then sent to a chopper-stabilized amplifier that amplifies and rectifies the waveform to produce a dc voltage proportional to ΔV_{BE}. The ADC digitizes this voltage, and a temperature measurement is produced. To reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

The results of remote temperature measurements are stored in 10-bit twos complement format, as listed in Table 7. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (0x77). This produces temperature readings with a resolution of 0.25°C.

Series Resistance Cancellation

Parasitic resistance to the ADT7467 D+ and D− inputs (seen in series with the remote diode) is caused by a variety of factors, including PCB track resistance and track length. This series resistance appears as a temperature offset in the remote sensor's temperature measurement. This error typically causes a 0.5°C offset per 1 Ω of parasitic resistance in series with the remote diode.

The ADT7467 automatically cancels the effect of this series resistance on the temperature reading, providing a more accurate result without the need for user characterization of this resistance. The ADT7467 is designed to automatically cancel, typically up to 3 kΩ of resistance. By using an advanced temperature measurement method, this is transparent to the user. This feature allows resistances to be added to the sensor path to produce a filter, allowing the part to be used in noisy environments. See the Noise Filtering section for details.

Noise Filtering

For temperature sensors operating in noisy environments, previous practice involved placing a capacitor across the D+ and D− pins to help combat the effects of noise. However, large capacitances affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1,000 pF. A capacitor of this value reduces the noise but does not eliminate it, making use of the sensor difficult in a very noisy environment.

The ADT7467 has a major advantage over other devices for eliminating the effects of noise on the external sensor. Using the series resistance cancellation feature, a filter can be constructed between the external temperature sensor and the device. The effect of filter resistance seen in series with the remote sensor is automatically canceled from the temperature result.

The construction of a filter allows the ADT7467 and the remote temperature sensor to operate in noisy environments. Figure 23 shows a low-pass R-C-R filter with the following values:

R = 100 Ω, C = 1 nF

This filtering reduces both common-mode noise and differential noise.

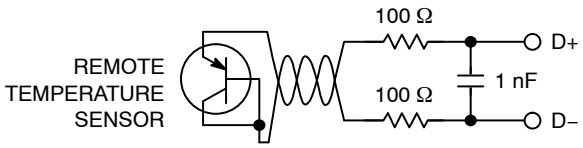


Figure 23. Filter Between Remote Sensor and ADT7467

Factors Affecting Diode Accuracy

Remote Sensing Diode

The ADT7467 is designed to work with either substrate transistors built into processors or discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base-shorted to the collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter is connected to D−. If a PNP transistor is used, the collector and base are connected to D− and the emitter is connected to D+.

To reduce the error due to variations in both substrate and discrete transistors, a number of factors should be taken into consideration:

- The ideality factor, n_f, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The ADT7467 is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a temperature, T (°C), when using a transistor whose n_f does not equal 1.008. See the processor's data sheet for the n_f values.
  $\Delta T = (n_f - 1.008)/1.008 \times (273.15\ K + T)$
- To correct for this error, the user can write the ΔT value to the offset register, and the ADT7467 automatically adds it to or subtracts it from the temperature measurement.
- Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the ADT7467, I_{HIGH}, is 96 μA, and the low level current, I_{LOW}, is 6 μA. If the ADT7467 current levels do not match the current levels specified by the CPU manufacturer, it may be necessary to remove an offset. The CPU's data sheet should provide information relating to n_f to compensate for differences. An offset can be programmed to the offset register. It is important to note that if more than one offset must be considered, the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the ADT7467, the best accuracy is obtained by choosing devices according to the following criteria:

- Base-emitter voltage is greater than 0.25 V at 6 μA with the highest operating temperature.
- Base-emitter voltage is less than 0.95 V at 100 μA with the lowest operating temperature.
- Base resistance is less than 100 Ω.
- There is a small variation in h_{FE} (for example, 50 to 150) that indicates tight control of V_{BE} characteristics.

Transistors such as 2N3904, 2N3906, or equivalents in SOT−23 packages are suitable devices to use.

Table 7. TWOS COMPLEMENT TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-bit) (Note 1)
−128°C	1000 0000 **00**
−125°C	1000 0011 **00**
−100°C	1001 1100 **00**
−75°C	1011 0101 **00**
−50°C	1100 1110 **00**
−25°C	1110 0111 **00**
−10°C	1111 0110 **00**
0°C	0000 0000 **00**
+10.25°C	0000 1010 **01**
+25.5°C	0001 1001 **10**
+50.75°C	0011 0010 **11**
+75°C	0100 1011 **00**
+100°C	0110 0100 **00**
+125°C	0111 1101 **00**
+127°C	0111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in Extended Resolution Register 2 (0x77) with 0.25°C resolution.

Table 8. OFFSET 64 TEMPERATURE DATA FORMAT

Temperature	Digital Output (10-bit) (Note 1)
−64°C	0000 0000 **00**
−1°C	0011 1111 **00**
0°C	0100 0000 **00**
+1°C	0100 0001 **00**
+10°C	0100 1010 **00**
+25°C	0101 1001 **00**
+50°C	0111 0010 **00**
+75°C	1000 1001 **00**
+100°C	1010 0100 **00**
+125°C	1011 1101 **00**
+191°C	1111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in Extended Resolution Register 2 (0x77) with 0.25°C resolution.

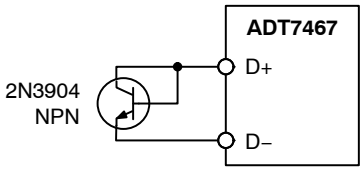


Figure 24. Measuring Temperature by Using an NPN Transistor

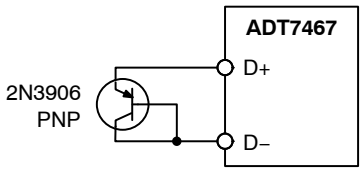


Figure 25. Measuring Temperature by Using a PNP Transistor

Nulling Temperature Errors

As CPUs run faster, it is more difficult to avoid high frequency clocks when routing the D+/D− traces around a system board. Even when recommended layout guidelines are followed, some temperature errors may still be attributed to noise coupled onto the D+/D− lines. Constant high frequency noise usually attenuates or increases temperature measurements by a linear, constant value.

The ADT7467 has temperature offset registers at Address 0x70 and Address 0x72 for the Remote 1 and Remote 2 temperature channels, respectively. By performing a one-time calibration of the system, the user can determine the offset caused by system board noise and null it using the offset registers. The offset registers automatically add an Offset 64/twos complement 8-bit reading to every temperature measurement. The LSBs add 0.5°C offset to the temperature reading; therefore, the 8-bit register effectively allows temperature offsets of up to ±64°C with a resolution of 0.5°C. This ensures that the readings in the temperature measurement registers are as accurate as possible.

Temperature Offset Registers

Register 0x70 Remote 1 Temperature Iffset = 0x00 (0°C Default)

Register 0x71 Local Temperature Offset = 0x00 (0°C Default)

Register 0x72 Remote 2 Temperature Offset = 0x00 (0°C Default)

ADT7460/ADT7467 Backwards-compatible Mode

By setting Bit 1 of Configuration Register 5 (0x7C), all temperature measurements are stored in the zone temperature value registers (Register 0x25, Register 0x26, and Register 0x27) in twos complement format in the range −128°C to +127°C. (The ADT7468 makes calculations based on the Offset 64 extended range and clamps the results if necessary.) The temperature limits must be reprogrammed in twos complement format. If a twos complement

temperature below −63°C is entered, the temperature is clamped to −63°C. In this mode, the diode fault condition remains −128°C = 1000 0000, whereas the fault condition is represented by −64°C = 0000 0000 in the extended temperature range (−64°C to +191°C).

Table 9. TEMPERATURE MEASUREMENT REGISTERS

Register	Description	Default
0x25	Remote 1 Temperature	0x01
0x26	Local Temperature	0x01
0x27	Remote 2 Temperature	0x01
0x77	Extended Resolution 2	0x00

Table 10. EXTENDED RESOLUTION TEMPERATURE MEASUREMENT REGISTER BITS

Bit	Mnemonic	Description
<7:6>	TDM2	Remote 2 Temperature LSBs
<5:4>	LTMP	Local Temperature LSBs
<3:2>	TDM1	Remote 1 Temperature LSBs

Temperature Measurement Limit Registers

High and low limit registers are associated with each temperature measurement channel. Exceeding the programmed high or low limit sets the appropriate status bit and can also generate $\overline{\text{SMBALERT}}$ interrupts.

Table 11. TEMPERATURE MEASUREMENT LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x01
0x4F	Remote 1 Temperature High Limit	0x7F
0x50	Local Temperature Low Limit	0x01
0x51	Local Temperature High Limit	0x7F
0x52	Remote 2 Temperature Low Limit	0x01
0x53	Remote 2 Temperature High Limit	0x7F

Reading Temperature from the ADT7467

It is important to note that temperature can be read from the ADT7467 as an 8-bit value (with 1°C resolution) or as a 10-bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read at any time and in no particular order.

If the 10-bit measurement is required, this involves a 2-register read for each measurement. The extended resolution register (0x77) should be read first. Then all temperature reading registers freeze until all temperature reading registers are read. This prevents updating of an MSB reading while its two LSBs are read and vice versa.

Additional ADC Functions for Temperature Measurement

A number of other functions are available on the ADT7467 to offer the system designer increased flexibility.

Turn-off Averaging

For each temperature measurement read from a value register, 16 readings are made internally, the results of which are averaged and then placed into the value register. Sometimes it is necessary to perform a very fast measurement. Setting Bit 4 of Configuration Register 2 (0x73) turns averaging off.

Table 12. CONVERSION TIME WITH AVERAGING DISABLED

Channel	Measurement Time
Voltage Channels	0.7 ms
Remote Temperature 1	7 ms
Remote Temperature 2	7 ms
Local Temperature	1.3 ms

Table 13. CONVERSION TIME WITH AVERAGING ENABLED

Channel	Measurement Time
Voltage Channels	11 ms
Remote Temperature	39 ms
Local Temperature	12 ms

Single-channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (0x73) places the ADT7467 into single-channel ADC conversion mode. In this mode, users can read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits <7:5> of the TACH1 minimum high byte register (0x55).

Table 14. CHANNEL SELECTION

Bits <7:5>, Register 0x55	Channel Selected
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

Configuration Register 2 (0x73)

<4> = 1, Averaging Off

<6> = 1, Single-channel Convert Mode

TACH1 Minimum High Byte (0x55)

<7:5> Selects ADC Channel for Single-channel Convert Mode

Overtemperature Events

Overtemperature events on a temperature channel can be automatically detected and dealt with in automatic fan speed control mode. Register 0x6A to Register 0x6C contain the $\overline{\text{THERM}}$ temperature limits. When a temperature exceeds its $\overline{\text{THERM}}$ temperature limit, all PWM outputs run at the maximum PWM duty cycle (0x38, 0x39, 0x3A); therefore, fans run at the fastest speed allowed and continue running at this speed until the temperature drops below $\overline{\text{THERM}}$ minus hysteresis. (This can be disabled by setting the BOOST bit in Configuration Register 3, Bit 2, Register 0x78.) The hysteresis value for that $\overline{\text{THERM}}$ temperature limit is the value programmed into Register 0x6D and Register 0x6E (hysteresis registers). The default hysteresis value is 4°C.

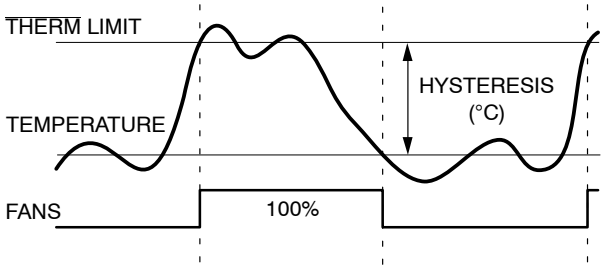


Figure 26. $\overline{\text{THERM}}$ Temperature Limit Operation

Limits, Status Registers, and Interrupts

Limit Values

High and low limits are associated with each measurement channel on the ADT7467. These limits form the basis of system-status monitoring in that a status bit can be set for any out-of-limit condition and detected by polling the device. Alternatively, $\overline{\text{SMBALERT}}$ interrupts can be generated to flag a processor or microcontroller of out-of-limit conditions.

8-bit Limits

The following is a list of 8-bit limits on the ADT7467.

Table 15. VOLTAGE LIMIT REGISTERS

Register	Description	Default
0x46	V_{CCP} Low Limit	0x00
0x47	V_{CCP} High Limit	0xFF
0x48	V_{CC} Low Limit	0x00
0x49	V_{CC} High Limit	0xFF

Table 16. $\overline{\text{THERM}}$ TIMER LIMIT REGISTERS

Register	Description	Default
0x7A	$\overline{\text{THERM}}$ Timer Limit	0x00

Table 17. TEMPERATURE LIMIT REGISTERS

Register	Description	Default
0x4E	Remote 1 Temperature Low Limit	0x01
0x4F	Remote 1 Temperature High Limit	0x7F
0x6A	Remote 1 $\overline{\text{THERM}}$ Limit	0xA4
0x50	Local Temperature Low Limit	0x01
0x51	Local Temperature High Limit	0x7F
0x6B	Local $\overline{\text{THERM}}$ Limit	0xA4
0x52	Remote 2 Temperature Low Limit	0x01
0x53	Remote 2 Temperature High Limit	0x7F
0x6C	Remote 2 $\overline{\text{THERM}}$ Limit	0xA4

16-bit Limits

The fan TACH measurements are 16-bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Because slow or stalled fans are normally the only conditions of interest, only high limits exist for fan TACHs. Because the fan TACH period is measured, exceeding the limit indicates a slow or stalled fan.

Table 18. FAN LIMIT REGISTERS

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Out-of-Limit Comparisons

Once all limits are programmed, the ADT7467 can be enabled for monitoring. The ADT7467 measures all voltage and temperature measurements in round-robin format and sets the appropriate status bit for out-of-limit conditions. TACH measurements are not part of this round-robin cycle. Comparisons are done differently, depending on whether the measured value is being compared to a high or low limit.

High limit: > comparison performed

Low limit: ≤ comparison performed

Voltage and temperature channels use a window comparator for error detecting and, therefore, have high and low limits. Fan speed measurements use only a low limit. This fan limit is needed only in manual fan control mode.

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (0x40). By default, the ADT7463 powers up with this bit set. The ADC measures each analog input in turn and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round-robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally left to free-run in this manner, the time to monitor all analog inputs is normally not of interest because the most recently measured value of an input can be read at any time.

For applications where the monitoring cycle time is important, it can be calculated easily. The total number of channels measured is

- One Dedicated Supply Voltage Input (V_{CCP})
- One Supply Voltage (V_{CC} Pin)
- One Local Temperature
- Two Remote Temperatures

As mentioned previously, the ADC performs round-robin conversions. The total monitoring cycle time for averaged voltage and temperature monitoring is 145 ms. The total monitoring cycle time for voltage and temperature monitoring with averaging disabled is 19 ms. The ADT7467 is a derivative of the ADT7468. As a result, the total conversion time for the ADT7467 and ADT7468 are the same, even though the ADT7467 has less monitored channels.

Fan TACH measurements are made in parallel and are not synchronized with the analog measurements in any way.

Status Registers

The results of limit comparisons are stored in Interrupt Status Register 1 and Interrupt Status Register 2. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding status register bit is cleared to 0. If the measurement is out of limit, the corresponding status register bit is set to 1.

The state of the various measurement channels can be polled by reading the status registers over the serial bus. In Bit 7 (OOL) of Interrupt Status Register 1 (0x41), 1 means that an out-of-limit event has been flagged in Interrupt Status Register 2. This means that the user also should read Interrupt Status Register 2. Alternatively, Pin 5 or Pin 9 can be configured as an $\overline{\text{SMBALERT}}$ output. This hardware interrupt automatically notifies the system supervisor of an out-of-limit condition. Reading the status registers clears the appropriate status bit if the error condition that caused the interrupt is absent. Status register bits are sticky. Whenever a status bit is set, indicating an out-of-limit condition, it remains set until read, even if the event that caused it is absent. The only way to clear the status bit is to read the status register after the event is absent. Interrupt mask registers (0x74 and 0x75) allow masking of individual interrupt sources to prevent an $\overline{\text{SMBALERT}}$. However, if a masked interrupt source goes out of limit, its associated status bit is set in the interrupt status registers.

Table 19. STATUS REGISTER 1 (REG. 0X41)

Bit	Mnemonic	Description
7	OOL	1 denotes a bit in Status Register 2 is set and Status Register 2 should be read.
6	R2T	1 indicates that the Remote 2 temperature high or low limit has been exceeded.
5	LT	1 indicates that the Local temperature high or low limit has been exceeded.
4	R1T	1 indicates that the Remote 1 temperature high or low limit has been exceeded.
2	V_{CC}	1 indicates that the V_{CC} high or low limit has been exceeded.
1	V_{CCP}	1 indicates that the V_{CCP} high or low limit has been exceeded.

Table 20. STATUS REGISTER 2 (REG. 0X42)

Bit	Mnemonic	Description
7	D2	1 indicates an open or short on D2+/D2− inputs.
6	D1	1 indicates an open or short on D2+/D2− inputs.
5	F4P	1 indicates that Fan 4 has dropped below minimum speed. Alternatively, indicates that $\overline{\text{THERM}}$ timer limit has been exceeded if the $\overline{\text{THERM}}$ timer function is used.
4	FAN3	1 indicates that Fan 3 has dropped below minimum speed.
3	FAN2	1 indicates that Fan 2 has dropped below minimum speed.
2	FAN1	1 indicates that Fan 1 has dropped below minimum speed.
1	OVT	1 indicates that a $\overline{\text{THERM}}$ overtemperature limit has been exceeded.

Interrupts

$\overline{\text{SMBALERT}}$ Interrupt Behavior

The ADT7467 can be polled for status, or an $\overline{\text{SMBALERT}}$ interrupt can be generated for out-of-limit conditions. It is important to note how the $\overline{\text{SMBALERT}}$ output and status bits behave when writing interrupt handler software.

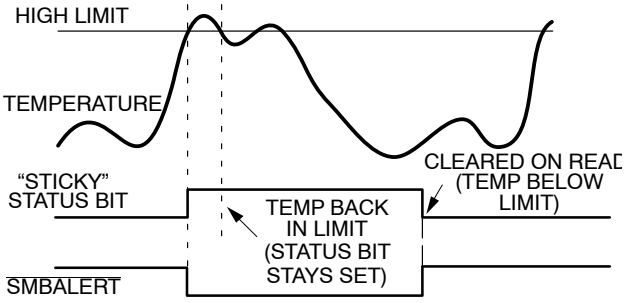


Figure 27. SMBALERT and Status Bit Behavior

Figure 27 shows how the SMBALERT output and sticky status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The status bit remains set until the error condition subsides and the status register is read. The status bits are referred to as sticky because they remain set until read by software. This ensures that an out-of-limit event cannot be missed if software is polling the device periodically. Note that the SMBALERT output remains low both for the duration that a reading is out of limit and until the status register has been read. This has implications on how software handles the interrupt.

Handling SMBALERT Interrupts

To prevent the system from being tied up with servicing interrupts, it is recommend to handle the SMBALERT interrupt as follows:

1. Detect the SMBALERT assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (Register 0x74 and Register 0x75).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the SMBALERT output and status bits to behave as shown in Figure 28.

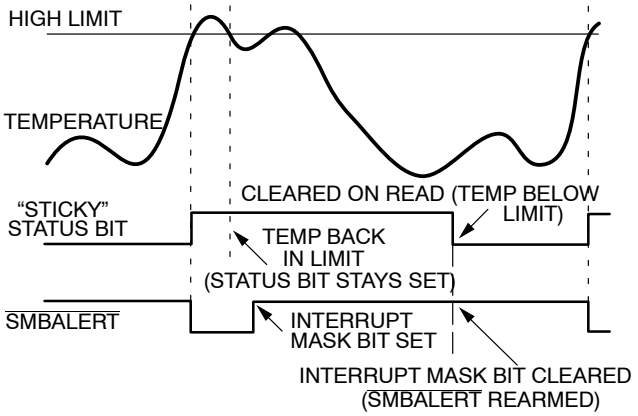


Figure 28. Effect of Masking the Interrupt Source on SMBALERT Output

Masking Interrupt Sources

Interrupt Mask Registers 1 and 2 are located at Address 0x74 and Address 0x75, respectively, and allow individual interrupt sources to be masked to prevent SMBALERT interrupts. Note that masking an interrupt source prevents only the SMBALERT output from being asserted; the appropriate status bit is set normally.

Table 21. INTERRUPT MASK REGISTER 1 (REG. 0X74)

Bit	Mnemonic	Description
7	OOL	1 masks SMBALERT for any alert condition flagged in Status Register 2.
6	R2T	1 masks SMBALERT for Remote 2 temperature channel.
5	LT	1 masks SMBALERT for local temperature channel.
4	R1T	1 masks SMBALERT for Remote 1 temperature channel.
2	V_{CC}	1 masks SMBALERT for the V_{CC} channel.
0	V_{CCP}	1 masks SMBALERT for the V_{CCP} channel.

Table 22. INTERRUPT MASK REGISTER 2 (REG. 0X75)

Bit	Mnemonic	Description
7	D2	1 masks SMBALERT for Diode 2 errors.
6	D1	1 masks SMBALERT for Diode 1 errors.
5	FAN4	1 masks SMBALERT for Fan 4 failure. If the TACH4 pin is being used as the THERM input, this bit masks SMBALERT for a THERM event.
4	FAN3	1 masks SMBALERT for Fan 3.
3	FAN2	1 masks SMBALERT for Fan 2.
2	FAN1	1 masks SMBALERT for Fan 1.
1	OVT	1 masks SMBALERT for overtemperature (exceeding THERM limits).

Enabling the SMBALERT Interrupt Output

The SMBALERT interrupt function is disabled by default. Pin 5 or Pin 9 can be reconfigured as an SMBALERT output to signal out-of-limit conditions.

Table 23. CONFIGURING PIN 5 AS SMBALERT OUTPUT

Register	Bit Setting
Configuration Register 3 (0x78)	<0> ALERT Enable = 1

Assigning THERM Functionality to a Pin

Pin 9 on the ADT7467 has four possible functions: SMBALERT, THERM, GPIO, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 at Address 0x7D.

Table 24. CONFIGURING PIN 9

Bit 1	Bit 0	Function
0	0	TACH4
0	1	$\overline{\text{THERM}}$
1	0	$\overline{\text{SMBALERT}}$
1	1	GPIO

Once Pin 9 is configured as $\overline{\text{THERM}}$, it must be enabled (Bit 1, Configuration Register 3 at Address 0x78).

$\overline{\text{THERM}}$ as an Input

When $\overline{\text{THERM}}$ is configured as an input, the user can time assertions on the $\overline{\text{THERM}}$ pin. This can be useful for connecting to the $\overline{\text{PROCHOT}}$ output of a CPU to gauge system performance.

The user can also set up the ADT7467 so that when the $\overline{\text{THERM}}$ pin is driven low externally, the fans run at 100%. The fans run at 100% for the duration of the time that the $\overline{\text{THERM}}$ pin is pulled low. This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (0x78) to 1. This only works if the fan is already running, for example, in manual mode when the current duty cycle is above 0x00, or in automatic mode when the temperature is above T_{MIN}. If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, externally pulling $\overline{\text{THERM}}$ low has no effect. See Figure 29 for more information.

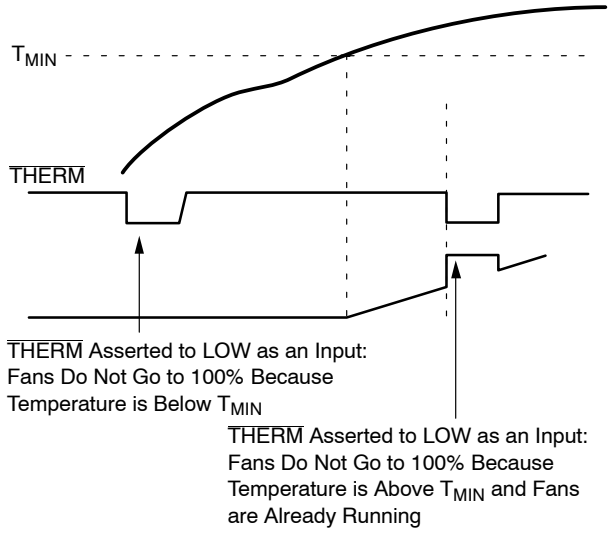


Figure 29. Asserting $\overline{\text{THERM}}$ Low as an Input in Automatic Fan Speed Control Mode

$\overline{\text{THERM}}$ Timer

The ADT7467 has an internal timer to measure $\overline{\text{THERM}}$ assertion time. For example, the $\overline{\text{THERM}}$ input can be connected to the $\overline{\text{PROCHOT}}$ output of a Pentium® 4 CPU to measure system performance. The $\overline{\text{THERM}}$ input can also be connected to the output of a trip point temperature sensor.

The timer is started on the assertion of the $\overline{\text{THERM}}$ input and stopped when $\overline{\text{THERM}}$ is deasserted. The timer counts $\overline{\text{THERM}}$ times cumulatively, that is, the timer resumes counting on the next $\overline{\text{THERM}}$ assertion. The $\overline{\text{THERM}}$ timer continues to accumulate $\overline{\text{THERM}}$ assertion times until the timer is read (it is cleared upon a read) or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8-bit $\overline{\text{THERM}}$ timer register (0x79) is designed such that Bit 0 is set to 1 upon the first $\overline{\text{THERM}}$ assertion. Once the cumulative $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms, Bit 1 of the $\overline{\text{THERM}}$ timer is set and Bit 0 becomes the LSB of the timer with a resolution of 22.76 ms (see Figure 30).

It is important to be aware of the following when using the $\overline{\text{THERM}}$ timer.

After a $\overline{\text{THERM}}$ timer is read (Register 0x79), the following occurs:

- The contents of the timer are cleared upon a read.
- The F4P bit (Bit 5) of Interrupt Status Register 2 must be cleared, assuming that the $\overline{\text{THERM}}$ timer limit has been exceeded.

If the $\overline{\text{THERM}}$ timer is read during a $\overline{\text{THERM}}$ assertion, the following occurs:

- The contents of the timer are cleared.
- Bit 0 of the $\overline{\text{THERM}}$ timer is set to 1 because a $\overline{\text{THERM}}$ assertion is occurring.
- The $\overline{\text{THERM}}$ timer increments from 0.
- If the $\overline{\text{THERM}}$ timer limit (Register 0x7A) is 0x00, the F4P bit is set.

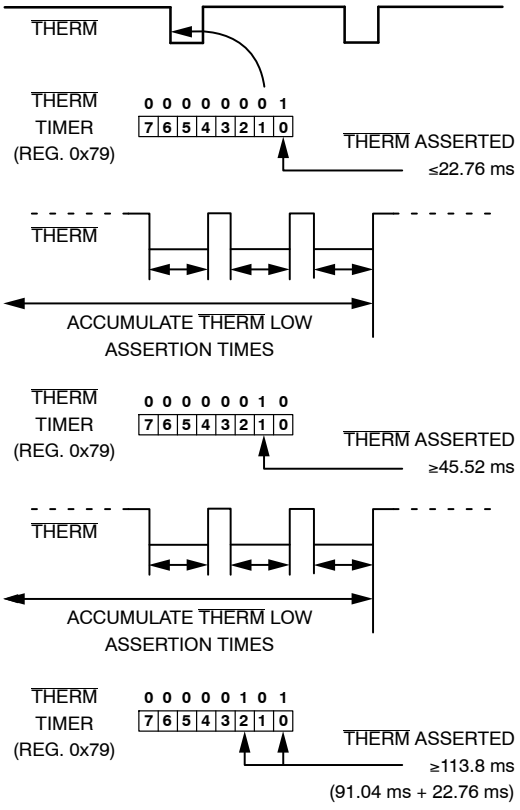


Figure 30. Understanding the $\overline{\text{THERM}}$ Timer

Generating SMBALERT Interrupts from THERM Timer Events

The ADT7467 can generate SMBALERTs when a programmable THERM timer limit has been exceeded. This allows the system designer to ignore brief, infrequent THERM assertions while capturing longer THERM timer events. Register 0x7A is the THERM timer limit register. This 8-bit register allows a limit from 0 sec (first THERM assertion) to 5.825 sec to be set before an SMBALERT is generated. The THERM timer value is compared with the contents of the THERM timer limit register. If the THERM timer value exceeds the THERM timer limit, the F4P bit (Bit 5) of Interrupt Status Register 2 is set and an SMBALERT is generated. Note that the F4P bit (Bit 5) of Interrupt Mask Register 2 (0x75) masks SMBALERT if this bit is set to 1; however, the F4P bit of Interrupt Status Register 2 remains set if the THERM timer limit is exceeded.

Figure 31 is a functional block diagram of the THERM timer, limit, and associated circuitry. Writing a value of 0x00 to the THERM timer limit register (0x7A) causes SMBALERT to be generated upon the first THERM assertion. A THERM timer limit value of 0x01 generates an SMBALERT once cumulative THERM assertions exceed 45.52 ms.

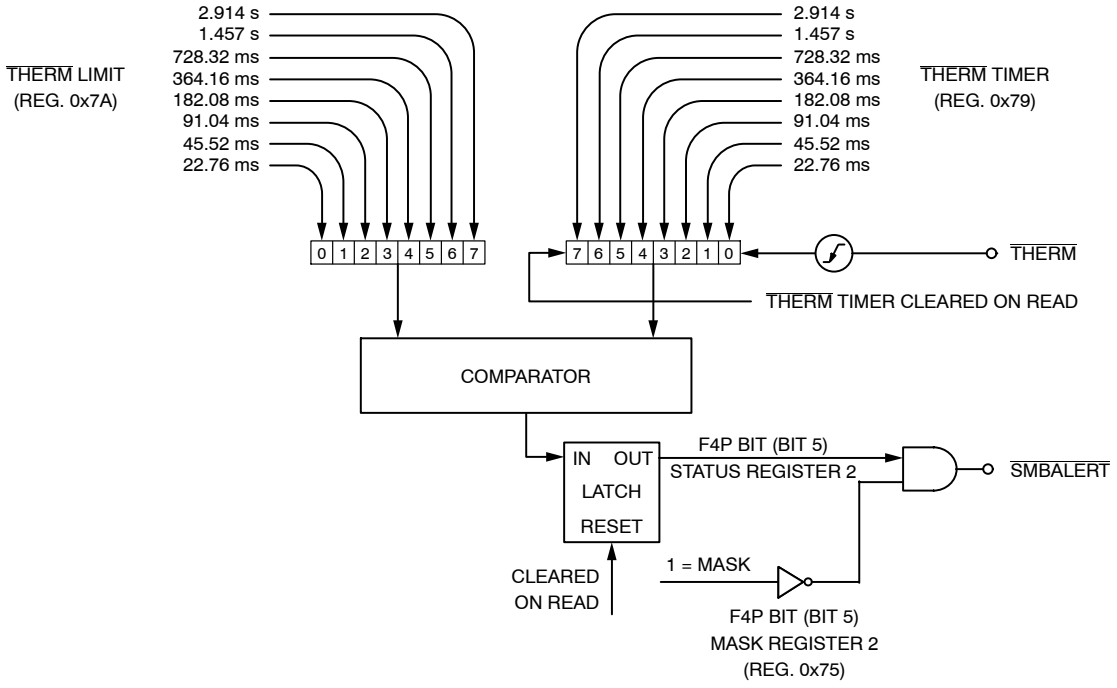


Figure 31. Functional Diagram of THERM Monitoring Circuitry

Configuring THERM Behavior

1. Configure the relevant pin as the THERM timer input:
   Setting Bit 1 (THERM timer enable) of Configuration Register 3 (0x78) enables the THERM timer monitoring functionality. This is disabled on Pin 9 by default.
   Setting Bit 0 and Bit 1 (Pin 9 Func) of Configuration Register 4 (0x7D) enables THERM timer/output functionality on Pin 9 (Bit 1, THERM, of Configuration Register 3 must also be set). Pin 9 can also be used as TACH4.
2. Select the desired fan behavior for THERM timer events:
   Assuming that the fans are running, setting Bit 2 (BOOST bit) of Configuration Register 3 (0x78) causes all fans to run at 100% duty cycle whenever THERM is asserted. This allows fail-safe system cooling. If this bit is 0, the fans run at their current settings and are not affected by THERM events. If the fans are not already running when THERM is asserted, the fans do not run to full speed.
3. Select whether THERM timer events should generate SMBALERT interrupts:
   When set, Bit 5 (F4P) of Mask Register 2 (0x75) masks SMBALERTs when the THERM timer limit value is exceeded. This bit should be cleared if SMBALERT based on THERM events are required.
4. Select a suitable THERM limit value:
   This value determines whether an SMBALERT is generated upon the first THERM assertion, or if only a cumulative THERM assertion time limit is exceeded. A value of 0x00 causes an SMBALERT to be generated upon the first THERM assertion.
5. Select a THERM monitoring time:
   This value specifies how often OS or BIOS level software checks the THERM timer. For example,

BIOS could read the $\overline{\text{THERM}}$ timer once an hour to determine the cumulative $\overline{\text{THERM}}$ assertion time. If, for example, the total $\overline{\text{THERM}}$ assertion time is <22.76 ms in Hour 1, >182.08 ms in Hour 2, and >2.914 sec in Hour 3, this can indicate that system performance is degrading significantly, because $\overline{\text{THERM}}$ is asserting more frequently on an hourly basis.

Alternatively, OS or BIOS level software can timestamp when the system is powered on. If an $\overline{\text{SMBALERT}}$ is generated because the $\overline{\text{THERM}}$ timer limit has been exceeded, another timestamp can be taken. The difference in time can be calculated for a fixed $\overline{\text{THERM}}$ timer limit. For example, if it takes one week for a $\overline{\text{THERM}}$ timer limit of 2.914 sec to be exceeded and the next time it takes only 1 hour, this is an indication of a serious degradation in system performance.

Configuring the $\overline{\text{THERM}}$ Pin as an Output

In addition to monitoring $\overline{\text{THERM}}$ as an input, the ADT7467 can optionally drive $\overline{\text{THERM}}$ low as an output. In cases where $\overline{\text{PROCHOT}}$ is bidirectional, $\overline{\text{THERM}}$ can be used to throttle the processor by asserting $\overline{\text{PROCHOT}}$. The user can preprogram system-critical thermal limits. If the temperature exceeds a thermal limit by 0.25°C, $\overline{\text{THERM}}$ asserts low. If the temperature is still above the thermal limit on the next monitoring cycle, $\overline{\text{THERM}}$ stays low. $\overline{\text{THERM}}$ remains asserted low until the temperature is equal to or below the thermal limit. Because the temperature for that channel is measured only once for every monitoring cycle, it is guaranteed to remain low for at least one monitoring cycle after $\overline{\text{THERM}}$ is asserted.

The $\overline{\text{THERM}}$ pin can be configured to assert low if the Remote 1, local, or Remote 2 $\overline{\text{THERM}}$ temperature limits are exceeded by 0.25°C. The $\overline{\text{THERM}}$ temperature limit registers are at Register 0x6A, Register 0x6B, and Register 0x6C, respectively. Setting Bit 3 of Register 0x5F, Register 0x60, and Register 0x61 enables the $\overline{\text{THERM}}$ output feature for the Remote 1, local, and Remote 2 temperature channels, respectively. Figure 32 shows how the $\overline{\text{THERM}}$ pin asserts low as an output in the event of a critical overtemperature.

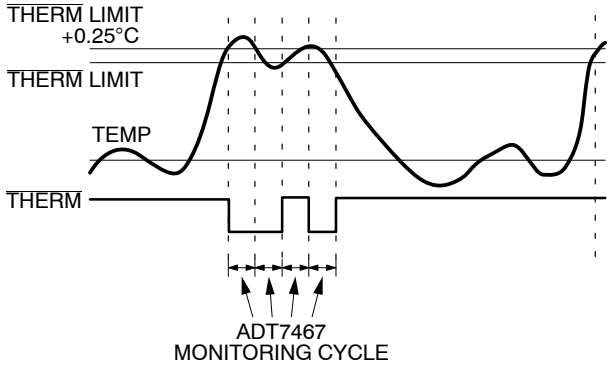


Figure 32. Asserting $\overline{\text{THERM}}$ as an Output, Based on Tripping $\overline{\text{THERM}}$ Limits

An alternative method of disabling $\overline{\text{THERM}}$ is to program the $\overline{\text{THERM}}$ temperature limit to −64°C or less in Offset 64 mode, or to −128°C or less in twos complement mode; therefore, for $\overline{\text{THERM}}$ temperature limit values less than −64°C or −128°C, respectively, $\overline{\text{THERM}}$ is disabled.

Active Cooling

Driving the Fan using PWM Control

The ADT7467 uses pulse-width modulation (PWM) to control fan speed. This relies on varying the duty cycle (or on/off ratio) of a square wave applied to the fan to vary the fan speed. The external circuitry required to drive a fan using PWM control is extremely simple. For 4-wire fans, the PWM drive may need only a pull-up resistor. In many cases, the 4-wire fan PWM input has a built-in pull-up resistor.

The ADT7467 PWM frequency can be set to a selection of low frequencies or a single high PWM frequency. The low frequency options are usually used for 2-wire and 3-wire fans, and the high frequency option is usually used for 4-wire fans.

For 2-wire or 3-wire fans, a single N-channel MOSFET is the only drive device required. The specifications of the MOSFET depend on the maximum current required by the fan being driven. Typical notebook fans draw a nominal 170 mA; therefore, SOT devices can be used where board space is a concern. In desktops, fans can typically draw 250 mA to 300 mA each. If you drive several fans in parallel from a single PWM output or drive larger server fans, the MOSFET must handle the higher current requirements. The only other stipulation is that the MOSFET have a gate voltage drive of V_{GS} < 3.3 V for direct interfacing to the PWMx pin. V_{GS} can be greater than 3.3 V as long as the pull-up on the gate is tied to 5 V. The MOSFET should also have a low on resistance to ensure that there is not significant voltage drop across the FET, which would reduce the voltage applied across the fan and, therefore, the maximum operating speed of the fan.

Figure 33 shows how to drive a 3-wire fan using PWM control.

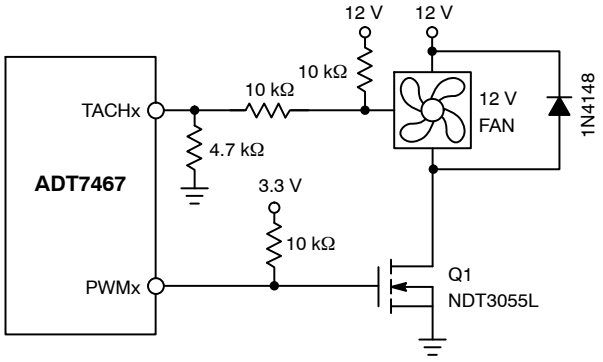


Figure 33. Driving a 3-wire Fan Using an N-channel MOSFET

Figure 33 uses a 10 kΩ pull-up resistor for the TACH signal. This assumes that the TACH signal is an open-collector from the fan. In all cases, the TACH signal from the fan must be kept below 5 V maximum to prevent damaging the ADT7467. If in doubt as to whether the fan used has an open-collector or totem pole TACH output, use one of the input signal conditioning circuits shown in the Fan Speed Measurement section.

Figure 34 shows a fan drive circuit using an NPN transistor such as a general-purpose MMBT2222. Although these devices are inexpensive, they tend to have much lower current handling capabilities and higher on resistance than MOSFETs. When choosing a transistor, care should be taken to ensure that it meets the fan's current requirements.

Ensure that the base resistor is chosen such that the transistor is saturated when the fan is powered on.

Because 4-wire fans are powered continuously, the fan speed is not switched on or off as with previous PWM driven/powered fans. This enables it to perform better than 3-wire fans, especially for high frequency applications. Figure 35 shows a typical drive circuit for 4-wire fans.

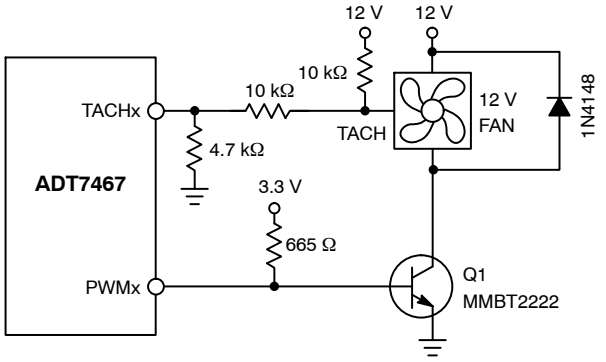


Figure 34. Driving a 3-wire Fan Using an NPN Transistor

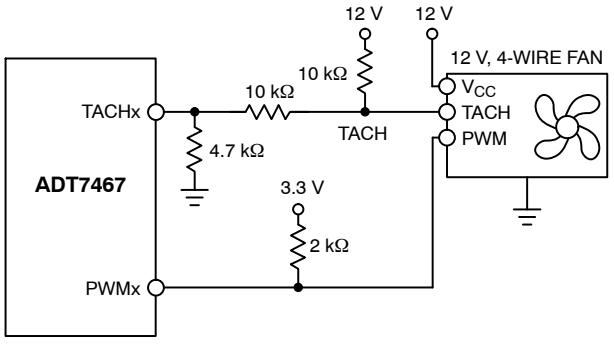


Figure 35. Driving a 4-wire Fan

Driving Two Fans from PWM3

The ADT7467 has four TACH inputs available for fan speed measurement, but only three PWM drive outputs. If a fourth fan is used in the system, it should be driven from the PWM3 output in parallel with the third fan. Figure 36 shows how to drive two fans in parallel using low cost NPN transistors. Figure 37 shows the equivalent circuit using a MOSFET.

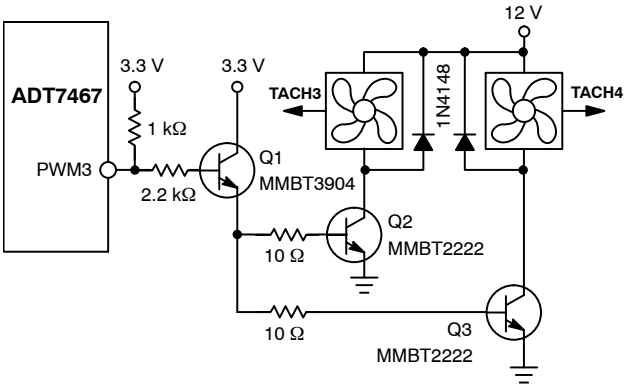


Figure 36. Interfacing Two Fans in Parallel to the PWM3 Output Using Low Cost NPN Transistors

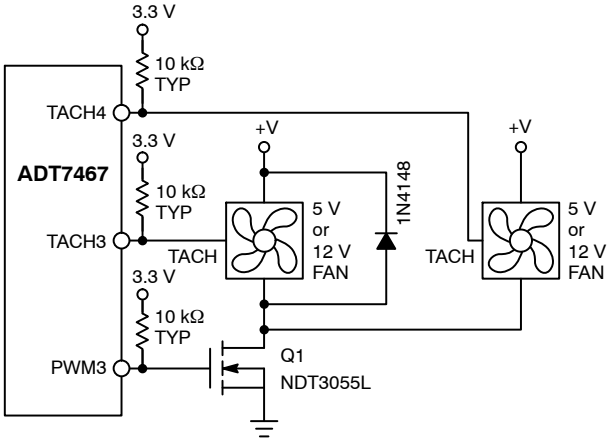


Figure 37. Interfacing Two Fans in Parallel to the PWM3 Output Using a Single N-channel MOSFET

Because the MOSFET can handle up to 3.5 A, it is simply a matter of connecting another fan directly in parallel with the first. Care should be taken in designing drive circuits with transistors and FETs to ensure that the PWM pins are not required to source current and that they sink less than the 5 mA maximum current specified on the data sheet.

Driving up to Three Fans from PWM3

TACH measurements for fans are synchronized to particular PWM channels; for example, TACH1 is synchronized to PWM1. TACH3 and TACH4 are both synchronized to PWM3; therefore, PWM3 can drive two fans. Alternatively, PWM3 can be programmed to synchronize TACH2, TACH3, and TACH4 to the PWM3 output. This allows PWM3 to drive two or three fans. In this case, the drive circuitry is as shown in Figure 36 and Figure 37. The SYNC bit in Register 0x62 enables this function.

Synchronization is not required in high frequency mode when used with 4-wire fans.

Table 25. SYNC: ENHANCE ACOUSTICS REGISTER 1 (REG. 0X62)

Bit	Mnemonic	Description
<4>	SYNC	1 Synchronizes TACH2, TACH3, and TACH4 to PWM3.

Driving 2-wire Fans

The ADT7467 can only support 2-wire fans when low frequency PWM mode is selected in Configuration Register 5, Bit 2. If this bit is not set to 1, the ADT7467 cannot measure the speed of 2-wire fans.

Figure 38 shows how a 2-wire fan can be connected to the ADT7467. This circuit allows the speed of a 2-wire fan to be measured, even though the fan has no dedicated TACH signal. A series resistor, R_{SENSE}, in the fan circuit converts the fan commutation pulses into a voltage, which is ac-coupled into the ADT7467 through the 0.01 μF capacitor. On-chip signal conditioning allows accurate monitoring of fan speed. The value of R_{SENSE} depends on the programmed input threshold and the current drawn by the fan. For fans drawing approximately 200 mA, a 2 Ω R_{SENSE} value is suitable when the threshold is programmed as 40 mV.

For fans that draw more current, such as larger desktop or server fans, R_{SENSE} can be reduced for the same programmed threshold. The smaller the threshold programmed, the better, because more voltage is developed across the fan and the fan spins faster. Figure 39 shows a typical plot of the sensing waveform at the TACHx pin.

Note that when the voltage spikes (either negative going or positive going) are more than 40 mV in amplitude, the fan speed can be reliably determined.

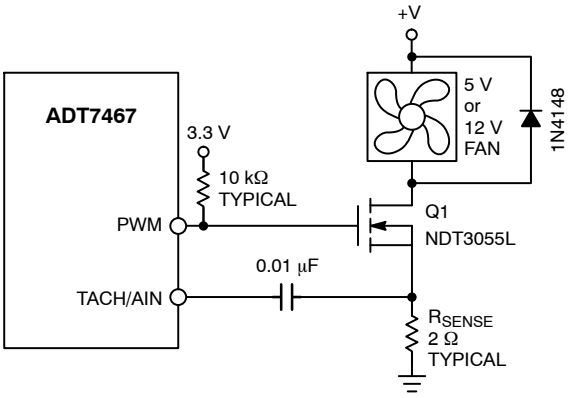


Figure 38. Driving a 2-wire Fan

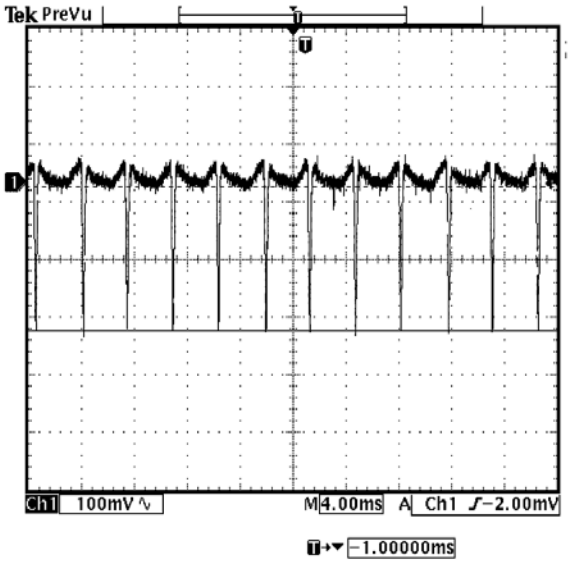


Figure 39. Fan Speed Sensing Waveform at TACHx Pin

Laying Out 2-wire and 3-wire Fans

Figure 40 shows how to lay out a common circuit arrangement for 2-wire and 3-wire fans. Some components are not populated, depending on whether a 2-wire or 3-wire fan is used.

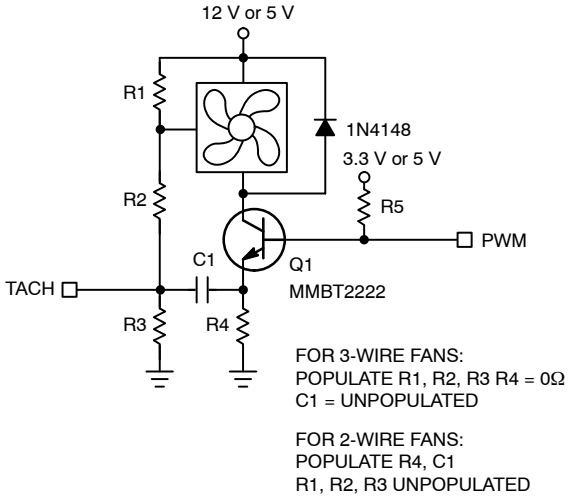


Figure 40. Planning for 2-wire or 3-wire Fans on a PCB

TACH Inputs

When configured as TACH inputs, Pin 4, Pin 6, Pin 7, and Pin 9 are open-drain TACH inputs intended for fan speed measurement.

Signal conditioning in the ADT7467 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 V to 5 V, even when V_{CC} is less than 5 V. In the event that these inputs are supplied from fan outputs that exceed 0 V to 5 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figure 41 to Figure 44 show circuits for most common fan TACH outputs. If the fan TACH output has a resistive pull-up to V_{CC}, it can be connected directly to the fan input, as shown in Figure 41.

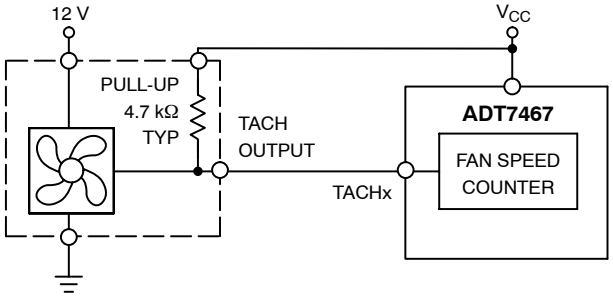


Figure 41. Fan with TACH Pull-up to V_{CC}

If the fan output has a resistive pull-up to 12 V (or another voltage that is greater than 5 V), the fan output can be clamped with a Zener diode, as shown in Figure 42. The Zener diode voltage should be chosen so that it is greater than the V_{IH} of the TACH input but less than 5 V, allowing for the voltage tolerance of the Zener. A value between 3 V and 5 V is suitable.

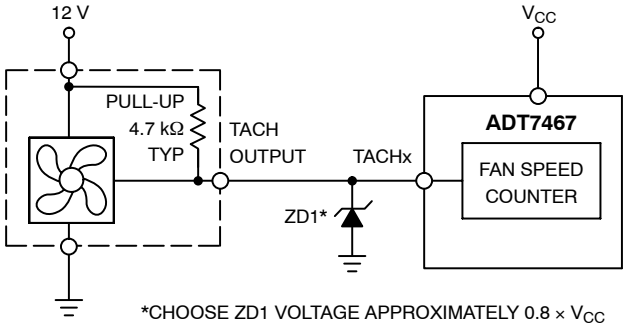


Figure 42. Fan with TACH Pull-up to Voltage > 5.0 V, (for Example, 12 V), Clamped with Zener Diode

If the fan has a strong pull-up (less than 1 kΩ) to 12 V or a totem-pole output, a series resistor can be added to limit the Zener current, as shown in Figure 43.

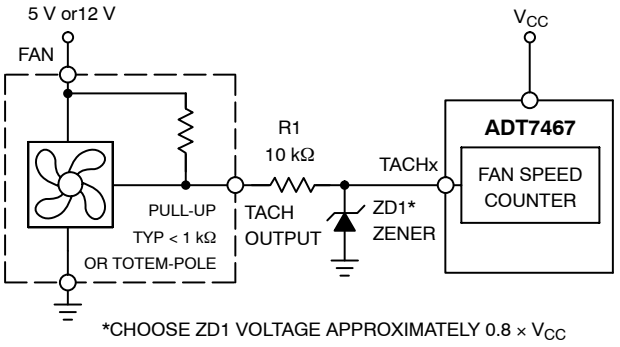


Figure 43. Fan with Strong TACH. Pull-up to > V_{CC} or Totem-Pole Output, Clamped with Zener and Resistor

Alternatively, a resistive attenuator can be used, as shown in Figure 44. R1 and R2 should be chosen such that

$$2\ V < V_{PULLUP} \times R2/(R_{PULLUP} + R1 + R2) < 5\ V \quad \text{(eq. 2)}$$

The fan inputs have an input resistance of nominally 160 kΩ to ground, which should be taken into account when calculating resistor values.

With a pull-up voltage of 12 V and a pull-up resistor of less than 1 kΩ, suitable values for R1 and R2 are 100 kΩ and 47 kΩ, respectively. This gives a high input voltage of 3.83 V.

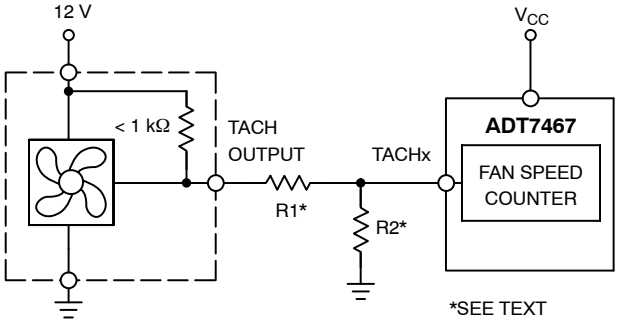


Figure 44. Fan with Strong TACH. Pull-up to > V_{CC} or Totem-Pole Output, Attenuated with R1/R2

Fan Speed Measurement

The fan counter does not count the fan TACH output pulses directly, because the fan speed could be less than 1000 RPM, and it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on-chip 90 kHz oscillator into the input of a 16-bit counter for N periods of the fan TACH output (see Figure 45); therefore, the accumulated count is actually proportional to the fan tachometer period and inversely proportional to the fan speed.

The number of pulses counted, N, is determined by the settings of Register 0x7B (TACH pulses per revolution

register). This register contains two bits for each fan, allowing counting of one, two (default), three, or four TACH pulses.

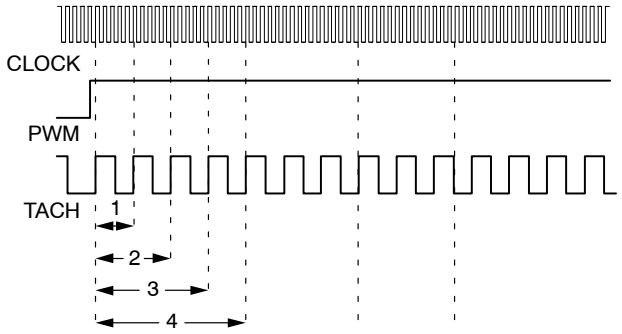


Figure 45. Fan Speed Measurement

Fan Speed Measurement Registers

The fan tachometer readings are 16-bit values consisting of a 2-byte read from the ADT7467.

Table 26. FAN SPEED MEASUREMENT REGISTERS

Register	Description	Default
0x28	TACH1 Low Byte	0x00
0x29	TACH1 High Byte	0x00
0x2A	TACH2 Low Byte	0x00
0x2B	TACH2 High Byte	0x00
0x2C	TACH3 Low Byte	0x00
0x2D	TACH3 High Byte	0x00
0x2E	TACH4 Low Byte	0x00
0x2F	TACH4 High Byte	0x00

Reading Fan Speed from the ADT7467

The measurement of fan speeds involves a 2-register read for each measurement. The low byte should be read first. This freezes the high byte until both high and low byte registers are read, preventing erroneous TACH readings. The fan tachometer reading registers report the number of 11.11 μs period clocks (90 kHz oscillator) gated to the fan speed counter from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse, assuming two pulses per revolution are being counted. Because the device is essentially measuring the fan TACH period, the higher the count value, the slower the fan runs. A 16-bit fan tachometer reading of 0xFFFF indicates either that the fan has stalled or is running very slowly (<100 RPM).

High limit > comparison performed

Because the actual fan TACH period is being measured, falling below a fan TACH limit by 1 sets the appropriate status bit and can be used to generate an $\overline{\text{SMBALERT}}$.

Fan TACH Limit Registers

The fan TACH limit registers are 16-bit values consisting of two bytes.

Table 27. FAN TACH LIMIT REGISTERS

Register	Description	Default
0x54	TACH1 Minimum Low Byte	0xFF
0x55	TACH1 Minimum High Byte	0xFF
0x56	TACH2 Minimum Low Byte	0xFF
0x57	TACH2 Minimum High Byte	0xFF
0x58	TACH3 Minimum Low Byte	0xFF
0x59	TACH3 Minimum High Byte	0xFF
0x5A	TACH4 Minimum Low Byte	0xFF
0x5B	TACH4 Minimum High Byte	0xFF

Fan Speed Measurement Rate

The fan TACH readings are normally updated once every second.

When set, the FAST bit (Bit 3) of Configuration Register 3 (0x78) updates the fan TACH readings every 250 ms.

If a fan is powered directly from 5 V or 12 V and is not driven by a PWM channel, its associated dc bit in Configuration Register 3 should be set. This allows TACH readings to be taken on a continuous basis for fans connected directly to a dc source. For optimal results, the associated dc bit should always be set when using 4-wire fans.

Calculating Fan Speed

Assuming a fan with two pulses per revolution (and two pulses per revolution being measured), fan speed is calculated by

Fan Speed (RPM) = (90,000 × 60)/Fan TACH Reading

where *Fan TACH Reading* is the 16-bit fan tachometer reading.

Example

TACH1 high byte (Register 0x29) = 0x17
TACH1 low byte (Register 0x28) = 0xFF

What is Fan 1 speed in RPM?

Fan 1 TACH Reading = 0x17FF = 6143 (decimal)
RPM = (f × 60)/Fan 1 TACH Reading
RPM = (90,000 × 60)/6143
Fan Speed = 879 RPM

Fan Pulses per Revolution

Different fan models can output either one, two, three, or four TACH pulses per revolution. Once the number of fan TACH pulses has been determined, it can be programmed into the fan pulses per revolution register (0x7B) for each fan. Alternatively, this register can be used to determine the

number of pulses per revolution output for a given fan. By plotting fan speed measurements at 100% speed with different pulses per revolution setting, the smoothest graph with the lowest ripple determines the correct pulses per revolution value.

Table 28. FAN PULSES/REVOLUTION REGISTER (REG. 0X7B)

Bit	Mnemonic	Description
<1:0>	FAN1 Default	2 Pulses per Revolution
<3:2>	FAN2 Default	2 Pulses per Revolution
<5:4>	FAN3 Default	2 Pulses per Revolution
<7:6>	FAN4 Default	2 Pulses per Revolution

Table 29. FAN PULSES/REVOLUTION REGISTER BIT VALUES

Value	Description
00	1 Pulse per Revolution
01	2 Pulses per Revolution
10	3 Pulses per Revolution
11	4 Pulses per Revolution

2-wire Fan Speed Measurements (Low Frequency Mode Only)

The ADT7467 is capable of measuring the speed of 2-wire fans, that is, fans without TACH outputs. To do this, the fan must be interfaced as shown in the Driving 2-Wire Fans section. In this case, the TACH inputs should be reprogrammed as analog inputs, AIN.

Table 30. CONFIGURATION REGISTER 2 (REG. 0X73)

Bit	Mnemonic	Description
3	AIN4	1 indicates that Pin 9 is reconfigured to measure the speed of a 2-wire fan using an external sensing resistor and coupling capacitor.
2	AIN3	1 indicates that Pin 4 is reconfigured to measure the speed of a 2-wire fan using an external sensing resistor and coupling capacitor.
1	AIN2	1 indicates that Pin 7 is reconfigured to measure the speed of a 2-wire fan using an external sensing resistor and coupling capacitor.
0	AIN1	1 indicates that Pin 6 is reconfigured to measure the speed of a 2-wire fan using an external sensing resistor and coupling capacitor.

AIN Switching Threshold

Having configured the TACH inputs as AIN inputs for 2-wire measurements, a user can select the sensing threshold for the AIN signal.

Table 31. CONFIGURATION REGISTER 4 (REG. 0X7D)

Bit	Mnemonic	Description
<3:2>	AINL	Input threshold for 2-wire fan speed measurements. 00 = ±20 mV 01 = ±40 mV 10 = ±80 mV 11 = ±130 mV

Fan Spin-up

The ADT7467 has a unique fan spin-up function. It spins the fan at 100% PWM duty cycle until two TACH pulses are detected on the TACH input. Then, the PWM duty cycle goes to the expected running value, for example, 33%. The advantage is that fans have different spin-up characteristics and take different times to overcome inertia. The ADT7467 runs the fans just fast enough to overcome inertia and is quieter during spin-up than other fans programmed to spin up for a given spin-up time.

Fan Start-up Timeout

To prevent the generation of false interrupts as a fan spins up (because it is below running speed), the ADT7467 includes a fan start-up timeout function. During this time, the ADT7467 looks for two TACH pulses. If two TACH pulses are not detected, an interrupt is generated. Using Configuration Register 1 (0x40) Bit 5 (FSPDIS), the functionality of this bit can be changed (see the Disabling Fan Start-up Timeout section).

Table 32. PWM1 TO PWM3 CONFIGURATION (REG. 0X5C TO 0X5E)

Bit	Mnemonic	Description
<2:0>	SPIN	These bits control the start-up timeout for PWM1, PWM2, PWM3. 000 = No Start-up Timeout 001 = 100 ms 010 = 250 ms (Default) 011 = 400 ms 100 = 667 ms 101 = 1 s 110 = 2 s 111 = 4 s

Disabling Fan Start-up Timeout

Although a fan start-up makes fan spin-ups more quiet than fixed-time spin-ups, users can use fixed spin-up times. Setting Bit 5 (FSPDIS) to 1 in Configuration Register 1 (0x40) disables the spin-up for two TACH pulses, and the fan spins up for the fixed time selected in Register 0x5C to Register 0x5E.

PWM Logic State

The PWM outputs can be programmed high for 100% duty cycle (non-inverted) or programmed low for 100% duty cycle (inverted).

Table 33. PWM1 TO PWM3 CONFIGURATION (REG. 0X5C TO 0X5E) BITS

Bit	Mnemonic	Description
<4>	INV	0 = logic high for 100% PWM duty cycle 1 = logic low for 100% PWM duty cycle

Low Frequency Mode PWM Drive Frequency

The PWM drive frequency can be adjusted for the application. Register 0x5F to Register 0x61 configure the PWM frequency for PWM1 to PWM3, respectively. In high frequency mode, the PWM drive frequency is 22.5 kHz and cannot be changed.

Table 34. PWM1 FREQUENCY REGISTERS (REG. 0X5F TO 0X61)

Bit	Mnemonic	Description
<2:0>	FREQ	000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (Default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz

Fan Speed Control

The ADT7467 controls fan speed using two modes: automatic and manual.

In automatic fan speed control mode, fan speed is varied with temperature without CPU intervention once initial parameters are set up. The advantage of this is that if the system hangs, it is guaranteed that the system is protected from overheating. The automatic fan speed control incorporates a feature called dynamic T_{MIN} calibration. This feature reduces the design effort required to program the automatic fan speed control loop. For information on programming the automatic fan speed control loop and the dynamic T_{MIN} calibration, see the Automatic Fan Control Overview section.

In manual fan speed control mode, the ADT7467 allows the duty cycle of any PWM output to be manually adjusted. This can be useful if the user wants to change fan speed in software or adjust PWM duty cycle output for test purposes. Bits <7:5> of Register 0x5C to Register 0x5E (PWM Configuration) control the behavior of each PWM output.

Table 35. PWM1 TO PWM3 CONFIGURATION (REG. 0X5C TO 0X5E) BITS

Bit	Mnemonic	Description
<7:5>	BHVR	111 = Manual Mode

In manual fan speed control mode, each PWM output can be manually updated by writing to Register 0x30 through Register 0x32 (PWMx current duty cycle registers).

Programming the PWM Current Duty Cycle Registers

The PWM current duty cycle registers are 8-bit registers that allow the PWM duty cycle for each output to be set anywhere from 0% to 100% in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by

Value (decimal) = $PWM_{MIN}/0.39$

Example 1: For a PWM duty cycle of 50%,
Value (decimal) = 50/0.39 = 128 (decimal)
Value = 128 (decimal) or 0x80 (hexadecimal)

Example 2: For a PWM duty cycle of 33%,
Value (decimal) = 33/0.39 = 85 (decimal)
Value = 85 (decimal) or 0x54 (hexadecimal)

PWM Current Duty Cycle Registers

By reading the PWMx current duty cycle registers, the user can keep track of the current duty cycle on each PWM output even when the fans are running in automatic fan speed control mode or acoustic enhancement mode. See the Automatic Fan Control Overview section for details.

Table 36. PWM CURRENT DUTY CYCLE REGISTERS

Register	Description	Default
0x30	PWM1 Current Duty Cycle	0x00 (0%)
0x31	PWM2 Current Duty Cycle	0x00 (0%)
0x32	PWM3 Current Duty Cycle	0x00 (0%)

Miscellaneous Functions

Operating from 3.3 V Standby

The ADT7467 has been specifically designed to operate from a 3.3 V STANDBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. If using the dynamic T_{MIN} mode, lowering the core voltage of the processor changes the CPU temperature and changes the dynamics of the system under dynamic T_{MIN} control. Likewise, when monitoring $\overline{\text{THERM}}$, the $\overline{\text{THERM}}$ timer should be disabled during these states.

Dynamic T_{MIN} Control Register 1 (0x36) <1> V_{CCP}LO = 1

When the power is supplied from 3.3 V STANDBY and the V_{CCP} voltage drops below the V_{CCP} low limit, the following occurs:

1. Status Bit 1 (V_{CCP}) in Interrupt Status Register 1 is set.
2. $\overline{\text{SMBALERT}}$ is generated if enabled.
3. $\overline{\text{THERM}}$ monitoring is disabled. The $\overline{\text{THERM}}$ timer should hold its value prior to the S3 or S5 state.
4. Dynamic T_{MIN} control is disabled. This prevents T_{MIN} from being adjusted due to an S3 or S5 state.
5. The ADT7467 is prevented from shutting down.

Once the core voltage, V_{CCP}, goes above the V_{CCP} low limit, everything is re-enabled and the system resumes normal operation.

XNOR Tree Test Mode

The ADT7467 includes an XNOR tree test mode. This mode is useful for in-circuit test equipment at board-level testing. By applying stimulus to the pins included in the XNOR tree, it is possible to detect opens or shorts on the system board.

Figure 46 shows the signals that are exercised in the XNOR tree test mode. The XNOR tree test is invoked by setting Bit 0 (XEN) of the XNOR tree test enable register (0x6F).

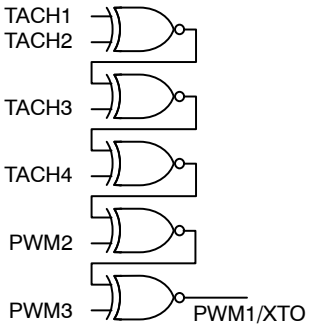


Figure 46. XNOR Tree Test

Power-On Default

When the ADT7467 is powered up, it polls the V_{CCP} input.

If V_{CCP} stays below 0.75 V (the system CPU power rail is not powered up), the ADT7467 assumes the functionality of the default registers after the ADT7467 is addressed via any valid SMBus transaction.

If V_{CC} goes high (the system processor power rail is powered up), a fail-safe timer begins to count down. If the ADT7467 is not addressed by a valid SMBus transaction before the fail-safe timeout (4.6 sec) lapses, the ADT7467 drives the fans to full speed. If the ADT7467 is addressed by a valid SMBus transaction after this point, the fans stop and the ADT7467 assumes its default settings and begins normal operation.

If V_{CCP} goes high (the system processor power rail is powered up), a fail-safe timer begins to count down. If the ADT7467 is addressed by a valid SMBus transaction before the fail-safe timeout (4.6 sec) lapses, the ADT7467 operates normally, assuming the functionality of all default registers. See the flow chart in Figure 47.

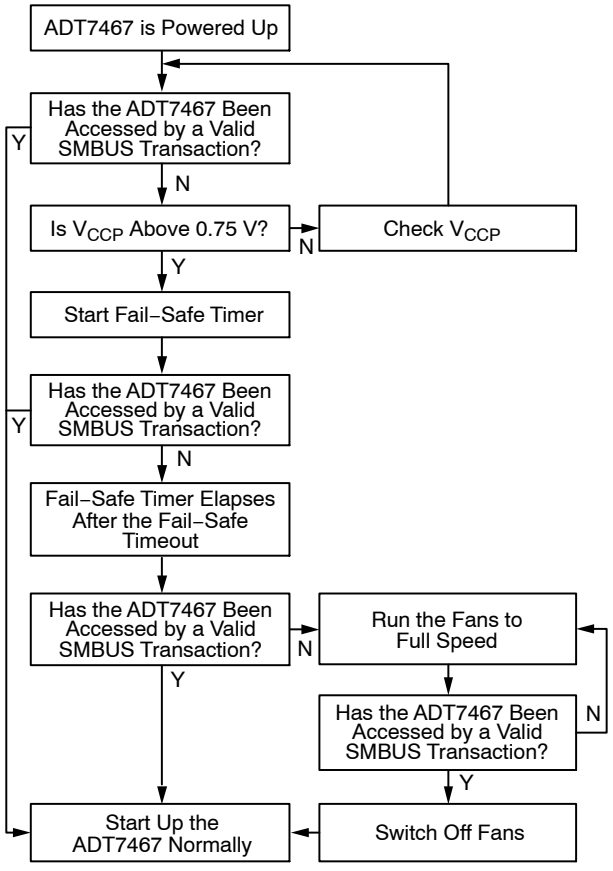


Figure 47. Power-On Flowchart

Automatic Fan Control Overview

The ADT7467 can automatically control the speed of fans based on the measured temperature. This is done independently of CPU intervention once initial parameters are set up.

The ADT7467 has a local temperature sensor and two remote temperature channels that can be connected to a CPU on-chip thermal diode (available on Intel® Pentium® class and other CPUs). These three temperature channels can be used as the basis for automatic fan speed control to drive fans using pulse-width modulation (PWM).

Automatic fan speed control reduces acoustic noise by optimizing fan speed according to accurately measured temperature. Reducing fan speed can also decrease system current consumption. The automatic fan speed control mode is very flexible due to the number of programmable parameters, including T_{MIN} and T_{RANGE}. The T_{MIN} and T_{RANGE} values for a temperature channel and, therefore, for a given fan are critical because they define the thermal characteristics of the system. Thermal validation of the system is one of the most important steps in the design process; therefore, these values should be selected carefully.

Figure 48 shows a top-level overview of the automatic fan control circuitry on the ADT7467. From a systems-level perspective, up to three system temperatures can be monitored and used to control three PWM outputs. The three PWM outputs can be used to control up to four fans. The ADT7467 allows the speed of four fans to be monitored. Each temperature channel has a thermal calibration block, allowing the designer to individually configure the thermal characteristics of each temperature channel. For example, one can decide to run the CPU fan when CPU temperature increases above 60°C and to run a chassis fan when the local temperature increases above 45°C. At this stage, the designer has not assigned these thermal calibration settings to a particular fan drive (PWM) channel. The right side of Figure 48 shows controls that are fan specific. The designer can individually control parameters such as minimum PWM duty cycle, fan speed failure thresholds, and even ramp control of the PWM outputs. Therefore, automatic fan control ultimately allows gracefully changing fan speed so that it is less perceptible to the system user.

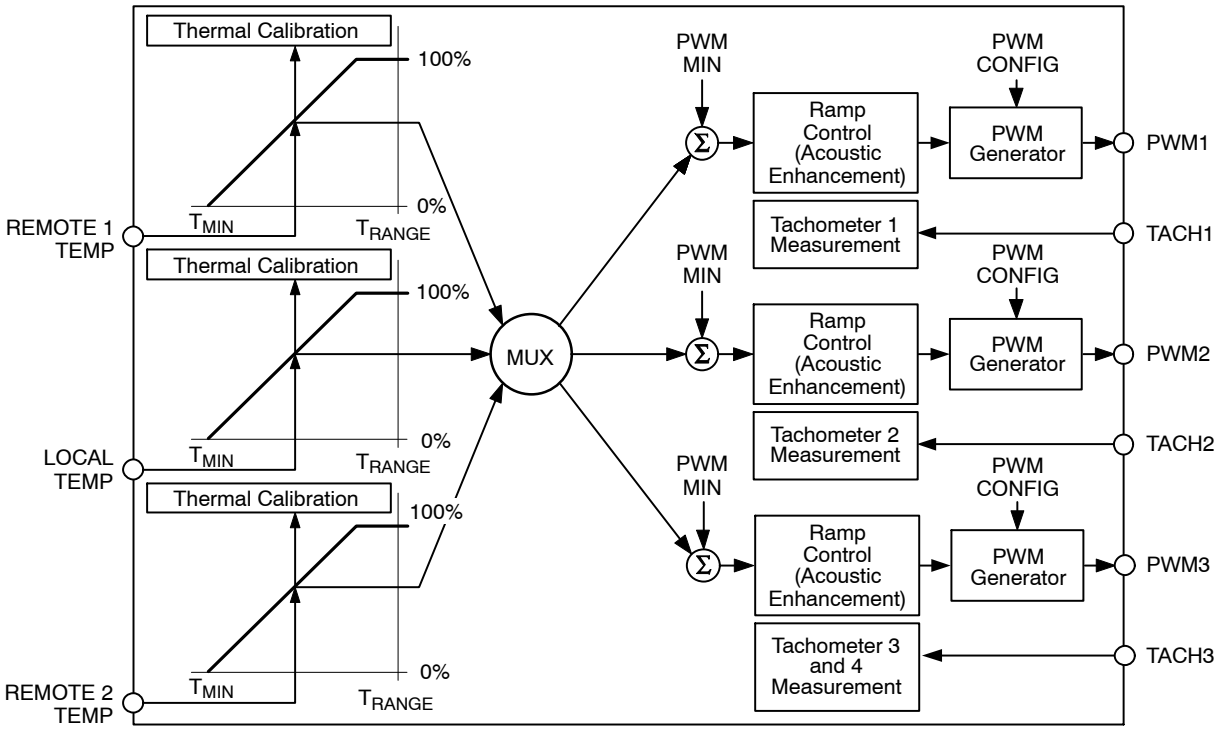


Figure 48. Automatic Fan Control Block Diagram

Dynamic T_{MIN} Control Mode

In addition to the automatic fan speed control mode, the ADT7467 has a mode that extends the basic automatic fan speed control loop. Dynamic T_{MIN} control allows the ADT7467 to intelligently adapt the system's cooling solution to optimize system performance or system acoustics, depending on user or design requirements. Use of dynamic T_{MIN} control alleviates the need to design for worst-case conditions, and it significantly reduces the time required for system design and validation.

Designing for Worst-case Conditions

System design must always allow for worst-case conditions. In PC design, the worst-case conditions include, but are not limited to, the following:

- Worst-case Altitude
  A computer can be operated at different altitudes. The altitude affects the relative air density, which alters the effectiveness of the fan cooling solution. For example, comparing 40°C air temperature at 10,000 ft. to 20°C air temperature at sea level, relative air density is increased by 40%. This means that at a given temperature, the fan can spin 40% slower and make less noise at sea level than it can at 10,000 ft.
- Worst-case Fan
  Due to manufacturing tolerances, fan speeds in RPM are normally quoted with a tolerance of ±20%. The designer should assume that the fan RPM is 20% below tolerance. This translates to reduced system airflow and elevated system temperature. Note that a difference of 20% in the fans' tolerance can negatively impact system acoustics because the fans run faster and generate more noise.
- Worst-case Chassis Airflow
  The same motherboard can be used in a number of different chassis configurations. The design of the chassis and the physical location of fans and components determine the system thermal characteristics. Moreover, for a given chassis, the addition of add-in cards, cables, and other system configuration options can alter the system airflow and reduce the effectiveness of the system cooling solution. The cooling solution can also be inadvertently altered by the end user. (For example, placing a computer against a wall can block the air ducts and reduce system airflow.)

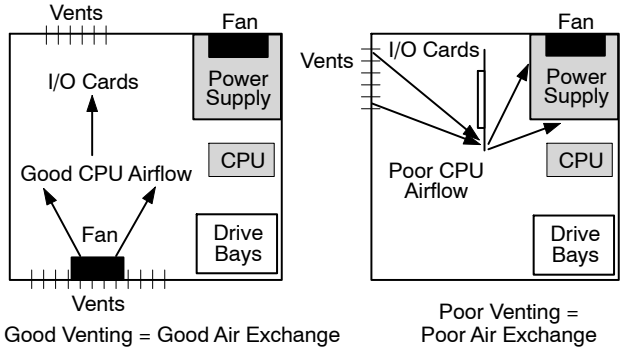


Figure 49. Chassis Airflow Issues

- Worst-case Processor Power Consumption
  Designing for worst-case CPU power consumption can result in a processor becoming overcooled, generating excess system noise.
- Worst-case Peripheral Power Consumption
  The tendency is to design to data sheet maximums for peripheral components (again overcooling the system).
- Worst-case Assembly
  Every system is unique because of manufacturing variations. Heat sinks may be loose fitting or slightly misaligned. Too much or too little thermal grease might be used, or variations in application pressure for thermal interface material could affect the efficiency of the thermal solution. Accounting for manufacturing variations in every system is difficult; therefore, the system must be designed for worst-case conditions.

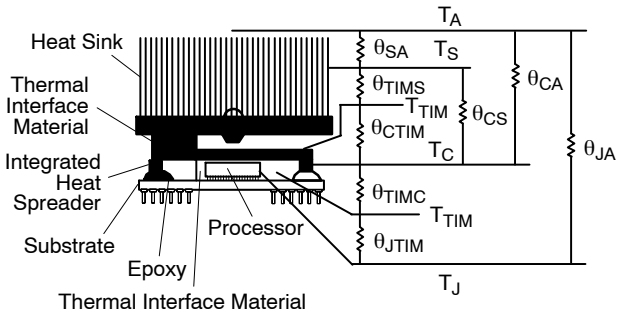


Figure 50. Thermal Model

Although a design usually accounts for such worst-case conditions, the system is almost never operated at worst-case conditions. An alternative to designing for the worst case is to use the dynamic T_{MIN} control function.

Dynamic T_{MIN} Control Overview

Dynamic T_{MIN} control mode builds on the basic automatic fan control loop by adjusting the T_{MIN} value based on system performance and measured temperature. Therefore, instead of designing for the worst case, the system thermals can be defined as operating zones. ADT7467 can self-adjust its fan control loop to maintain either an operating zone temperature or a system target temperature. For example, users can specify that the ambient temperature in a system be maintained at 50°C. If the temperature is below 50°C, the fans may not run or may run very slowly. If the temperature is higher than 50°C, the fans may throttle up.

The challenge presented by any thermal design is finding the right settings to suit the system's fan control solution. This can involve designing for the worst case, followed by weeks of system thermal characterization, and finally fan acoustic optimization (for psychoacoustic reasons). Optimizing the automatic fan control mode involves characterizing the system to determine the best T_{MIN} and T_{RANGE} settings for the control loop and the PWM_{MIN} value that produces the quietest fan speed setting. Using the ADT7467 dynamic T_{MIN} control mode, however, shortens the characterization time and alleviates tweaking the control loop settings because the device can self-adjust during system operation.

Dynamic T_{MIN} control mode is operated by specifying the operating zone temperatures required for the system. Associated with this control mode are three operating point registers, one for each temperature channel. This allows the system thermal solution to be broken down into distinct thermal zones. For example, CPU operating temperature is 70°C, VRM operating temperature is 80°C, and ambient

operating temperature is 50°C. The ADT7467 dynamically alters the control solution to maintain each zone temperature as closely as possible to its target operating point.

Operating Point Registers

Register 0x33, Remote 1 Operating Point = 0xA4 (100°C Default)

Register 0x34, Local Operating Point = 0xA4 (100°C Default)

Register 0x35, Remote 2 Operating Point = 0xA4 (100°C Default)

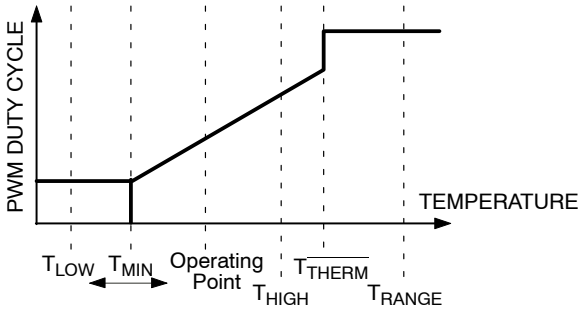


Figure 51. Dynamic T_{MIN} Control Loop

Figure 51 shows an overview of the parameters that affect the operation of the dynamic T_{MIN} control loop.

Table 37 provides a brief description of each parameter.

Table 37. T_{MIN} CONTROL LOOP PARAMETERS

Parameter	Description
T_{LOW}	If the temperature drops below the T_{LOW} limit, an error flag is set in a status register and an $\overline{SMBALERT}$ interrupt can be generated.
T_{HIGH}	If the temperature exceeds the T_{HIGH} limit, an error flag is set in a status register and an $\overline{SMBALERT}$ interrupt can be generated.
T_{MIN}	The temperature at which the fan turns on in automatic fan speed control mode.
Operating Point	The target temperature for a particular temperature zone. The ADT7467 attempts to maintain system temperature at approximately the operating point by adjusting the T_{MIN} parameter of the control loop.
T_{THERM}	If the temperature exceeds this critical limit, the fans can run at 100% for maximum cooling.
T_{RANGE}	Programs the PWM duty cycle vs. temperature control slope.

Dynamic T_{MIN} Control Programming

Because the dynamic T_{MIN} control mode is a basic extension of the automatic fan control mode, program the automatic fan control mode parameters as described in Step 1 to Step 8 in the Programming the Automatic Fan Speed Control Loop section, and then proceed with dynamic T_{MIN} control mode programming.

Programming the Automatic Fan Speed Control Loop

To more efficiently understand the automatic fan speed control loop, it is strongly recommended to use the ADT7467 evaluation board and software while reading this section.

This section provides the system designer with an understanding of the automatic fan control loop and provides step-by-step guidance on effectively evaluating and selecting critical system parameters. To optimize the system characteristics, the designer should consider several aspects of the system configuration, including the number of fans, where fans are located, and what temperatures are measured.

The mechanical or thermal engineer who is tasked with the system thermal characterization should also be involved at the beginning of the process.

STEP 1: Hardware Configuration

The motherboard sensing and control capabilities should be addressed in the early stages of designing a system, and decisions about how these capabilities are used should involve the system's thermal/mechanical engineer. Ask the following questions:

1. What ADT7467 functionality will be used?
   PWM2 or $\overline{SMBALERT}$
   TACH4 fan speed measurement or overtemperature $\overline{THERM}$ function
   5 V voltage monitoring or overtemperature $\overline{THERM}$ function
   12 V voltage monitoring or VID5 input
   The ADT7467 offers multifunctional pins that can be reconfigured to suit different system requirements and physical layouts. These multifunction pins are software programmable.
2. How many fans will be supported in the system, three or four? This influences the choice of whether to use the TACH4 pin or to reconfigure it for the $\overline{THERM}$ function.
3. Will the CPU fan be controlled using the ADT7467, or will it run at full speed 100% of the time?
   Running it at 100% frees up a PWM output, but the system is louder.
4. Where will the ADT7467 be physically located in the system?
   This influences the assignment of the temperature measurement channels to particular system thermal zones. For example, locating the ADT7467 close to the VRM controller circuitry allows the VRM temperature to be monitored using the local temperature channel.

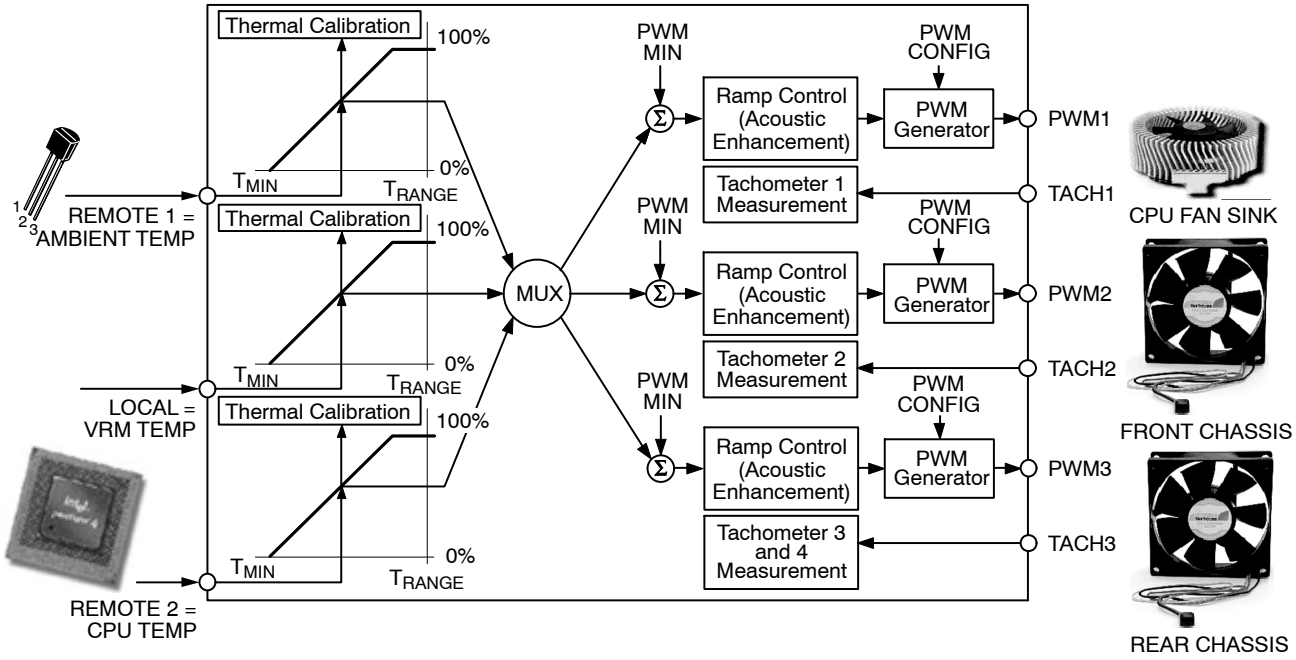


Figure 52. Hardware Configuration Example

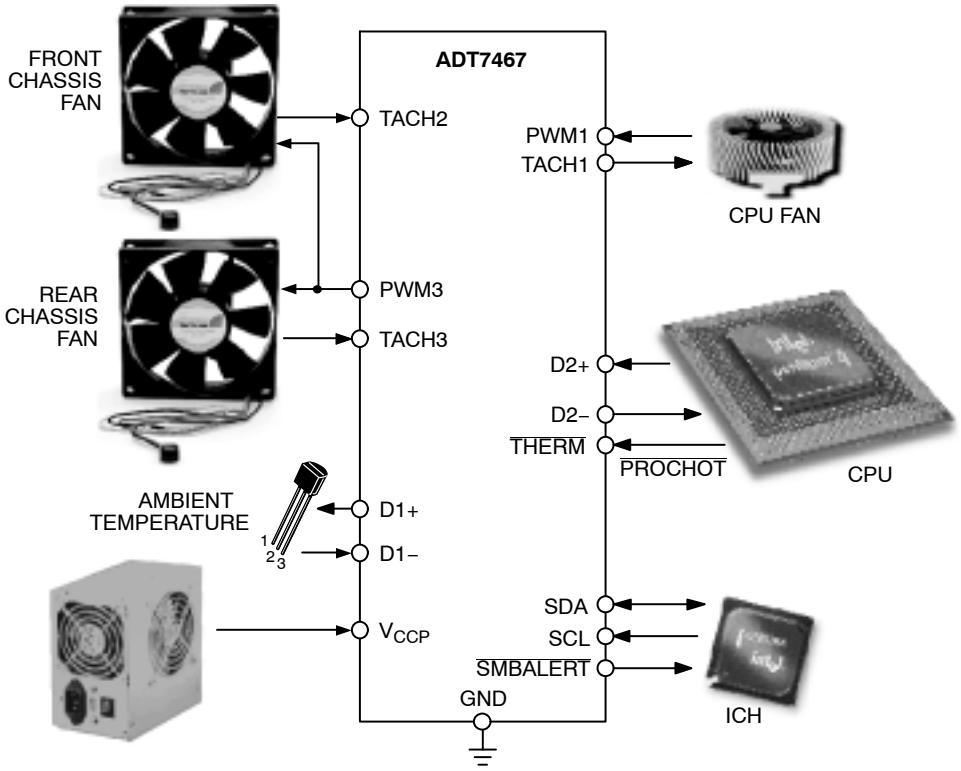


Figure 53. Recommended Implementation

Recommended Implementation

Configuring the ADT7467 as shown in Figure 53 provides the system designer with the following features:

- Two PWM outputs for control of up to three fans. (The front and rear chassis fans are connected in parallel.)
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 3.
- CPU core voltage measurement (V_{CORE}).
- CPU temperature measured using the Remote 1 temperature channel.
- Ambient temperature measured through the Remote 2 temperature channel.
- The bidirectional $\overline{\text{THERM}}$ pin allows monitoring $\overline{\text{PROCHOT}}$ output from, for example, an Intel® Pentium® 4 processor, or it can be used as an overtemperature $\overline{\text{THERM}}$ output.
- $\overline{\text{SMBALERT}}$ system interrupt output.

STEP 2: Configuring the MUX

After the system hardware configuration is determined, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels, but the behavior of the fans is also configurable. For example, fans can run using automatic fan control, can run manually (using software control), or can run at the fastest speed calculated by multiple temperature channels. The mux is the bridge between temperature measurement channels and the three PWM outputs.

Bits <7:5> (BHVR) of Register 0x5C, Register 0x5D, and Register 0x5E (PWM configuration registers) control the behavior of the fans connected to the PWM1, PWM2, and PWM3 outputs. The values selected for these bits determine how the mux connects a temperature measurement channel to a PWM output.

Automatic Fan Control Mux Options

<7:5> (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E

000 = Remote 1 temperature controls PWMx
001 = Local temperature controls PWMx
010 = Remote 2 temperature controls PWMx
101 = Fastest Speed calculated by Local and Remote 2 temperature controls PWMx
110 = Fastest Speed Calculated by All Three Temperature Channels Controls PWMx

The fastest speed calculated option pertains to controlling one PWM output based on multiple temperature channels. The thermal characteristics of the three temperature zones can be set to drive a single fan. An example would be the fan turning on when the Remote 1 temperature exceeds 60°C or when the local temperature exceeds 45°C.

Other Mux Options

<7:5> (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E

011 = PWMx Runs at Full speed
100 = PWMx disabled (default)
111 = manual mode. PWMx is run using software control. In this mode, PWM duty cycle registers (Register 0x30 to Register 0x32) are writable and control the PWM outputs.

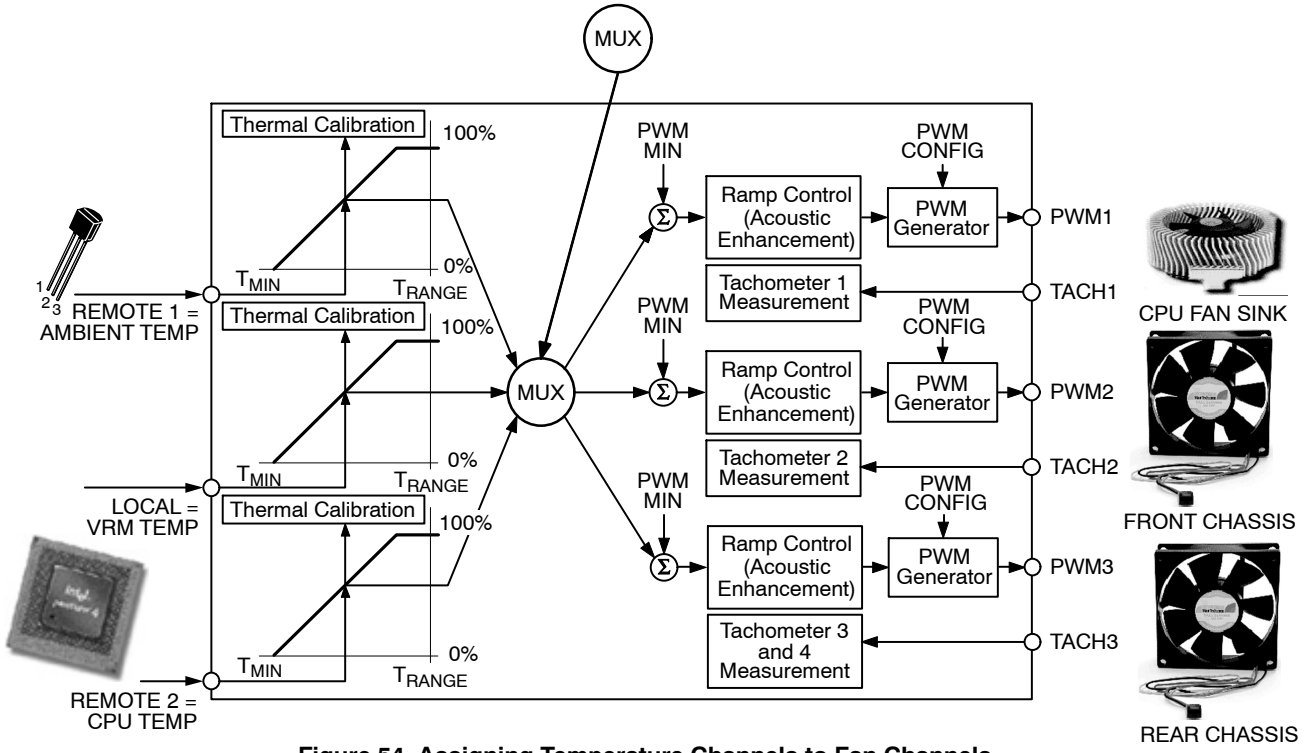


Figure 54. Assigning Temperature Channels to Fan Channels

Mux Configuration Example

This is an example of how to configure the mux in a system using the ADT7467 to control three fans. The CPU fan sink is controlled by PWM1, the front chassis fan is controlled by PWM2, and the rear chassis fan is controlled by PWM3. The mux is configured for the following fan control behavior:

- PWM1 (CPU fan sink) is controlled by the fastest speed calculated by the local (VRM temperature) and Remote 2 (processor) temperature. In this case, the CPU fan sink is also used to cool the VRM.
- PWM2 (front chassis fan) is controlled by the Remote 1 temperature (ambient).
- PWM3 (rear chassis fan) is controlled by the Remote 1 temperature (ambient).

Example Mux Settings

<7:5> (BHVR), PWM1 Configuration Register 0x5C
101 = fastest speed calculated by local and Remote 2 temperature controls PWM1

<7:5> (BHVR), PWM2 Configuration Register 0x5D
000 = Remote 1 temperature controls PWM2

<7:5> (BHVR), PWM3 Configuration Register 0x5E
000 = Remote 1 temperature controls PWM3

These settings configure the mux as shown in Figure 55.

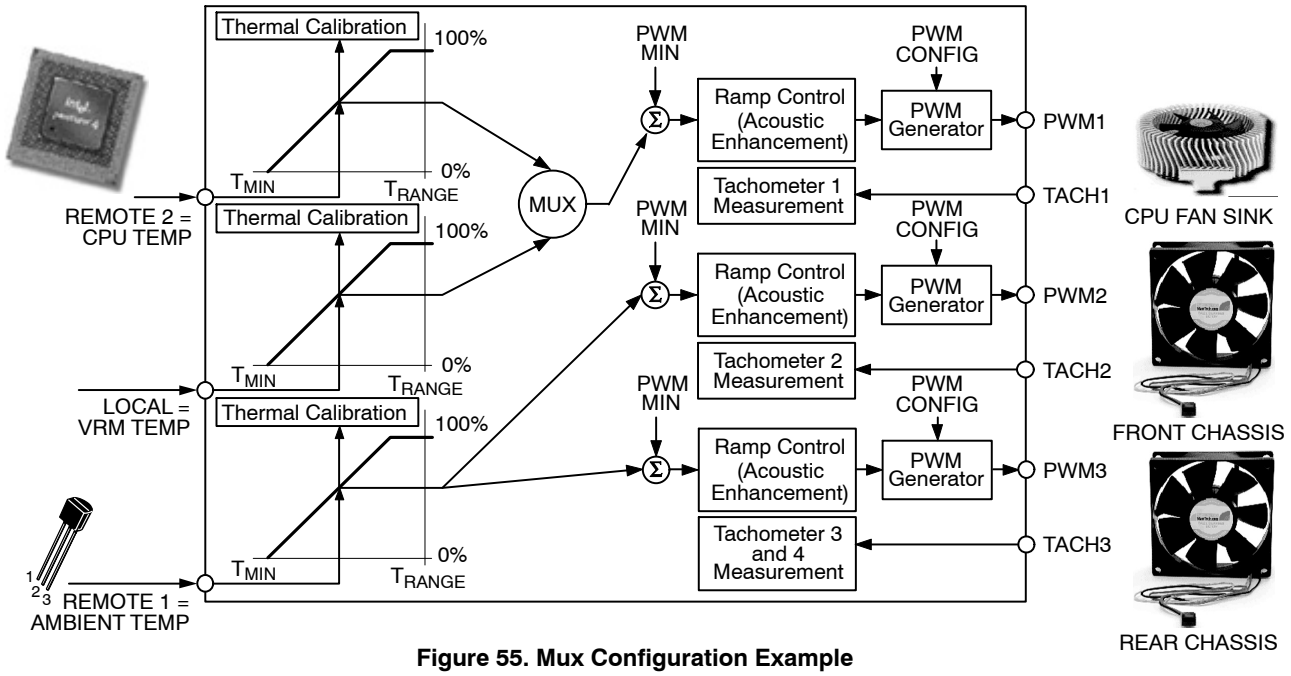


Figure 55. Mux Configuration Example

STEP 3: T_{MIN} Settings for Thermal Calibration Channels

T_{MIN} is the temperature at which the fans start to turn on when using automatic fan control mode. The speed at which the fan runs at T_{MIN} is programmed later. The T_{MIN} values chosen are temperature-channel specific, for example, 25°C for ambient channel, 30°C for VRM temperature, and 40°C for processor temperature.

T_{MIN} is an 8-bit value, either twos complement or Offset 64, that can be programmed in 1°C increments. There is a T_{MIN} register associated with each temperature measurement channel: Remote 1, local, and Remote 2 temperature. Once the T_{MIN} value is exceeded, the fan turns on and runs at the minimum PWM duty cycle. The fan turns off once the temperature has dropped below $T_{MIN} - T_{HYST}$.

To overcome fan inertia, the fan spins up until two valid TACH rising edges are counted. See the Fan Start-up Timeout section for more details. In some cases, primarily for psychoacoustic reasons, it is desirable that the fan never switch off below T_{MIN}. When set, Bits <7:5> of the Enhanced Acoustics Register 1 (0x62) keep the fans running at the PWM minimum duty cycle if the temperature falls below T_{MIN}.

T_{MIN} Registers

Register 0x67, Remote 1 temperature T_{MIN} = 0x9A (90°C)

Register 0x68, Local temperature T_{MIN} = 0x9A (90°C)

Register 0x69, Remote 2 temperature T_{MIN} = 0x9A (90°C)

Enhanced Acoustics Register 1 (0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle when the temperature is below $T_{MIN} - T_{HYST}$.

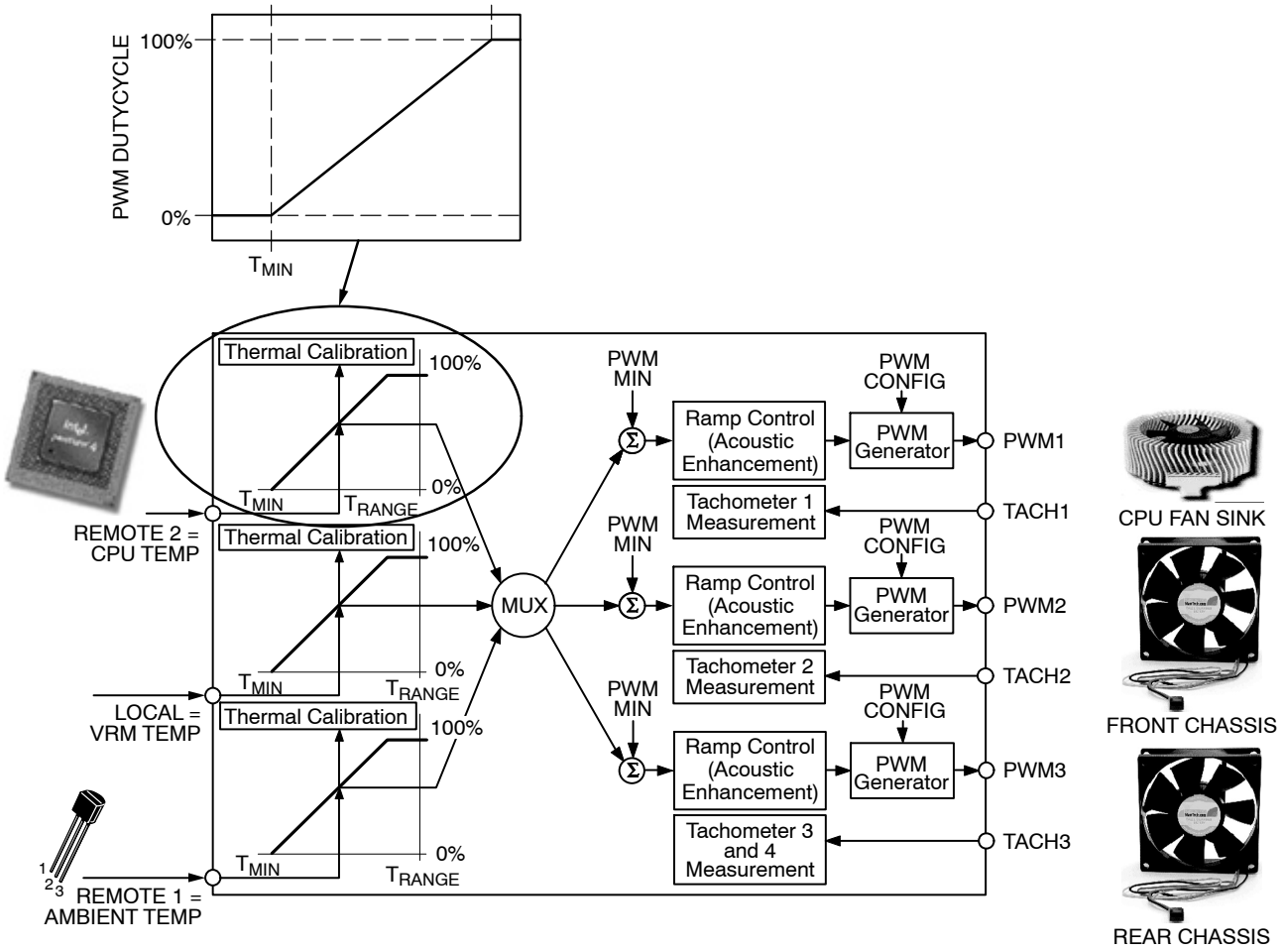


Figure 56. Understanding the T_{MIN} Parameter

STEP 4: PWM_{MIN} for PWM (Fan) Outputs

PWM_{MIN} is the minimum PWM duty cycle at which each fan in the system runs. It is also the start speed for each fan in automatic fan control mode when the temperature rises above T_{MIN}. For maximum system acoustic benefit, PWM_{MIN} should be as low as possible. Depending on the fan used, the PWM_{MIN} setting is usually in the 20% to 33% duty cycle range. This value can be found through fan validation.

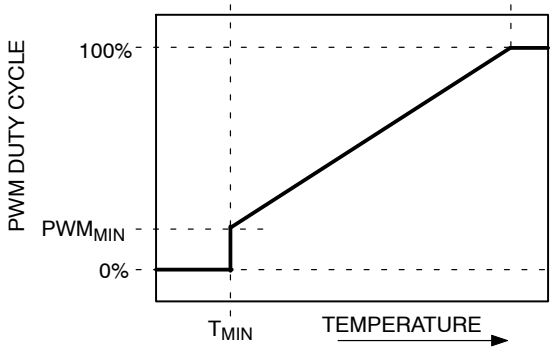


Figure 57. PWM_{MIN} Determines Minimum PWM Duty Cycle

More than one PWM output can be controlled from a single temperature measurement channel. For example, Remote 1 temperature can control PWM1 and PWM2 outputs. If two fans are used on PWM1 and PWM2, each fan's characteristics can be set up differently. As a result, Fan 1 driven by PWM1 can have a different PWM_{MIN} value than that of Fan 2 connected to PWM2. In Figure 58, $PWM1_{MIN}$ (front fan) is turned on at a minimum duty cycle of 20%, and $PWM2_{MIN}$ (rear fan) turns on at a minimum of 40% duty cycle; however, both fans turn on at the same temperature, defined by T_{MIN}.

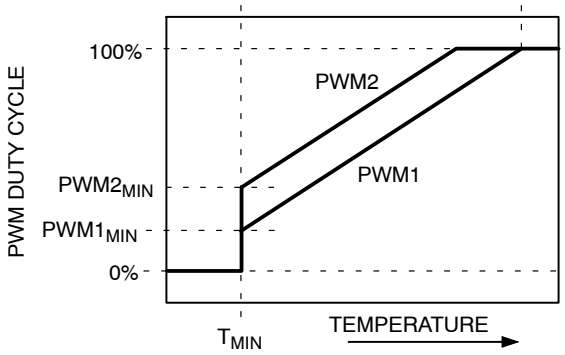


Figure 58. Operating Two Fans from a Single Temperature Channel

Programming the PWM_{MIN} Registers

The PWM_{MIN} registers are 8-bit registers that allow the minimum PWM duty cycle for each output to be configured from 0% to 100%. This allows the minimum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by:

Value (decimal) = PWM_{MIN}/0.39%

Example 1: For a minimum PWM duty cycle of 50%,

Value (decimal) = 50%/0.39% = 128 (decimal)
Value = 128 (decimal) or 0x80 (hexadecimal)

Example 2: For a minimum PWM duty cycle of 33%,

Value (decimal) = 33%/0.39% = 85 (decimal)
Value = 85 (decimal)l or 0x54 (hexadecimal)

PWM_{MIN} Registers

Register 0x64, PWM1 minimum duty cycle = 0x80 (50% default)
Register 0x65 PWM2 minimum duty cycle = 0x80 (50% default)
Register 0x66, PWM3 minimum duty cycle = 0x80 (50% default)

Fan Speed and PWM Duty Cycle

The PWM duty cycle does not directly correlate to fan speed in RPM. Running a fan at 33% PWM duty cycle does not equate to running the fan at 33% speed. Driving a fan at 33% PWM duty cycle runs the fan at closer to 50% of its full speed, because fan speed as a percentage of RPM generally relates to the square root of the PWM duty cycle. Given a PWM square wave as the drive signal, fan speed in RPM approximates to

$$\%\ \text{fan speed} = \sqrt{\text{PWM duty cycle} \times 10}$$

STEP 5: PWM_{MAX} for PWM (Fan) Outputs

PWM_{MAX} is the maximum duty cycle that each fan in the system runs at during the automatic fan speed control loop. For maximum system acoustic benefit, PWM_{MAX} should be as low as possible but capable of keeping the processor below its maximum temperature limit, even in a worst-case scenario. If the $\overline{\text{THERM}}$ temperature limit is exceeded, the fans are still boosted to 100% for fail-safe cooling.

There is a PWM_{MAX} limit for each fan channel. The default value of this register is 0xFF and, therefore, has no effect unless it is programmed.

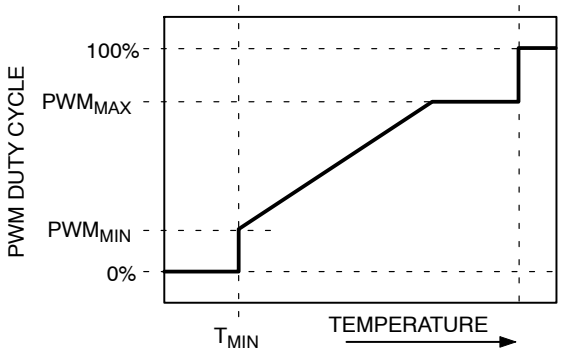


Figure 59. PWM_{MAX} Determines Maximum PWM Duty Cycle Below the $\overline{\text{THERM}}$ Temperature Limit

Programming the PWM_{MAX} Registers

The PWM_{MAX} registers are 8-bit registers that allow the maximum PWM duty cycle for each output to be configured from 0% to 100%. This allows the maximum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MAX} register is given by

Value (decimal) = PWM_{MAX}/0.39%

Example 1: For a maximum PWM duty cycle of 50%,
Value (decimal) = 50%/0.39% = 128 (decimal)
Value = 128 (decimal) or 0x80 (hexadecimal)

Example 2: For a minimum PWM duty cycle of 75%,
Value (decimal) = 75%/0.39% = 192 (decimal)
Value = 192 (decimal) or 0xC0 (hexadecimal)

PWM_{MAX} Registers

Register 0x38, PWM1 maximum duty cycle = 0xFF (100% default)

Register 0x39, PWM2 maximum duty cycle = 0xFF (100% default)

Register 0x3A, PWM3 maximum duty cycle = 0xFF (100% default)

See the Fan Speed and PWM Duty Cycle section.

STEP 6: T_{RANGE} for Temperature Channels

T_{RANGE} is the range of temperature over which automatic fan control occurs once the programmed T_{MIN} temperature has been exceeded. T_{RANGE} is a temperature slope, not an arbitrary value, that is, a T_{RANGE} of 40°C holds true only for PWM_{MIN} = 33%. If PWM_{MIN} is increased or decreased, the effective T_{RANGE} changes.

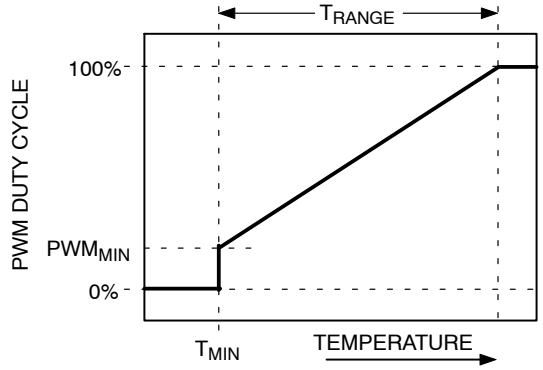


Figure 60. T_{RANGE} Parameter Affects Cooling Slope

The T_{RANGE} or fan control slope is determined by the following procedure:

1. Determine the maximum operating temperature for that channel (for example, 70°C).
2. Through experimentation, determine the fan speed (PWM duty cycle value) that does not exceed the temperature at the worst-case operating points. (For example, 70°C is reached when the fans are running at 50% PWM duty cycle.)
3. Determine the slope of the required control loop to meet these requirements.
4. The ADT7467 evaluation software can graphically program and visualize this functionality. Ask your local Analog Devices sales representative for details.

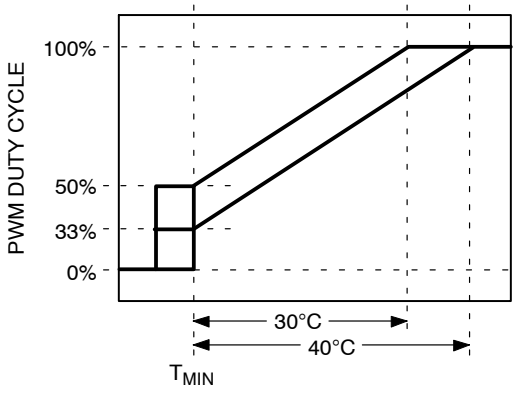


Figure 61. Adjusting PWM_{MIN} Affects T_{RANGE}

T_{RANGE} is implemented as a slope, which means that as PWM_{MIN} is changed, T_{RANGE} changes, but the actual slope remains the same. The higher the PWM_{MIN} value, the smaller the effective T_{RANGE}, that is, the fan reaches full speed (100%) at a lower temperature.

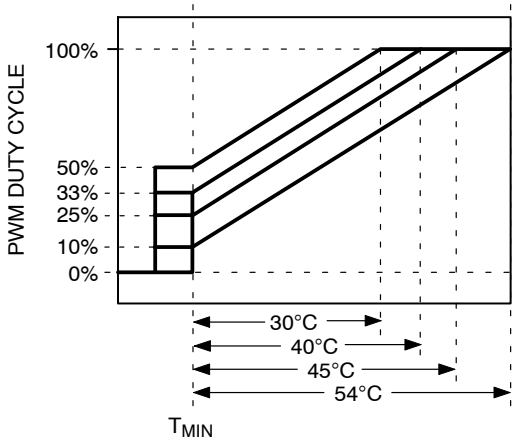


Figure 62. Increasing PWM_{MIN} Changes Effective T_{RANGE}

For a given T_{RANGE} value, the temperature at which the fan runs at full speed, which varies with the PWM_{MIN} value, can be easily calculated.

$T_{MAX} = T_{MIN} + (Max\ DC - Min\ DC) \times T_{RANGE}/170$

where:

T_{MAX} is the temperature at which the fan runs full speed.
T_{MIN} is the temperature at which the fan turns on.
Max DC is the maximum duty cycle (100%) = 255 decimal.
Min DC is equal to PWM_{MIN}.
T_{RANGE} is the duty PWM duty cycle vs. temperature slope.

Example 1:
Calculate T, given that T_{MIN} = 30°C, T_{RANGE} = 40°C, and PWM_{MIN} = 10% duty cycle = 26 (decimal).

$T_{MAX} = T_{MIN} + (Max\ DC - Min\ DC) \times T_{RANGE}/170$
T_{MAX} = 30°C + (100% − 10%) × 40°C/170
T_{MAX} = 30°C + (255 − 26) × 40°C/170
T_{MAX} = 84°C (Effective T_{RANGE} = 54°C)

Example 2:
Calculate T_{MAX}, given that T_{MIN} = 30°C, T_{RANGE} = 40°C, and PWM_{MIN} = 25% duty cycle = 64 (decimal).

$T_{MAX} = T_{MIN} + (Max\ DC - Min\ DC) \times T_{RANGE}/170$
T_{MAX} = 30°C + (100% − 25%) × 40°C/170
T_{MAX} = 30°C + (255 − 64) × 40°C/170
T_{MAX} = 75°C (Effective T_{RANGE} = 45°C)

Example 3:
Calculate T_{MAX}, given that T_{MIN} = 30°C, T_{RANGE} = 40°C, and PWM_{MIN} = 33% duty cycle = 85 (decimal).

$T_{MAX} = T_{MIN} + (Max\ DC - Min\ DC) \times T_{RANGE}/170$
T_{MAX} = 30°C + (100% − 33%) × 40°C/170
T_{MAX} = 30°C + (255 − 85) × 40°C/170
T_{MAX} = 70°C (Effective T_{RANGE} = 40°C)

Example 4:
Calculate T_{MAX}, given that T_{MIN} = 30°C, T_{RANGE} = 40°C, and PWM_{MIN} = 50% duty cycle = 128 (decimal).

$T_{MAX} = T_{MIN} + (Max\ DC - Min\ DC) \times T_{RANGE}/170$
T_{MAX} = 30°C + (100% − 50%) × 40°C/170

T_{MAX} = 30°C + (255 − 128) × 40°C/170
T_{MAX} = 60°C (Effective T_{RANGE} = 30°C)

Selecting a T_{RANGE} Slope

The T_{RANGE} value can be selected for each temperature channel: Remote 1, local, and Remote 2 temperature. Bits <7:4> (T_{RANGE}) of Register 0x5F to Register 0x61 define the T_{RANGE} value for each temperature channel.

Table 38. SELECTING A T_{RANGE} VALUE

Bits <7:4> (Note 1)	T_{RANGE} (°C)
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32 (default)
1101	40
1110	53.33
1111	80

1. Register 0x5F configures Remote 1 T_{RANGE}.
Register 0x60 configures local T_{RANGE}.
Register 0x61 configures Remote 2 T_{RANGE}.

Summary of T_{RANGE} Function

When using the automatic fan control function, the temperature at which the fan reaches full speed can be calculated by

$$T_{MAX} = T_{MIN} + T_{RANGE} \quad \text{(eq. 1)}$$

Equation 1 holds true only when PWM_{MIN} is equal to 33% PWM duty cycle.

Increasing or decreasing PWM_{MIN} changes the effective T_{RANGE}, but the fan control still follows the same PWM duty cycle to temperature slope. The effective T_{RANGE} for a PWM_{MIN} value can be calculated using Equation 2:

$$T_{MAX} = T_{MIN} + (\text{Max DC} - \text{Min DC}) \times T_{RANGE}/170 \quad \text{(eq. 2)}$$

where:
$(Max\ DC - Min\ DC) \times T_{RANGE}/170$ is the effective T_{RANGE} value.

See the Fan Speed and PWM Duty Cycle section.

Figure 63 shows PWM duty cycle vs. temperature for each T_{RANGE} setting. The lower graph shows how each T_{RANGE} setting affects fan speed vs. temperature. As can be seen from the graph, the effect on fan speed is nonlinear.

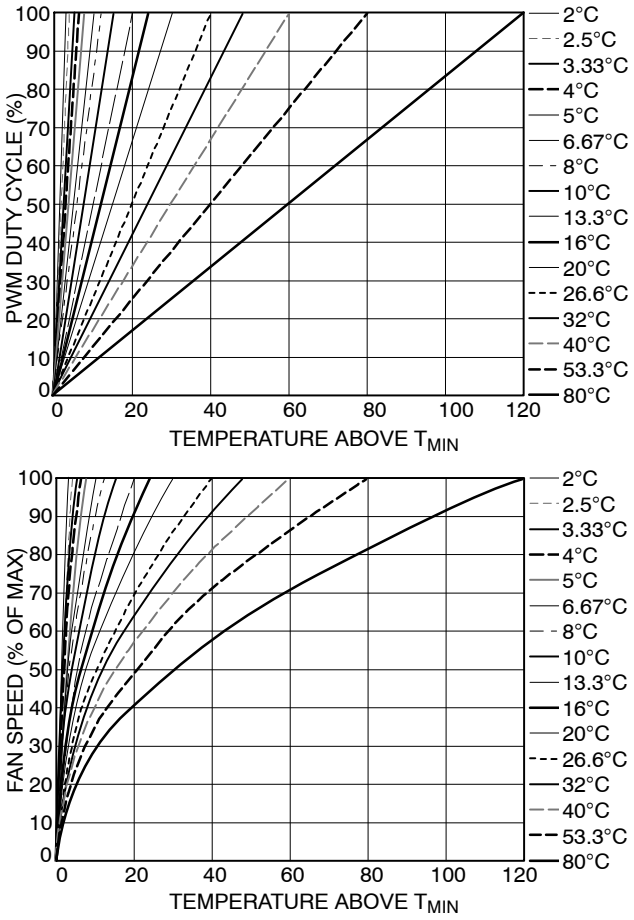


Figure 63. T_{RANGE} vs. Fan Speed Profile

The graphs in Figure 63 assume that the fan starts from 0% PWM duty cycle. The minimum PWM duty cycle, PWM_{MIN}, must be factored in to determine how the loop performs in the system. Figure 64 shows how T_{RANGE} is affected when the PWM_{MIN} value is set to 20%. It can be seen that the fan runs at about 45% fan speed when the temperature exceeds T_{MIN}.

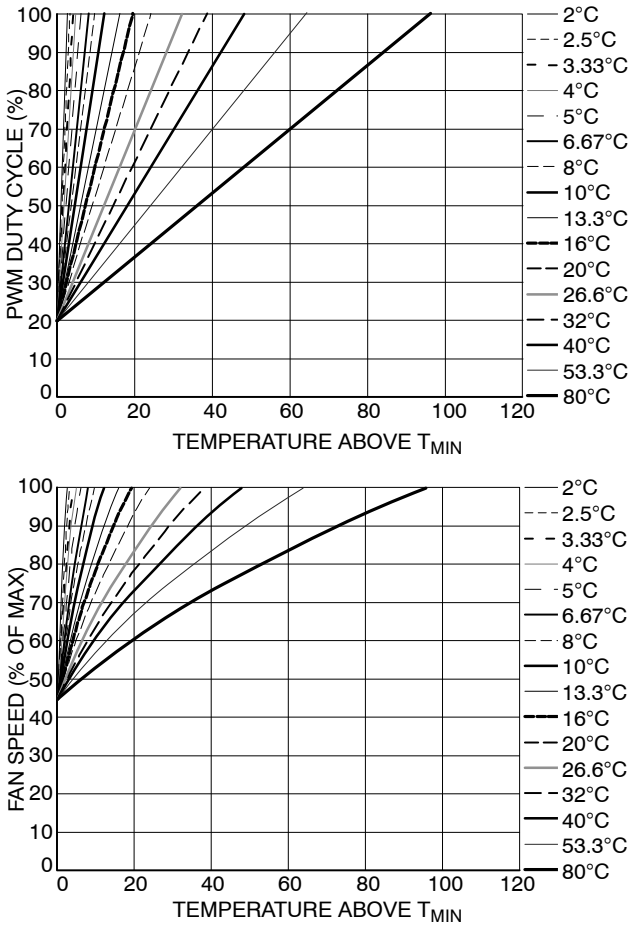


Figure 64. T_{RANGE} and Percentage of Fan Speed Slopes with PWM_{MIN} = 20%

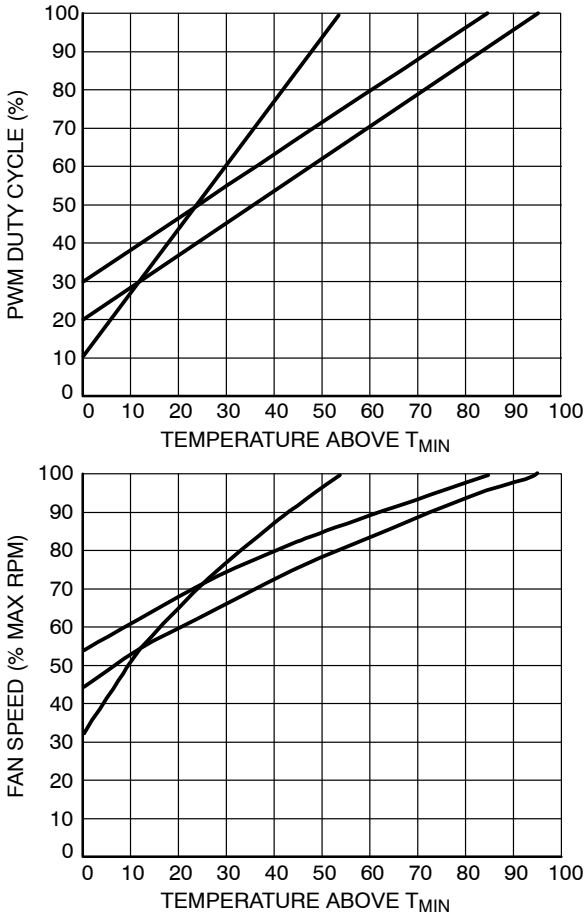


Figure 65. T_{RANGE} and Percentage of Fan Speed Slopes for VRM, Ambient, and CPU Temperature Channels

Determining T_{RANGE} for Each Temperature Channel

The following example shows how different T_{MIN} and T_{RANGE} settings can be applied to three thermal zones. In this example, the following T_{RANGE} values apply:

T_{RANGE} = 80°C for ambient temperature

T_{RANGE} = 53.3°C for CPU temperature

T_{RANGE} = 40°C for VRM temperature

This example uses the mux configuration described in the Step 2: Configuring the Mux section, with the ADT7467 connected as shown in Figure 55. Both CPU temperature and VRM temperature drive the CPU fan connected to PWM1. Ambient temperature drives the front chassis fan and the rear chassis fan connected to PWM2 and PWM3. The front chassis fan is configured to run at PWM_{MIN} = 20%; the rear chassis fan is configured to run at PWM_{MIN} = 30%. The CPU fan is configured to run at PWM_{MIN} = 10%.

4-wire Fans

The control range for 4-wire fans is much wider than that of 2-wire or 3-wire fans. In many cases, 4-wire fans can start with a PWM drive of as little as 20%.

STEP 7: $T_{\overline{THERM}}$ for Temperature Channels

$T_{\overline{THERM}}$ is the absolute maximum temperature allowed on a temperature channel. Above this temperature, a component such as the CPU or VRM might be operating beyond its safe operating limit. When the temperature measured exceeds $T_{\overline{THERM}}$, all fans are driven at 100% PWM duty cycle (full speed) to provide critical system cooling.

The fans remain running at 100% until the temperature drops below $T_{\overline{THERM}}$ minus hysteresis, where hysteresis is the number programmed into the Hysteresis Registers 0x6D and 0x6E. The default hysteresis value is 4°C.

The $T_{\overline{THERM}}$ limit should be considered the maximum worst-case operating temperature of the system. Because exceeding any $T_{\overline{THERM}}$ limit runs all fans at 100%, it has significant negative acoustic effects. Ultimately, this limit should be set up as a fail-safe, and users should ensure that it is not exceeded under normal system operating conditions.

Note that the $T_{\overline{THERM}}$ limits are nonmaskable and affect the fan speed regardless of the configuration of the automatic fan control settings. This allows some flexibility, because a T_{RANGE} value can be selected based on its slope,

and a hard limit (such as 70°C) can be programmed as T_{MAX} (the temperature at which the fan reaches full speed) by setting $T_{\overline{THERM}}$ to that limit (for example, 70°C).

$\overline{THERM}$ Limit Registers

Register 0x6A, Remote 1 $\overline{THERM}$ limit = 0xA4 (100°C default)

Register 0x6B, local $\overline{THERM}$ limit = 0xA4 (100°C default)

Register 0x6C, Remote 2 $\overline{THERM}$ limit = 0xA4 (100°C default)

Hysteresis Registers

Register 0x6D, Remote 1 and Local hysteresis register

<7:4>, Remote 1 temperature hysteresis (4°C default)

<3:0>, local temperature hysteresis (4°C default)

Register 0x6E, Remote 2 temperature hysteresis register

<7:4>, Remote 2 temperature hysteresis (4°C default)

Because each hysteresis setting is four bits, hysteresis values are programmable from 1°C to 15°C. It is recommended that hysteresis values are not programmed to 0°C because this disables hysteresis. In effect, this would cause the fans to cycle between normal speed and 100% speed, creating unsettling acoustic noise.

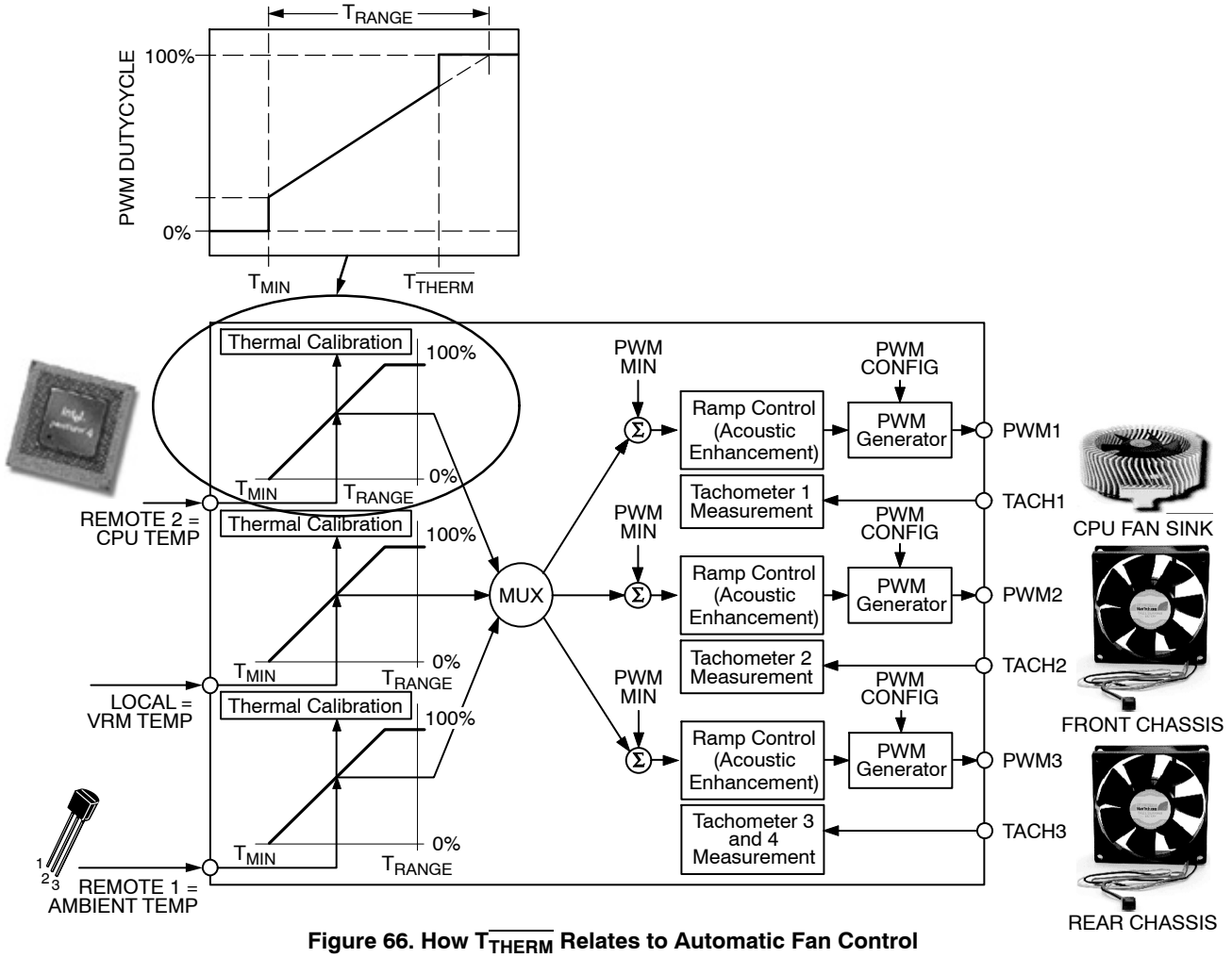


Figure 66. How $T_{\overline{THERM}}$ Relates to Automatic Fan Control

STEP 8: T_{HYST} for Temperature Channels

T_{HYST} is the amount of extra cooling a fan provides after the temperature measured drops below T_{MIN} before the fan turns off. The premise for temperature hysteresis (T_{HYST}) is that, without it, the fan would merely chatter or cycle on and off repeatedly whenever the temperature hovered near the T_{MIN} setting.

The T_{HYST} value determines the amount of time needed for the system to cool down or heat up as the fan turns on and off. Values of hysteresis are programmable in the range 1°C to 15°C. Larger values of T_{HYST} prevent the fans from chattering on and off. The T_{HYST} default value is set at 4°C.

The T_{HYST} setting not only applies to the temperature hysteresis for fan on/off, but also is used for the $T_{\overline{THERM}}$ hysteresis value, as described in Step 6: T_{RANGE} for Temperature Channels. Therefore, programming Register 0x6D and Register 0x6E sets the hysteresis for both fan on/off and the $\overline{THERM}$ function.

Hysteresis Registers

Register 0x6D, Remote 1 and local hysteresis register <7:4>, Remote 1 temperature hysteresis (4°C default) <3:0>, local temperature hysteresis (4°C default)

Register 0x6E, Remote 2 temperature hysteresis register <7:4>, Remote 2 temperature hysteresis (4°C default)

In some applications, it is required that fans continue to run at PWM_{MIN}, instead of turning off when the temperature drops below T_{MIN}. Bits <7:5> of Enhanced Acoustics Register 1 (0x62) allow the fans to be either turned off or kept spinning below T_{MIN}. If the fans are always on, the T_{HYST} value has no effect on the fan when the temperature drops below T_{MIN}.

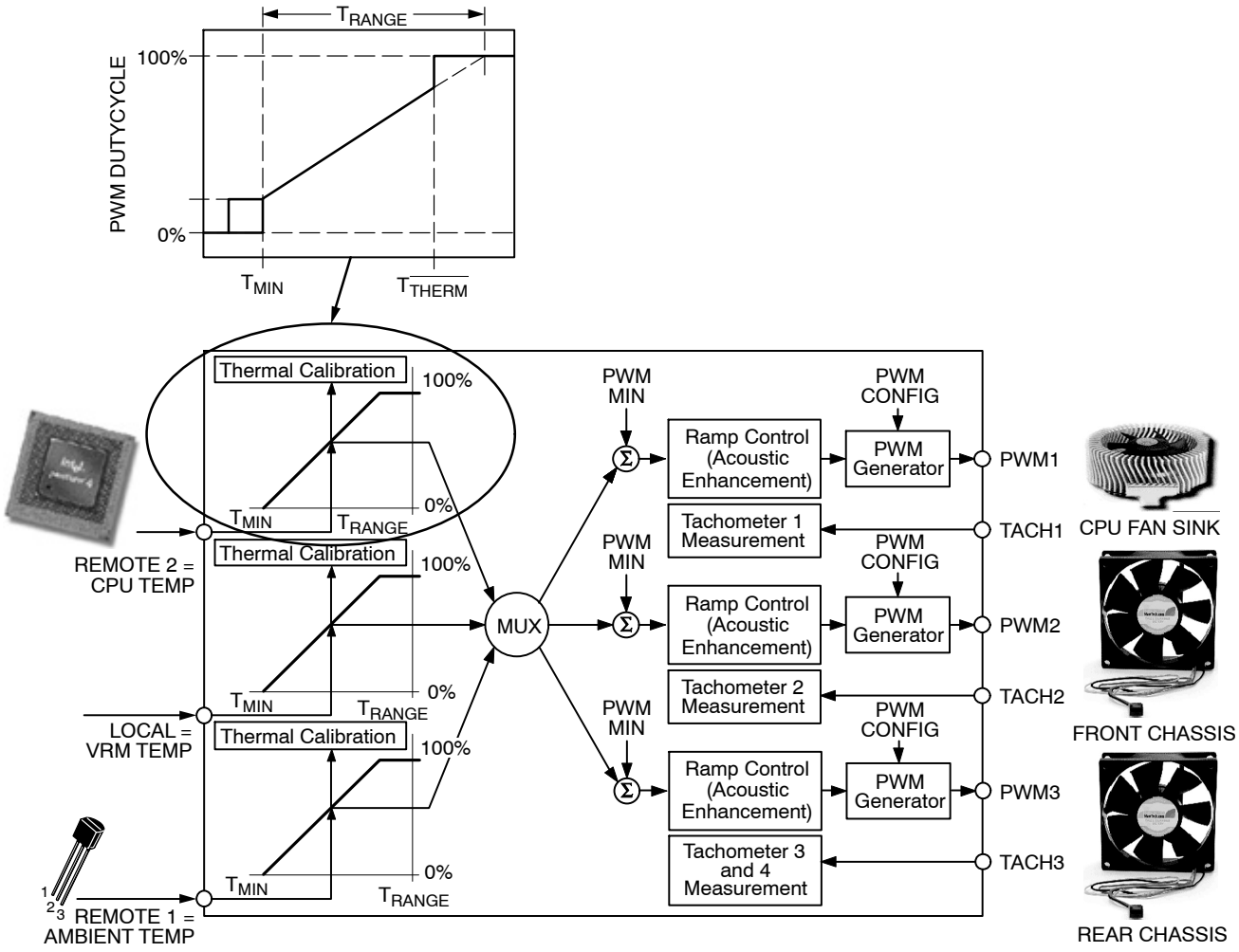


Figure 67. The T_{HYST} Value Applies to Fan On/Off Hysteresis and $\overline{THERM}$ Hysteresis

Enhanced Acoustics Register 1 (0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when the temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

STEP 9: Operating Points for Temperature Channels

The operating point for each temperature channel is the optimal temperature for that thermal zone. The hotter each zone is allowed to be, the more quiet the system, because the fans are not required to run as fast. The ADT7467 increases or decreases fan speeds as necessary to maintain the operating point temperature, allowing for system-to- system variations and eliminating the need to design for the worst case. If a sensible operating point value is chosen, any T_{MIN} value can be selected in the system characterization. If the T_{MIN} value is too low, the fans run sooner than required and the temperature is below the operating point. In response, the ADT7467 increases T_{MIN} to keep the fans off longer and to allow the temperature zone to approach the operating

point. Likewise, too high a T_{MIN} value causes the operating point to be exceeded, and, in turn, the ADT7467 reduces T_{MIN} to turn the fans on sooner to cool the system.

Programming Operating Point Registers

There are three operating point registers, one for each temperature channel. These 8-bit registers allow the operating point temperatures to be programmed with 1°C resolution.

Operating Point Registers

Register 0x33, Remote 1 operating point = 0xA4 (100°C default)

Register 0x34, local temperature operating point = 0xA4 (100°C default)

Register 0x35, Remote 2 operating point = 0xA4 (100°C default)

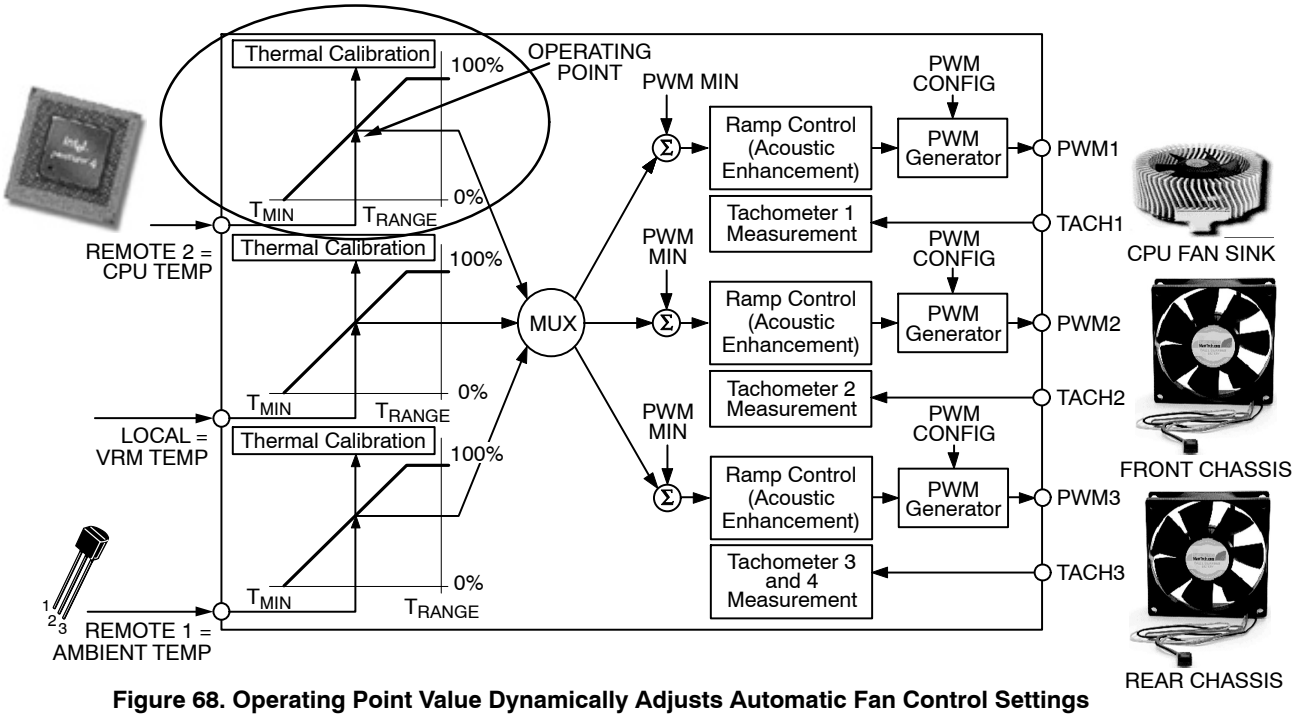


Figure 68. Operating Point Value Dynamically Adjusts Automatic Fan Control Settings

STEP 10: High and Low Limits for Temperature Channels

If the temperature falls below the temperature channel's low limit, T_{MIN} increases. This reduces fan speed, allowing the system to heat up. An interrupt can be generated when the temperature drops below the low limit.

If the temperature increases above the temperature channel's high limit, T_{MIN} decreases. This increases fan speed to cool down the system. An interrupt can be generated when the temperature rises above the high limit.

Programming High and Low Limits

There are six limit registers; a high limit and a low limit are associated with each temperature channel. These 8-bit registers allow the high and low limit temperatures to be programmed with 1°C resolution.

Temperature Limit Registers

Register 0x4E, Remote 1 temperature low limit = 0x01 default

Register 0x4F, Remote 1 temperature high limit = 0x7F default

Register 0x50, Local temperature low limit = 0x01 default

Register 0x51, Local temperature high limit = 0x7F default

Register 0x52, Remote 2 temperature low limit = 0x01 default

Register 0x53, Remote 2 temperature high limit = 0x7F default

How Dynamic T_{MIN} Control Works

The basic premise is as follows:

- Set the target temperature for the temperature zone, for example, the Remote 1 thermal diode. This value is programmed to the Remote 1 operating temperature register.
- As the temperature in that zone (Remote 1 temperature) exceeds the operating point temperature, T_{MIN} is reduced and the fan speed increases.
- As the temperature drops below the operating point temperature, T_{MIN} is increased and the fan speed is reduced.

However, the loop operation is not as simple as described in these steps. A number of conditions govern the situations in which T_{MIN} can increase or decrease.

Short Cycle and Long Cycle

The ADT7467 implements two loops: a short cycle and a long cycle. The short cycle takes place every n monitoring cycles. The long cycle takes place every 2n monitoring cycles. The value of n is programmable for each temperature channel. The bits are located at the following register locations:

Remote 1 = CYR1 = Bits <2:0> of Dynamic T_{MIN} Control Register 2 (Address 0x37)

Local = CYL = Bits <5:3> of Dynamic T_{MIN} Control Register 2 (Address 0x37)

Remote 2 = CYR2 = Bits <7:6> of Dynamic T_{MIN} Control Register 2 and Bit 0 of Dynamic T_{MIN} Control Register 1 (0x36)

Table 39. CYCLE BIT ASSIGNMENTS

Code	Short Cycle		Long Cycle	
000	8 cycles	(1 sec)	16 cycles	(2 sec)
001	16 cycles	(4 sec)	32 cycles	(2 sec)
010	32 cycles	(4 sec)	64 cycles	(8 sec)
011	64 cycles	(8 sec)	128 cycles	(16 sec)
100	128 cycles	(16 sec)	256 cycles	(32 sec)
101	256 cycles	(32 sec)	512 cycles	(64 sec)
110	512 cycles	(64 sec)	1024 cycles	(128 sec)
111	1024 cycles	(128 sec)	2048 cycles	(256 sec)

Care should be taken when choosing the cycle time. A long cycle time means that T_{MIN} is updated less often. If a system has very fast temperature transients, the dynamic T_{MIN} control loop lags. If a cycle time is chosen that is too fast, the full benefit of changing T_{MIN} might not be realized and will need to change upon the next cycle; in effect, it is overshooting. Some calibration is necessary to identify the most suitable response time.

Figure 69 shows the steps taken during the short cycle.

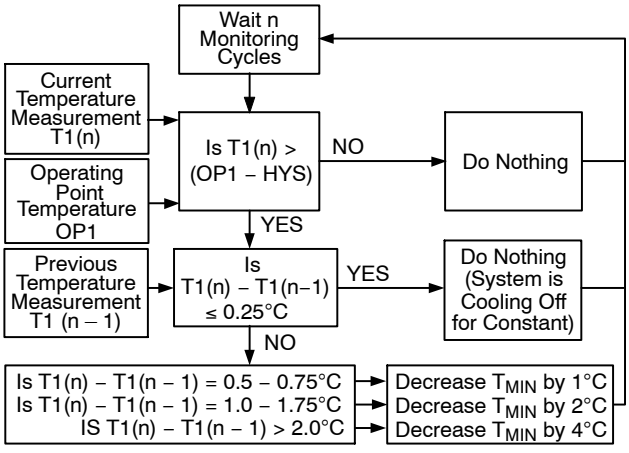


Figure 69. Short Cycle Steps

Figure 70 shows the steps taken during the long cycle.

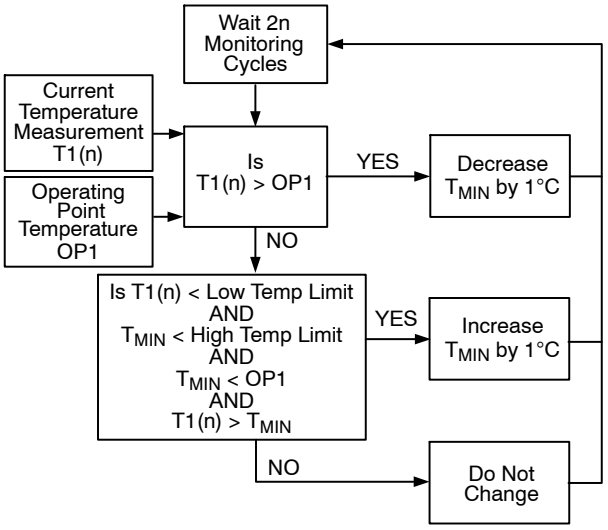


Figure 70. Long Cycle Steps

The following examples illustrate circumstances that may cause T_{MIN} to increase, decrease, or stay the same.

Normal Operation-No T_{MIN} Adjustment

- If measured temperature never exceeds the programmed operating point minus the hysteresis temperature, T_{MIN} is not adjusted, that is, it remains at its current setting.
- If measured temperature never drops below the low temperature limit, T_{MIN} is not adjusted.

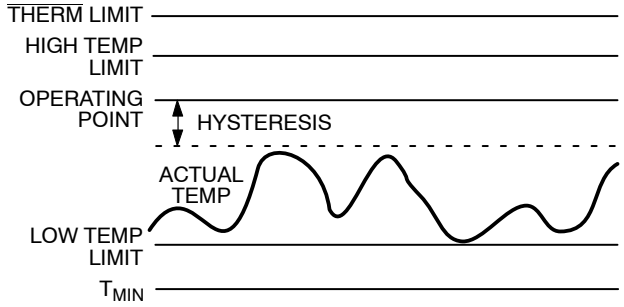


Figure 71. Temperature Between Operating Point and Low Temperature Limit

Because neither the operating point minus the hysteresis temperature nor the low temperature limit has been exceeded, the T_{MIN} value is not adjusted and the fan runs at a speed determined by the fixed T_{MIN} and T_{RANGE} values, defined in the automatic fan speed control mode in the Enhancing System Acoustics section.

Operating Point Exceeded-T_{MIN} Reduced

When the measured temperature is below the operating point temperature minus the hysteresis, T_{MIN} remains the same.

Once the temperature exceeds the operating temperature minus the hysteresis (OP1 − Hyst), T_{MIN} decreases during the short cycle (see Figure 69) at a rate determined by the programmed value of n. This rate also depends on the amount that the temperature has increased between this monitoring cycle and the last monitoring cycle. For example, if the temperature has increased by 1°C, then T_{MIN} is reduced by 2°C. Decreasing T_{MIN} has the effect of increasing the fan speed, thus providing more cooling to the system.

If the temperature slowly increases only in the range (OP1 − Hyst), that is, the change in temperature is ≤ 0.25°C per short monitoring cycle, T_{MIN} does not decrease. This allows small changes in temperature in the desired operating zone without changing T_{MIN}. The long cycle makes no change to T_{MIN} in the temperature range (OP − Hyst), because the temperature has not exceeded the operating temperature.

Once the temperature exceeds the operating temperature, T_{MIN} reduces by 1°C per long cycle as long as the temperature remains above the operating temperature. This takes place in addition to the decrease in T_{MIN} that occurs during the short cycle. In Figure 72, because the temperature is increasing at a rate of ≤ 0.25°C per short cycle, no reduction in T_{MIN} takes place during the short cycle.

Once the temperature falls below the operating temperature, T_{MIN} remains fixed, even when the temperature starts to increase slowly, because the temperature only increases at a rate of ≤ 0.25°C per cycle.

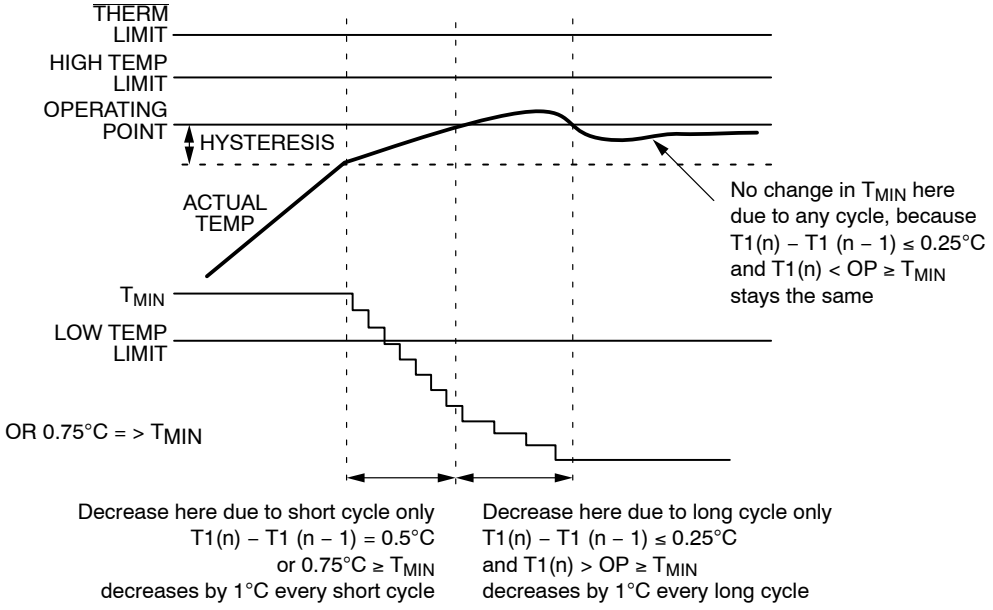


Figure 72. Effect of Exceeding Operating Point Minus Hysteresis Temperature

Increasing the T_{MIN} Cycle

When the temperature drops below the low temperature limit, T_{MIN} can increase during the long cycle. Increasing T_{MIN} has the effect of running the fan more slowly and, therefore, more quietly. The long cycle diagram in Figure 70 shows the conditions necessary for T_{MIN} to increase.

T_{MIN} can increase if:

- The measured temperature falls below the low temperature limit. This means that the user must choose the low limit carefully. It should not be so low that the temperature never falls below it, because T_{MIN} would never increase and the fans would run faster than necessary.

- T_{MIN} is below the high temperature limit. T_{MIN} is never allowed to exceed the high temperature limit. As a result, the high limit should be chosen carefully because it deter-mines the high limit of T_{MIN}.
- T_{MIN} is below the operating point temperature. T_{MIN} should never be allowed to increase above the operating point temperature, because the fans would not switch on until the temperature rose above the operating point.
- The temperature is above T_{MIN}. The dynamic T_{MIN} control is turned off below T_{MIN}.

Figure 73 shows how T_{MIN} increases when the current temperature is above T_{MIN} but below the low temperature limit, and how T_{MIN} is below the high temperature limit and below the operating point. Once the temperature rises above the low temperature limit, T_{MIN} remains fixed.

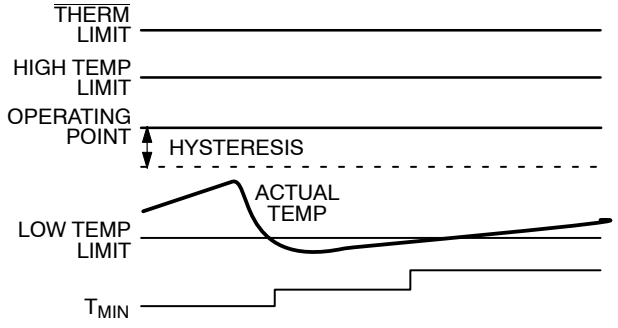


Figure 73. Increasing T_{MIN} for Quiet Operation

Preventing T_{MIN} from Reaching Full Scale

T_{MIN} is dynamically adjusted; therefore, it is undesirable for T_{MIN} to reach full scale (127°C), because the fan would never switch on. As a result, T_{MIN} is allowed to vary only within a specified range.

- The lowest possible value for T_{MIN} is –127°C (twos complement mode) or –64°C (Offset 64 mode).
- T_{MIN} cannot exceed the high temperature limit.
- If the temperature is below T_{MIN}, the fan switches off or runs at minimum speed and dynamic T_{MIN} control is disabled.

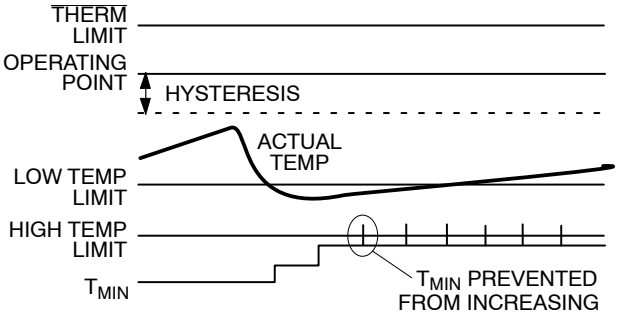


Figure 74. T_{MIN} Adjustments Limited by the High Temperature Limit

Step 11: Monitoring $\overline{\text{THERM}}$

Using the operating point limit ensures that the dynamic T_{MIN} control mode operates in the best possible acoustic position and that the temperature never exceeds the maximum operating temperature. Using the operating point limit allows T_{MIN} to be independent of system-level issues because of its self-corrective nature. In PC design, the operating point for the chassis is usually the worst-case internal chassis temperature.

The optimal operating point for the processor is determined by monitoring the thermal monitor in the Intel® Pentium® 4 processor. To do this, the $\overline{\text{PROCHOT}}$ output of the Pentium® 4 is connected to the $\overline{\text{THERM}}$ input of the ADT7467.

The operating point for the processor can be determined by allowing the current temperature to be copied to the operating point register when the $\overline{\text{PROCHOT}}$ output pulls the $\overline{\text{THERM}}$ input low on the ADT7467. This reveals the maximum temperature at which the Pentium® 4 can run before clock modulation occurs.

Enabling the $\overline{\text{THERM}}$ Trip Point as the Operating Point

Bits <4:2> of the dynamic T_{MIN} control Register 1 (0x36) enable/disable $\overline{\text{THERM}}$ monitoring to program the operating point.

Table 40. DYNAMIC T_{MIN} CONTROL REGISTER 1 (REG. 0X36)

Bit	Mnemonic	Description
<2>	PHTR1	1 copies the Remote 1 current temperature to the Remote 1 operating point register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted. This allows the system to run as quietly as possible without affecting system performance. 0 ignores $\overline{\text{THERM}}$ assertions. The Remote 1 operating point register reflects its programmed value.
<3>	PHTL	1 copies the local current temperature to the local temperature operating point register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted. This allows the system to run as quietly as possible without affecting system performance. 0 ignores $\overline{\text{THERM}}$ assertions. The local temperature operating point register reflects its programmed value.
<4>	PHTR2	1 copies the Remote 2 current temperature to the Remote 2 operating point register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted. This allows the system to run as quietly as possible without affecting system performance. 0 ignores $\overline{\text{THERM}}$ assertions. The Remote 2 operating point register reflects its programmed value.

Enabling Dynamic T_{MIN} Control Mode

Bits <7:5> of the dynamic T_{MIN} control Register 1 (0x36) enable/disable dynamic T_{MIN} control on the temperature channels.

Table 41. DYNAMIC T_{MIN} CONTROL REGISTER 1 (REG. 0X36)

Bit	Mnemonic	Description
<5>	R1T	1 enables dynamic T_{MIN} control on the Remote 1 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Automatic Fan Control Overview section.
<6>	LT	1 enables dynamic T_{MIN} control on the local temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone. 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Enhancing System Acoustics section.
<7>	R2T	1 enables the dynamic T_{MIN} control on the Remote 2 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for this zone.

R2T = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Enhancing System Acoustics section.

Step 12: Ramp Rate for Acoustic Enhancement

The optimal ramp rate for acoustic enhancement can be determined through system characterization after completing the thermal optimization. If possible, the effect of each ramp rate should be logged to determine the best setting for a given solution.

Enhanced Acoustics Register 1 (0x62)

<2:0> ACOU selects the ramp rate for PWM1.
000 = 1 time slot = 35 sec
001 = 2 time slots = 17.6 sec
010 = 3 time slots = 11.8 sec
011 = 5 time slots = 7 sec
100 = 8 time slots = 4.4 sec
101 = 12 time slots = 3 sec
110 = 24 time slots = 1.6 sec
111 = 48 time slots = 0.8 sec

Enhanced Acoustics Register 2 (0x63)

<2:0> ACOU3 selects the ramp rate for PWM3.
000 = 1 time slot = 35 sec
001 = 2 time slots = 17.6 sec
010 = 3 time slots = 11.8 sec
011 = 5 time slots = 7 sec
100 = 8 time slots = 4.4 sec
101 = 12 time slots = 3 sec
110 = 24 time slots = 1.6 sec
111 = 48 time slots = 0.8 sec

<6:4> ACOU2 selects the ramp rate for PWM2.
000 = 1 time slot = 35 sec
001 = 2 time slots = 17.6 sec
010 = 3 time slots = 11.8 sec
011 = 5 time slots = 7 sec
100 = 8 time slots = 4.4 sec
101 = 12 time slots = 3 sec
110 = 24 time slots = 1.6 sec
111 = 48 time slots = 0.8 sec

Another way to view the ramp rates is as the time it takes for the PWM output to ramp up from 0% to 100% duty cycle for an instantaneous change in temperature. This can be tested by putting the ADT7467 into manual mode and changing the PWM output from 0% to 100% PWM duty cycle. The PWM output takes 35 sec to reach 100% when a ramp rate of 1 time slot is selected.

Figure 75 shows remote temperature plotted against PWM duty cycle for enhanced acoustics mode. The ramp rate is set to 48, which corresponds to the fastest ramp rate. Assume that a new temperature reading is available every 115 ms. With these settings, it takes approximately 0.76 sec to go from 33% duty cycle to 100% duty cycle (full speed). Even though the temperature increases very rapidly, the fan ramps up to full speed gradually.

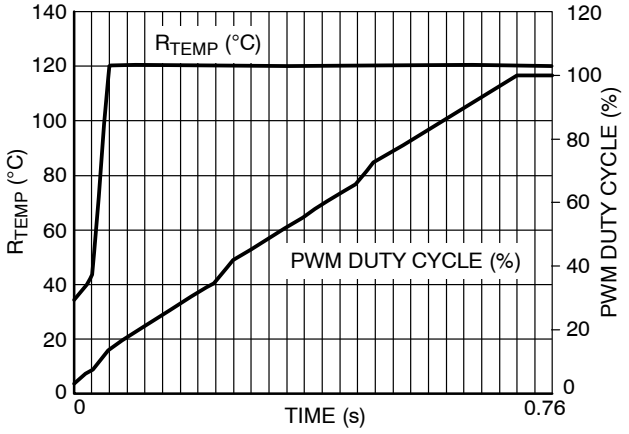


Figure 75. Enhanced Acoustics Mode with Ramp Rate = 48

Figure 76 shows how a ramp rate of 8 affects the control loop. The overall response of the fan is slower than it is with a ramp rate of 48. Because the ramp rate is reduced, it takes longer for the fan to achieve full running speed. In this case, it takes approximately 4.4 sec for the fan to reach full speed.

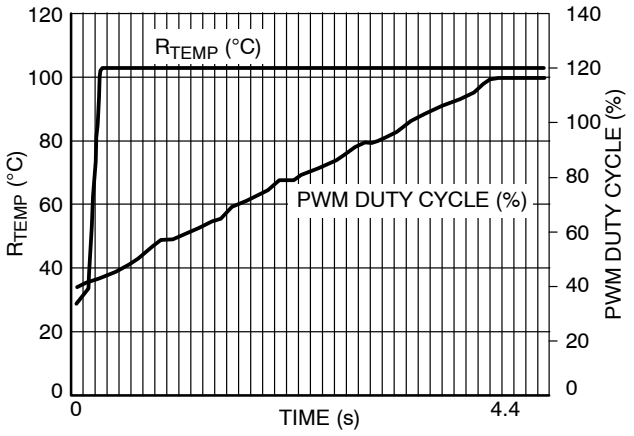


Figure 76. Enhanced Acoustics Mode with Ramp Rate = 8

Figure 77 shows the PWM output response for a ramp rate of 2. With these conditions, the fan takes about 17.6 sec to reach full running speed.

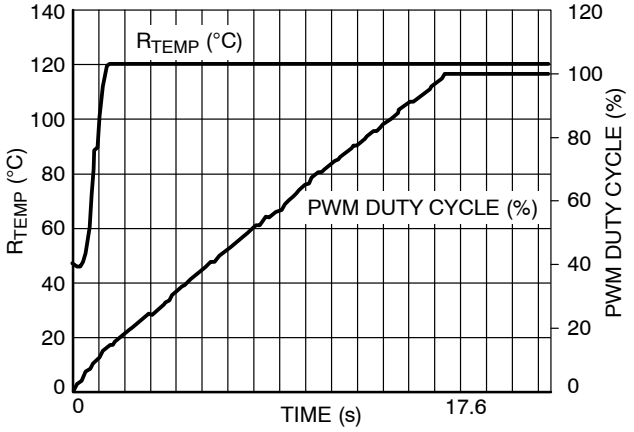


Figure 77. Enhanced Acoustics Mode with Ramp Rate = 2

Figure 78 shows how the control loop reacts to temperature with the slowest ramp rate. The ramp rate is set to 1; all other control parameters are the same as they are for Figure 75 through Figure 77. With the slowest ramp rate selected, it takes 35 sec for the fan to reach full speed.

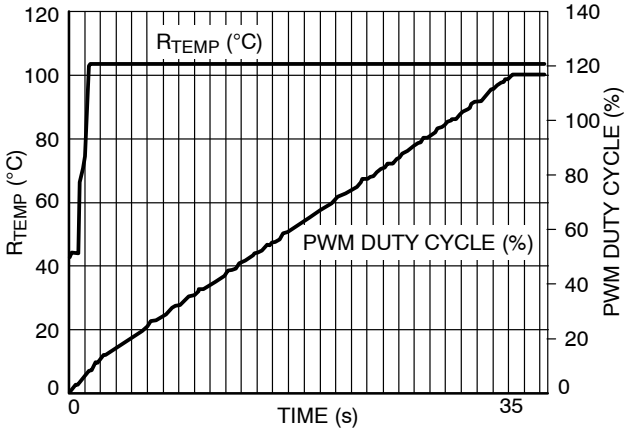


Figure 78. Enhanced Acoustics Mode with Ramp Rate = 1

As Figure 75 to Figure 78 show, the rate at which the fan reacts to a temperature change is dependent on the ramp rate selected in the enhanced acoustics registers. The higher the ramp rate, the faster the fan reaches the newly calculated fan speed.

Figure 79 shows the behavior of the PWM output as temperature varies. As the temperature increases, the fan speed ramps up. Small drops in temperature do not affect the ramp-up function because the newly calculated fan speed is higher than the previous PWM value. Enhanced acoustics mode allows the PWM output to be made less sensitive to temperature variations. This is dependent on the ramp rate selected and programmed into the enhanced acoustics registers.

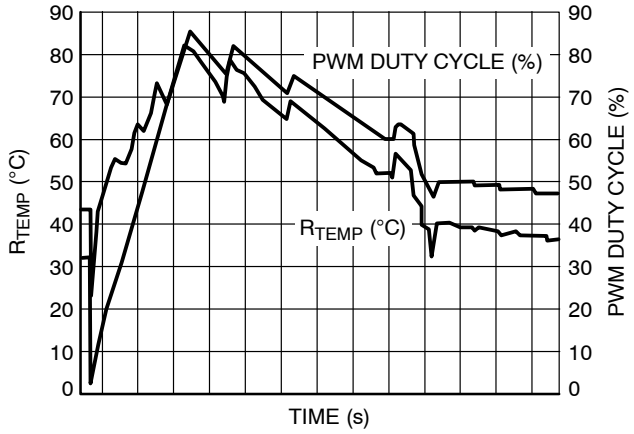


Figure 79. Fan Reaction to Temperature Variation in Enhanced Acoustics Mode

Slower Ramp Rates

The ADT7467 can be programmed for much longer ramp times by slowing the ramp rates. Each ramp rate can be slowed by a factor of 4.

PWM1 Configuration Register (0x5C)

<3> SLOW, a setting of 1 slows the ramp rate for PWM1 by 4.

PWM2 Configuration Register (0x5D)

<3> SLOW, a setting of 1 slows the ramp rate for PWM2 by 4.

PWM3 Configuration Register (0x5E)

<3> SLOW, a setting of 1 slows the ramp rate for PWM3 by 4.

The following sections list the ramp−up times when the SLOW bit is set for each PWM output.

Enhanced Acoustics Register 1 (0x62)

<2:0> ACOU selects the ramp rate for PWM1.

000 = 140 sec
001 = 70.4 sec
010 = 47.2 sec
011 = 28 sec
100 = 17.6 sec
101 = 12 sec
110 = 6.4 sec
111 = 3.2 sec

Enhanced Acoustics Register 2 (0x63)

<2:0> ACOU3 selects the ramp rate for PWM3.
000 = 140 sec
001 = 70.4 sec
010 = 47.2 sec
011 = 28 sec
100 = 17.6 sec
101 = 12 sec
110 = 6.4 sec
111 = 3.2 sec

<6:4> ACOU2 selects the ramp rate for PWM2.
000 = 140 sec
001 = 70.4 sec
010 = 47.2 sec
011 = 28 sec
100 = 17.6 sec
101 = 12 sec
110 = 6.4 sec
111 = 3.2 sec

Enhancing System Acoustics

Automatic fan speed control mode reacts instantaneously to changes in temperature, that is, the PWM duty cycle immediately responds to temperature change. Any impulses in temperature can cause an impulse in fan noise. For psychoacoustic reasons, the ADT7467 can prevent the PWM output from reacting instantaneously to temperature changes. Enhanced acoustic mode controls the maximum change in PWM duty cycle at a given time. The objective is to prevent the fan from repeatedly cycling up and down, annoying the user.

Acoustic Enhancement Mode Overview

Figure 80 shows a top-level overview of the ADT7467 automatic fan control circuitry and where acoustic enhancement fits in. Acoustic enhancement is intended as a postdesign tweak made by a system or mechanical engineer evaluating the best settings for the system. Having determined the optimal settings for the thermal solution, the engineer can adjust the system acoustics. The goal is to implement a system that is acoustically pleasing and does not cause user annoyance due to fan cycling. It is important to realize that although a system may pass an acoustic noise requirement specification (for example, 36 dB), it fails the consumer test if the fan is annoying.

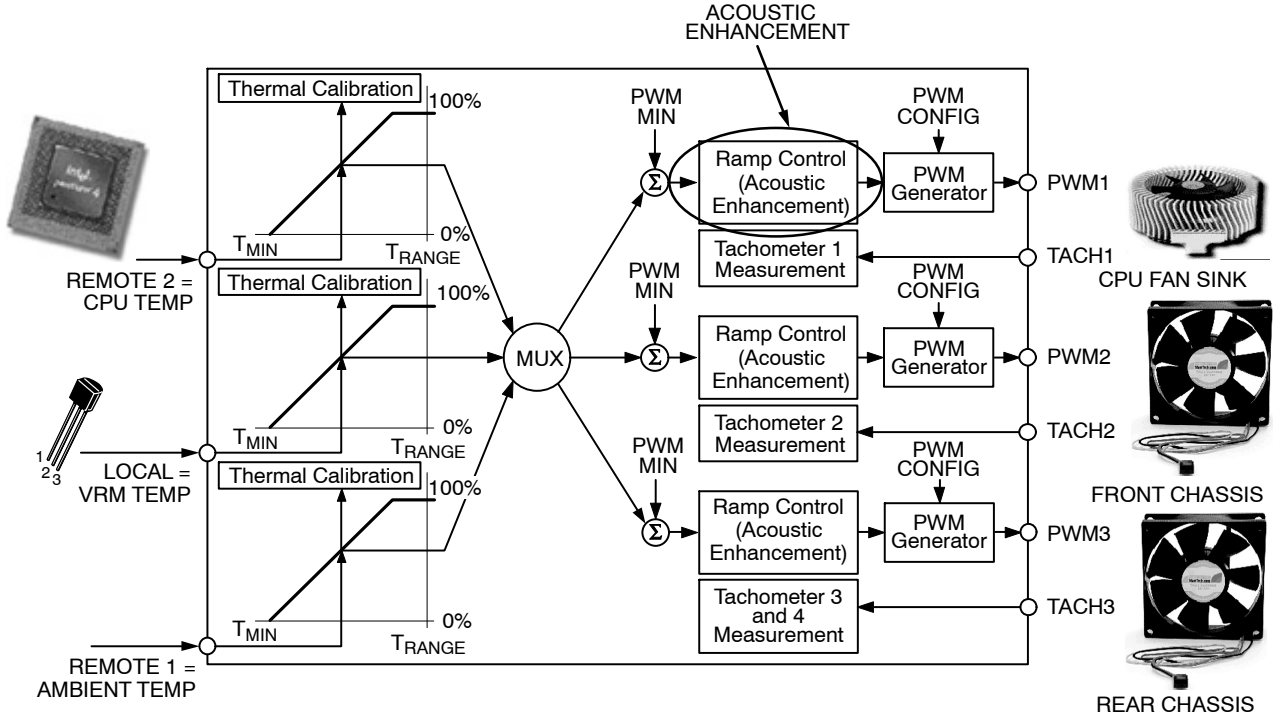


Figure 80. Acoustic Enhancement Smoothes Fan Speed Variations in Automatic Fan Speed Control

Approaches to System Acoustic Enhancement

There are two different approaches to implementing system acoustic enhancement: temperature-centric and fan-centric. The ADT7467 uses the fan-centric approach.

The temperature-centric approach involves smoothing transient temperatures as they are measured by a temperature source (for example, Remote 1 temperature). The temperature values used to calculate the PWM duty cycle values are smoothed, reducing fan speed variation. However, this approach causes an inherent delay in updating fan speed and causes the thermal characteristics of the system to change. It also causes the system fans to run longer than necessary, because the fan's reaction is merely delayed. The user has no control over noise from different fans driven by the same temperature source. Consider, for example, a system in which control of a CPU cooler fan (on PWM1) and

a chassis fan (on PWM2) use Remote 1 temperature. Because the Remote 1 temperature is smoothed, both fans are updated at exactly the same rate. If the chassis fan is much louder than the CPU fan, there is no way to improve its acoustics without changing the thermal solution of the CPU cooling fan.

The fan-centric approach to system acoustic enhancement controls the PWM duty cycle, driving the fan at a fixed rate (for example, 6%). Each time the PWM duty cycle is updated, it is incremented by a fixed 6%. As a result, the fan ramps smoothly to its newly calculated speed. If the temperature starts to drop, the PWM duty cycle immediately decreases by 6% at every update. Therefore, the fan ramps up or down smoothly without inherent system delay. Consider, for example, controlling the same CPU cooler fan (on PWM1) and chassis fan (on PWM2) using Remote 1 temperature. The T_{MIN} and T_{RANGE} settings have been defined in automatic fan speed control mode; that is, thermal characterization of the control loop has been optimized. Now the chassis fan is noisier than the CPU cooling fan. Using the fan-centric approach, PWM2 can be placed into acoustic enhancement mode independently of PWM1. The acoustics of the chassis fan can, therefore, be adjusted without affecting the acoustic behavior of the CPU cooling fan, even though both fans are controlled by Remote 1 temperature.

Enabling Acoustic Enhancement for Each PWM Output

Enhanced Acoustics Register 1 (0x62)

<3> = 1 enables acoustic enhancement on PWM1 output.

Enhanced Acoustics Register 2 (0x63)

<7> = 1 enables acoustic enhancement on PWM2 output.

<3> = 1 enables acoustic enhancement on PWM3 output.

Effect of Ramp Rate on Enhanced Acoustics Mode

The PWM signal driving the fan has a period, T, given by the PWM drive frequency, f, because T = 1/f. For a given PWM period, T, the PWM period is subdivided into 255 equal time slots. One time slot corresponds to the smallest possible increment in the PWM duty cycle. A PWM signal of 33% duty cycle is, therefore, high for 1/3 × 255 time slots and low for 2/3 × 255 time slots. Therefore, a 33% PWM duty cycle corresponds to a signal that is high for 85 time slots and low for 170 time slots.

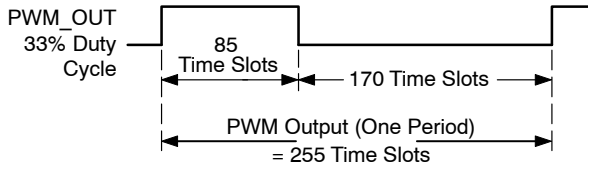


Figure 81. 33% PWM Duty Cycle, Represented in Time Slots

The ramp rates in the enhanced acoustics mode are selectable from the values 1, 2, 3, 5, 8, 12, 24, and 48. The ramp rates are discrete time slots. For example, if the ramp rate is 8, eight time slots are added or subtracted to increase or decrease, respectively, the PWM high duty cycle. Figure 82 shows how the enhanced acoustics mode algorithm operates.

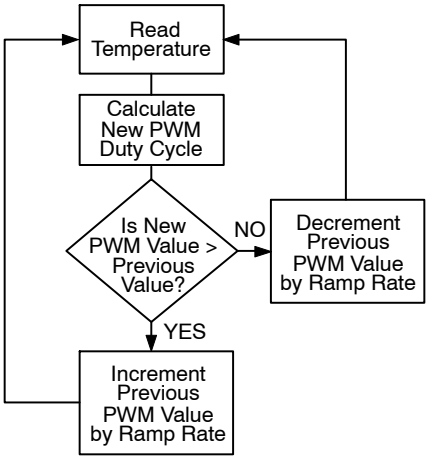


Figure 82. Enhanced Acoustics Algorithm

The enhanced acoustics mode algorithm calculates a new PWM duty cycle based on the temperature measured. If the new PWM duty cycle value is greater than the previous PWM value, the previous PWM duty cycle value is incremented by 1, 2, 3, 5, 8, 12, 24, or 48 time slots, depending on the settings of the enhanced acoustics registers. If the new PWM duty cycle value is less than the previous PWM value, the previous PWM duty cycle is decremented by 1, 2, 3, 5, 8, 12, 24, or 48 time slots. Each time the PWM duty cycle is incremented or decremented, its value is stored as the previous PWM duty cycle for the next comparison. A ramp rate of 1 corresponds to one time slot, which is 1/255 of the PWM period. In enhanced acoustics mode, incrementing or decrementing by 1 changes the PWM output by 1/255 × 100%.

Register Map

Table 42. ADT7467 REGISTERS

Addr.	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock–able
0x21	R	V_{CCP} reading	9	8	7	6	5	4	3	2	0x00	
0x22	R	V_{CC} reading	9	8	7	6	5	4	3	2	0x00	
0x25	R	Remote 1 temperature	9	8	7	6	5	4	3	2	0x01	
0x26	R	Local temperature	9	8	7	6	5	4	3	2	0x01	
0x27	R	Remote 2 temperature	9	8	7	6	5	4	3	2	0x01	
0x28	R	TACH1 low byte	7	6	5	4	3	2	1	0	0x00	
0x29	R	TACH1 high byte	15	14	13	12	11	10	9	8	0x00	
0x2A	R	TACH2 low byte	7	6	5	4	3	2	1	0	0x00	
0x2B	R	TACH2 high byte	15	14	13	12	11	10	9	8	0x00	
0x2C	R	TACH3 low byte	7	6	5	4	3	2	1	0	0x00	
0x2D	R	TACH3 high byte	15	14	13	12	11	10	9	8	0x00	
0x2E	R	TACH4 low byte	7	6	5	4	3	2	1	0	0x00	
0x2F	R	TACH4 high byte	15	14	13	12	11	10	9	8	0x00	
0x30	R/W	PWM1 current duty cycle	7	6	5	4	3	2	1	0	0x00	
0x31	R/W	PWM2 current duty cycle	7	6	5	4	3	2	1	0	0x00	
0x32	R/W	PWM3 current duty cycle	7	6	5	4	3	2	1	0	0x00	
0x33	R/W	Remote 1 operating point	7	6	5	4	3	2	1	0	0xA4	Yes
0x34	R/W	Local temperature operating point	7	6	5	4	3	2	1	0	0xA4	Yes
0x35	R/W	Remote 2 operating point	7	6	5	4	3	2	1	0	0xA4	Yes
0x36	R/W	Dynamic T_{MIN} Control Reg. 1	R2T	LT	R1T	PHTR2	PHTL	PHTR1	V_{CCP}LO	CYR2	0x00	Yes
0x37	R/W	Dynamic T_{MIN} Control Reg. 2	CYR2	CYR2	CYL	CYL	CYL	CYR1	CYR1	CYR1	0x00	Yes
0x38	R/W	Max PWM1 duty cycle	7	6	5	4	3	2	1	0	0xFF	
0x39	R/W	Max PWM2 duty cycle	7	6	5	4	3	2	1	0	0xFF	
0x3A	R/W	Max PWM3 duty cycle	7	6	5	4	3	2	1	0	0xFF	
0x3D	R	Device ID register	7	6	5	4	3	2	1	0	0x68	
0x3E	R	Company ID number	7	6	5	4	3	2	1	0	0x41	
0x3F	R	Revision number	VER	VER	VER	VER	STP	STP	STP	STP	0x71/ 0x72	
0x40	R/W	Configuration Register 1	V_{CC}	TODIS	FSPDIS	VxI	FSPD	RDY	LOCK	STRT	0x01	Yes
0x41	R	Interrupt Status Register 1	OOL	R2T	LT	R1T	RES	V_{CC}	V_{CCP}	RES	0x00	
0x42	R	Interrupt Status Register 2	D2	D1	F4P	FAN3	FAN2	FAN1	OVT	RES	0x00	
0x46	R/W	V_{CCP} low limit	7	6	5	4	3	2	1	0	0x00	

Table 42. ADT7467 REGISTERS (continued)

Addr.	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock–able
0x47	R/W	V_{CCP} high limit	7	6	5	4	3	2	1	0	0xFF	
0x48	R/W	V_{CC} low limit	7	6	5	4	3	2	1	0	0x00	
0x49	R/W	V_{CC} high limit	7	6	5	4	3	2	1	0	0xFF	
0x4E	R/W	Remote 1 temper-ature low limit	7	6	5	4	3	2	1	0	0x01	
0x4F	R/W	Remote 1 temper-ature high limit	7	6	5	4	3	2	1	0	0x7F	
0x50	R/W	Local temperature low limit	7	6	5	4	3	2	1	0	0x01	
0x51	R/W	Local temperature high limit	7	6	5	4	3	2	1	0	0x7F	
0x52	R/W	Remote 2 temper-ature low limit	7	6	5	4	3	2	1	0	0x01	
0x53	R/W	Remote 2 temper-ature high limit	7	6	5	4	3	2	1	0	0x7F	
0x54	R/W	TACH1 minimum low byte	7	6	5	4	3	2	1	0	0xFF	
0x55	R/W	TACH1 minimum high byte	15	14	13	12	11	10	9	8	0xFF	
0x56	R/W	TACH2 minimum low byte	7	6	5	4	3	2	1	0	0xFF	
0x57	R/W	TACH2 minimum high byte	15	14	13	12	11	10	9	8	0xFF	
0x58	R/W	TACH3 minimum low byte	7	6	5	4	3	2	1	0	0xFF	
0x59	R/W	TACH3 minimum high byte	15	14	13	12	11	10	9	8	0xFF	
0x5A	R/W	TACH4 minimum low byte	7	6	5	4	3	2	1	0	0xFF	
0x5B	R/W	TACH4 minimum high byte	15	14	13	12	11	10	9	8	0xFF	
0x5C	R/W	PWM1 configura-tion register	BHVR	BHVR	BHVR	INV	SLOW	SPIN	SPIN	SPIN	0x82	Yes
0x5D	R/W	PWM2 configura-tion register	BHVR	BHVR	BHVR	INV	SLOW	SPIN	SPIN	SPIN	0x82	Yes
0x5E	R/W	PWM3 configura-tion register	BHVR	BHVR	BHVR	INV	SLOW	SPIN	SPIN	SPIN	0x82	Yes
0x5F	R/W	Remote 1 T_{RANGE}/PWM1 frequency	RANGE	RANGE	RANGE	RANGE	THRM	FREQ	FREQ	FREQ	0xC4	Yes
0x60	R/W	Local T_{RANGE}/ PWM2 frequency	RANGE	RANGE	RANGE	RANGE	THRM	FREQ	FREQ	FREQ	0xC4	Yes
0x61	R/W	Remote 2 T_{RANGE}/PWM3 frequency	RANGE	RANGE	RANGE	RANGE	THRM	FREQ	FREQ	FREQ	0xC4	Yes
0x62	R/W	Enhanced acous-tics Register 1	MIN3	MIN2	MIN1	SYNC	EN1	ACOU	ACOU	ACOU	0x00	Yes
0x63	R/W	Enhanced acous-tics Register 2	EN2	ACOU2	ACOU2	ACOU2	EN3	ACOU3	ACOU3	ACOU3	0x00	Yes
0x64	R/W	PWM1 min duty cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x65	R/W	PWM2 min duty cycle	7	6	5	4	3	2	1	0	0x80	Yes

Table 42. ADT7467 REGISTERS (continued)

Addr.	R/W	Description	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock–able
0x66	R/W	PWM3 min duty cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x67	R/W	Remote 1 temp T_{MIN}	7	6	5	4	3	2	1	0	0x9A	Yes
0x68	R/W	Local temp T_{MIN}	7	6	5	4	3	2	1	0	0x9A	Yes
0x69	R/W	Remote 2 temp T_{MIN}	7	6	5	4	3	2	1	0	0x9A	Yes
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ temperature limit	7	6	5	4	3	2	1	0	0xA4	Yes
0x6B	R/W	Local $\overline{\text{THERM}}$ temperature limit	7	6	5	4	3	2	1	0	0xA4	Yes
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$ temperature limit	7	6	5	4	3	2	1	0	0xA4	Yes
0x6D	R/W	Remote 1 and local temp/T_{MIN} hysteresis	HYSR1	HYSR1	HYSR1	HYSR1	HYSL	HYSL	HYSL	HYSL	0x44	Yes
0x6E	R/W	Remote 2 temp/ T_{MIN} hysteresis	HYSR2	HYSR2	HYSR2	HYRS	RES	RES	RES	RES	0x40	Yes
0x6F	R/W	XNOR tree test enable	RES	RES	RES	RES	RES	RES	RES	XEN	0x00	Yes
0x70	R/W	Remote 1 temper-ature offset	7	6	5	4	3	2	1	0	0x00	Yes
0x71	R/W	Local temperature offset	7	6	5	4	3	2	1	0	0x00	Yes
0x72	R/W	Remote 2 temper-ature offset	7	6	5	4	3	2	1	0	0x00	Yes
0x73	R/W	Configuration Register 2	SHDN	CONV	ATTN	AVG	AIN4	AIN3	AIN2	AIN1	0x00	Yes
0x74	R/W	Interrupt Mask 1 register	OOL	R2T	LT	RIT	RES	V_{CC}	V_{CCP}	RES	0x00	
0x75	R/W	Interrupt Mask 2 register	D2	D1	F4P	FAN3	FAN2	FAN1	OVT	RES	0x00	
0x76	R/W	Extended Resolution 1	RES	RES	V_{CC}	V_{CC}	V_{CCP}	V_{CCP}	RES	RES	0x00	
0x77	R/W	Extended Resolution 2	TDM2	TDM2	LTMP	LTMP	TDM1	TDM1	RES	RES	0x00	
0x78	R/W	Configuration Register 3	DC4	DC3	DC2	DC1	FAST	BOOST	$\overline{\text{THERM}}$	ALERT Enable	0x00	Yes
0x79	R	$\overline{\text{THERM}}$ timer status register	TMR	TMR	TMR	TMR	TMR	TMR	TMR	ASRT/ TMR0	0x00	
0x7A	R/W	$\overline{\text{THERM}}$ timer limit register	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	0x00	
0x7B	R/W	TACH pulses per revolution	FAN4	FAN4	FAN3	FAN3	FAN2	FAN2	FAN1	FAN1	0x55	
0x7C	R/W	Configuration Register 5	RES	RES	RES	RES	GPIOP	GPIOD	LF/HF	Twos Compl	0x00	Yes
0x7D	R/W	Configuration Register 4	RES	RES	BpAtt V_{CCP}	RES	AINL	AINL	Pin 9 Func	Pin 9 Func	0x00	Yes
0x7E	R	Manufacturer's Test Register 1	DO NOT WRITE TO THESE REGISTERS								0x00	Yes
0x7F	R	Manufacturer's Test Register 2	DO NOT WRITE TO THESE REGISTERS								0x00	Yes

Table 43. VOLTAGE READING REGISTERS (POWER-ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x21	Read Only	Reflects the Voltage Measurement (Note 2) at the V_{CCP} Input on Pin 14 (8 MSBs of Reading)
0x22	Read Only	Reflects the Voltage Measurement (Note 3) at the V_{CC} Input on Pin 3 (8 MSBs of Reading)

1. If the extended resolution bits of these readings are also being read, the extended resolution registers (0x76, 0x77) must be read first. Once the extended resolution registers have been read, the associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
2. If V_{CCP}LO (Bit 1 of the Dynamic T_{MIN} Control Register 1, 0x36) is set, V_{CCP} can control the sleep state of the ADT7467.
3. V_{CC} (Pin 3) is the supply voltage for the ADT7467.

Table 44. TEMPERATURE READING REGISTERS (POWER-ON DEFAULT = 0X01) (Notes 1, 2)

Register Address	R/W	Description
0x25	Read Only	Remote 1 Temperature Reading (Notes 3, 4) (8 MSBs of Reading)
0x26	Read Only	Local Temperature Reading (8 MSBs of Reading)
0x27	Read Only	Remote 2 Temperature Reading (8 MSBs of Reading)

1. These temperature readings can be in twos complement or Offset 64 format; this interpretation is determined by Bit 0 of Configuration Register 5 (0x7C).
2. If the extended resolution bits of these readings are also being read, the extended resolution registers (0x76, 0x77) must be read first. Once the extended resolution registers have been read, all associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
3. In twos complement mode, a temperature reading of −128°C (0x80) indicates a diode fault (open or short) on that channel.
4. In Offset 64 mode, a temperature reading of −64°C (0x00) indicates a diode fault (open or short) on that channel.

Table 45. FAN TACHOMETER READING REGISTERS (POWER-ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x28	Read Only	TACH1 Low Byte
0x29	Read Only	TACH1 High Byte
0x2A	Read Only	TACH2 Low Byte
0x2B	Read Only	TACH2 High Byte
0x2C	Read Only	TACH3 Low Byte
0x2D	Read Only	TACH3 High Byte
0x2E	Read Only	TACH4 Low Byte
0x2F	Read Only	TACH4 High Byte

1. These registers count the number of 11.11 μs periods (based on an internal 90 kHz clock) that occur between a number of consecutive fan TACH pulses (default = 2). The number of TACH pulses used to count can be changed using the TACH pulses per revolution register (0x7B). This allows the fan speed to be accurately measured. Because a valid fan tachometer reading requires that two bytes are read, the low byte must be read first. Both the low and high bytes are then frozen until read. At power-on, these registers contain 0x0000 until the first valid fan TACH measurement is read into these registers. This prevents false interrupts from occurring while the fans are spinning up.
   A count of 0xFFFF indicates that a fan is one of the following:
   - Stalled or blocked (object jamming the fan).
   - Failed (internal circuitry destroyed).
   - Not populated. (The ADT7467 expects to see a fan connected to each TACH. If a fan is not connected to a TACH, the minimum high and low bytes of that TACH should be set to 0xFFFF.)
   - Alternate function (for example, TACH4 reconfigured as $\overline{\text{THERM}}$ pin).
   - 2-wire instead of 3-wire fan.

Table 46. CURRENT PWM DUTY CYCLE REGISTERS (POWER-ON DEFAULT = 0X00) (Note 1)

Register Address	R/W	Description
0x30	Read/Write	PWM1 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)
0x31	Read/Write	PWM2 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)
0x32	Read/Write	PWM3 Current Duty Cycle (0% to 100% Duty Cycle = 0x00 to 0xFF)

1. These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the ADT7467 reports the PWM duty cycles through these registers. The PWM duty cycle values vary according to the temperature in automatic fan speed control mode. During fan startup, these registers report 0x00. In software mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

Table 47. OPERATING POINT REGISTERS (POWER-ON DEFAULT = 0XA4) (Notes 1, 2, 3)

Register Address	R/W	Description
0x33	Read/Write	Remote 1 Operating Point Register (Default = 100°C)
0x34	Read/Write	Local Temperature Operating Point Register (Default = 100°C)
0x35	Read/Write	Remote 2 Operating Point Register (Default = 100°C)

1. These registers set the target operating point for each temperature channel when the dynamic T_{MIN} control feature is enabled.
2. The fans being controlled are adjusted to maintain temperature about an operating point.
3. These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 48. REGISTER 0X36 – DYNAMIC T_{MIN} CONTROL REGISTER 1 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit	Name	R/W	Description
<0>	CYR2	Read/Write	MSB of 3-bit Remote 2 cycle value. The other two bits of the code reside in Dynamic T_{MIN} Control Register 2 (0x37). These three bits define the delay time, in terms of the number of monitoring cycles, for making subsequent T_{MIN} adjustments in the control loop. The system is associated with thermal time constants that must be found to optimize the response of the fans and the control loop.
<1>	V_{CCP}LO	Read/Write	V_{CCP}LO = 1. When the power is supplied from 3.3 V STANDBY and the core voltage (V_{CCP}) drops below its V_{CCP} low limit value (Register 0x46), the following occurs: Status Bit 1 in Interrupt Status Register 1 is set. $\overline{\text{SMBALERT}}$ is generated if enabled. $\overline{\text{PROCHOT}}$ monitoring is disabled. Dynamic T_{MIN} control is disabled. The device is prevented from entering shutdown. Everything is re-enabled once V_{CCP} increases above the VCCPLO limit.
<2>	PHTR1	Read/Write	PHTR1 = 1 copies the Remote 1 current temperature to the Remote 1 operating point register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted, allowing the system to run as quietly as possible without affecting system performance. PHTR1 = 0 ignores $\overline{\text{THERM}}$ assertions on the $\overline{\text{THERM}}$ pin. The Remote 1 operating point register reflects its programmed value.
<3>	PHTL	Read/Write	PHTL = 1 copies the local channel's current temperature to the local operating point register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted. This allows the system to run as quietly as possible without affecting system performance. PHTL = 0 ignores $\overline{\text{THERM}}$ assertions on the $\overline{\text{THERM}}$ pin. The local temperature operating point register reflects its programmed value.
<4>	PHTR2	Read/Write	PHTR2 = 1 copies the Remote 2 current temperature to the Remote 2 operating point register if $\overline{\text{THERM}}$ is asserted. The operating point contains the temperature at which $\overline{\text{THERM}}$ is asserted, allowing the system to run as quietly as possible without affecting system performance. PHTR2 = 0 ignores $\overline{\text{THERM}}$ assertions on the $\overline{\text{THERM}}$ pin. The Remote 2 operating point register reflects its programmed value.
<5>	R1T	Read/Write	R1T = 1 enables dynamic T_{MIN} control on the Remote 1 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for the zone. R1T = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Fan Speed Control section.
<6>	LT	Read/Write	LT = 1 enables dynamic T_{MIN} control on the local temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for the zone. LT = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Fan Speed Control section.
<7>	R2T	Read/Write	R2T = 1 enables dynamic T_{MIN} control on the Remote 2 temperature channel. The chosen T_{MIN} value is dynamically adjusted based on the current temperature, operating point, and high and low limits for the zone. R2T = 0 disables dynamic T_{MIN} control. The T_{MIN} value chosen is not adjusted, and the channel behaves as described in the Fan Speed Control section.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 49. REGISTER 0X37 – DYNAMIC T_{MIN} CONTROL REGISTER 2 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit	Name	R/W	Description
<2:0>	CYR1	Read/Write	3-bit Remote 1 cycle value. These three bits define the delay time, in terms of the number of monitoring cycles, for making subsequent T_{MIN} adjustments in the control loop for the Remote 1 channel. The system is associated with thermal time constants that must be found to optimize the response of the fans and the control loop. **Bits** **Decrease (Short) Cycle** **Increase (Long) Cycle** 000 8 cycles (1 sec) 16 cycles (2 sec) 001 16 cycles (2 sec) 32 cycles (4 sec) 010 32 cycles (4 sec) 64 cycles (8 sec) 011 64 cycles (8 sec) 128 cycles (16 sec) 100 128 cycles (16 sec) 256 cycles (32 sec) 101 256 cycles (32 sec) 512 cycles (64 sec) 110 512 cycles (64 sec) 1024 cycles (128 sec) 111 1024 cycles (128 sec) 2048 cycles (256 sec)
<5:3>	CYL	Read/Write	3-bit local temperature cycle value. These three bits define the delay time, in terms of number of monitoring cycles, for making subsequent T_{MIN} adjustments in the control loop for the local temperature channel. The system is associated with thermal time constants that must be found to optimize the response of the fans and the control loop. **Bits** **Decrease (Short) Cycle** **Increase (Long) Cycle** 000 8 cycles (1 sec) 16 cycles (2 sec) 001 16 cycles (2 sec) 32 cycles (4 sec) 010 32 cycles (4 sec) 64 cycles (8 sec) 011 64 cycles (8 sec) 128 cycles (16 sec) 100 128 cycles (16 sec) 256 cycles (32 sec) 101 256 cycles (32 sec) 512 cycles (64 sec) 110 512 cycles (64 sec) 1024 cycles (128 sec) 111 1024 cycles (128 sec) 2048 cycles (256 sec)
<7:6>	CYR2	Read/Write	2 LSBs of 3-bit Remote 2 cycle value. The MSB of the 3-bit code resides in dynamic T_{MIN} Control Register 1 (0x36). These three bits define the delay time, in terms of number of monitoring cycles, for making subsequent T_{MIN} adjustments in the control loop for the Remote 2 channel. The system is associated with thermal time constants that must be found to optimize the response of fans and the control loop. **Bits** **Decrease Cycle** **Increase Cycle** 000 8 cycles (1 sec) 16 cycles (2 sec) 001 16 cycles (2 sec) 32 cycles (4 sec) 010 32 cycles (4 sec) 64 cycles (8 sec) 011 64 cycles (8 sec) 128 cycles (16 sec) 100 128 cycles (16 sec) 256 cycles (32 sec) 101 256 cycles (32 sec) 512 cycles (64 sec) 110 512 cycles (64 sec) 1024 cycles (128 sec) 111 1024 cycles (128 sec) 2048 cycles (256 sec)

1. These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 50. MAXIMUM PWM DUTY CYCLE REGISTERS (POWER-ON DEFAULT = 0XFF) (Note 1)

Register Address	R/W	Description
0x38	Read/Write	Maximum Duty Cycle for PWM1 Output, Default = 100% (0xFF)
0x39	Read/Write	Maximum Duty Cycle for PWM2 Output, Default = 100% (0xFF)
0x3A	Read/Write	Maximum Duty Cycle for PWM3 Output, Default = 100% (0xFF)

1. These registers set the maximum PWM duty cycle of the PWM output.

Table 51. REGISTER 0X40 − CONFIGURATION REGISTER 1 (POWER-ON DEFAULT = 0X01) (Note 1)

Bit	Name	R/W	Description
<0>	STRT	Read/Write	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control based on the default power-up limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit becomes a read-only bit and cannot be changed once Bit 1 (LOCK bit) has been written. All limit registers should be programmed by BIOS before setting this bit to 1. (Lockable)
<1>	LOCK	Write Once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read-only registers and cannot be modified until the ADT7467 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable)
<2>	RDY	Read Only	This bit is only set to 1 by the ADT7467 to indicate that the device is fully powered up and ready to begin system monitoring.
<3>	FSPD	Read/Write	When set to 1, this bit runs all fans at full speed. Power-on default = 0. This bit cannot be locked at any time.
<4>	VxI	Read/Write	BIOS should set this bit to a 1 when the ADT7467 is configured to measure current from an ADI ADOPT VRM controller and to measure the CPU's core voltage. This bit allows monitoring software to display the watts used by the CPU. (Lockable)
<5>	FSPDIS	Read/Write	Logic 1 disables fan spin-up for two TACH pulses, and the PWM outputs go high for the entire fan spin-up timeout selected.
<6>	TODIS	Read/Write	When this bit is set to 1, the SMBus timeout feature is disabled. This allows the ADT7467 to be used with SMBus controllers that cannot handle SMBus timeouts. (Lockable)
<7>	V_{CC}	Read/Write	When this bit is set to 1, the ADT7467 rescales its V_{CC} pin to measure 5 V supply. If this bit is 0, the ADT7467 measures V_{CC} as a 3.3 V supply. (Lockable)

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 52. REGISTER 0X41 − INTERRUPT STATUS REGISTER 1 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<1>	V_{CCP}	Read Only	V_{CCP} = 1 indicates that the V_{CCP} high or low limit has been exceeded. This bit is cleared upon a read of the status register if the error condition has subsided.
<2>	V_{CC}	Read Only	V_{CC} = 1 indicates that the V_{CC} high or low limit has been exceeded. This bit is cleared upon a read of the status register if the error condition has subsided.
<4>	R1T	Read Only	R1T = 1 indicates that the Remote 1 low or high temperature has been exceeded. This bit is cleared upon a read of the status register if the error condition has subsided.
<5>	LT	Read Only	LT = 1 indicates that the local low or high temperature has been exceeded. This bit is cleared upon a read of the status register if the error condition has subsided.
<6>	R2T	Read Only	R2T = 1 indicates that the Remote 2 low or high temperature has been exceeded. This bit is cleared upon a read of the status register if the error condition has subsided.
<7>	OOL	Read Only	OOL = 1 indicates that an out-of-limit event has been latched in Status Register 2. This bit is a logical OR of all status bits in Status Register 2. Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Status Register 2 are out of limit, which eliminates the need to read Status Register 2 at every interrupt or in every polling cycle.

Table 53. REGISTER 0X42 – INTERRUPT STATUS REGISTER 2 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<1>	OVT	Read Only	OVT = 1 indicates that one of the $\overline{\text{THERM}}$ overtemperature limits has been exceeded. This bit is cleared upon a read of the status register when the temperature drops below $\overline{\text{THERM}}$ – T_{HYST}.
<2>	FAN1	Read Only	FAN1 = 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is not set when the PWM1 output is off.
<3>	FAN2	Read Only	FAN2 = 1 indicates that Fan 2 has dropped below minimum speed or has stalled. This bit is not set when the PWM2 output is off.
<4>	FAN3	Read Only	FAN3 = 1 indicates that Fan 3 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off.
<5>	F4P	Read Only	F4P = 1 indicates that Fan 4 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off.
		Read/Write	When Pin 9 is programmed as a GPIO output, writing to this bit determines the logic output of the GPIO.
		Read Only	If Pin 9 is configured as the $\overline{\text{THERM}}$ timer input for $\overline{\text{THERM}}$ monitoring, then this bit is set when the $\overline{\text{THERM}}$ assertion time exceeds the limit programmed in the $\overline{\text{THERM}}$ limit register (0x7A).
<6>	D1	Read Only	D1 = 1 indicates either an open or short circuit on the Thermal Diode 1 inputs.
<7>	D2	Read Only	D2 = 1 indicates either an open or short circuit on the Thermal Diode 2 inputs.

Table 54. VOLTAGE LIMIT REGISTERS (Note 1)

Register Address	R/W	Description (Note 2)	Power-On Default
0x46	Read/Write	V_{CCP} Low Limit	0x00
0x47	Read/Write	V_{CCP} High Limit	0xFF
0x48	Read/Write	V_{CC} Low Limit	0x00
0x49	Read/Write	V_{CC} High Limit	0xFF

1. Setting the Configuration Register 1 LOCK bit has no effect on these registers.
2. High limit: An interrupt is generated when a value exceeds its high limit (>comparison). Low limit: An interrupt is generated when a value is equal to or below its low limit (≤comparison).

Table 55. TEMPERATURE LIMIT REGISTERS (Note 1)

Register Address	R/W	Description (Note 2)	Power-On Default
0x4E	Read/Write	Remote 1 Temperature Low Limit	0x01
0x4F	Read/Write	Remote 1 Temperature High Limit	0x7F
0x50	Read/Write	Local Temperature Low Limit	0x01
0x51	Read/Write	Local Temperature High Limit	0x7F
0x52	Read/Write	Remote 2 Temperature Low Limit	0x01
0x53	Read/Write	Remote 2 Temperature High Limit	0x7F

1. Exceeding any temperature limit by 1°C sets the appropriate status bit in the interrupt status register. Setting the Configuration Register 1 LOCK bit has no effect on these registers.
2. High limit: An interrupt is generated when a value exceeds its high limit (>comparison). Low limit: An interrupt is generated when a value is equal to or below its low limit (≤comparison).

Table 56. FAN TACHOMETER LIMIT REGISTERS (Note 1)

Register Address	R/W	Description	Power-On Default
0x54	Read/Write	TACH1 Minimum Low Byte	0xFF
0x55	Read/Write	TACH1 Minimum High Byte/Single-channel ADC Channel Select	0xFF
0x56	Read/Write	TACH2 Minimum Low Byte	0xFF
0x57	Read/Write	TACH2 Minimum High Byte	0xFF
0x58	Read/Write	TACH3 Minimum Low Byte	0xFF
0x59	Read/Write	TACH3 Minimum High Byte	0xFF
0x5A	Read/Write	TACH4 Minimum Low Byte	0xFF
0x5B	Read/Write	TACH4 Minimum High Byte	0xFF

1. Exceeding any TACH limit register by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 LOCK bit has no effect on these registers.

Table 57. REGISTER 0X55 – TACH 1 MINIMUM HIGH BYTE (POWER-ON DEFAULT = 0XFF)

Bit	Name	R/W	Description
<4:0>	Reserved	Read Only	These bits are reserved when Bit 6 of Configuration 2 Register (0x73) is set (single-channel ADC mode). Otherwise, these bits represent Bits <4:0> of the TACH1 minimum high byte.
<7:5>	SCADC	Read/Write	When Bit 6 of Configuration 2 Register (0x73) is set (single-channel ADC mode), these bits are used to select the only channel from which the ADC makes measurements. Otherwise, these bits represent Bits <7:5> of the TACH1 minimum high byte.

Table 58. PWM CONFIGURATION REGISTERS

Register Address	R/W (Note 1)	Description	Power-On Default
0x5C	Read/Write	PWM1 Configuration	0x82
0x5D	Read/Write	PWM2 Configuration	0x82
0x5E	Read/Write	PWM3 Configuration	0x82

1. These registers become read−only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 59. REGISTER 0X5C, REGISTER 0X5D, AND REGISTER 0X5E – PWM1, PWM2, AND PWM3 CONFIGURATION REGISTERS (POWER-ON DEFAULT = 0X82)

Bit	Name	R/W (Note 1)	Description
<2:0>	SPIN	Read/Write	These bits control the start-up timeout for PWMx. The PWM output stays high until two valid TACH rising edges are seen from the fan. If there is not a valid TACH signal during the fan TACH measurement immediately after the fan start-up timeout period, the TACH measurement reads 0xFFFF and Status Register 2 reflects the fan fault. If the TACH minimum high and low bytes contain 0xFFFF or 0x0000, the Status Register 2 bit is not set, even if the fan has not started. 000 = No start-up timeout 001 = 100 ms 010 = 250 ms (default) 011 = 400 ms 100 = 667 ms 101 = 1 sec 110 = 2 sec 111 = 4 sec
<3>	SLOW	Read/Write	SLOW = 1 makes the ramp rates for acoustic enhancement four times longer.
<4>	INV	Read/Write	This bit inverts the PWM output. The default is 0, which corresponds to a logic high output for 100% duty cycle. Setting this bit to 1 inverts the PWM output so that 100% duty cycle corresponds to a logic low output.
<7:5>	BHVR	Read/Write	These bits assign each fan to a particular temperature sensor for localized cooling. 000 = Remote 1 temperature controls PWMx (automatic fan control mode). 001 = local temperature controls PWMx (automatic fan control mode). 010 = Remote 2 temperature controls PWMx (automatic fan control mode). 011 = PWMx runs at full speed. 100 = PWMx disabled (default). 101 = fastest speed calculated by local and Remote 2 temperature controls PWMx. 110 = fastest speed calculated by all three temperature channel controls PWMx. 111 = manual mode. PWM duty cycle registers (0x30 to 0x32) become writable.

1. These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 60. T_{RANGE}/PWM FREQUENCY REGISTERS

Register Address	R/W (Note 1)	Description	Power-On Default
0x5F	Read/Write	Remote 1 T_{RANGE}/PWM1 Frequency	0xC4
0x60	Read/Write	Local T_{RANGE}/PWM2 Frequency	0xC4
0x61	Read/Write	Remote 2 T_{RANGE}/PWM3 Frequency	0xC4

1. These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 61. REGISTER 0X5F, REGISTER 0X60, AND REGISTER 0X61 − REMOTE 1, LOCAL, AND REMOTE 2 T_{RANGE}/PWMX FREQUENCY REGISTERS (POWER-ON DEFAULT = 0XC4)

Bit	Name	R/W (Note 1)	Description
<2:0>	FREQ	Read/Write	These bits control the PWMx frequency. 000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz
<3>	THRM	Read/Write	THRM = 1 causes the $\overline{\text{THERM}}$ pin (Pin 9) to assert low as an output when this temperature channel's $\overline{\text{THERM}}$ limit is exceeded by 0.25°C. The $\overline{\text{THERM}}$ pin remains asserted until the temperature is equal to or below the $\overline{\text{THERM}}$ limit. The minimum time that $\overline{\text{THERM}}$ asserts is one monitoring cycle. This allows clock modulation of devices that incorporate this feature. THRM = 0 makes the $\overline{\text{THERM}}$ pin act as an input when Pin 9 is configured as $\overline{\text{THERM}}$, for example, for Pentium® 4 $\overline{\text{PROCHOT}}$ monitoring.
<7:4>	RANGE	Read/Write	These bits determine the PWM duty cycle vs. the temperature slope for automatic fan control. 0000 = 2°C 0001 = 2.5°C 0010 = 3.33°C 0011 = 4°C 0100 = 5°C 0101 = 6.67°C 0110 = 8°C 0111 = 10°C 1000 = 13.33°C 1001 = 16°C 1010 = 20°C 1011 = 26.67°C 1100 = 32°C (default) 1101 = 40°C 1110 = 53.33°C 1111 = 80°C

1. These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 62. REGISTER 0X62 – ENHANCED ACOUSTICS REGISTER 1 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W (Note 1)	Description
<2:0>	ACOU	Read/Write	These bits select the ramp rate applied to the PWM1 output. Instead of PWM1 jumping instantaneously to its newly calculated speed, PWM1 ramps gracefully at the rate determined by these bits. This feature enhances the acoustics of the fan being driven by the PWM1 output. **Time Slot Increase** — **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 5 — 7 sec 100 = 8 — 4.4 sec 101 = 12 — 3 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
<3>	EN1	Read/Write	When this bit is 1, acoustic enhancement is enabled on PWM1 output.
<4>	SYNC	Read/Write	SYNC = 1 synchronizes fan speed measurements on TACH2, TACH3, and TACH4 to PWM3. This allows up to three fans to be driven from PWM3 output and their speeds to be measured. SYNC = 0 synchronizes only TACH3 and TACH4 to PWM3 output.
<5>	MIN1	Read/Write	When the ADT7467 is in automatic fan control mode, this bit defines whether PWM1 is off (0% duty cycle) or at PWM1 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis. 1 = PWM1 minimum duty cycle below T_{MIN} – hysteresis.
<6>	MIN2	Read/Write	When the ADT7467 is in automatic fan speed control mode and the controlling temperature is below its T_{MIN} – hysteresis value, this bit defines whether PWM2 is off (0% duty cycle) or at PWM2 minimum duty cycle. 0 = 0% duty cycle below T_{MIN} – hysteresis. 1 = PWM2 minimum duty cycle below T_{MIN} – hysteresis.
<7>	MIN3	Read/Write	When the ADT7467 is in automatic fan speed control mode, this bit defines whether PWM3 is off (0% duty cycle) or at PWM3 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis. 1 = PWM3 minimum duty cycle below T_{MIN} – hysteresis.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 63. REGISTER 0X63 – ENHANCED ACOUSTICS REGISTER 2 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W (Note 1)	Description
<2:0>	ACOU3	Read/Write	These bits select the ramp rate applied to the PWM3 output. Instead of PWM3 jumping instantaneously to its newly calculated speed, PWM3 ramps gracefully at the rate determined by these bits. This effect enhances the acoustics of the fan being driven by the PWM3 output. **Time Slot Increase** — **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 5 — 7 sec 100 = 8 — 4.4 sec 101 = 12 — 3 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
<3>	EN3	Read/Write	When this bit is 1, acoustic enhancement is enabled on PWM3 output.
<6:4>	ACOU2	Read/Write	These bits select the ramp rate applied to the PWM2 output. Instead of PWM2 jumping instantaneously to its newly calculated speed, PWM2 ramps gracefully at the rate determined by these bits. This effect enhances the acoustics of the fans being driven by the PWM2 output. **Time Slot Increase** — **Time for 33% to 100%** 000 = 1 — 35 sec 001 = 2 — 17.6 sec 010 = 3 — 11.8 sec 011 = 5 — 7 sec 100 = 8 — 4.4 sec 101 = 12 — 3 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
<7>	EN2	Read/Write	When this bit is 1, acoustic enhancement is enabled on PWM2 output.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 64. PWM MINIMUM DUTY CYCLE REGISTERS

Register Address	R/W (Note 1)	Description	Power-On Default
0x64	Read/Write	PWM1 Minimum Duty Cycle	0x80 (50% Duty Cycle)
0x65	Read/Write	PWM2 Minimum Duty Cycle	0x80 (50% Duty Cycle)
0x66	Read/Write	PWM3 Minimum Duty Cycle	0x80 (50% Duty Cycle)

1. These registers become read-only registers when the ADT7467 is in automatic fan control mode.

Table 65. REGISTER 0x64, REGISTER 0x65, AND REGISTER 0x66 – PWM1, PWM2, and PWM3 Minimum Duty Cycle Registers

Bit	R/W (Note 1)	Description
<7:0>	Read/Write	These bits define the PWM_{MIN} duty cycle for PWMx. 0x00 = 0% Duty Cycle (Fan Off) 0x40 = 25% Duty Cycle 0x80 = 50% Duty Cycle 0xFF = 100% Duty Cycle (Fan Full Speed)

1. These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 66. T_{MIN} REGISTERS (Note 1)

Register Address	R/W (Note 2)	Description	Power-On Default
0x67	Read/Write	Remote 1 T_{MIN}	0x9A (90°C)
0x68	Read/Write	Local T_{MIN}	0x9A (90°C)
0x69	Read/Write	Remote 2 T_{MIN}	0x9A (90°C)

1. These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan runs at minimum speed and increases with temperature according to T_{RANGE}.
2. These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 67. $\overline{\text{THERM}}$ TEMPERATURE LIMIT REGISTERS (Note 1)

Register Address	R/W (Note 2)	Description	Power-On Default
0x6A	Read/Write	Remote 1 $\overline{\text{THERM}}$ Temperature Limit	0xA4 (100°C)
0x6B	Read/Write	Local $\overline{\text{THERM}}$ Temperature Limit	0xA4 (100°C)
0x6C	Read/Write	Remote 2 $\overline{\text{THERM}}$ Temperature Limit	0xA4 (100°C)

1. If any temperature measured exceeds its $\overline{\text{THERM}}$ limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail-safe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below $\overline{\text{THERM}}$ limit − hysteresis. If the $\overline{\text{THERM}}$ pin is programmed as an output, exceeding these limits by 0.25°C can cause the $\overline{\text{THERM}}$ pin to assert low as an output.
2. These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 68. TEMPERATURE/T_{MIN} HYSTERESIS REGISTERS (Note 1)

Register Address	R/W (Note 2)	Description	Power-On Default
0x6D	Read/Write	Remote 1 and Local Temperature Hysteresis	0x44
0x6E	Read/Write	Remote 2 Temperature Hysteresis	0x40

1. Each 4-bit value controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan remains running at PWM_{MIN} duty cycle until the temperature = T_{MIN} − hysteresis. Up to 15°C of hysteresis can be assigned to any temperature channel. The hysteresis value chosen also applies to that temperature channel if its $\overline{\text{THERM}}$ limit is exceeded. If the $\overline{\text{THERM}}$ limit is exceeded, the PWM output being controlled goes to 100% and remains at 100% until the temperature drops below $\overline{\text{THERM}}$ − hysteresis. For acoustic reasons, it is recommended that the hysteresis value not be programmed to less than 4°C. Setting the hysteresis value lower than 4°C causes the fan to switch on and off regularly when the temperature is close to T_{MIN}.
2. These registers become read-only registers when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 69. REGISTER 0X6D − REMOTE 1 AND LOCAL TEMPERATURE HYSTERESIS

Bit	Name	R/W (Note 1)	Description
<3:0>	HYSL	Read/Write	Local temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature AFC and dynamic T_{MIN} control loops.
<7:4>	HYSR1	Read/Write	Remote 1 temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the Remote 1 temperature AFC and dynamic T_{MIN} control loops.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 70. REGISTER 0X6E − REMOTE 2 TEMPERATURE HYSTERESIS

Bit	Name	R/W (Note 1)	Description
<7:4>	HYSR2	Read/Write	Local temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature AFC and dynamic T_{MIN} control loops.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 71. REGISTER 0X6F − XNOR TREE TEST ENABLE (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W (Note 1)	Description
<0>	XEN	Read/Write	If the XEN bit is set to 1, the device enters the XNOR tree test mode. Clearing the bit removes the device from the XNOR tree test mode.
<7:1>	Reserved	Read Only	Unused. Do not write to these bits.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 72. REGISTER 0X70 − REMOTE 1 TEMPERATURE OFFSET (POWER-ON DEFAULT = 0X00)

Bit	R/W (Note 1)	Description
<7:0>	Read/write	Allows a twos complement offset value to be automatically added to or subtracted from the Remote 1 temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance. LSB value = 0.5°C.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 73. REGISTER 0X71 – LOCAL TEMPERATURE OFFSET (POWER-ON DEFAULT = 0X00)

Bit	**R/W** (Note 1)	Description
<7:0>	Read/Write	Allows a twos complement offset value to be automatically added to or subtracted from the local temperature reading. LSB value = 0.5°C.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 74. REGISTER 0X72 – REMOTE 2 TEMPERATURE OFFSET (POWER-ON DEFAULT = 0X00)

Bit	**R/W** (Note 1)	Description
<7:0>	Read/Write	Allows a twos complement offset value to be automatically added to or subtracted from the Remote 2 temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance. LSB value = 0.5°C.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 75. REGISTER 0X73 – CONFIGURATION REGISTER 2 (POWER-ON DEFAULT = 0X00)

Bit	Name	**R/W** (Note 1)	Description
<0>	AIN1	Read/Write	AIN1 = 0, speed of 3-wire fans measured using the TACH output from the fan. AIN1 = 1, Pin 6 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (0x7D). Only relevant in low frequency mode.
<1>	AIN2	Read/Write	AIN2 = 0, speed of 3-wire fans measured using the TACH output from the fan. AIN2 = 1, Pin 7 is reconfigured to measure the speed of 2 wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (0x7D). Only relevant in low frequency mode.
<2>	AIN3	Read/Write	AIN3 = 0, speed of 3-wire fans measured using the TACH output from the fan. AIN3 = 1, Pin 4 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (0x7D). Only relevant in low frequency mode.
<3>	AIN4	Read/Write	AIN4 = 0, speed of 3-wire fans measured using the TACH output from the fan. AIN4 = 1, Pin 9 is reconfigured to measure the speed of 2-wire fans using an external sensing resistor and coupling capacitor. AIN voltage threshold is set via Configuration Register 4 (0x7D). Only relevant in low frequency mode.
<4>	AVG	Read/Write	AVG = 1, averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster.
<5>	ATTN	Read/Write	ATTN = 1, the ADT7467 removes the attenuators from the V_{CCP} input. The V_{CCP} input can be used for other functions such as connecting external sensors.
<6>	CONV	Read/Write	CONV = 1, the ADT7467 is put into a single-channel ADC conversion mode. In this mode, the ADT7467 can be set to read continuously from one input only, for example, Remote 1 temperature. The appropriate ADC channel is selected by writing to bits <7:5> of the TACH1 minimum high byte register (0x55). **Bits <7:5>, Register 0x55** 000 Reserved 001 V_{CCP} 010 V_{CC} (3.3 V) 011 Reserved 100 Reserved 101 Remote 1 Temperature 110 Local Temperature 111 Remote 2 Temperature
<7>	SHDN	Read/Write	SHDN = 1, ADT7467 goes into shutdown mode. All PWM outputs assert low (or high depending on the state of the INV bit) to switch off all fans. The PWM current duty cycle registers read 0x00 to indicate that the fans are not being driven.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 76. REGISTER 0X74 – INTERRUPT MASK 1 REGISTER (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<1>	V_{CCP}	Read/Write	V_{CCP} = 1 masks $\overline{SMBALERT}$ for out-of-limit conditions on the V_{CCP} channel
<2>	V_{CC}	Read/Write	V_{CC} = 1 masks $\overline{SMBALERT}$ for out-of-limit conditions on the V_{CC} channel
<4>	R1T	Read/Write	R1T = 1 masks $\overline{SMBALERT}$ for out-of-limit conditions on the Remote 1 temperature channel
<5>	LT	Read/Write	LT = 1 masks $\overline{SMBALERT}$ for out-of-limit conditions on the local temperature channel
<6>	R2T	Read/Write	R2T = 1 masks $\overline{SMBALERT}$ for out-of-limit conditions on the Remote 2 temperature channel
<7>	OOL	Read/Write	OOL = 1 masks $\overline{SMBALERT}$ for any out-of-limit condition in Interrupt Status Register 2

Table 77. REGISTER 0X75 – INTERRUPT MASK 2 REGISTER (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<1>	OVT	Read/Write	OVT = 1 masks $\overline{SMBALERT}$ for overtemperature $\overline{THERM}$ conditions
<2>	FAN1	Read/Write	FAN1 = 1 masks $\overline{SMBALERT}$ for a Fan 1 fault
<3>	FAN2	Read/Write	FAN2 = 1 masks $\overline{SMBALERT}$ for a Fan 2 fault
<4>	FAN3	Read/Write	FAN3 = 1 masks $\overline{SMBALERT}$ for a Fan 3 fault
<5>	F4P	Read/Write	F4P = 1 masks $\overline{SMBALERT}$ for a Fan 4 fault. If the TACH4 pin is used as the $\overline{THERM}$ input, this bit masks $\overline{SMBALERT}$ for a $\overline{THERM}$ timer event.
<6>	D1	Read/Write	D1 = 1 masks $\overline{SMBALERT}$ for a diode open or short on a Remote 1 channel
<7>	D2	Read/Write	D2 = 1 masks $\overline{SMBALERT}$ for a diode open or short on a Remote 2 channel

Table 78. REGISTER 0X76 – EXTENDED RESOLUTION REGISTER 1 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit	Name	R/W	Description
<3:2>	V_{CCP}	Read/Write	V_{CCP} LSBs. Holds the 2 LSBs of the 10-bit V_{CCP} measurement
<5:4>	V_{CC}	Read/Write	V_{CC} LSBs. Holds the 2 LSBs of the 10-bit V_{CC} measurement

1. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 79. REGISTER 0X77 – EXTENDED RESOLUTION REGISTER 2 (POWER-ON DEFAULT = 0X00) (Note 1)

Bit	Name	R/W	Description
<3:2>	TDM1	Read/Write	Remote 1 temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 1 temperature measurement
<5:4>	LTMP	Read/Write	Local temperature LSBs. Holds the 2 LSBs of the 10-bit local temperature measurement
<7:6>	TDM2	Read/Write	Remote 2 temperature LSBs. Holds the 2 LSBs of the 10-bit Remote 2 temperature measurement

1. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 80. REGISTER 0X78 – CONFIGURATION REGISTER 3 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W (Note 1)	Description
<0>	ALERT Enable	Read/Write	ALERT = 1, Pin 5 (PWM2/$\overline{\text{SMBALERT}}$) is configured as an $\overline{\text{SMBALERT}}$ interrupt output to indicate out-of-limit error conditions.
<1>	$\overline{\text{THERM}}$	Read/Write	$\overline{\text{THERM}}$ Enable = 1 enables $\overline{\text{THERM}}$ timer monitoring functionality on Pin 9. Also determined by Bit 0 and Bit 1 (Pin 9 Func) of Configuration Register 4. When $\overline{\text{THERM}}$ is asserted, the fans run at full speed if the fans are running and the boost bit is set. Alternatively, $\overline{\text{THERM}}$ can be programmed so that a timer is triggered to time how long $\overline{\text{THERM}}$ has been asserted.
<2>	BOOST	Read/Write	When $\overline{\text{THERM}}$ is an input and BOOST = 1, assertion of $\overline{\text{THERM}}$ causes all fans to run at the maximum programmed duty cycle for fail-safe cooling.
<3>	FAST	Read/Write	FAST = 1 enables fast TACH measurements on all channels. This increases the TACH measurement rate from once per second to once every 250 ms (4 ×).
<4>	DC1	Read/Write	DC1 = 1 enables TACH measurements to be continuously made on TACH1. Fans must be driven by dc. Setting this bit prevents pulse stretching, because it is not required for dc-driven motors.
<5>	DC2	Read/Write	DC2 = 1 enables TACH measurements to be continuously made on TACH2. Fans must be driven by dc. Setting this bit prevents pulse stretching, because it is not required for dc-driven motors.
<6>	DC3	Read/Write	DC = 1 enables TACH measurements to be continuously made on TACH3. Fans must be driven by dc. Setting this bit prevents pulse stretching, because it is not required for dc-driven motors.
<7>	DC4	Read/Write	DC4 = 1 enables TACH measurements to be continuously made on TACH4. Fans must be driven by dc. Setting this bit prevents pulse stretching, because it is not required for dc-driven motors.

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 81. REGISTER 0X79 – $\overline{\text{THERM}}$ TIMER STATUS REGISTER (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<7:1>	TMR	Read Only	Times how long $\overline{\text{THERM}}$ input is asserted. These seven bits read 0 until the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms.
<0>	ASRT/TMR0	Read Only	This bit is set high upon the assertion of the $\overline{\text{THERM}}$ input and is cleared upon a read. If the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms, this bit is set and becomes the LSB of the 8-bit TMR reading. This allows $\overline{\text{THERM}}$ assertion times from 45.52 ms to 5.82 sec to be reported back with a resolution of 22.76 ms.

Table 82. REGISTER 0X7A – $\overline{\text{THERM}}$ TIMER LIMIT REGISTER (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<7:0>	LIMT	Read/Write	Sets the maximum $\overline{\text{THERM}}$ assertion length before an interrupt is generated. This is an 8-bit limit with a resolution of 22.76 ms, allowing $\overline{\text{THERM}}$ assertion limits of 45.52 ms to 5.82 sec to be programmed. If the $\overline{\text{THERM}}$ assertion time exceeds this limit, Bit 5 (F4P) of Interrupt Status Register 2 (0x42) is set. If the limit value is 0x00, an interrupt is generated immediately upon the assertion of the $\overline{\text{THERM}}$ input.

Table 83. REGISTER 0X7B – TACH PULSES PER REVOLUTION REGISTER (POWER-ON DEFAULT = 0X55)

Bit	Name	R/W	Description
<1:0>	FAN1	Read/Write	Sets the number of pulses to be counted when measuring Fan 1 speed. Can be used to determine fan pulses per revolution for an unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
<3:2>	FAN2	Read/Write	Sets the number of pulses to be counted when measuring Fan 2 speed. Can be used to determine fan pulses per revolution for an unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
<5:4>	FAN3	Read/Write	Sets the number of pulses to be counted when measuring Fan 3 speed. Can be used to determine fan pulses per revolution for an unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4
<7:6>	FAN4	Read/Write	Sets the number of pulses to be counted when measuring Fan 4 speed. Can be used to determine fan pulses per revolution for an unknown fan type. **Pulses Counted** 00 = 1 01 = 2 (Default) 10 = 3 11 = 4

Table 84. REGISTER 0X7C – CONFIGURATION REGISTER 5 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W (Note 1)	Description
<0>	Twos Compl	Read/Write	Twos Compl = 1 sets the temperature range to twos complement temperature range. Twos Compl = 0 changes the temperature range to Offset 64. When this bit is changed, the ADT7467 interprets all relevant temperature register values as defined by this bit.
<1>	LF/HF	Read/Write	Sets the PWM drive frequency to high frequency mode (0) or low frequency mode (1).
<2>	GPIOD	Read/Write	GPIO direction. When GPIO function is enabled, this determines whether the GPIO is an input (0) or an output (1).
<3>	GPIOP	Read/Write	GPIO polarity. When the GPIO function is enabled and programmed as an output, this bit determines whether the GPIO is active low (0) or high (1).
<4:7>	RES	Read/Write	Unused

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 85. REGISTER 0X7D − CONFIGURATION REGISTER 4 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W (Note 1)	Description
<1:0>	Pin 9 Func	Read/Write	These bits set the functionality of Pin 9. 00 = TACH4 (default) 01 = bidirectional $\overline{\text{THERM}}$ 10 = $\overline{\text{SMBALERT}}$ 11 = GPIO
<3:2>	AINL	Read/Write	These two bits define the input threshold for 2−wire fan speed measurements (low frequency mode only). 00 = ±20 Mv 01 = ±40 mV 10 = ±80 mV 11 = ±130 mV
<4>	RES		Unused
<5>	BpAtt V_{CCP}		Bypass V_{CCP} attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.2965 V (0xFF).
<6:7>	RES		Unused

1. This register becomes a read-only register when the Configuration Register 1 LOCK bit is set to 1. Any subsequent attempts to write to this register fail.

Table 86. REGISTER 0X7E − MANUFACTURER'S TEST REGISTER 1 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<7:0>	Reserved	Read Only	Manufacturer's test register. These bits are reserved for the manufacturer's testing purposes and should not be written to under normal operation.

Table 87. REGISTER 0X7F − MANUFACTURER'S TEST REGISTER 2 (POWER-ON DEFAULT = 0X00)

Bit	Name	R/W	Description
<7:0>	Reserved	Read Only	Manufacturer's test register. These bits are reserved for the manufacturer's testing purposes and should not be written to under normal operation.

Table 88. ORDERING INFORMATION

Device Number*	Temperature Range	Package Description	Package Option	Shipping†
ADT7467ARQZ−REEL	−40°C to +120°C	16-lead QSOP	RQ−16	2,500 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*The "Z" suffix indicates RoHS Compliant part.

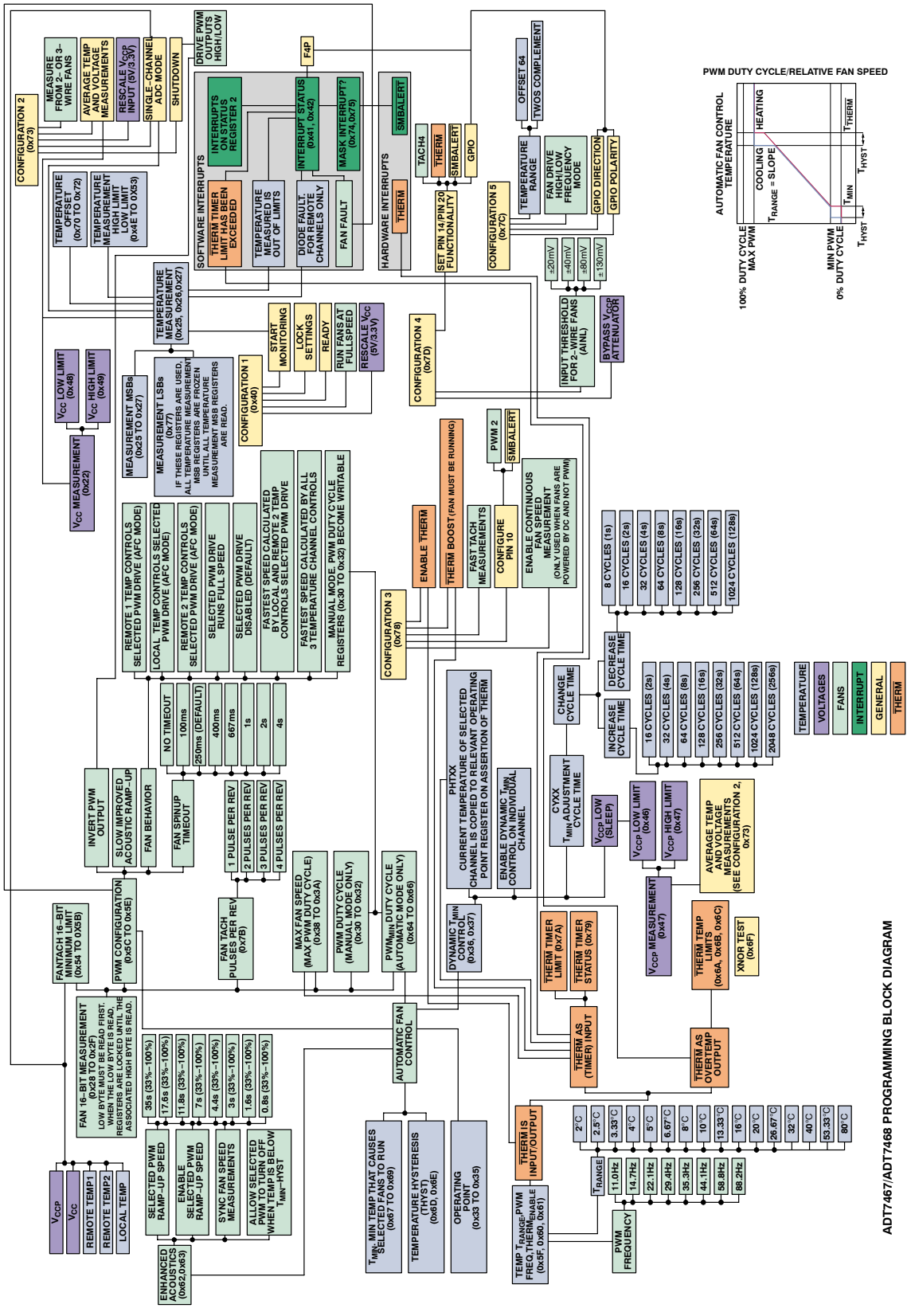


Figure 83. Block Diagram

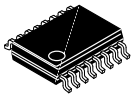
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

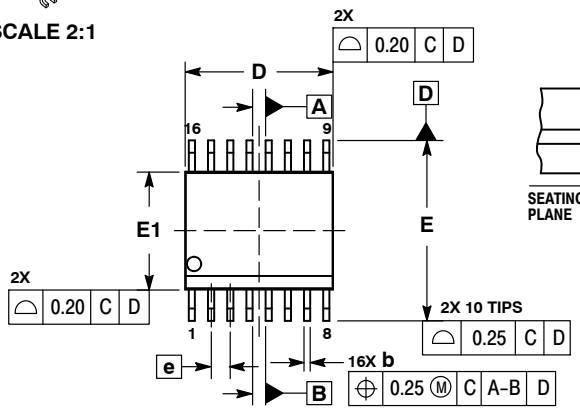
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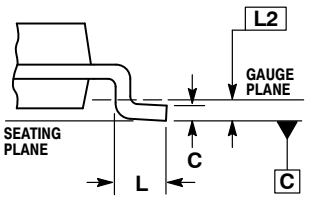
QSOP16
CASE 492−01
ISSUE A

DATE 23 MAR 2011

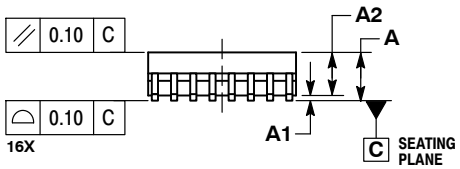


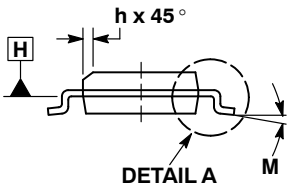
SCALE 2:1





DETAIL A

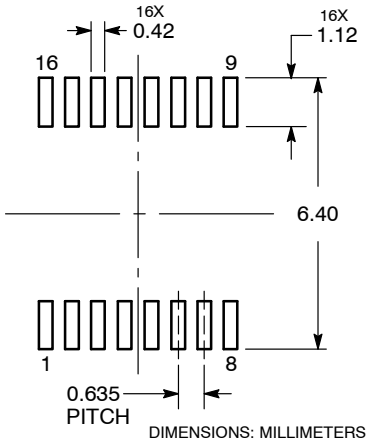




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.005 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.005 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

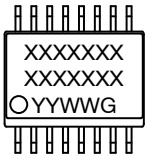
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.049	----	1.24	----
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.19	0.25
D	0.193 BSC		4.89 BSC	
E	0.237 BSC		6.00 BSC	
E1	0.154 BSC		3.90 BSC	
e	0.025 BSC		0.635 BSC	
h	0.009	0.020	0.22	0.50
L	0.016	0.050	0.40	1.27
L2	0.010 BSC		0.25 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G”, may or not be present.

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DESCRIPTION:	QSOP16	PAGE 1 OF 1

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