CAT5136, CAT5137, CAT5138

Digital Potentiometers (POTs) with 128 Taps and I²C Interface

ON Semiconductor®

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SC−70
SD SUFFIX
CASE 419AD

Description

CAT5136, CAT5137, and CAT5138 are a family of digital POTs operating like mechanical potentiometers in various configurations. The tap points between the 127 equal resistive elements are connected to the wiper output via CMOS switches. The switches are controlled by a 7-bit Wiper Control Register (WCR) via the I²C serial bus. CAT5136 is configured as a variable resistor. CAT5137 and CAT5138 are resistive voltage dividers, with one terminal of the potentiometer connected to GND. CAT5137 and CAT5138 have different device IDs, which makes it possible to use both on the same I²C bus. Upon power-up, the WCR is set to mid-scale (1000000).

Features

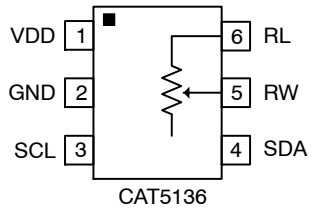
- Single Linear Digital Potentiometer with 128 Taps
- End-to-End Resistance of 10 kΩ, 50 kΩ and 100 kΩ
- I²C Interface
- Wiper goes to Midscale at Power-up
- Digital Supply Range (V_{DD}): 2.7 V to 5.5 V
- Low Standby Current
- Industrial Temperature Range: −40°C to +85°C
- 6-pin SC−70 Package
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

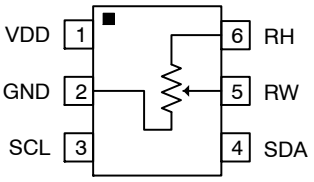
- LCD Screen Adjustment
- Volume Control
- Mechanical Potentiometer Replacement
- Gain Adjustment
- Line Impedance Matching
- VCOM Setting Adjustments

PIN CONNECTIONS

(for low pin count devices)



CAT5136



CAT5137
CAT5138

(Top Views)

See detailed pin function descriptions on page 2.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

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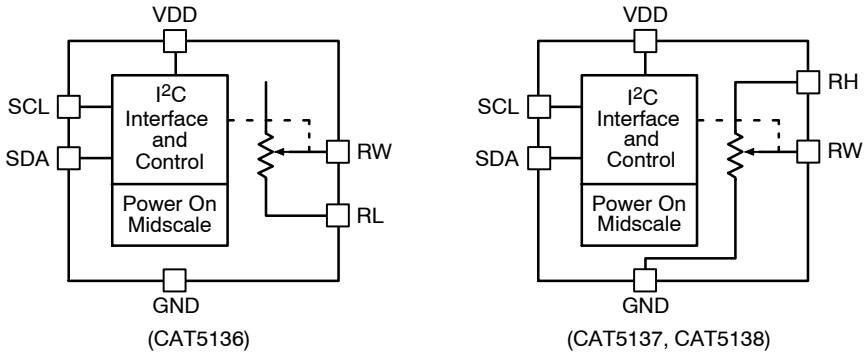


Figure 1. Block Diagram

Table 1. PIN FUNCTION DESCRIPTION

Pin No.		Pin Name	Description
CAT5136	CAT5137/CAT5138		
1	1	VDD	Digital Supply Voltage (2.7 V to 5.5 V)
2	2	GND	Ground
3	3	SCL	Serial Bus Clock input for the I^2C Serial Bus. This clock is used to clock all data transfers into and out of the CAT5136−8
4	4	SDA	Serial Data Input/Output − Bidirectional Serial Data pin used to transfer data into and out of the CAT5136−8. This is an Open-Drain I/O and can be wire OR'd with other Open-Drain (or Open Collector) I/Os.
5	5	RW	Wiper Terminal for the potentiometer
6	−	RL	Low Reference Terminal for the potentiometer
−	6	RH	High Reference Terminal for the potentiometer

Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Range	Unit
Temperature Under Bias		−55 to +125	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
Voltage on any SDA, SCL, A0 & A1 pins with respect to Ground (Note 1)		−0.3 to V_{DD} + 0.3	V
Voltage on RH, RL & RW pins with respect to Ground		−0.3 to V_{DD} + 0.3	V
V_{DD} with respect to Ground		−0.3 to +6	V
Wiper Current (10 sec)		±6	mA
Lead Soldering temperature (10 sec)		+300	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Latch-up protection is provided for stresses up to 100 mA on address and data pins from −0.3 V to V_{DD} +0.3 V.

Table 3. RECOMMENDED OPERATION CONDITIONS

Parameter	Symbol	Value	Unit
Digital Supply Voltage	V_{DD}	+2.7 to +5.5	V
Operating Temperature Range		−40 to +85	°C

Table 4. POTENTIOMETERS CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Parameter	Symbol	Test Conditions	Limits			Units
			Min	Typ	Max	
Potentiometer Resistance (10 kΩ)	R_{POT}			10		kΩ
Potentiometer Resistance (50 kΩ)	R_{POT}			50		kΩ
Potentiometer Resistance (100 kΩ)	R_{POT}			100		kΩ
Potentiometer Resistance Tolerance	R_{TOL}				±20	%
Power Rating		25°C			50	mW
Wiper Current	I_W				±3	mA
Wiper Resistance	R_W	V_{DD} = 3.3 V		85	200	Ω
Voltage on R_W, R_H or R_L	V_{TERM}	GND = 0 V; V_{DD} = 2.7 V to +5.5 V	GND		V_{DD}	V
Resolution	RES			0.78		%
Integral Non-Linearity (Note 3)	INL	$V_{W(n)(actual)} - V_{W(n)(expected)}$ (Notes 6, 7)			±1	LSB (Note 5)
Differential Non-Linearity (Note 4)	DNL	$V_{W(n+1)} - [V_{W(n)}+LSB]$ (Notes 6, 7)			1	LSB (Note 5)
Resistor Integral Non-Linearity	R_{INL}	R_n – n*LSB (Notes 6, 8)			± 2	LSB (Note 5)
Resistor Differential Non-Linearity	R_{DNL}	$R_n - [R_{n-1} + LSB]$ (Notes 6, 8)			± 1	LSB (Note 5)
Temperature Coefficient of R_{POT}	T_{CRPOT}	(Note 2)		±300		ppm/°C
Ratiometric Temperature Coefficient	T_{CRatio}	(Note 2)			30	ppm/°C
Potentiometer Capacitances	$C_H/C_L/C_W$	(Note 2)		10/10/25		pF
Frequency Response	fc	R_{POT}		0.4		MHz

2. This parameter is tested initially and after a design or process change that affects the parameter.
3. Integral Non-Linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
4. Differential Non-Linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer.
5. LSB = $(R_{HM} - R_{LM})/127$; where R_{HM} and R_{LM} are the highest and lowest measured values on the wiper terminal.
6. n = 1, 2, ..., 127
7. V_{DD} @ R_H; V_W measured @ R_W with no load.
8. Rw and R_L in the range of 0 V and V_{DD}.

Table 5. D.C. ELECTRICAL CHARACTERISTICS (Over recommended operating conditions unless otherwise stated.)

Parameter	Symbol	Test Conditions	Min	Max	Units
Power Supply Current (Write/Read)	I_{DD}	F_{SCL} = 400 kHz, SDA Open, V_{DD} = 5.5 V, Input = GND		200	μA
Standby Current	$I_{SB(VDD)}$	V_{IN} = GND or V_{DD} , SDA = V_{DD}		0.5	μA
Input Leakage Current	I_{LI}	V_{IN} = GND to V_{DD}	−1	1	μA
Output Leakage Current	I_{LO}	V_{OUT} = GND to V_{DD}	−1	1	μA
Input Low Voltage	V_{IL}		−0.3	V_{DD} x 0.3	V
Input High Voltage	V_{IH}		V_{DD} x 0.7	V_{DD} + 0.3	V
Output Low Voltage (V_{DD} = 3.0 V)	V_{OL}	I_{OL} = 3 mA		0.4	V

Table 6. A.C. CHARACTERISTICS

Parameter (see Figure 6)	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Clock Frequency	F_{SCL}			400	kHz
Noise Suppression Time Constant at SCL & SDA Inputs	T_I (Note 9)			50	ns
SCL Low to SDA Data Out and ACK Out	t_{AA}			1	μs
Time the bus must be free before a new transmission can start	t_{BUF} (Note 9)	1.2			μs
Start Condition Hold Time	$t_{HD:STA}$	0.6			μs
Clock Low Period	t_{LOW}	1.2			μs
Clock High Period	t_{HIGH}	0.6			μs
Start Condition Setup Time (for a Repeated Start Condition)	$t_{SU:STA}$	0.6			μs
Data In Setup Time	$t_{SU:DAT}$	100			ns
Data in Hold Time	$t_{HD:DAT}$	0			μs
SDA and SCL Rise Time	t_R (Note 9)			0.3	μs
SDA and SCL Fall Time	t_F (Note 9)			300	ns
Stop Conditions Setup Time	$t_{SU:STO}$	0.6			μs
Data Out Hold Time	t_{DH}	100			ns

9. This parameter is tested initially and after a design or process change that affects the parameter.

Table 7. CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{DD} = 5.0 V)

Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Unit**
Input/Output Capacitance (SDA, SDC)	$C_{I/O}$	$V_{I/O}$ = 0 V (Note 10)			10	pF

10. This parameter is tested initially and after a design or process change that affects the parameter.

Table 8. POWER-UP TIMING (Notes 11, 12)

Symbol	**Parameter**	**Min**	**Max**	**Units**
t_{PUR}	Power-up to Read Operation		1	ms
t_{PUW}	Power-up to Write Operation		1	ms

11. This parameter is tested initially and after a design or process change that affects the parameter.
12. t_{PUR} and t_{PUW} are the delays required from the time V_{DD} is stable until the specified operation can be initiated.

Table 9. WIPER TIMING

Symbol	**Parameter**	**Min**	**Max**	**Units**
t_{WRPO}	Wiper Response Time After Power Supply Stable	5	10	μs
t_{WRL}	Wiper Response Time After Instruction Issued	5	10	μs

TYPICAL PERFORMANCE CHARACTERISTICS

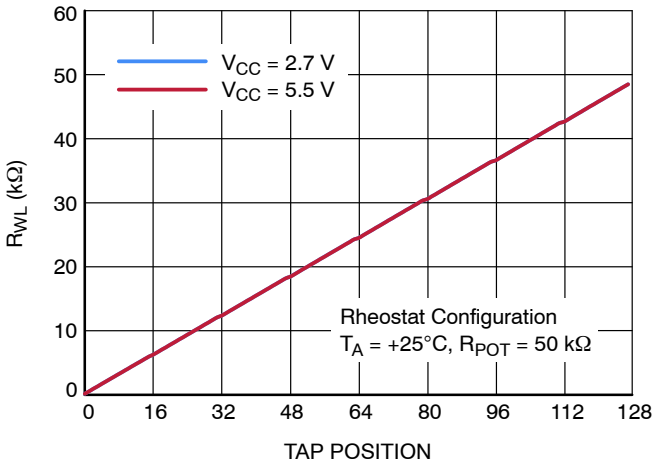


Figure 2. Resistance between R_W and R_L

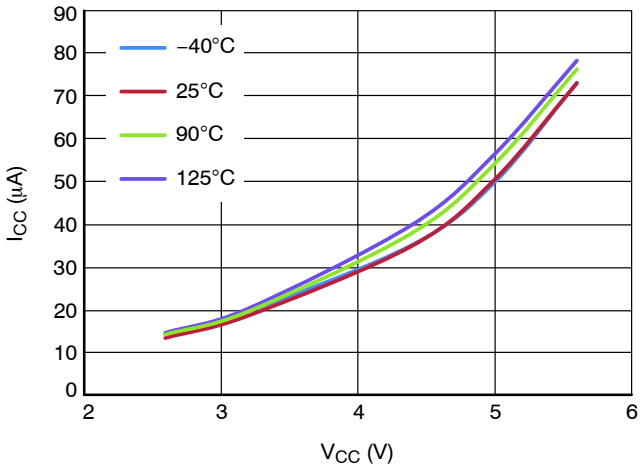


Figure 3. Power Supply Current

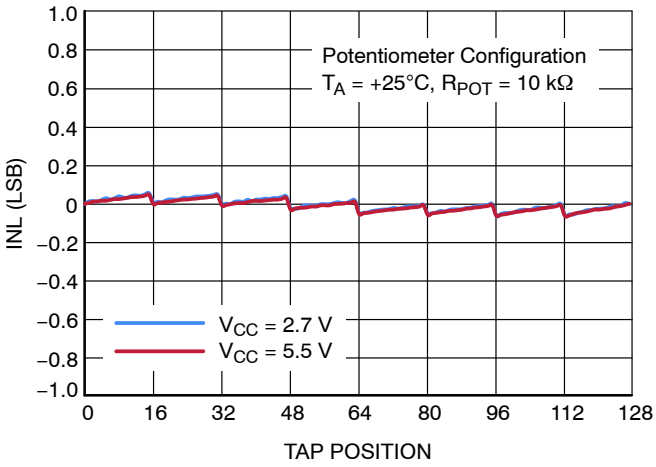


Figure 4. Integral Non−Linearity

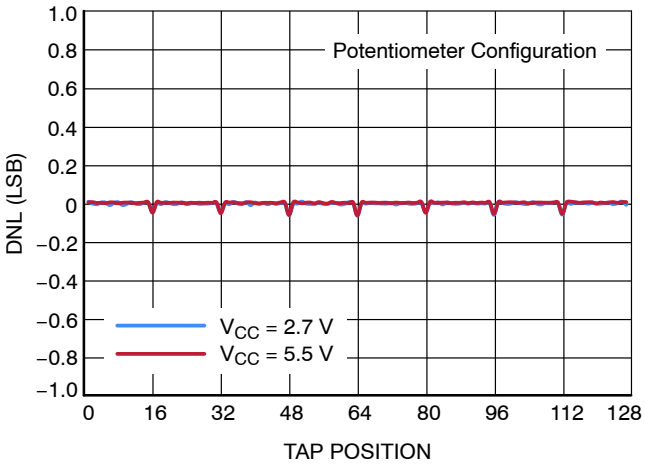


Figure 5. Differential Non−Linearity

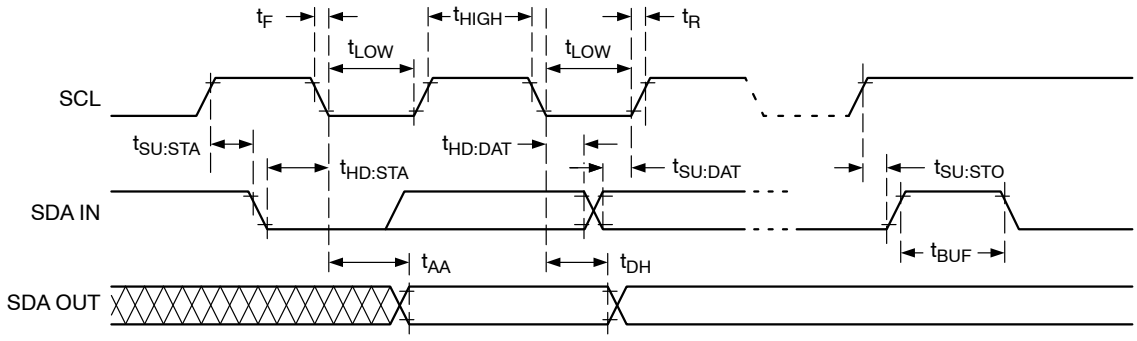


Figure 6. Bus Timing

SERIAL BUS PROTOCOL

The following defines the features of the I^2C bus protocol:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock is high will be interpreted as a START or STOP condition.

The device controlling the transfer is a master, typically a processor or controller, and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the CAT513x will be considered a slave device in all applications.

START Condition

The START Condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT513x monitors the SDA and SCL lines and will not respond until this condition is met (see Figure 7).

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition (see Figure 7).

Acknowledge

After a successful data transfer, each receiving device is required to generate an acknowledge. The acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data (see Figure 8).

The CAT513x responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte.

When the CAT513x is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT513x will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

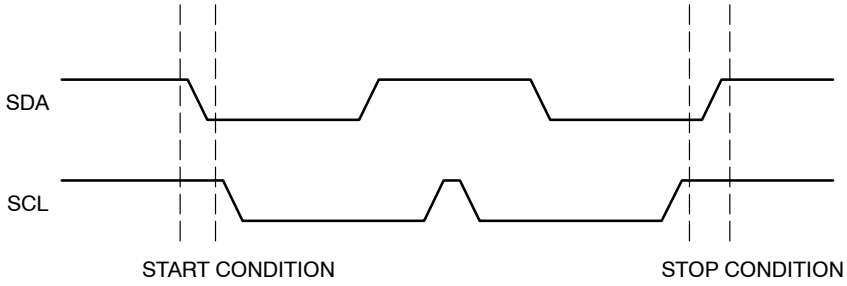


Figure 7. Start/Stop Condition

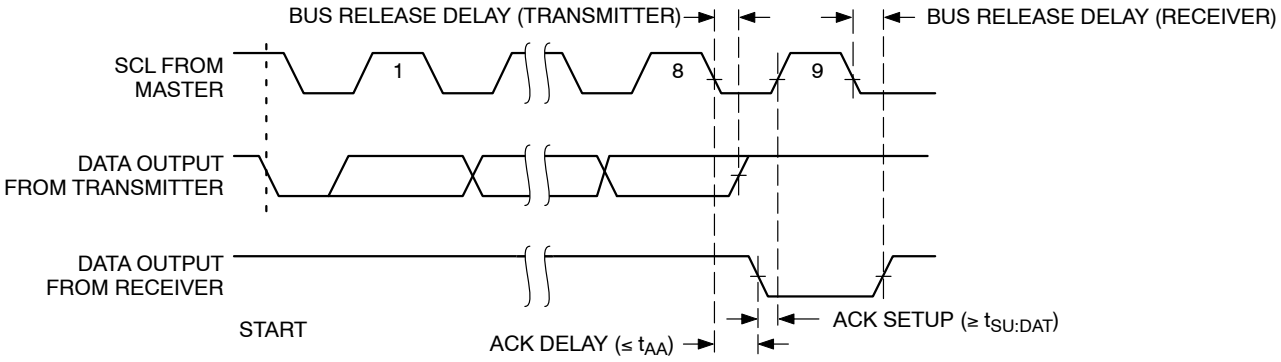


Figure 8. Acknowledge Condition

DEVICE DESCRIPTION

Slave Address Instruction Byte Description

The first byte sent to the CAT513x from the master processor is called the Slave Address Byte. The most significant seven bits of the slave address are a device type identifier. For CAT5136 and CAT5137 these bits are fixed at 0101110. For CAT5138, they are 0111110. This allows both CAT5137 and CAT5138, which are functionally identical, to reside on the same bus (refer to Table 10).

Only the device with slave address matching the input byte will be accessed by the master.

The last bit is the READ/WRITE bit and determines the function to be performed. If it is a “1” a read command is initiated and if it is a “0” a write is initiated.

After the Master sends a START condition and the slave address byte, the CAT513x monitors the bus and responds with an acknowledge when its address matches the transmitted slave address.

Table 10. BYTE 1 SLAVE ADDRESS AND INSTRUCTION BYTE

Device	Device Type Identifier							Read/$\overline{\text{Write}}$
	ID6	ID5	ID4	ID3	ID2	ID1	ID0	
CAT5136	0	1	0	1	1	1	0	R/$\overline{\text{W}}$
CAT5137	0	1	0	1	1	1	0	R/$\overline{\text{W}}$
CAT5138	0	1	1	1	1	1	0	R/$\overline{\text{W}}$
	(MSB)							(LSB)

Wiper Control Register (WCR) Description

The CAT513x contains a 7-bit volatile Wiper Control Register which is decoded to select one of the 128 switches along its resistor array. The Wiper Control Register loses its contents when the CAT513x is powered-down. At power-up, the register is loaded with the midscale value 40h. The contents of the WCR may be read or changed directly by the host using a READ/WRITE command on the I^2C bus (see Table 1 to access WCR). Since the CAT513x will only make use of the 7 LSB bits, the first data bit, or MSB, is ignored on write instructions and will always come back as a “0” on read commands.

A write operation (see Table 11) requires a Start condition, followed by a valid slave address byte, a valid address byte 00h, a data byte and a STOP condition. After each of the three bytes, the CAT513x responds with an acknowledge. After the third byte, the data is written to the Wiper Control Register, and the wiper changes position accordingly.

A read operation (see Table 12) requires a Start condition, followed by a valid slave address byte for write, a valid address byte 00h, a second START and a second slave address byte for read. After each of the three bytes, the CAT513x responds with an acknowledge and then the device transmits the data byte. The master terminates the read operation by issuing a STOP condition following the last bit of Data byte.

Table 11. WRITE OPERATION

CAT5136 and CAT5137

START	1st byte									2nd byte									3rd byte										
	SLAVE ADDRESS							Wb	ACK	ADDRESS BYTE								ACK	DATA BYTE IN								ACK	STOP
S	0	1	0	1	1	1	0	0	A	0	0	0	0	0	0	0	0	A	X	D6	D5	D4	D3	D2	D1	D0	A	P

CAT5138

START	1st byte									2nd byte									3rd byte										
	SLAVE ADDRESS							Wb	ACK	ADDRESS BYTE								ACK	DATA BYTE IN								ACK	STOP
S	0	1	1	1	1	1	0	0	A	0	0	0	0	0	0	0	0	A	X	D6	D5	D4	D3	D2	D1	D0	A	P

Table 12. READ OPERATION

CAT5136 and CAT5137

START	1st byte									2nd byte									START	3rd byte									4th byte										
	SLAVE ADDRESS							Wb	ACK	ADDRESS BYTE								ACK		SLAVE ADDRESS							R	ACK	OUTPUT DATA BYTE								NoACK	STOP
S	0	1	0	1	1	1	0	0	A	0	0	0	0	0	0	0	0	A	S	0	1	0	1	1	1	0	1	A	0	D6	D5	D4	D3	D2	D1	D0	NA	P

CAT5138

START	1st byte									2nd byte									START	3rd byte									4th byte										
	SLAVE ADDRESS							Wb	ACK	ADDRESS BYTE								ACK		SLAVE ADDRESS							R	ACK	OUTPUT DATA BYTE								NoACK	STOP
S	0	1	1	1	1	1	0	0	A	0	0	0	0	0	0	0	0	A	S	0	1	1	1	1	1	0	1	A	0	D6	D5	D4	D3	D2	D1	D0	NA	P

POTENTIOMETER OPERATION

CAT5136, CAT5137, CAT5138 are a family of a 128-position, digital controlled potentiometers. When V_{DD} is applied, the device automatically turns on at the mid-point wiper location (64).

At power-down, it is recommended to turn-off first the signals on RH, RW and RL, followed by VDD, in order to avoid unexpected transitions of the wiper and uncontrolled current overload of the potentiometer.

The end-to-end nominal resistance of the potentiometer has 128 contact points linearly distributed across the total resistor. Each of these contact points is addressed by the 7 bit wiper register which is decoded to select one of these 128 contact points.

Each contact point generates a linear resistive value between the 0 position and the 127 position. These values can be determined by dividing the end-to-end value of the potentiometer by 127. In the case of the 50 kΩ potentiometer ~390 Ω is the resistance between each wiper position. However in addition to the ~390 Ω for each resistive segment of the potentiometer, a wiper resistance offset must be considered. Table 13 shows the effect of this value and how it would appear on the wiper terminal.

Table 13. POTENTIOMETER RESISTANCE AND WIPER RESISTANCE OFFSET EFFECTS

Position	Typical RW to RL Resistance for 50 kΩ Digital Potentiometer
00	70 Ω or 0 Ω + 70 Ω
01	460 Ω or 390 Ω + 70 Ω
63	24,870 Ω or 24,800 Ω + 70 Ω
127	50,070 Ω or 50,000 Ω + 70 Ω

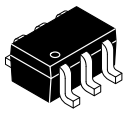
Table 14. ORDERING INFORMATION

Device Order Number	Specific Device Marking	Package Type	Temperature Range	Resistance (kΩ)	Lead Finish	Shipping†
CAT5136SDI−50GT3	P64	SC−70−6	I = Industrial (−40°C to +85°C)	50	NiPdAu	3,000 / Tape & Reel
CAT5137SDI−10GT3 (Note 14)	P72	SC−70−6	I = Industrial (−40°C to +85°C)	10	NiPdAu	3,000 / Tape & Reel
CAT5137SDI−00GT3	P75	SC−70−6	I = Industrial (−40°C to +85°C)	100	NiPdAu	3,000 / Tape & Reel
CAT5138SDI−10GT3	P82	SC−70−6	I = Industrial (−40°C to +85°C)	10	NiPdAu	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

13. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com

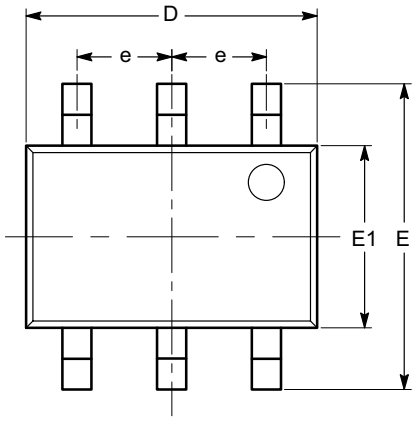
14. Contact factory for availability.



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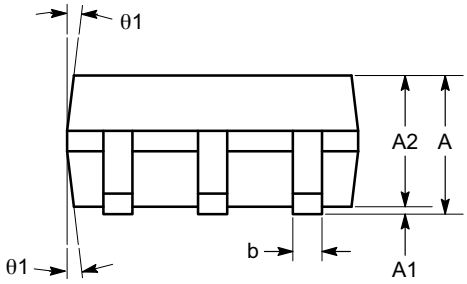
SC−88 (SC−70 6 Lead), 1.25x2
CASE 419AD
ISSUE A

DATE 07 JUL 2010

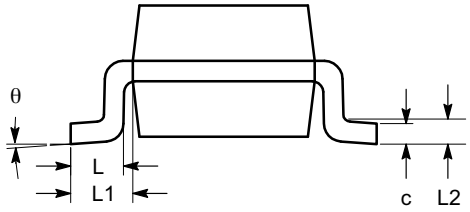


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	0.80		1.10
A1	0.00		0.10
A2	0.80		1.00
b	0.15		0.30
c	0.10		0.18
D	1.80	2.00	2.20
E	1.80	2.10	2.40
E1	1.15	1.25	1.35
e		0.65 BSC	
L	0.26	0.36	0.46
L1		0.42 REF	
L2		0.15 BSC	
θ	0°		8°
θ1	4°		10°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-203.

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DESCRIPTION:	**SC−88 (SC−70 6 LEAD), 1.25X2**		**PAGE 1 OF 1**

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