CS8101

Micropower 5.0 V, 100 mA Low Dropout Linear Regulator with $\overline{\text{RESET}}$ and $\overline{\text{ENABLE}}$

The CS8101 is a precision 5.0 V micropower voltage regulator with very low quiescent current (70 μA typ at 100 μA load). The 5.0 V output is accurate within ±2.0% and supplies 100 mA of load current with a typical dropout voltage of only 400 mV. Microprocessor control logic includes an $\overline{\text{ENABLE}}$ input and an active $\overline{\text{RESET}}$. This combination of low quiescent current, outstanding regulator performance and control logic makes the CS8101 ideal for any battery operated, microprocessor controlled equipment.

The active $\overline{\text{RESET}}$ circuit includes hysteresis, and operates correctly at an output voltage as low as 1.0 V. The $\overline{\text{RESET}}$ function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits by more than 200 mV typ. The logic level compatible $\overline{\text{ENABLE}}$ input allows the user to put the regulator into a shutdown mode where it draws only 20 μA typical of quiescent current.

The regulator is protected against reverse battery, short circuit, over voltage, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

The CS8101 is functionally equivalent to the National Semiconductor LP2951 series low current regulators.

Features

- 5.0 V ±2.0% Output
- Low 70 μA Quiescent Current
- Active $\overline{\text{RESET}}$
- $\overline{\text{ENABLE}}$ Input for ON/OFF and Active/Sleep Mode Control
- 100 mA Output Current Capability
- Fault Protection
  - +60 V Peak Transient Voltage
  - −15 V Reverse Voltage Short Circuit Thermal Overload
- Low Reverse Current (Output to Input)
- Internally Fused Leads Available in SO−20 WB Package
- These are Pb−Free Devices

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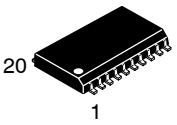
http://onsemi.com



SO−20 WB
DWF SUFFIX
CASE 751D



SOIC−8
D SUFFIX
CASE 751

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 9 of this data sheet.

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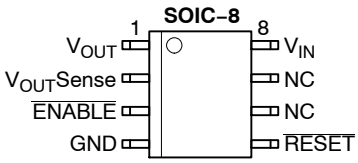
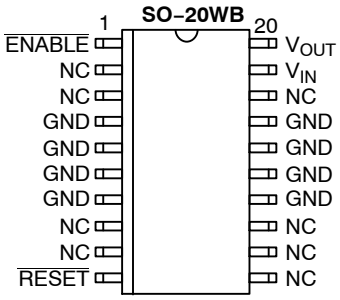
PIN CONNECTIONS





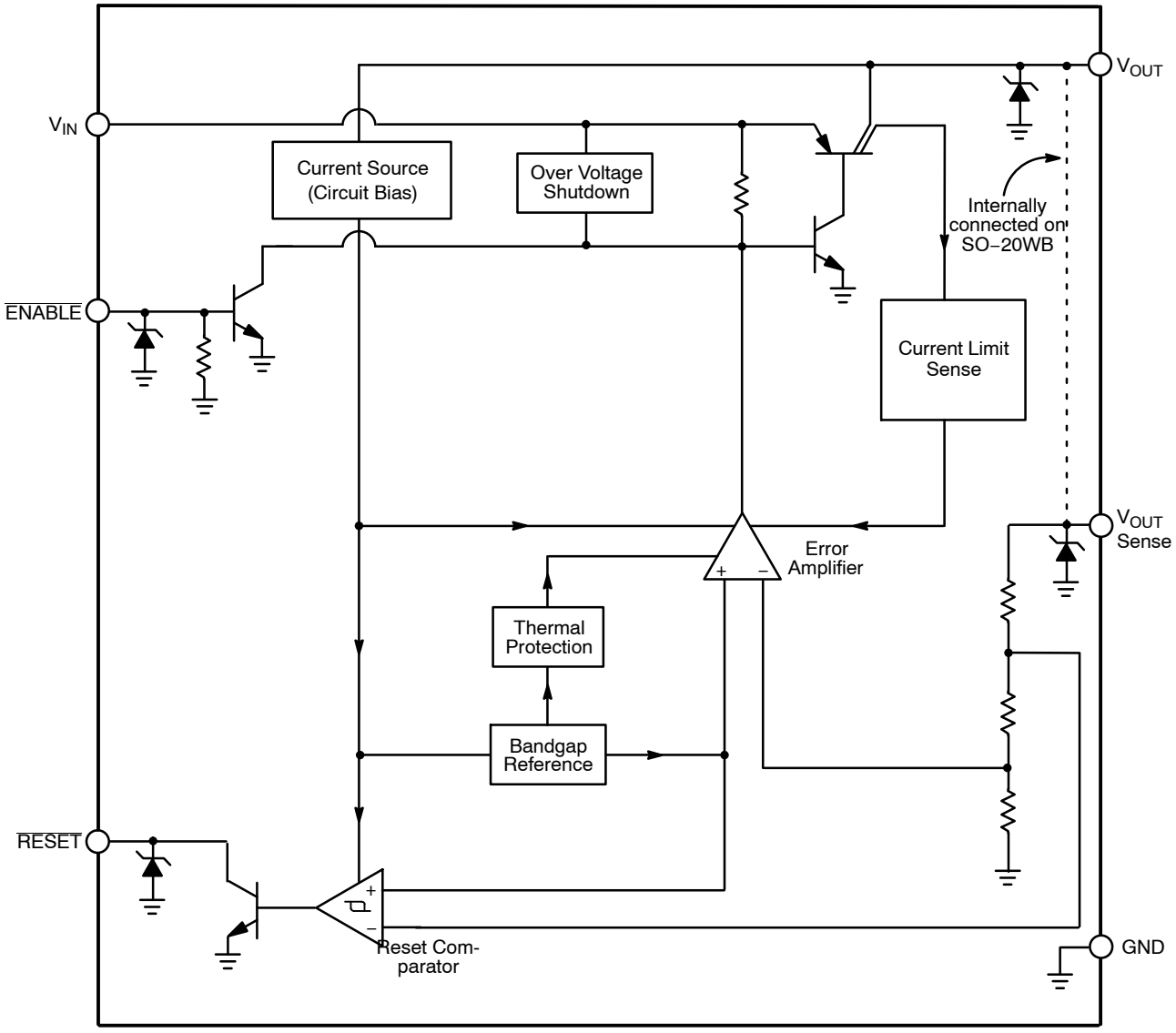


Figure 1. Block Diagram

MAXIMUM RATINGS*

Rating		Value	Unit
Power Dissipation		Internally Limited	–
Peak Transient Voltage (46 V Load Dump @ V_{IN} = 14 V)		–15, 60	V
Operating DC Voltage		30	V
$\overline{\text{ENABLE}}$ (Up to V_{IN} with external resistor)		10	V
Output Current		Internally Limited	–
ESD Susceptibility (Human Body Model)		2.0	kV
ESD Susceptibility (Machine Model)		200	V
Operating Temperature		–40 to +125	°C
Junction Temperature Range		–40 to +150	°C
Storage Temperature Range		–55 to +150	°C
Lead Temperature Soldering:	Wave Solder (through hole styles only) (Note 1) Reflow (SMD styles only) (Notes 2 & 3)	260 peak 240 peak	°C °C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. 10 second maximum.
2. 60 second maximum above 183°C.
3. –5°C / +0°C allowable conditions.

*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (6.0 V ≤ V_{IN} ≤ 26 V; I_{OUT} = 1.0 mA; –40 ≤ T_A ≤ 125, –40°C ≤ T_J ≤ 150°C, unless otherwise noted.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Stage					
Output Voltage, V_{OUT}	9.0 V < V_{IN} < 16 V, 100 μA ≤ I_{OUT} ≤ 100 mA 6.0 V < V_{IN} < 26 V, 100 μA ≤ I_{OUT} ≤ 100 mA	4.90 4.85	5.00 5.00	5.10 5.15	V V
Dropout Voltage (V_{IN} – V_{OUT})	I_{OUT} = 100 mA I_{OUT} = 100 μA	– –	400 100	600 150	mV mV
Load Regulation	V_{IN} = 14 V, 100 μA ≤ I_{OUT} ≤ 100 mA	–	5.0	50	mV
Line Regulation	6.0 < V < 26 V, I_{OUT} = 1.0 mA	–	5.0	50	mV
Quiescent Current, (I_Q) Active Mode	I_{OUT} = 100 μA, V_{IN} = 6.0 V I_{OUT} = 50 mA I_{OUT} = 100 mA	– – –	70 4.0 12	140 6.0 20	μA mA mA
Quiescent Current, (I_Q) Sleep Mode	V_{OUT} = OFF, V_{IN} = 6.0 V, $V_{\overline{\text{ENABLE}}}$ = 2.0 V	–	20	50	μA
Ripple Rejection	7.0 ≤ V_{IN} ≤ 17 V, I_{OUT} = 100 mA, f = 120 Hz	60	75	–	dB
Current Limit	–	105	200	–	mA
Short Circuit Output Current	V_{OUT} = 0 V	25	125	–	mA
Thermal Shutdown	–	150	180	–	°C
Overvoltage Shutdown	V_{OUT} ≤ 1.0 V	30	34	38	V
Reverse Current	V_{OUT} = 5.0 V, V_{IN} = 0 V	–	100	200	μA

ELECTRICAL CHARACTERISTICS (continued) ($6.0\ V \le V_{IN} \le 26\ V$; $I_{OUT} = 1.0\ mA$; $-40 \le T_A \le 125$, $-40°C \le T_J \le 150°C$, unless otherwise noted.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
ENABLE Input ($\overline{ENABLE}$)					
Threshold HIGH LOW	 (V_{OUT} OFF) (V_{OUT} ON)	 – 0.6	 1.4 1.4	 2.0 –	 V V
Input Current	$V_{\overline{ENABLE}} = 2.4\ V$	–	30	100	μA
Reset Functions ($\overline{RESET}$)					
$\overline{RESET}$ Threshold HIGH (V_{RH}) LOW (V_{RL})	 V_{OUT} Increasing V_{OUT} Decreasing	 4.525 4.500	 4.75 4.70	 $V_{OUT} - 0.05$ $V_{OUT} - 0.075$	 V V
$\overline{RESET}$ Hysteresis	(HIGH – LOW)	25	50	100	mV
Reset Output Leakage $\overline{RESET}$ = HIGH	$V_{OUT} \ge V_{RH}$	–	–	25	μA
Output Voltage Low (V_{RLO}) Low (VR_{PEAK})	 $1.0\ V \le V_{OUT} \le V_{RL}$, $R_{\overline{RESET}} = 10\ k$ V_{OUT}, Power up, Power down, $R_{\overline{RESET}} = 10\ k$	 – –	 0.1 0.6	 0.4 1.0	 V V

PACKAGE LEAD DESCRIPTION

PACKAGE LEAD #			
SO−20 WB	**SOIC−8**	**LEAD SYMBOL**	**FUNCTION**
20	1	V_{OUT}	5.0 V, ±2.0%, 100 mA output.
–	2	V_{OUT}SENSE	Kelvin connection which allows remote sensing of output voltage for improved regulation. If remote sensing is not required, connect to V_{OUT}.
1	3	$\overline{ENABLE}$	Logic level switches output off when toggled HIGH.
4, 5, 6, 7 14, 15, 16, 17	4	GND	Ground. All GND leads must be connected to Ground.
10	5	$\overline{RESET}$	Active reset (accurate to $V_{OUT} \ge 1.0\ V$)
2, 3, 8, 9, 11, 12, 13, 18	6,7	NC	No Connection. True no−connect (i.e. is floating)
19	8	V_{IN}	Input voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

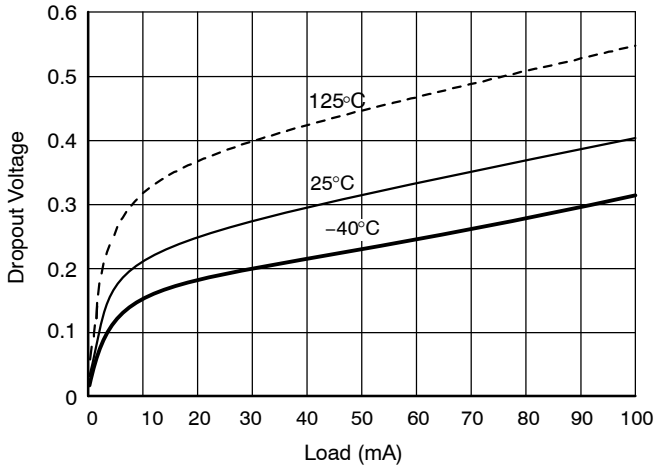


Figure 2. CS8101 Dropout Voltage vs. Load Over Temperature

CIRCUIT DESCRIPTION

VOLTAGE REFERENCE AND OUTPUT CIRCUITRY

Output Stage Protection

The output stage is protected against overvoltage, short circuit and thermal runaway conditions (Figure 3).

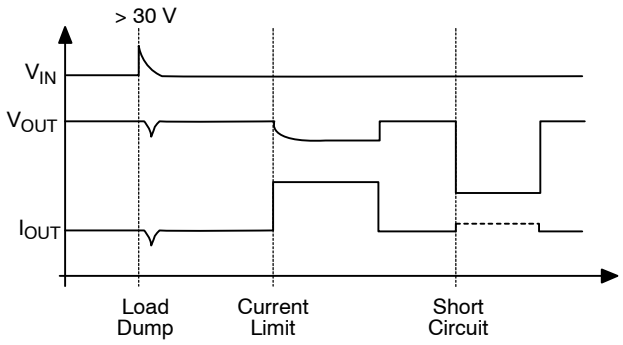


Figure 3. Typical Circuit Waveforms for Output Stage Protection

If the input voltage rises above 30 V (e.g. load dump), the output shuts down. This response protects the internal circuitry and enables the IC to survive unexpected voltage transients.

Should the junction temperature of the power device exceed 180°C (typ) the load current capability is reduced thereby preventing thermal overload. This thermal management function is an effective means to prevent die overheating since the load current is the principle heat source in the IC.

REGULATOR CONTROL FUNCTIONS

The CS8101 contains two microprocessor compatible control functions: $\overline{\text{ENABLE}}$ and $\overline{\text{RESET}}$ (Figure 4).

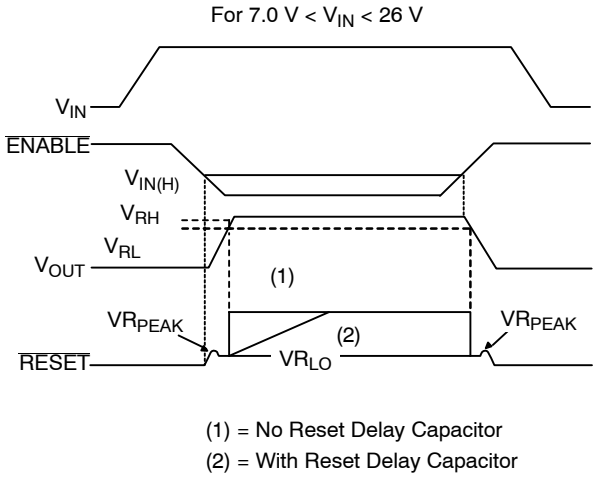


Figure 4. Circuit Waveform

$\overline{\text{ENABLE}}$ Function

The $\overline{\text{ENABLE}}$ function switches the output transistor ON and OFF. When the voltage on the $\overline{\text{ENABLE}}$ lead exceeds 1.4 V typ, the output pass transistor turns off, leaving a high impedance facing the load. The IC will remain in Sleep mode, drawing only 50 μA, until the voltage on this input drops below the $\overline{\text{ENABLE}}$ threshold.

$\overline{\text{RESET}}$ Function

A $\overline{\text{RESET}}$ signal (low voltage) is generated as the IC powers up until V_{OUT} is within 250 mV of the regulated output voltage, or when V_{OUT} drops out of regulation, and is lower than 300 mV below the regulated output voltage. A hysteresis of 50 mV is included in the function to minimize oscillations.

The $\overline{\text{RESET}}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the $\overline{\text{RESET}}$ signal is valid for V_{OUT} as low as 1.0 V.

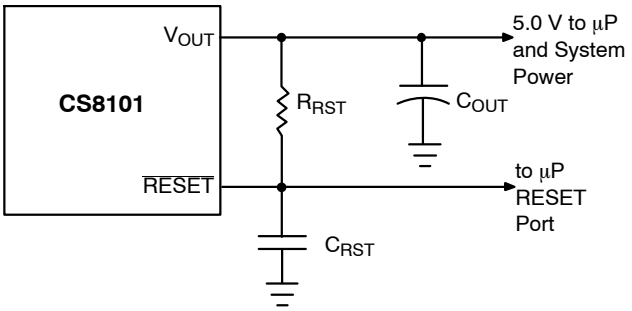


Figure 5. RC Network for $\overline{\text{RESET}}$ Delay

An external RC network on the lead (Figure 5) provides a sufficiently long delay for most microprocessor based applications. RC values can be chosen using the following formula:

$$R_{TOT}C_{RST} = \left[\frac{-t_{Delay}}{\ln\left(\frac{V_T - V_{OUT}}{V_{RST} - V_{OUT}}\right)}\right]$$

where:

R_{RST} = $\overline{\text{RESET}}$ Delay resistor
R_{IN} = μP port impedance
R_{TOT} = R_{RST} in parallel with R_{IN}
C_{RST} = $\overline{\text{RESET}}$ Delay capacitor
t_{Delay} = desired delay time
V_{RST} = V_{SAT} of $\overline{\text{RESET}}$ lead (0.7 V @ turn − ON)
V_T = $\overline{\text{RESET}}$ threshold.

The circuit depicted in Figure 6 lets the microprocessor control its power source, the CS8101 regulator. An I/O port on the μP and the SWITCH port are used to drive the base of Q1. When Q1 is driven into saturation, the voltage on the $\overline{\text{ENABLE}}$ lead falls below its lower threshold. The regulator's output is enabled. When the drive current is removed, the voltage on the $\overline{\text{ENABLE}}$ lead rises, the output is switched off and the IC moves into Sleep mode where it draws 50 μA (max).

By coupling these two controls with the $\overline{\text{ENABLE}}$ lead, the system has added flexibility. Once the system is running, the state of the SWITCH is irrelevant as long as the I/O port continues to drive Q1. The microprocessor can turn off its own power by withdrawing drive current, once the SWITCH is open. This software control at the I/O port allows the microprocessor to finish key housekeeping functions before power is removed.

The logic options are summarized in Table 1.

Table 1. Logic Control of CS8101 Output

Microprocessor I/O Drive	Switch	$\overline{\text{ENABLE}}$	Output
ON	Closed	LOW	ON
	Open	LOW	ON
OFF	Closed	LOW	ON
	Open	HIGH	OFF

The I/O port of the microprocessor typically provides 50 μA to Q1. In automotive applications the SWITCH is connected to the ignition switch.

APPLICATION NOTES

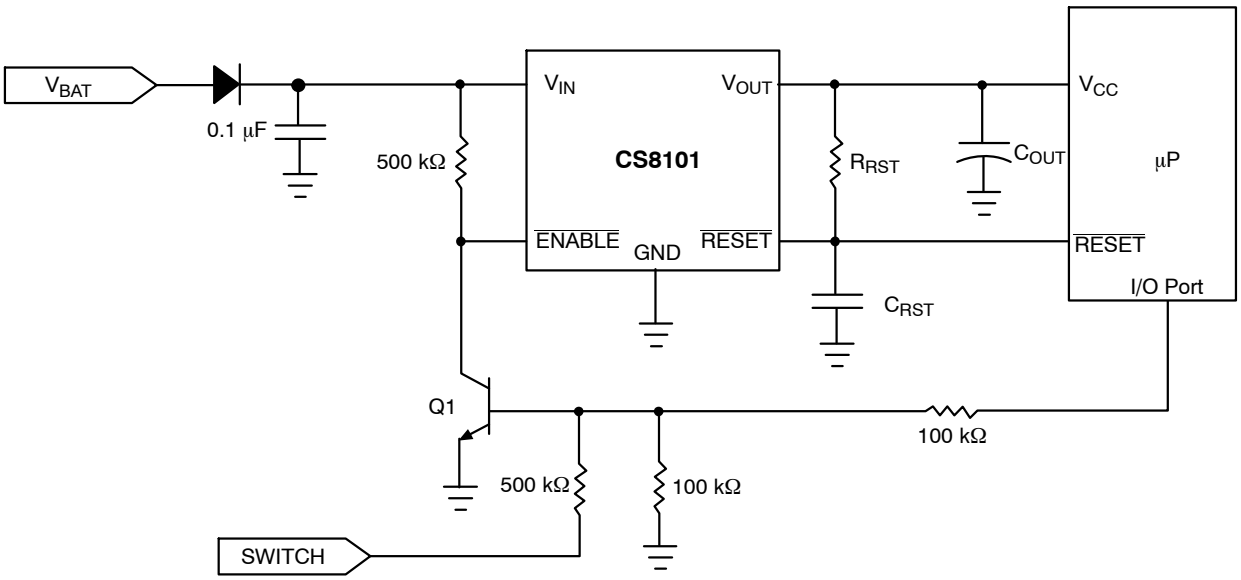


Figure 6. Microprocessor Control of CS8101 Using External Switching Transistor Q1

The $\overline{\text{ENABLE}}$ pin of the CS8101 can be tied to the battery voltage provided a series resistor is used as shown in Figure 7. The maximum allowed voltage on the $\overline{\text{ENABLE}}$ pin without the resistor is 10 V. Direct voltages greater than 10 V applied to the pin without the series resistor may damage the device. The system designer should note the turn−on threshold (typ 1.4 V) is on the $\overline{\text{ENABLE}}$ pin. The threshold will be higher on the other side of $R_{\overline{\text{ENABLE}}}$.

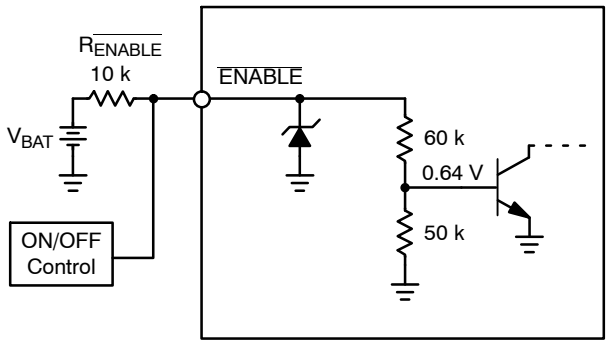
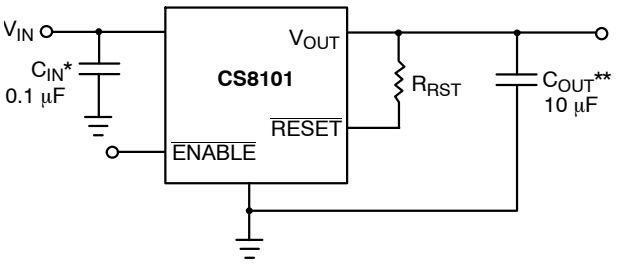


Figure 7. Using the $\overline{\text{ENABLE}}$ pin with V_{BAT}

STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start−up delay, load transient response and loop stability.



*C_{IN} required if regulator is located far from the power supply filter.

*C_{OUT} required for stability. Capacitor must operate at minimum temperature expected.

Figure 8. Test and Application Circuit Showing Output Compensation

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_{OUT} shown in Figure 8 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_{OUT} for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ± 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 9) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

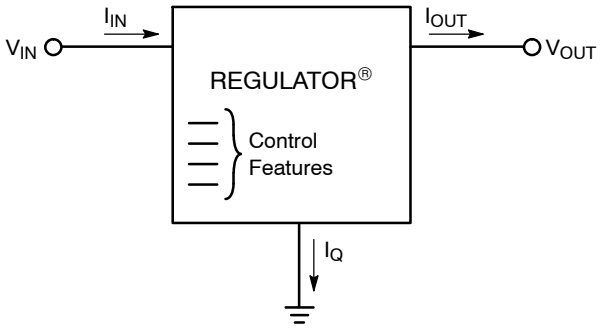


Figure 9. Single Output Regulator With Key Performance Parameters Labeled

HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$.

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

DEVICE ORDERING INFORMATION*

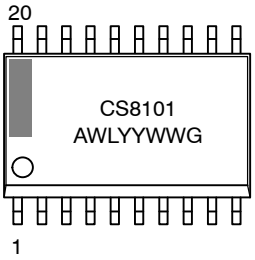
Device	Package	Shipping†
CS8101YD8G	SOIC−8 (Pb−Free)	98 Units/Rail
CS8101YDR8G	SOIC−8 (Pb−Free)	2500/Tape & Reel
CS8101YDWF20G	SO−20 WB (Pb−Free)	38 Units/Tube
CS8101YDWFR20G	SO−20 WB (Pb−Free)	1000/Tape & Reel

*Contact your local sales representative for D^2PAK package option.

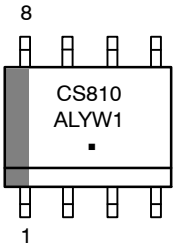
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MARKING DIAGRAMS

SO−20 WB
DWF SUFFIX
CASE 751D



SOIC−8
D SUFFIX
CASE 751



CS8101 = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package
▪ = Pb−Free Package

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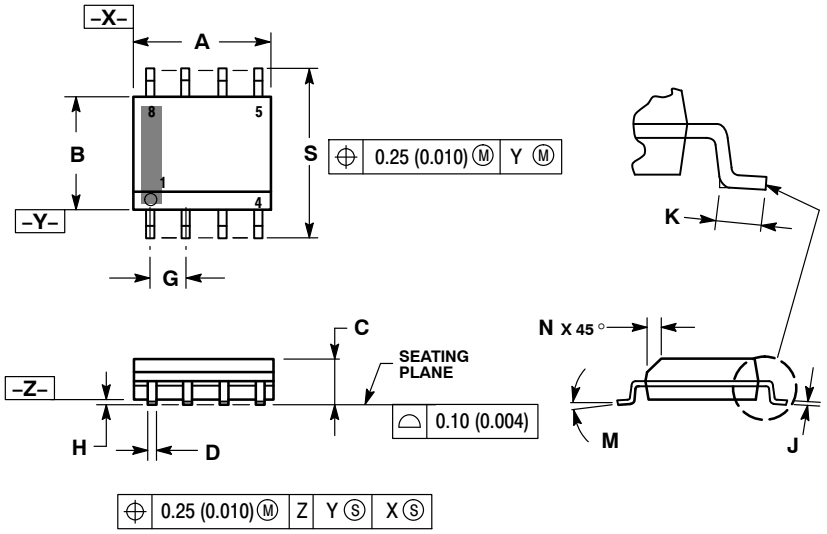
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

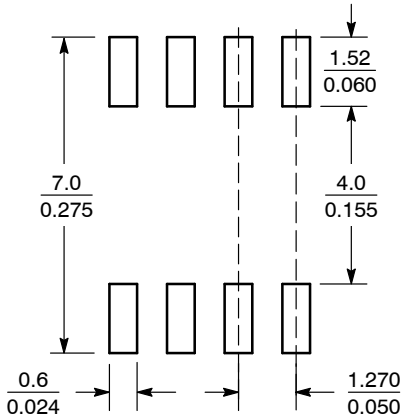
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

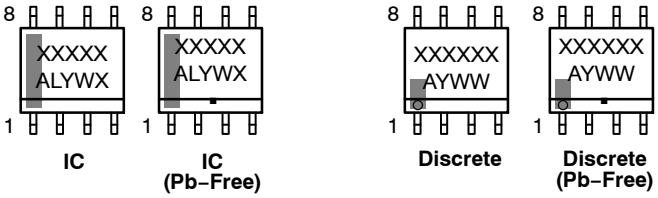
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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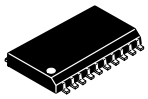
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



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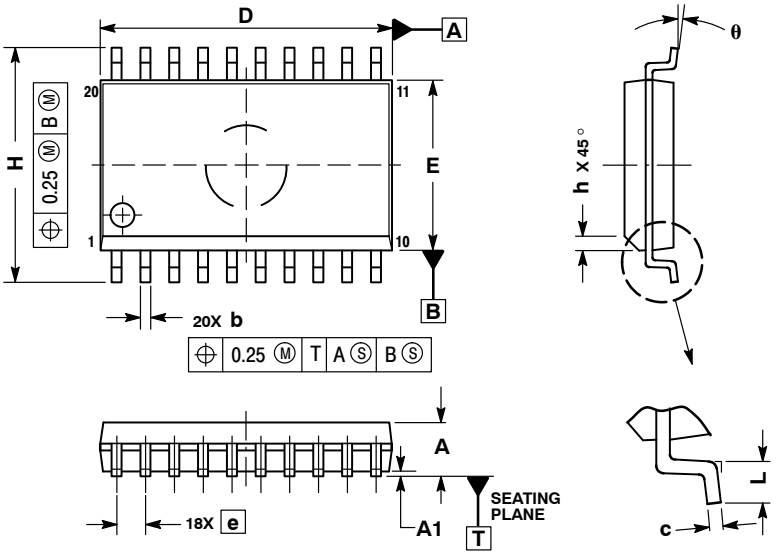
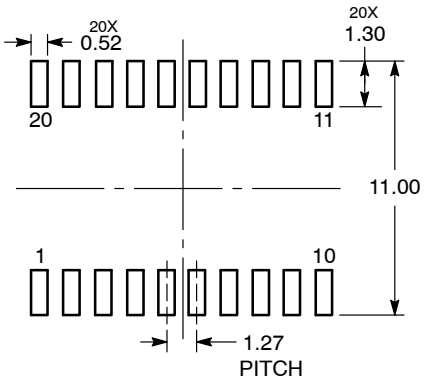


NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

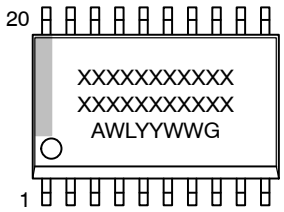
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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