CS8129

5.0 V, 750 mA Low Dropout Linear Regulator with Lower $\overline{\text{RESET}}$ Threshold

The CS8129 is a precision 5.0 V linear regulator capable of sourcing 750 mA. The $\overline{\text{RESET}}$ threshold voltage has been lowered to 4.2 V so that the regulator can be used with 4.0 V microprocessors. The lower $\overline{\text{RESET}}$ threshold also permits operation under low battery conditions (5.5 V plus a diode). The $\overline{\text{RESET}}$'s delay time is externally programmed using a discrete RC network. During powerup, or when the output goes out of regulation, $\overline{\text{RESET}}$ remains in the low state for the duration of the delay. This function is independent of the input voltage and will function correctly as long as the output voltage remains at or above 1.0 V. Hysteresis is included in the Delay and the $\overline{\text{RESET}}$ comparators to improve noise immunity. A latching discharge circuit is used to discharge the delay capacitor when it is triggered by a brief fault condition.

The regulator is protected against a variety of fault conditions: i.e. reverse battery, overvoltage, short circuit and thermal runaway conditions. The regulator is protected against voltage transients ranging from −50 V to +40 V. Short circuit current is limited to 1.2 A (typ).

The CS8129 is packaged in a 16 lead surface mount package.

Features

- 5.0 V ±3.0% Regulated Output
- Low Dropout Voltage (0.6 V @ 0.5 A)
- 750 mA Output Current Capability
- Reduced $\overline{\text{RESET}}$ Threshold for Use with 4.0 V Microprocessors
- Externally Programmed $\overline{\text{RESET}}$ Delay
- Fault Protection
  - Reverse Battery
  - 60 V, −50 V Peak Transient Voltage
  - Short Circuit
  - Thermal Shutdown
- These are Pb−Free Devices

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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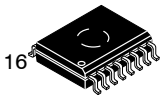
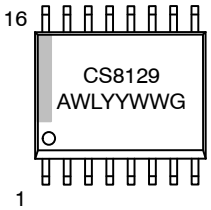
http://onsemi.com



SO−16WB
DW SUFFIX
CASE 751G

MARKING DIAGRAM



A	= Assembly Location
WL	= Wafer Lot
YY, Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

Device	Package	Shipping†
CS8129YDW16G	SO16WB (Pb−Free)	47 Units / Rail
CS8129YDWR16G	SO16WB (Pb−Free)	1000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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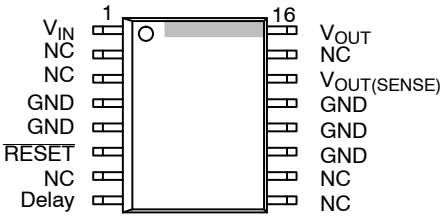
PIN CONNECTIONS



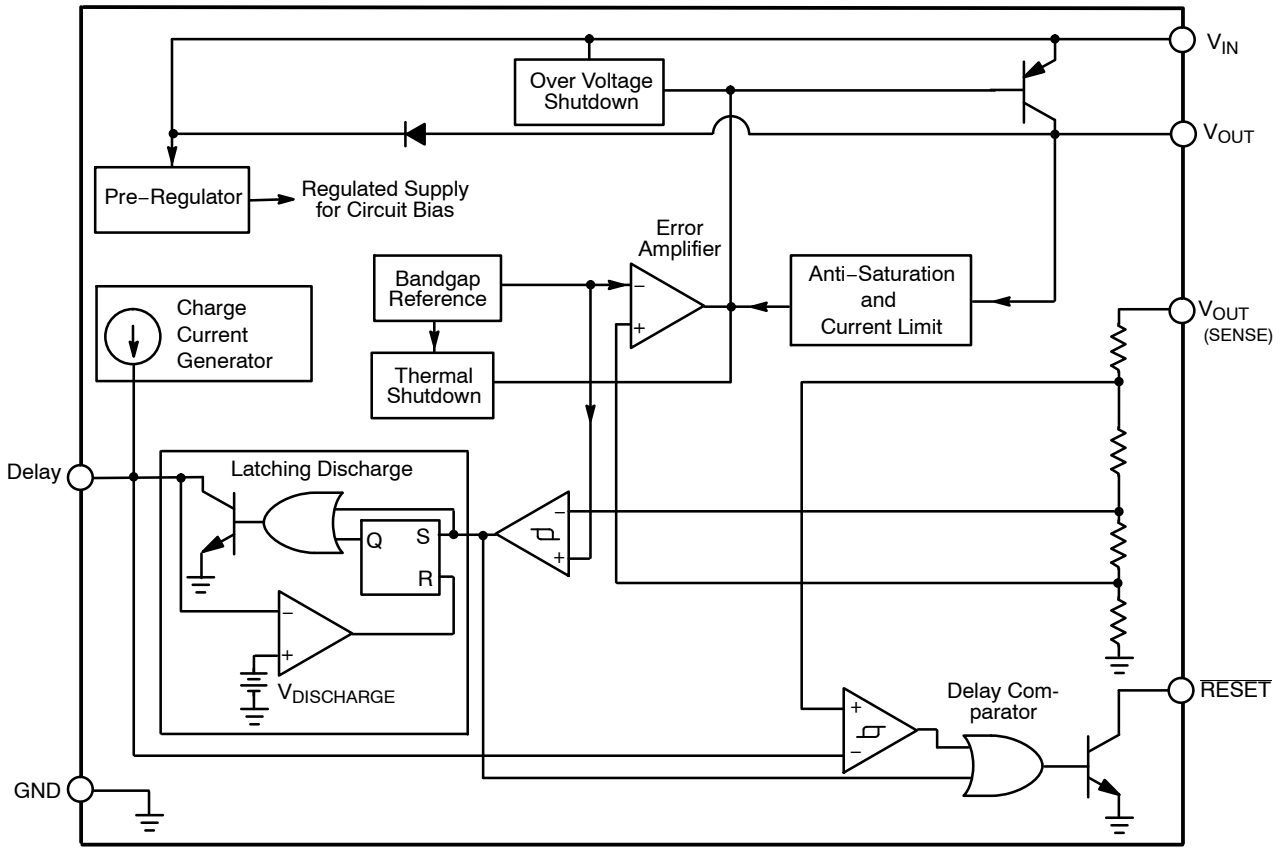


Figure 1. Block Diagram

ABSOLUTE MAXIMUM RATINGS

Rating	Value	Unit
Input Operating Range	−0.5 to 26	V
Power Dissipation	Internally Limited	−
Peak Transient Voltage (46 V Load Dump @ 14 V V_{IN})	−50, 60	V
Output Current	Internally Limited	−
Electrostatic Discharge (Human Body Model)	4.0	kV
Junction Temperature	−55 to +150	°C
Storage Temperature Range	−55 to +150	°C
Lead Temperature Soldering: Wave Solder (through hole styles only) (Note 1) Reflow (SMD styles only) (Note 2)	260 peak 230 peak	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. 10 second maximum.
2. 60 seconds max above 183°C.

ELECTRICAL CHARACTERISTICS (–40°C ≤ T_A ≤ 125°C, –40 ≤ T_J ≤ 150°C, 6.0 ≤ V_{IN} ≤ 26 V, 5.0 mA ≤ I_{OUT} ≤ 500 mA, $R_{\overline{RESET}}$ = 4.7 kΩ to V_{OUT} unless otherwise noted.) (Note 3)

Characteristic	Test Conditions	Min	Typ	Max	Unit
OUTPUT STAGE (V_{OUT})					
Output Voltage	–	4.85	5.0	5.15	V
Dropout Voltage	I_{OUT} = 500 mA	–	0.35	0.60	V
Supply Current	I_{OUT} = 10 mA I_{OUT} = 100 mA I_{OUT} = 500 mA	– – –	2.0 6.0 55	7.0 12 100	mA mA mA
Line Regulation	6.0 V ≤ V_{IN} ≤ 26 V, I_{OUT} = 50 mA	–	5.0	50	mV
Load Regulation	50 mA ≤ I_{OUT} ≤ 500 mA, V_{IN} = 14 V	–	10	50	mV
Ripple Rejection	f = 120 Hz, V_{IN} = 7.0 to 17 V, I_{OUT} = 250 mA	54	75	–	dB
Current Limit	–	0.75	1.20	–	A
Overvoltage Shutdown	–	32	–	40	V
Reverse Polarity Input Voltage DC	V_{OUT} ≥ –0.6 V, 10 Ω Load	–15	–30	–	V
Thermal Shutdown	Guaranteed by Design	150	180	210	°C
$\overline{RESET}$ AND DELAY FUNCTIONS					
Delay Charge Current	V_{DELAY} = 2.0 V	5.0	10	15	μA
$\overline{RESET}$ Threshold	V_{OUT} Increasing, $V_{RT(ON)}$ V_{OUT} Decreasing, $V_{RT(OFF)}$	4.05 4.00	4.35 4.20	4.50 4.45	V V
$\overline{RESET}$ Hysteresis	V_{RH} = $V_{RT(ON)}$ – $V_{RT(OFF)}$	50	150	250	mV
Delay Threshold	Charge, $V_{DC(HI)}$ Discharge, $V_{DC(LO)}$	3.25 2.85	3.50 3.10	3.75 3.35	V V
Delay Hysteresis	–	200	400	800	mV
$\overline{RESET}$ Output Voltage Low	1.0 V < V_{OUT} < $V_{RT(L)}$, 3.0 kΩ to V_{OUT}	–	0.1	0.4	V
$\overline{RESET}$ Output Leakage	V_{OUT} > $V_{RT(H)}$ Current	–	0	10	μA
Delay Capacitor Discharge Voltage	Discharge Latched “ON”, V_{OUT} > V_{RT}	–	0.2	0.5	V
Delay Time	C_{DELAY} = 0.1 μF, (Note 4)	16	32	48	ms

3. To observe safe operating junction temperatures, low duty cycle pulse testing is used in tests where applicable.
4. Assuming ideal capacitor.

$$\text{Delay Time} = \frac{C_{Delay} \times V_{Delay\ Threshold\ Charge}}{I_{Charge}} = C_{Delay} \times 3.5 \times 10^5 \text{ (typ)}$$

PACKAGE LEAD DESCRIPTION

PACKAGE LEAD #		
SO–16WB	**LEAD SYMBOL**	**FUNCTION**
1	V_{IN}	Unregulated supply voltage to IC.
16	V_{OUT}	Regulated 5.0 V output.
4, 5, 11, 12, 13	GND	Ground Connection.
8	Delay	Timing capacitor for $\overline{RESET}$ function.
6	$\overline{RESET}$	CMOS/TTL compatible output lead. $\overline{RESET}$ goes low whenever V_{OUT} drops below 6.0% of it’s regulated value.
14	$V_{OUT(SENSE)}$	Remote sensing of output voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

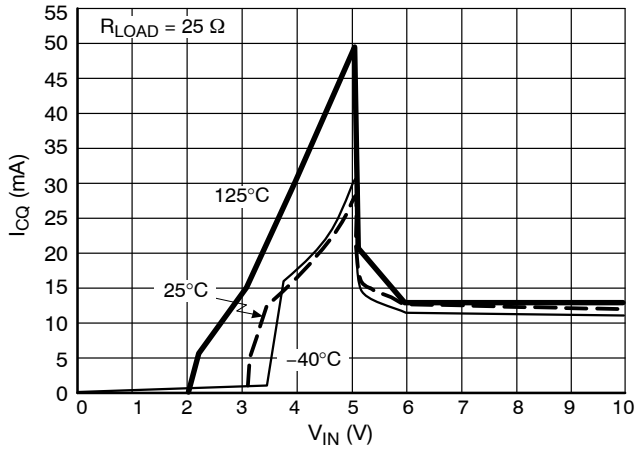


Figure 2. Quiescent Current vs. Input Voltage Over Temperature

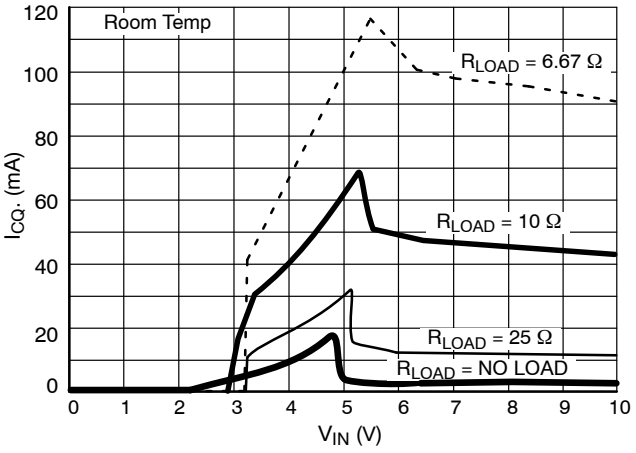


Figure 3. Quiescent Current vs. Input Voltage Over Load Resistance

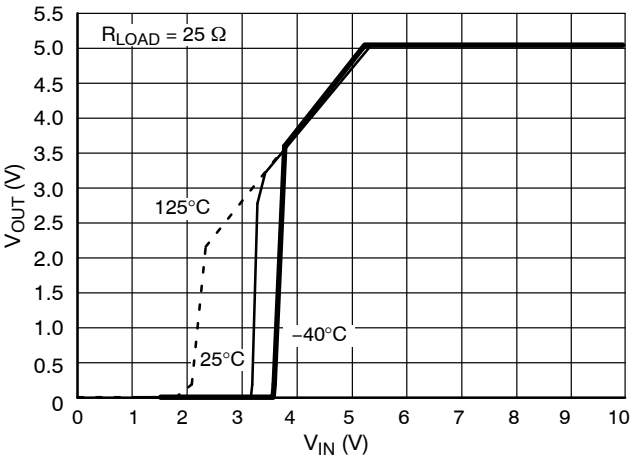


Figure 4. Output Voltage vs. Input Voltage Over Temperature

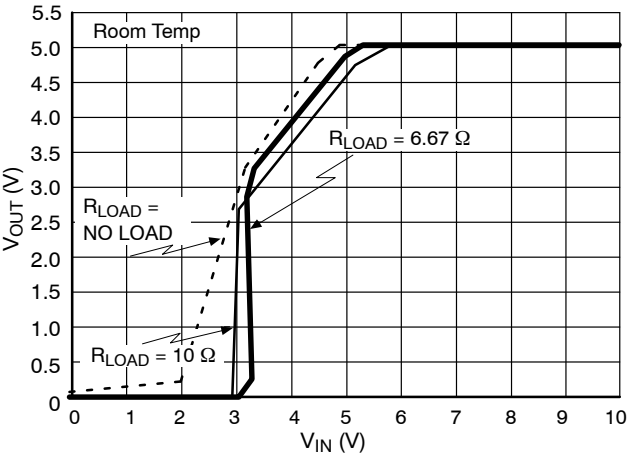


Figure 5. V_{OUT} vs. V_{IN} Over R_{LOAD}

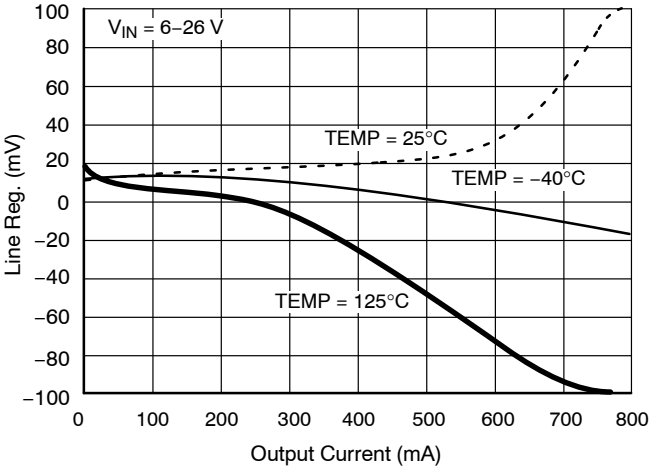


Figure 6. Line Regulation vs. Output Current

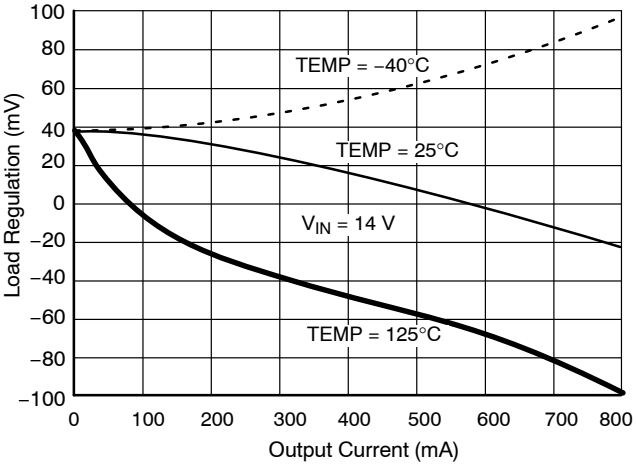


Figure 7. Load Regulation vs. Output Current

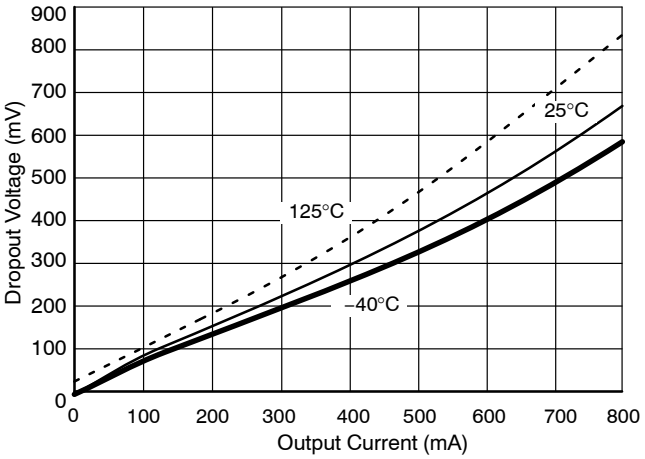


Figure 8. Dropout Voltage vs. Output Current

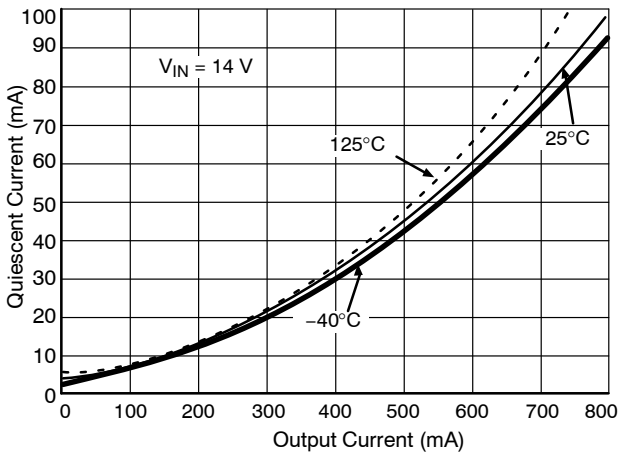


Figure 9. Quiescent Current vs. Output Current

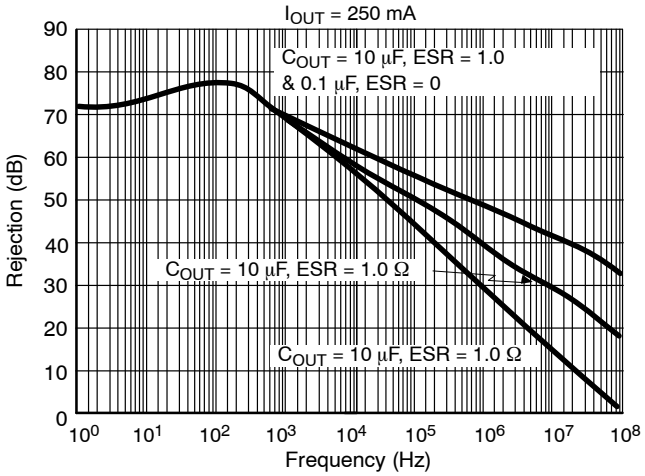


Figure 10. Ripple Rejection

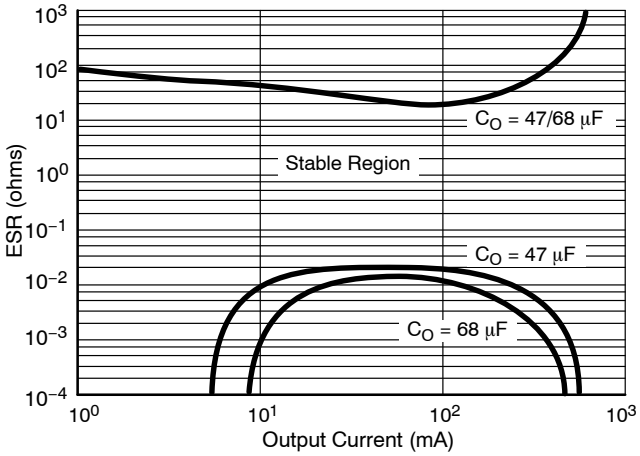


Figure 11. Output Capacitor ESR

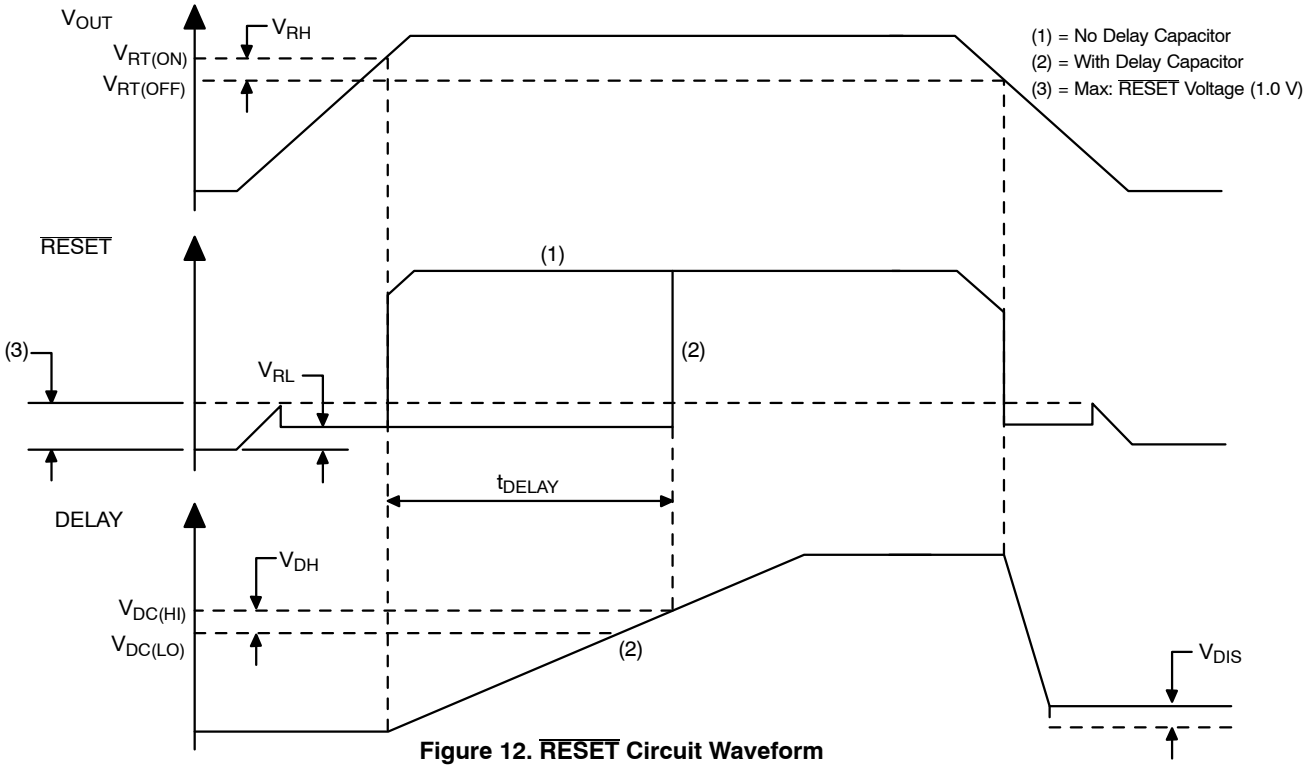


Figure 12. RESET Circuit Waveform

CIRCUIT DESCRIPTION

The CS8129 $\overline{\text{RESET}}$ function has hysteresis on both the reset and delay comparators, a latching Delay capacitor discharge circuit, and operates down to 1.0 V.

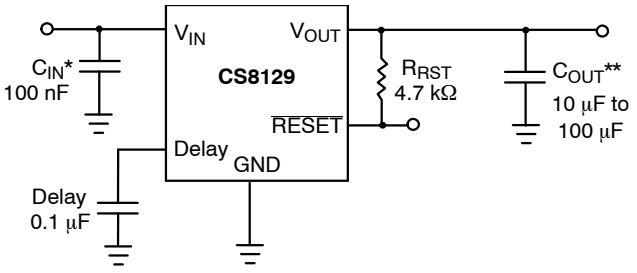
The $\overline{\text{RESET}}$ circuit output is an open collector type with ON and OFF parameters as specified. The $\overline{\text{RESET}}$ output NPN transistor is controlled by the two circuits described (see Block Diagram on page 2).

Low Voltage Inhibit Circuit

This circuit monitors output voltage, and when output voltage is below the specified minimum causes the $\overline{\text{RESET}}$ output transistor to be in the ON (saturation) state. When the output voltage is above the specified level, this circuit permits the $\overline{\text{RESET}}$ output transistor to go into the OFF state if allowed by the $\overline{\text{RESET}}$ Delay circuit.

Reset Delay Circuit

This circuit provides a programmable (by external capacitor) delay on the $\overline{\text{RESET}}$ output lead. The Delay lead provides source current to the external delay capacitor only when the "Low Voltage Inhibit" circuit indicates that output voltage is above $V_{RT(ON)}$. Otherwise, the Delay lead sinks current to ground (used to discharge the delay capacitor). The discharge current is latched ON when the output voltage is below $V_{RT(OFF)}$. The Delay capacitor is fully discharged anytime the output voltage falls out of regulation, even for a short period of time. This feature ensures that a controlled $\overline{\text{RESET}}$ pulse is generated following detection of an error condition. The circuit allows the $\overline{\text{RESET}}$ output transistor to go to the OFF (open) state only when the voltage on the Delay lead is higher than $V_{DC(HI)}$.



*C_{IN} is required if regulator is far from the power source filter.

**C_{OUT} is required for stability.

Figure 13. Test & Application Circuit

The Delay time for the $\overline{\text{RESET}}$ function is calculated from the formula:

$$\text{Delay time} = \frac{C_{Delay} \times V_{Delay\ Threshold}}{I_{Charge}}$$

$$\text{Delay time} = C_{Delay(\mu F)} \times 3.2 \times 10^5$$

If C_{Delay} = 0.1 μF, Delay time (ms) = 32 ms ±50%: i.e. 16 ms to 48 ms. The tolerance of the capacitor must be taken into account to calculate the total variation in the delay time.

APPLICATION NOTES

STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start−up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturers data sheet usually provides this information.

The value for the output capacitor C_{OUT} shown in Figure 13 should work for most applications, however it is not necessarily the optimized solution.

To determine an acceptable value for C_{OUT} for a particular application, start with a tantalum capacitor of the recommended value and work towards a less expensive alternative part.

Step 1: Place the completed circuit with a tantalum capacitor of the recommended value in an environmental chamber at the lowest specified operating temperature and monitor the outputs with an oscilloscope. A decade box connected in series with the capacitor will simulate the higher ESR of an aluminum capacitor. Leave the decade box outside the chamber, the small resistance added by the longer leads is negligible.

Step 2: With the input voltage at its maximum value, increase the load current slowly from zero to full load while observing the output for any oscillations. If no oscillations are observed, the capacitor is large enough to ensure a stable design under steady state conditions.

Step 3: Increase the ESR of the capacitor from zero using the decade box and vary the load current until oscillations appear. Record the values of load current and ESR that cause the greatest oscillation. This represents the worst case load conditions for the regulator at low temperature.

Step 4: Maintain the worst case load conditions set in step 3 and vary the input voltage until the oscillations increase. This point represents the worst case input voltage conditions.

Step 5: If the capacitor is adequate, repeat steps 3 and 4 with the next smaller valued capacitor. A smaller capacitor will usually cost less and occupy less board space. If the output oscillates within the range of expected operating conditions, repeat steps 3 and 4 with the next larger standard capacitor value.

Step 6: Test the load transient response by switching in various loads at several frequencies to simulate its real working environment. Vary the ESR to reduce ringing.

Step 7: Raise the temperature to the highest specified operating temperature. Vary the load current as instructed in step 5 to test for any oscillations.

Once the minimum capacitor value with the maximum ESR is found, a safety factor should be added to allow for the tolerance of the capacitor and any variations in regulator performance. Most good quality aluminum electrolytic capacitors have a tolerance of ± 20% so the minimum value found should be increased by at least 50% to allow for this tolerance plus the variation which will occur at low temperatures. The ESR of the capacitor should be less than 50% of the maximum allowable ESR found in step 3 above.

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 14) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

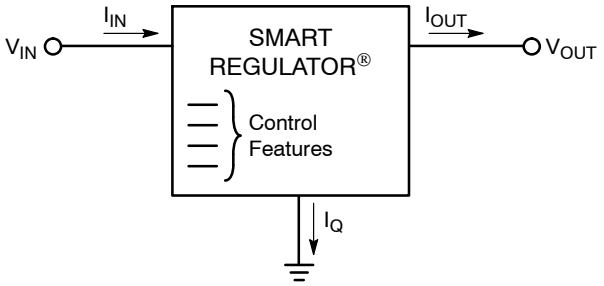


Figure 14. Single Output Regulator With Key Performance Parameters Labeled

HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$.

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

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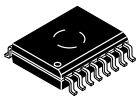
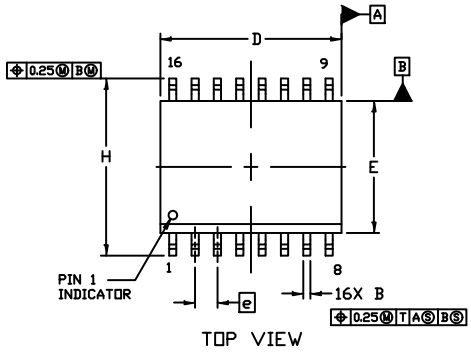
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−16 WB
CASE 751G
ISSUE E

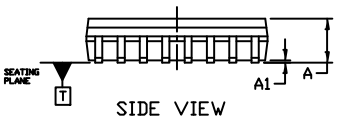
DATE 08 OCT 2021



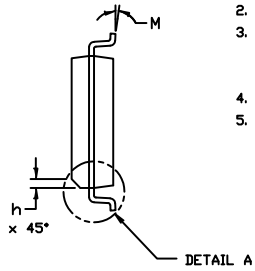
1
SCALE 1:1



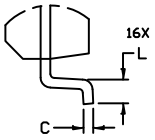
TOP VIEW



SIDE VIEW



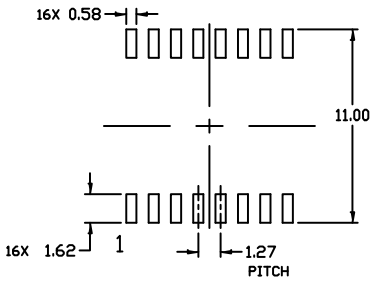
END VIEW



DETAIL A
2X SCALE

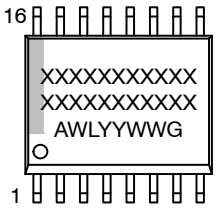
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOIC−16 WB**	**PAGE 1 OF 1**

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