CS8361

LDO Linear Voltage Regulator - Dual Micropower, Tracking, Reset, Enable

250 mA, 100 mA, 5.0 V

The CS8361 is a precision Micropower dual voltage regulator with $\overline{\text{ENABLE}}$ and $\overline{\text{RESET}}$.

The 5.0 V standby output is accurate within ±2% while supplying loads of 100 mA and has a typical dropout voltage of 400 mV. Quiescent current is low, typically 140 μA with a 300 μA load. The active $\overline{\text{RESET}}$ output monitors the 5.0 V standby output and is low during power−up and regulator dropout conditions. The $\overline{\text{RESET}}$ circuit includes hysteresis and is guaranteed to operate correctly with 1.0 V on the standby output.

The second output tracks the 5.0 V standby output through an external adjust lead, and can supply loads of 250 mA with a typical dropout voltage of 400 mV. The logic level $\overline{\text{ENABLE}}$ lead is used to control this tracking regulator output.

Both outputs are protected against overvoltage, short circuit, reverse battery and overtemperature conditions. The robustness and low quiescent current of the CS8361 makes it not only well suited for automotive microprocessor applications, but for any battery powered microprocessor applications.

Features

- 2 Regulated Outputs
  - Standby Output 5.0 V ± 2%; 100 mA
  - Tracking Output 5.0 V; 250 mA
- Low Dropout Voltage (0.4 V at Rated Current)
- RESET Option
- ENABLE Option
- Low Quiescent Current
- Protection Features
  - Independent Thermal Shutdown
  - Short Circuit
  - 60 V Load Dump
  - Reverse Battery
- Internally Fused Leads in SO−16L Package
- These are Pb−Free Devices

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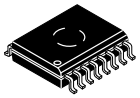
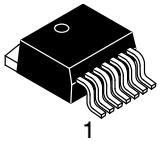
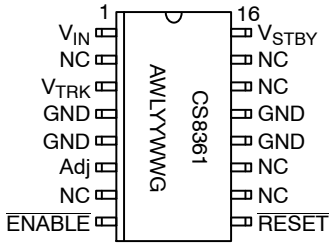


SO−16L
DW SUFFIX
CASE 751G

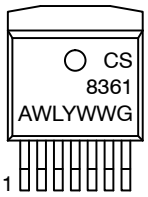


D²PAK−7
DPS SUFFIX
CASE 936AB

PIN CONNECTIONS AND MARKING DIAGRAM



SO−16L



Pin 1. V_{STBY}
2. V_{IN}
3. V_{TRK}
4. GND
5. Adj
6. $\overline{\text{ENABLE}}$
7. $\overline{\text{RESET}}$

D²PAK−7

CS8361	= Device Code
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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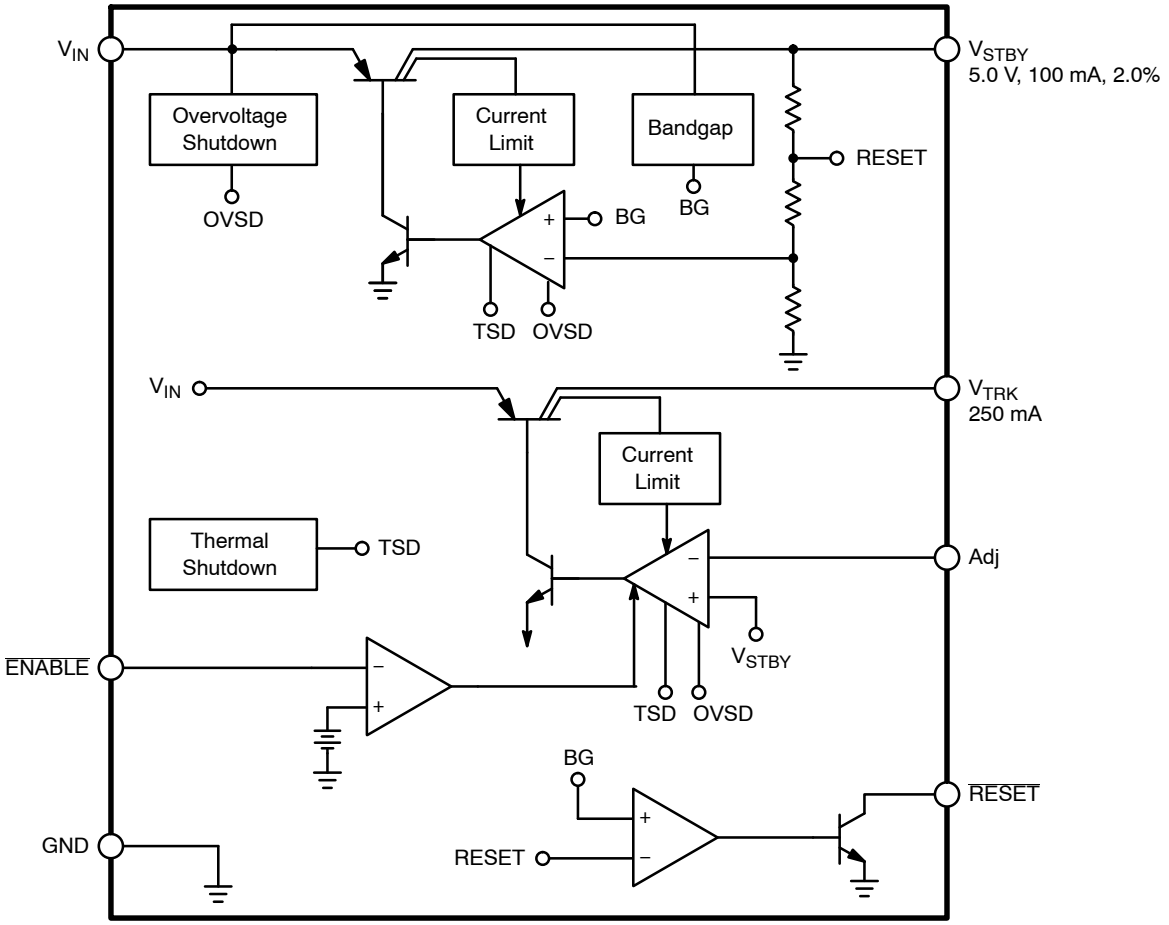


Figure 1. Block Diagram. Consult Your Local Sales Representative for Positive ENABLE Option

MAXIMUM RATINGS*

Rating		Value	Unit
Supply Voltage, V_{IN}		−16 to 26	V
Positive Transient Input Voltage, tr > 1.0 ms		60	V
Negative Transient Input Voltage, T < 100 ms, 1.0 % Duty Cycle		−50	V
Input Voltage Range ($\overline{ENABLE}$, $\overline{RESET}$)		−0.3 to 10	V
Tracking Regulator (V_{TRK}, Adj)		20	V
Standby Regulator (V_{STBY})		10	V
Junction Temperature		−40 to +150	°C
Storage Temperature Range		−55 to +150	°C
ESD Susceptibility (Human Body Model)		2.0	kV
Lead Temperature Soldering	Wave Solder (through hole styles only) Note 1 Reflow (SMD styles only) Note 2	260 peak 230 peak	°C °C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.
1. 10 seconds max.
2. 60 seconds max above 183°C
*The maximum package power dissipation must be observed.

ELECTRICAL CHARACTERISTICS (6.0 V ≤ V_{IN} ≤ 26 V, I_{OUT1} = I_{OUT2} = 100 μA, −40°C ≤ T_A ≤ +125°C, −40°C ≤ T_J ≤ +150°C; unless otherwise stated.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Tracking Output (V_{TRK})					
V_{TRK} Tracking Error (V_{STBY} − V_{TRK})	6.0 V ≤ V_{IN} ≤ 26 V, 100 μA ≤ I_{TRK} ≤ 250 mA. Note 3	−25	–	+25	mV
Adjust Pin Current, I_{Adj}	Loop in Regulation	–	1.5	5.0	μA
Line Regulation	6.0 V ≤ V_{IN} ≤ 26 V. Note 3	–	5.0	50	mV
Load Regulation	100 μA ≤ I_{TRK} ≤ 250 mA. Note 3	–	5.0	50	mV
Dropout Voltage (V_{IN} − V_{TRK})	I_{TRK} = 100 μA. I_{TRK} = 250 mA	– –	100 400	150 700	mV mV
Current Limit	V_{IN} = 12 V, V_{TRK} = 4.5 V	275	500	–	mA
Quiescent Current	V_{IN} = 12 V, I_{TRK} = 250 mA, No Load on V_{STBY}	–	25	50	mA
Reverse Current	V_{TRK} = 5.0 V, V_{IN} = 0 V	–	200	1500	μA
Ripple Rejection	f = 120 Hz, I_{TRK} = 250 mA, 7.0 V ≤ V_{IN} ≤ 17 V	60	70	–	dB
Standby Output (V_{STBY})					
Output Voltage, V_{STBY}	6.0 V ≤ V_{IN} ≤ 26 V, 100 μA ≤ I_{STBY} ≤ 100 mA.	4.9	5.0	5.1	V
Line Regulation	6.0 V ≤ V_{IN} ≤ 26 V.	–	5.0	50	mV
Load Regulation	100 μA ≤ I_{STBY} ≤ 100 mA.	–	5.0	50	mV
Dropout Voltage (V_{IN} − V_{STBY})	I_{STBY} = 100 μA. I_{STBY} = 100 mA	– –	100 400	150 600	mV mV
Current Limit	V_{IN} = 12 V, V_{STBY} = 4.5 V	125	200	–	mA
Short Circuit Current	V_{IN} = 12 V, V_{STBY} = 0 V	10	100	–	mA
Quiescent Current	V_{IN} = 12 V, I_{STBY} = 100 mA, I_{TRK} = 0 mA V_{IN} = 12 V, I_{STBY} = 300 μA, I_{TRK} = 0 mA	– –	10 140	20 200	mA μA
Reverse Current	V_{STBY} = 5.0 V, V_{IN} = 0 V	–	100	200	μA
Ripple Rejection	f = 120 Hz, I_{STBY} = 100 mA, 7.0 V ≤ V_{IN} ≤ 17 V	60	70	–	dB
$\overline{\text{RESET}}$ $\overline{\text{ENABLE}}$ Functions					
$\overline{\text{ENABLE}}$ Input Threshold	–	0.8	1.2	2.0	V
$\overline{\text{ENABLE}}$ Input Bias Current	V_{ENABLE} = 0 V to 10 V	−10	0	10	μA
$\overline{\text{RESET}}$ Threshold High (V_{RH})	V_{STBY} Increasing	4.59	4.87	V_{STBY} − 0.02	V
$\overline{\text{RESET}}$ Hysteresis	–	60	120	180	mV
$\overline{\text{RESET}}$ Threshold Low (V_{RL})	V_{STBY} Decreasing	4.53	4.75	V_{STBY} − 0.08	V
$\overline{\text{RESET}}$ Leakage	–	–	–	25	μA
Output Voltage, Low (V_{RLO})	1.0 V ≤ V_{STBY} ≤ V_{RL}, R_{RST} = 10 kΩ	–	0.1	0.4	V
Output Voltage, Low (V_{RPEAK})	V_{STBY}, Power Up, Power Down	–	0.6	1.0	V
Protection Circuitry (Both Outputs)					
Independent Thermal Shutdown	V_{STBY} V_{TRK}	150 150	180 165	– –	°C °C
Overvoltage Shutdown	–	30	34	38	V

3. V_{TRK} connected to Adj lead. V_{TRK} can be set to higher values by using an external resistor divider.

PACKAGE PIN DESCRIPTION

PACKAGE PIN #		PIN SYMBOL	FUNCTION
D^2PAK, 7 Pin	SO−16L		
1	16	V_{STBY}	Standby output voltage delivering 100 mA.
2	1	V_{IN}	Input voltage.
3	3	V_{TRK}	Tracking output voltage controlled by $\overline{\text{ENABLE}}$ delivering 250 mA.
4	4, 5, 12, 13	GND	Reference ground connection.
5	6	Adj	Resistor divider from V_{TRK} to Adj. Sets the output voltage on V_{TRK}. If tied to V_{TRK}, V_{TRK} will track V_{STBY}.
6	8	$\overline{\text{ENABLE}}$	Provides on/off control of the tracking output, active LOW.
7	9	$\overline{\text{RESET}}$	CMOS compatible output lead that goes low whenever V_{STBY} falls out of regulation.
	2, 7, 10, 11, 14, 15	NC	No connection.

CIRCUIT DESCRIPTION

$\overline{\text{ENABLE}}$ Function

The $\overline{\text{ENABLE}}$ function switches the output transistor for V_{TRK} on and off. When the $\overline{\text{ENABLE}}$ lead voltage exceeds 1.4 V (Typ), V_{TRK} turns off. This input has several hundred millivolts of hysteresis to prevent spurious output activity during power−up or power−down.

$\overline{\text{RESET}}$ Function

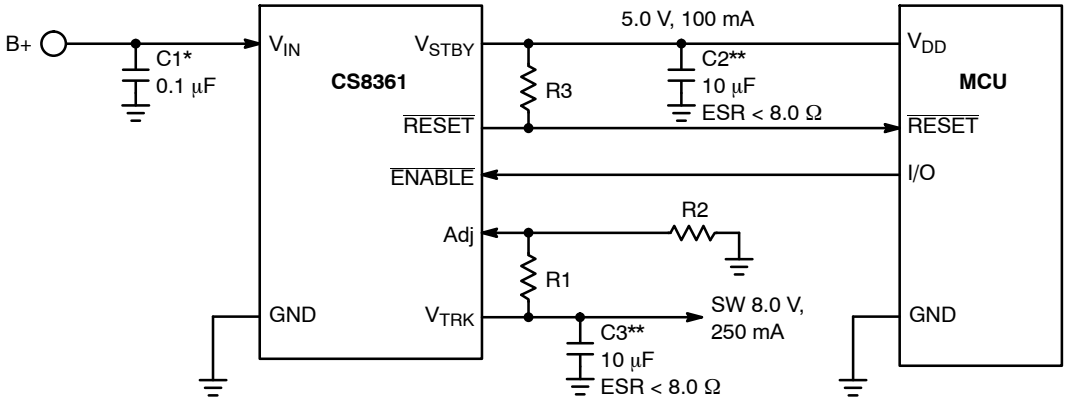
The $\overline{\text{RESET}}$ is an open collector NPN transistor, controlled by a low voltage detection circuit sensing the V_{STBY} (5.0 V) output voltage. This circuit guarantees the $\overline{\text{RESET}}$ output stays below 1.0 V (0.1 V Typ) when V_{STBY} is as low as 1.0 V to ensure reliable operation of microprocessor− based systems.

V_{TRK} Output Voltage

This output uses the same type of output device as V_{STBY}, but is rated for 250 mA. The output is configured as a tracking regulator of the standby output. By using the standby output as a voltage reference, giving the user an external programming lead (Adj lead), output voltages from 5.0 V to 20 V are easily realized. The programming is done with a simple resistor divider (Figure 2), and following the formula:

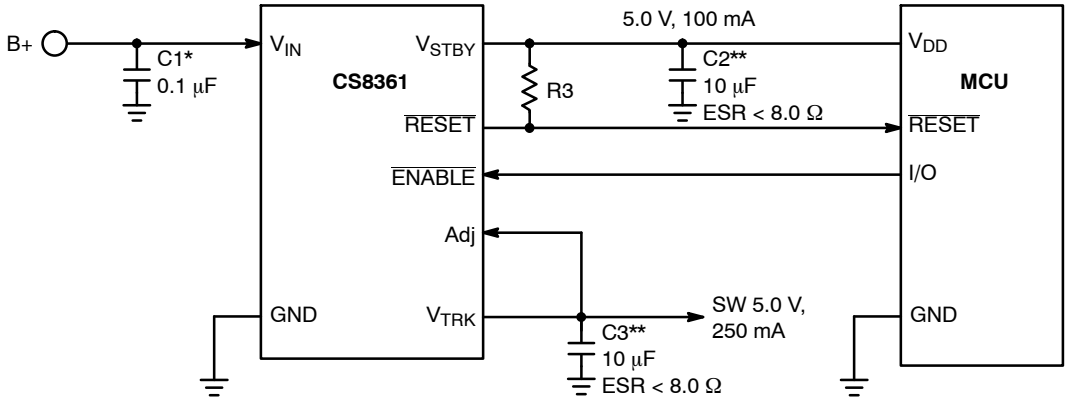
$$V_{TRK} = V_{STBY} \times (1 + R1/R2) + I_{Adj} \times R1$$

If another 5.0 V output is needed, simply connect the Adj lead to the V_{TRK} output lead.



$V_{TRK} \sim V_{STBY}(1 + R1/R2)$
For $V_{TRK} \sim 8.0$ V, $R1/R2 \sim 0.6$
*C1 is required if regulator is located far from power supply filter.
**C2 and C3 are required for stability.

Figure 2. Test and Application Circuit, 5.0 V, 8.0 V Regulator



*C1 is required if regulator is located far from power supply filter.
**C2 and C3 are required for stability.

Figure 3. Test and Application Circuit, Dual 5.0 V Regulator

APPLICATION NOTES

External Capacitors

Output capacitors for the CS8361 are required for stability. Without them, the regulator outputs will oscillate. Actual size and type may vary depending upon the application load and temperature range. Capacitor effective series resistance (ESR) is also a factor in the IC stability. Worst−case is determined at the minimum ambient temperature and maximum load expected.

Output capacitors can be increased in size to any desired value above the minimum. One possible purpose of this would be to maintain the output voltages during brief conditions of negative input transients that might be characteristic of a particular system.

Capacitors must also be rated at all ambient temperatures expected in the system. To maintain regulator stability down to −40°C, capacitors rated at that temperature must be used.

More information on capacitor selection for SMART REGULATOR®s is available in the SMART REGULATOR application note, “Compensation for Linear Regulators,” document number SR003AN/D, available through the Literature Distribution Center or via our website at http://www.onsemi.com.

Calculating Power Dissipation in a Dual Output Linear Regulator

The maximum power dissipation for a dual output regulator (Figure 4) is

$$P_{D(max)} = \{V_{IN(max)} - V_{OUT1(min)}\}I_{OUT1(max)} + \{V_{IN(max)} - V_{OUT2(min)}\}I_{OUT2(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT1(min)}$ is the minimum output voltage from V_{OUT1},

$V_{OUT2(min)}$ is the minimum output voltage from V_{OUT2},

$I_{OUT1(max)}$ is the maximum output current, for the application,

$I_{OUT2(max)}$ is the maximum output current, for the application, and

I_Q is the quiescent current the regulator consumes at both $I_{OUT1(max)}$ and $I_{OUT2(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\Theta JA} = \frac{150^\circ C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$’s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

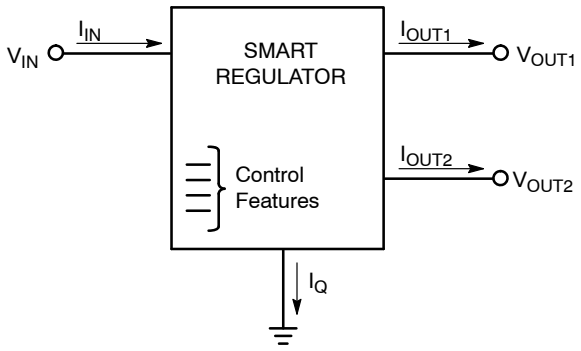


Figure 4. Dual Output Regulator With Key Performance Parameters Labeled.

Heat Sinks

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\Theta JA} = R_{\Theta JC} + R_{\Theta CS} + R_{\Theta SA} \quad (3)$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,
$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and
$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

ORDERING INFORMATION*

Device	Package	Shipping†
CS8361YDPS7G	D²PAK−7 (Pb−Free)	50 Units/Rail
CS8361YDPSR7G	D²PAK−7 (Pb−Free)	750 / Tape & Reel
CS8361YDWF16G	SO−16L (Pb−Free)	46 Units/Rail
CS8361YDWFR16G	SO−16L (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*Contact your local sales representative for other package options including PSOP−20, TO−220−7, DIP−16, and SO−20L.

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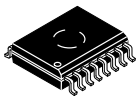
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−16 WB
CASE 751G
ISSUE E

DATE 08 OCT 2021



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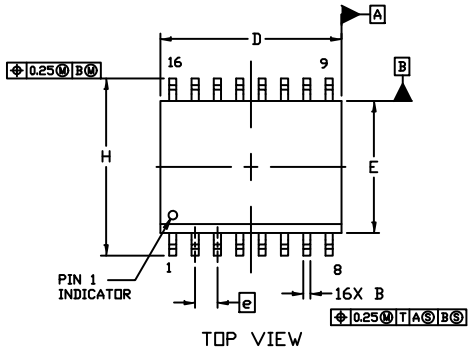
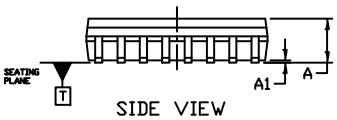
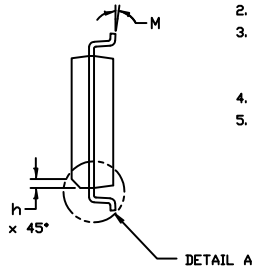


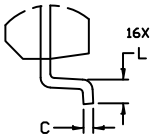
TOP VIEW



SIDE VIEW



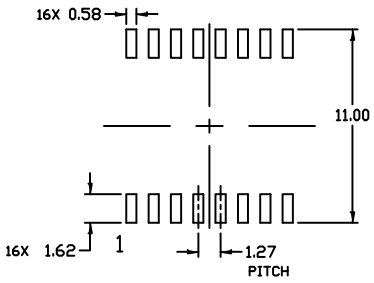
END VIEW



DETAIL A
2X SCALE

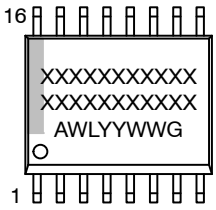
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOIC−16 WB**	**PAGE 1 OF 1**

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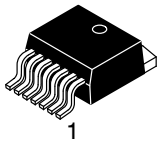
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

D²PAK–7 (SHORT LEAD)
CASE 936AB–01
ISSUE B

DATE 08 SEP 2009



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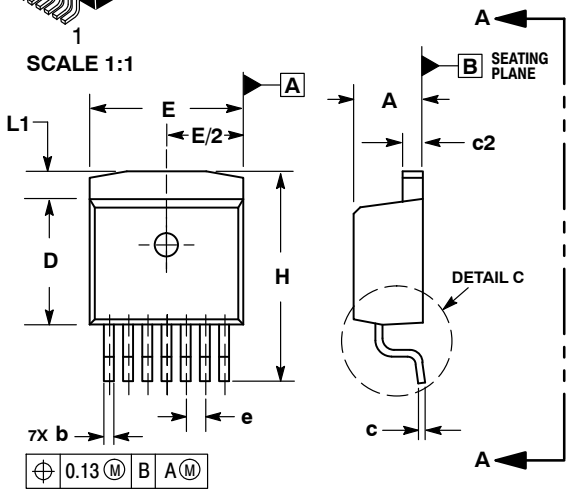
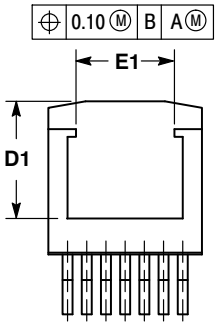
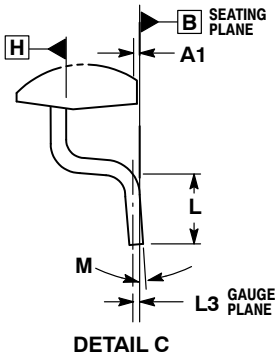




VIEW A–A

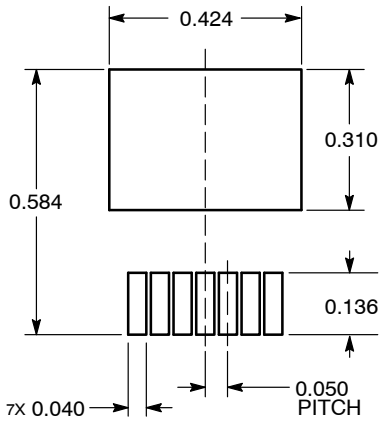


DETAIL C

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH AND GATE PROTRUSIONS. MOLD FLASH AND GATE PROTRUSIONS NOT TO EXCEED 0.005 MAXIMUM PER SIDE. THESE DIMENSIONS TO BE MEASURED AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1. DIMENSIONS D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THE THERMAL PAD.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.170	0.180	4.32	4.57
A1	0.000	0.010	0.00	0.25
b	0.026	0.036	0.66	0.91
c	0.017	0.026	0.43	0.66
c2	0.045	0.055	1.14	1.40
D	0.325	0.368	8.25	9.53
D1	0.270	---	6.86	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.050 BSC		1.27 BSC	
H	0.539	0.579	13.69	14.71
L	0.058	0.078	1.47	1.98
L1	---	0.066	---	1.68
L3	0.010 BSC		0.25 BSC	
M	0 °	8 °	0 °	8 °

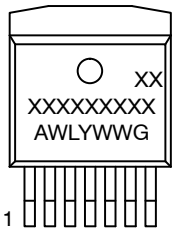
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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