MOSFET – N-Channel, UniFET™

200 V, 16 A, 125 mΩ

FDD18N20LZ

Description

UniFET MOSFET is ON Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on−state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

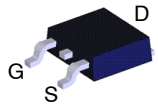
- $R_{DS(on)}$ = 125 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 8 A
- Low Gate Charge (Typ. 30 nC)
- Low C_{RSS} (Typ. 25 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- ESD Improved Capability
- These Device is Pb−Free and is RoHS Compliant

Applications

- LED TV
- Consumer Appliances
- Uninterruptible Power Supply

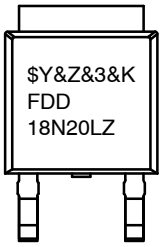
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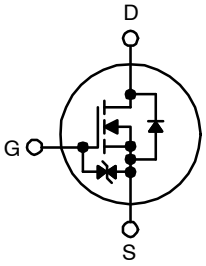


DPAK3 (TO−252 3 LD)
CASE 369AS

MARKING DIAGRAM



FDD18N20LZ	= Specific Device Code
$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= 3−Digit Date Code
&K	= 2−Digits Lot run Traceability Code



N−Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

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MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FDD18N20LZ	Unit
V_{DSS}	Drain to Source Voltage		200	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	Continuous (T_C = 25°C)	16	A
		Continuous (T_C = 100°C)	9.6	
I_{DM}	Drain Current (Note 1)	Pulsed	64	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		320	mJ
I_{AR}	Avalanche Current (Note 1)		16	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		8.9	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		10	V/ns
P_D	Power Dissipation	(T_C = 25°C)	89	W
		Derate above 25°C	0.7	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. L = 2.5 mH, I_{AS} = 16 A, V_{DD} = 50 V, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 16 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDD18N20LZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	83	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V, T_J = 25°C	200	–	–	V
ΔBV_{DSS} / Δ	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.2	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 200 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 160 V, T_C = 125°C	–	–	10	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±16 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.0	–	2.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 8 A	–	0.10	0.125	Ω
		V_{GS} = 5 V, I_D = 8 A	–	0.11	0.13	
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 2 A	–	11	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	1185	1575	pF
C_{oss}	Output Capacitance		–	190	255	pF
C_{rss}	Reverse Transfer Capacitance		–	25	40	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 200 V, I_D = 16 A, V_{GS} = 10 V (Note 4)	–	30	40	nC
Q_{gs}	Gate to Source Gate Charge		–	3.5	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	8.5	–	nC
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 100 V, I_D = 16 A, V_{GS} = 10 V, R_G = 25 Ω (Note 4)	–	15	40	ns
t_r	Turn−On Rise Time		–	20	50	ns
$t_{d(off)}$	Turn−Off Delay Time		–	135	280	ns
t_f	Turn−Off Fall Time		–	50	110	ns
DAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	16	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	64	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 4 A	–	–	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 4 A, dI_F/dt = 100 A/μs	–	105	–	ns
Q_{rr}	Reverse Recovery Charge		–	0.4	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

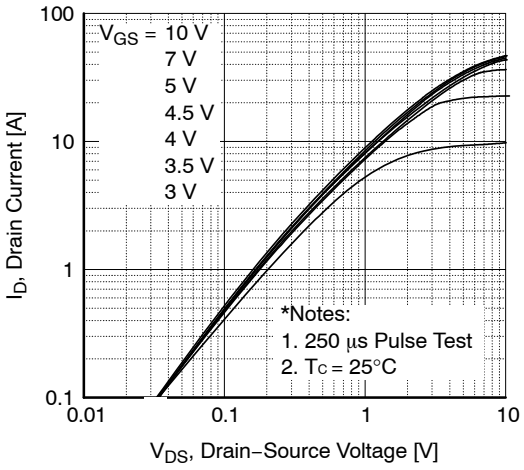


Figure 1. On−Region Characteristics

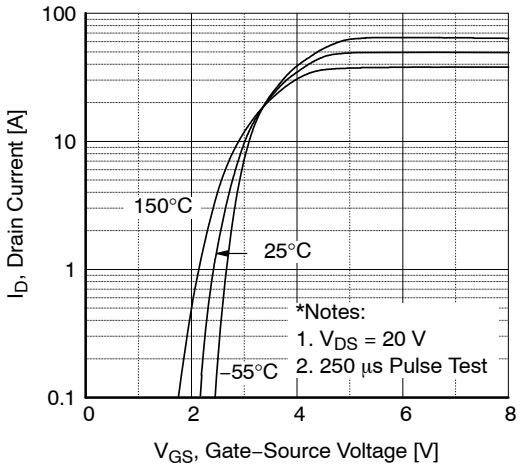


Figure 2. Transfer Characteristics

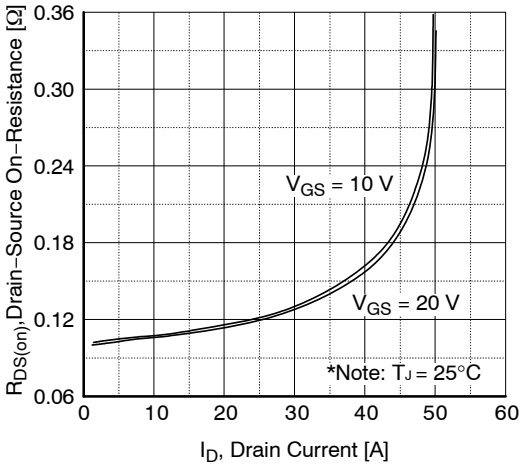


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

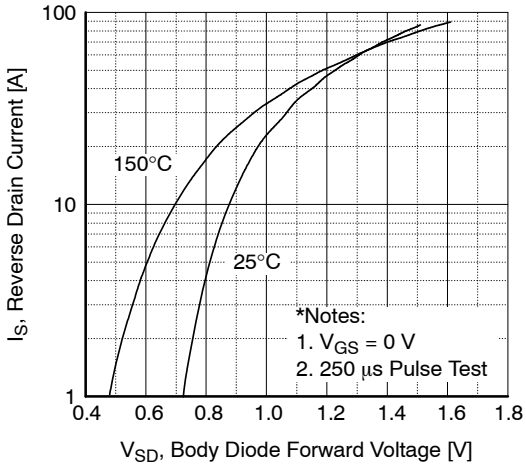


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

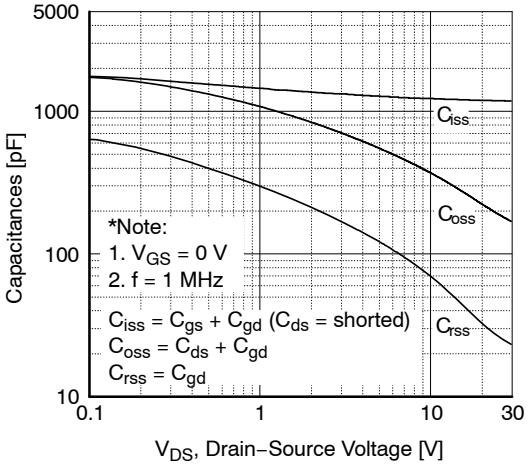


Figure 5. Capacitance Characteristics

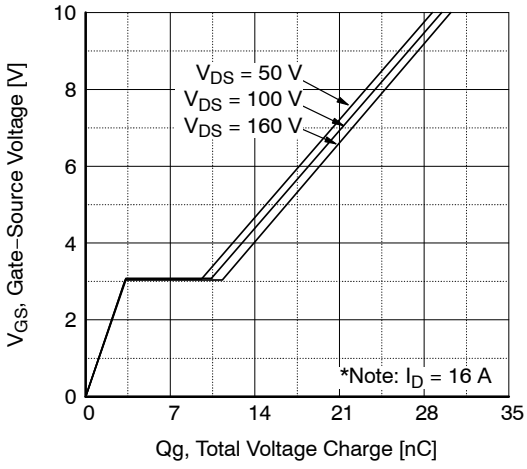


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

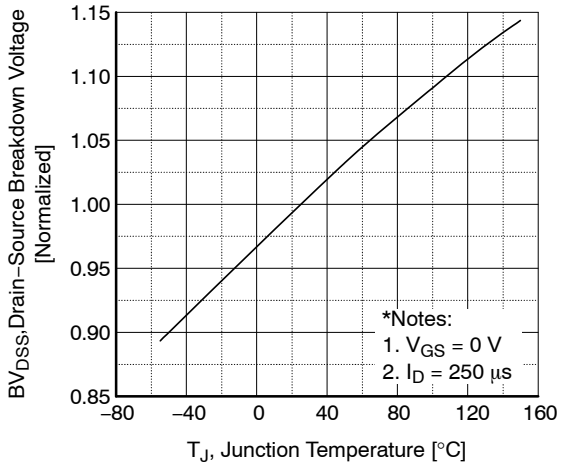


Figure 7. Breakdown Voltage Variation vs. Temperature

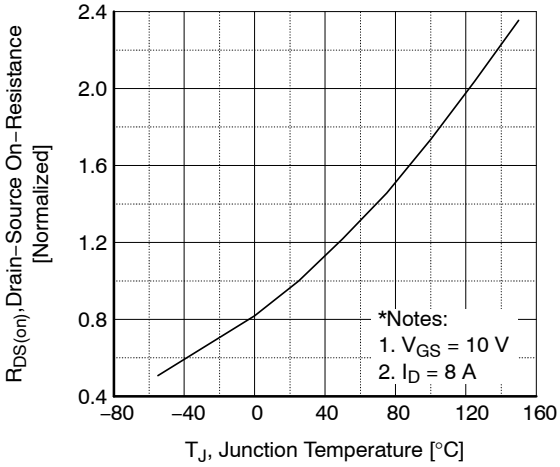


Figure 8. On−Resistance Variation vs. Temperature

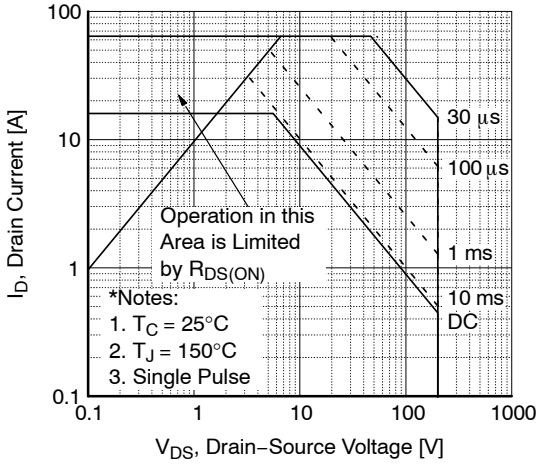


Figure 9. Maximum Safe Operating Area

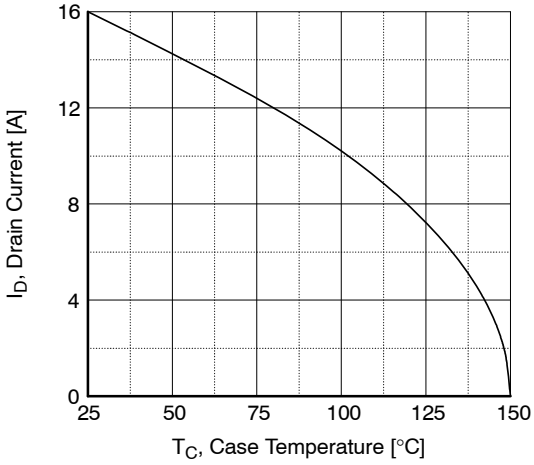


Figure 10. Maximum Drain Current vs. Case Temperature

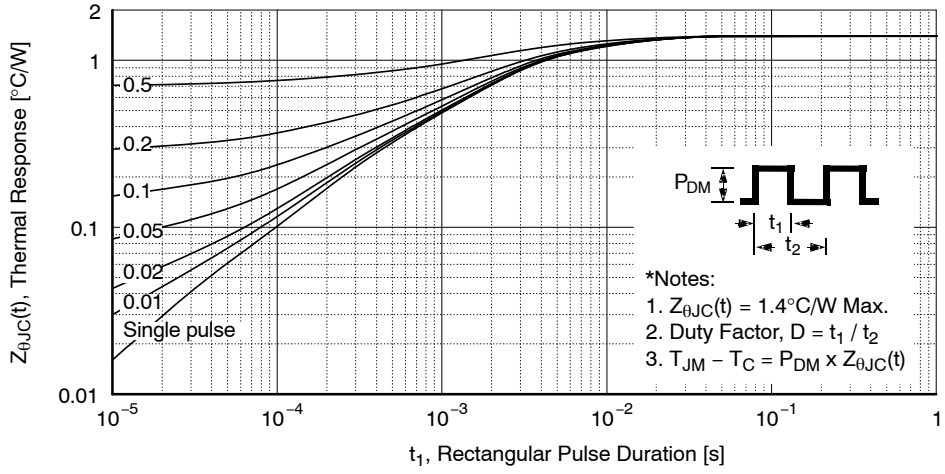


Figure 11. Transient Thermal Response Curve

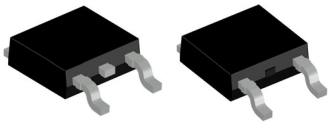
PACKAGE MARKING ANDORDERING INFORMATION

Part Number	Top Mark	Package	Reel Size	Tape Width	Shipping†
FDD18N20LZ	FDD18N20LZ	DPAK3 (TO−252 3 LD) (Pb−Free)	330 mm	16 mm	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

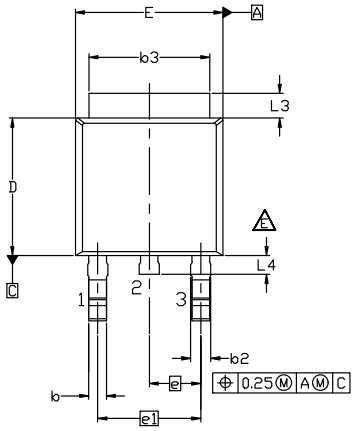
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

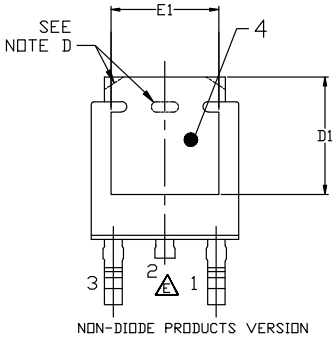


DPAK3 6.10x6.54x2.29, 4.57P
CASE 369AS
ISSUE B

DATE 20 DEC 2023

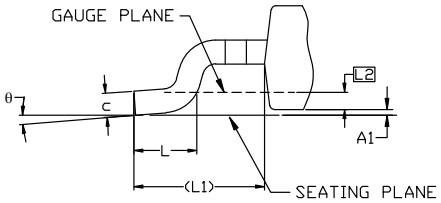


NON-DIODE PRODUCTS VERSION



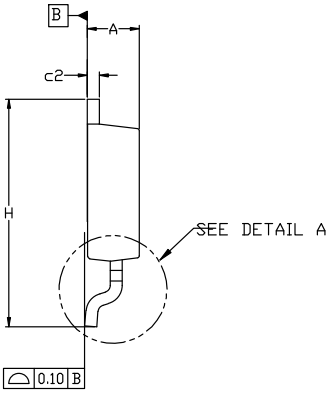
NON-DIODE PRODUCTS VERSION

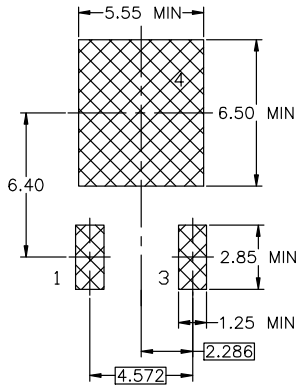
NOTES: UNLESS OTHERWISE SPECIFIED
A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE F, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX PLASTIC BODY STUB WITHOUT CENTER LEAD.
F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	–	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	---	---
E	6.35	6.54	6.73
E1	4.32	---	---
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	---	---	1.02
θ	0°	---	10°





LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

DOCUMENT NUMBER:	**98AON13810G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.
DESCRIPTION:	**DPAK3 6.10x6.54x2.29, 4.57P**	**PAGE 1 OF 1**

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