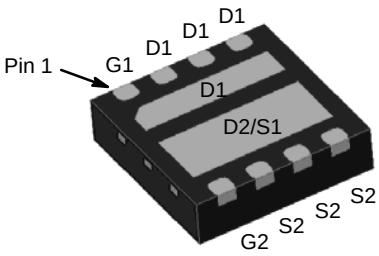
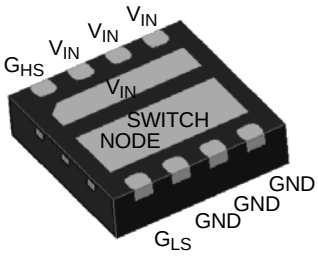
MOSFET – Dual, N-Channel, POWERTRENCH®

30 V, 9.5 mΩ and 20 mΩ

FDMC8200



Top



Bottom

WDFN8 3x3, 0.65P
(Power 33)
CASE 511DE

General Description

This device includes two specialized N−Channel MOSFETs in a dual Power33 (3 mm x 3 mm MLP) package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous MOSFET (Q2) have been designed to provide optimal power efficiency.

Features

- Q1: N−Channel
  - Max $r_{DS(on)}$ = 20 mΩ at V_{GS} = 10 V, I_D = 6 A
  - Max $r_{DS(on)}$ = 32 mΩ at V_{GS} = 4.5 V, I_D = 5 A
- Q2: N−Channel
  - Max $r_{DS(on)}$ = 9.5 mΩ at V_{GS} = 10 V, I_D = 9 A
  - Max $r_{DS(on)}$ = 13.5 mΩ at V_{GS} = 4.5 V, I_D = 7 A
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Applications

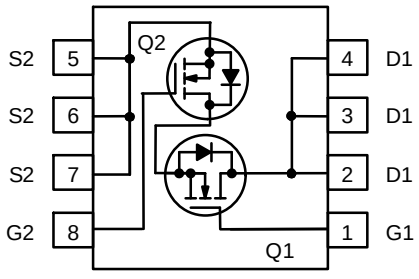
- Mobile Computing
- Mobile Internet Devices
- General Purpose Point of Load

MARKING DIAGRAM



$Y = Logo
&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
FDMC8200 = Device Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

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MOSFET MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

Symbol	Parameter		Q1	Q2	Unit
V_{DS}	Drain to Source Voltage		30	30	V
V_{GS}	Gate to Source Voltage	(Note 3)	±20	±20	V
I_D	Drain Current − Continuous (Package Limited)	T_C = 25°C	18	18	A
	− Continuous (Silicon Limited)	T_C = 25°C	23	45	
	− Continuous	T_A = 25°C	8 (Note 1a)	12 (Note 1b)	
	− Pulsed		40	40	
P_D	Power Dissipation	T_A = 25°C	1.9 (Note 1a)	2.2 (Note 1b)	W
	Power Dissipation	T_A = 25°C	0.7 (Note 1c)	0.9 (Note 1d)	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_C = 25°C, unless otherwise noted)

Symbol	Parameter	Q1	Q2	Unit
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	65 (Note 1a)	55 (Note 1b)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	180 (Note 1c)	145 (Note 1d)	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	7.5	4	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

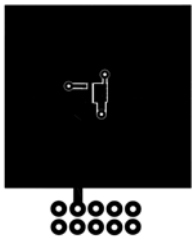
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V I_D = 250 μA, V_{GS} = 0 V	Q1 Q2	30 30	− −	− −	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 250 μA, referenced to 25°C	Q1 Q2	− −	14 14	− −	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V V_{DS} = 24 V, V_{GS} = 0 V	Q1 Q2	− −	− −	1 1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V, V_{GS} = 0 V	Q1 Q2	− −	− −	100 100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA V_{GS} = V_{DS}, I_D = 250 μA	Q1 Q2	1.0 1.0	2.3 2.3	3.0 3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, referenced to 25°C I_D = 250 μA, referenced to 25°C	Q1 Q2	− −	−5 −6	− −	mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 6 A V_{GS} = 4.5 V, I_D = 5 A V_{GS} = 10 V, I_D = 6 A, T_J = 125°C	Q1	− − −	16 24 22	20 32 28	mΩ
		V_{GS} = 10 V, I_D = 9 A V_{GS} = 4.5 V, I_D = 7 A V_{GS} = 10 V, I_D = 9 A, T_J = 125°C	Q2	− − −	7.3 9.5 10	9.5 13.5 13	
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 6 A V_{DD} = 5 V, I_D = 9 A	Q1 Q2	− −	29 56	− −	S
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHZ	Q1 Q2	− −	495 1180	660 1570	pF
C_{oss}	Output Capacitance		Q1 Q2	− −	145 330	195 440	pF
C_{rss}	Reverse Transfer Capacitance		Q1 Q2	− −	20 30	30 45	pF

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

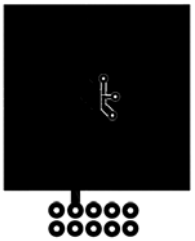
Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Unit
DYNAMIC CHARACTERISTICS							
R_g	Gate Resistance	f = 1 MHz	Q1 Q2	– –	1.4 1.4	– –	Ω
SWITCHING CHARACTERISTICS							
$t_{d(on)}$	Turn−On Delay Time	Q1 V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω Q2 V_{DD} = 15 V, I_D = 1 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	Q1 Q2	– –	11 13	20 23	ns
t_r	Rise Time		Q1 Q2	– –	3.1 4	10 10	ns
$t_{d(off)}$	Turn−Off Delay Time		Q1 Q2	– –	35 38	56 60	ns
t_f	Fall Time		Q1 Q2	– –	1.3 6	10 12	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V Q1: V_{DD} = 15 V, I_D = 6 A Q2: V_{DD} = 15 V, I_D = 9 A	Q1 Q2	– –	7.3 16	10 22	nC
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 4.5 V Q1: V_{DD} = 15 V, I_D = 6 A Q2: V_{DD} = 15 V, I_D = 9 A	Q1 Q2	– –	3.1 7	4.3 10	nC
Q_{gs}	Gate to Source Charge	Q1: V_{DD} = 15 V, I_D = 6 A Q2: V_{DD} = 15 V, I_D = 9 A	Q1 Q2	– –	1.8 4.1	– –	nC
Q_{gd}	Gate to Drain “Miller” Charge		Q1 Q2	– –	1 1.5	– –	nC
DRAIN−SOURCE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 6 A (Note 2) V_{GS} = 0 V, I_S = 9 A (Note 2)	Q1 Q2	– –	0.8 0.8	1.2 1.2	V
t_{rr}	Reverse Recovery Time	Q1 I_F = 6 A, di/dt = 100 A/μS Q2 I_F = 9 A, di/dt = 100 A/μS	Q1 Q2	– –	13 21	24 34	ns
Q_{rr}	Reverse Recovery Charge		Q1 Q2	– –	2.3 5.6	10 12	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

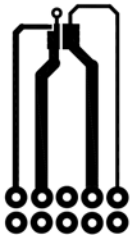
1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



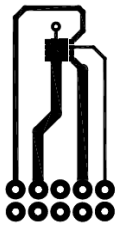
a. 65°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 55°C/W when mounted on a 1 in^2 pad of 2 oz copper



c. 180°C/W when mounted on a minimum pad of 2 oz copper



d. 145°C/W when mounted on a minimum pad of 2 oz copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. As an N−ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) (T_J = 25°C, unless otherwise noted)

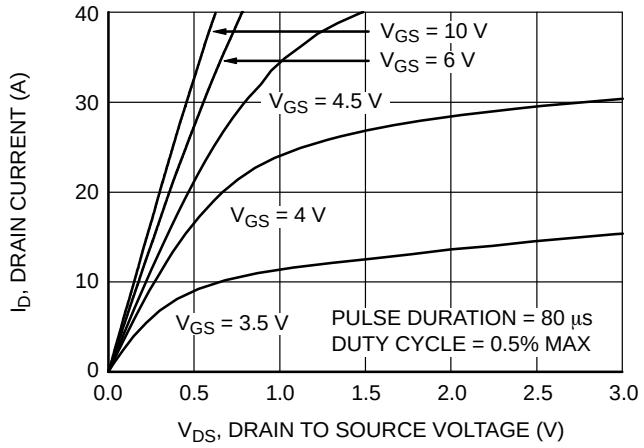


Figure 1. On Region Characteristics

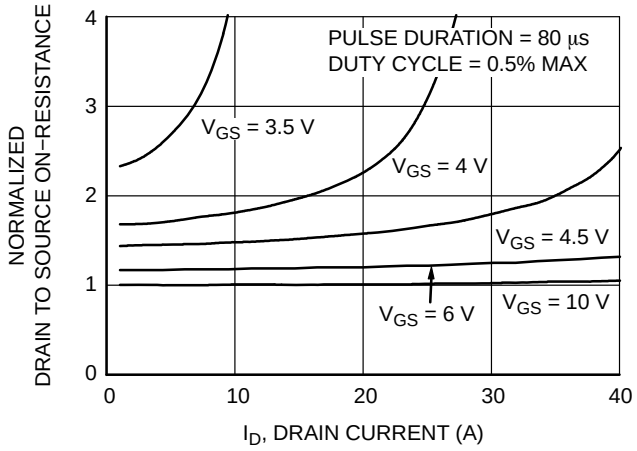


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

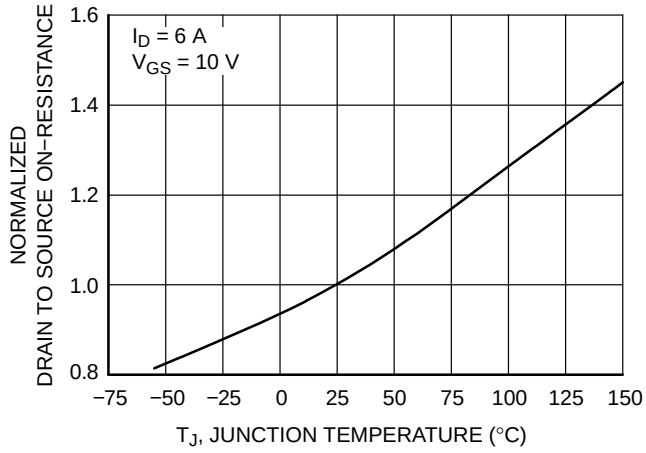


Figure 3. Normalized On Resistance vs. Junction Temperature

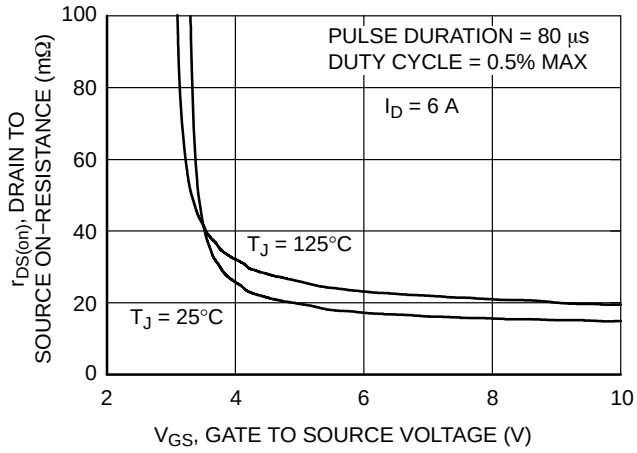


Figure 4. On−Resistance vs. Gate to Source Voltage

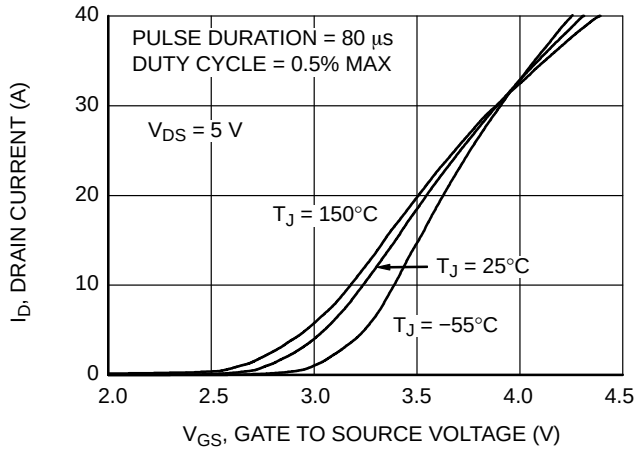


Figure 5. Transfer Characteristics

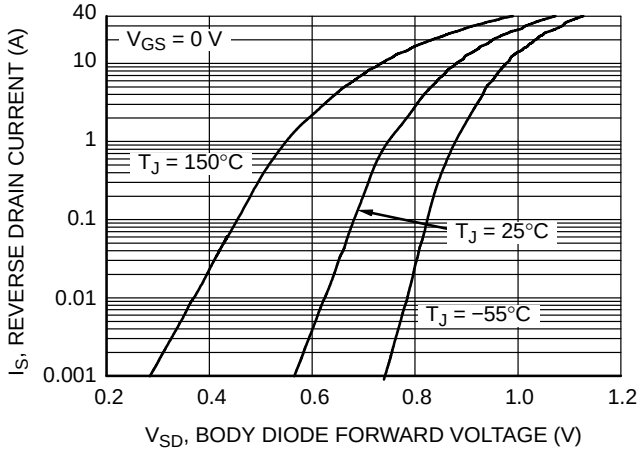


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) (T_J = 25°C, unless otherwise noted) (continued)

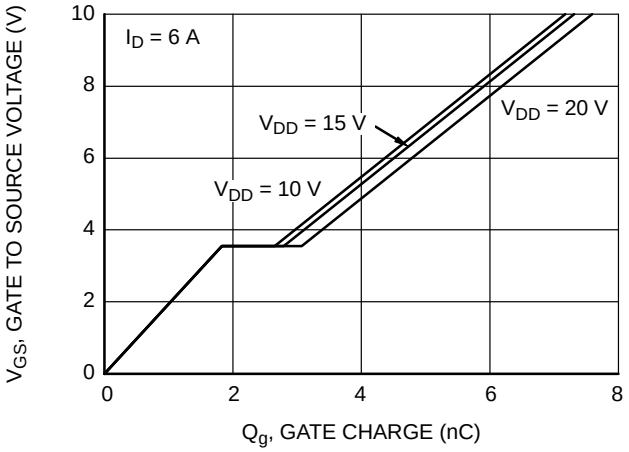


Figure 7. Gate Charge Characteristics

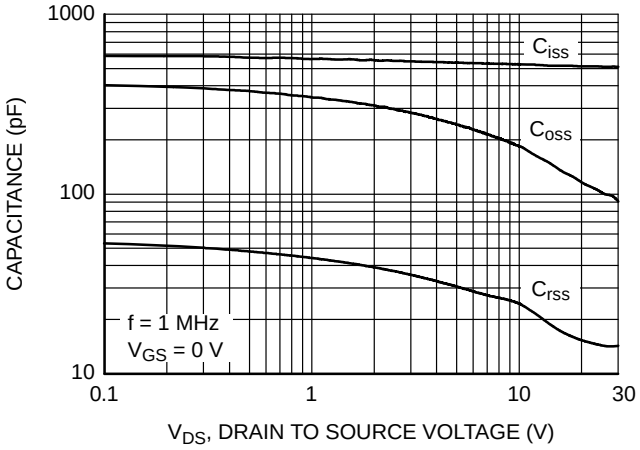


Figure 8. Capacitance vs. Drain to Source Voltage

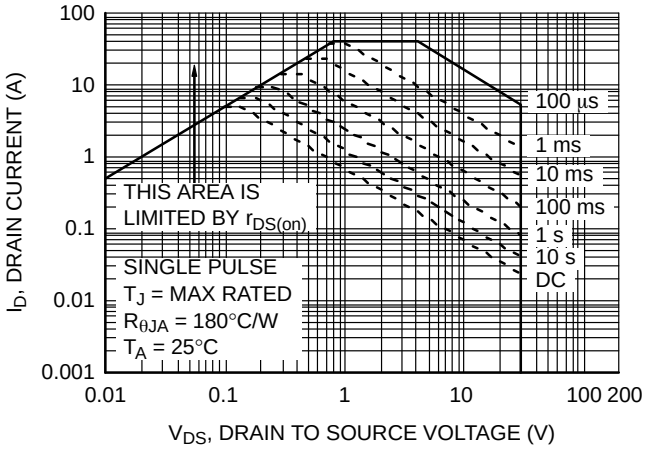


Figure 9. Forward Bias Safe Operating Area

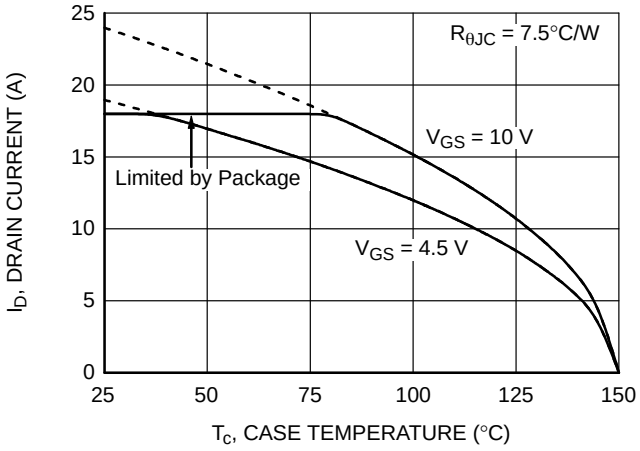


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

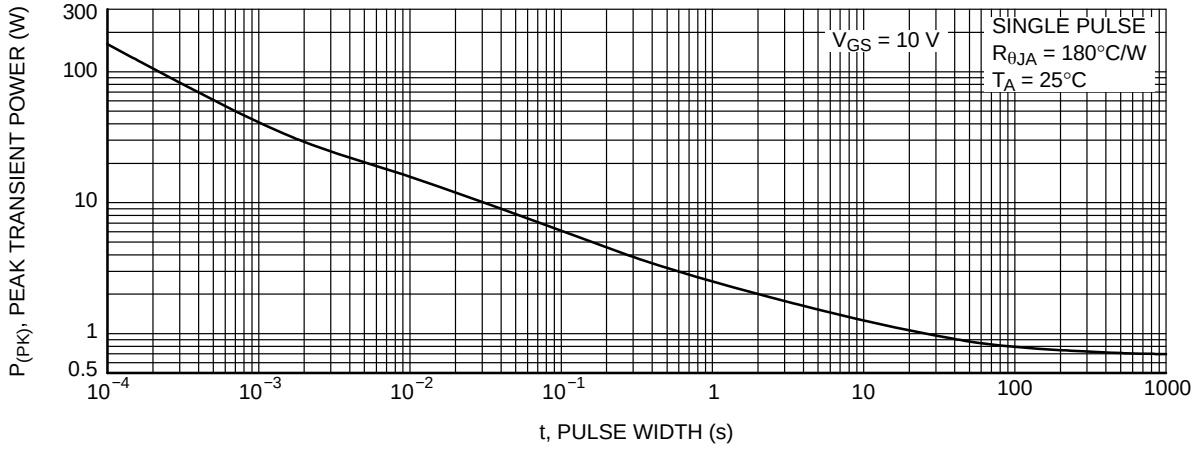


Figure 11. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q1 N−CHANNEL) (T_J = 25°C, unless otherwise noted) (continued)

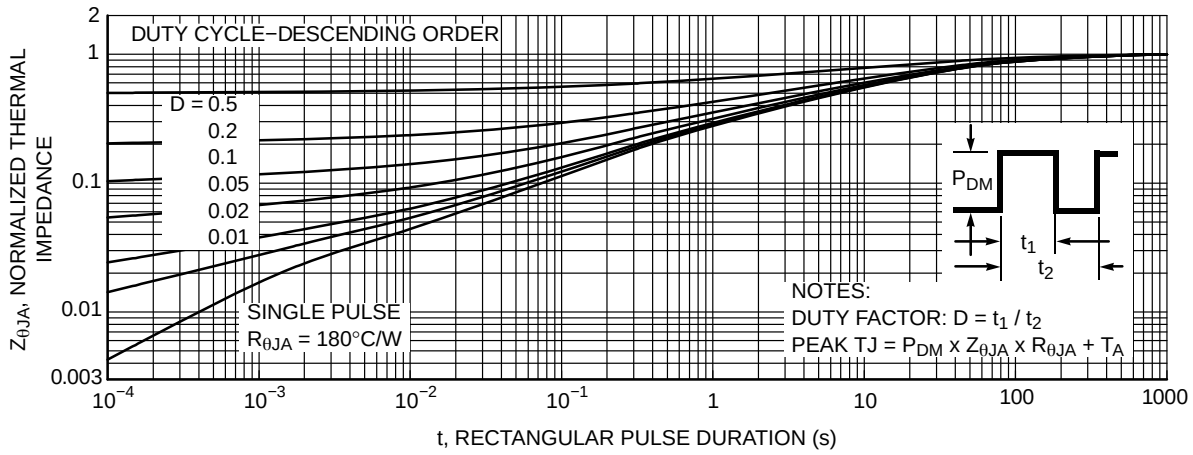


Figure 12. Junction−to−Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N−CHANNEL) (T_J = 25°C, unless otherwise noted)

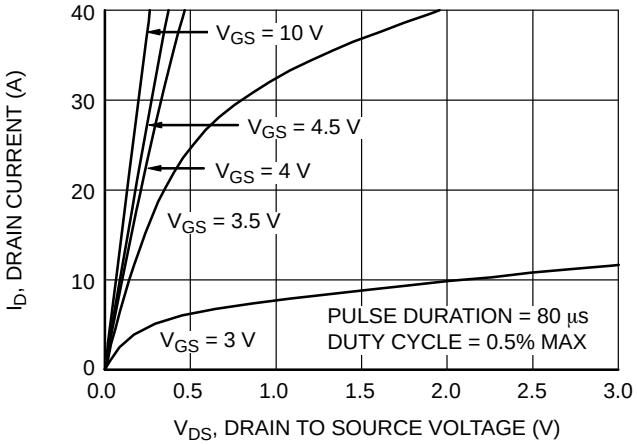


Figure 13. On−Region Characteristics

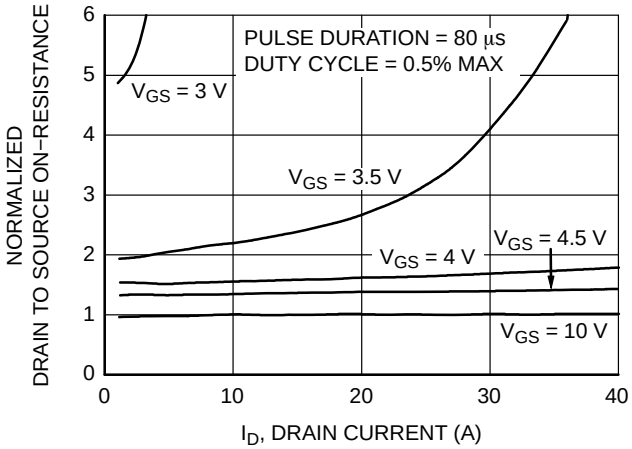


Figure 14. Normalized On−Resistance vs. Drain Current and Gate Voltage

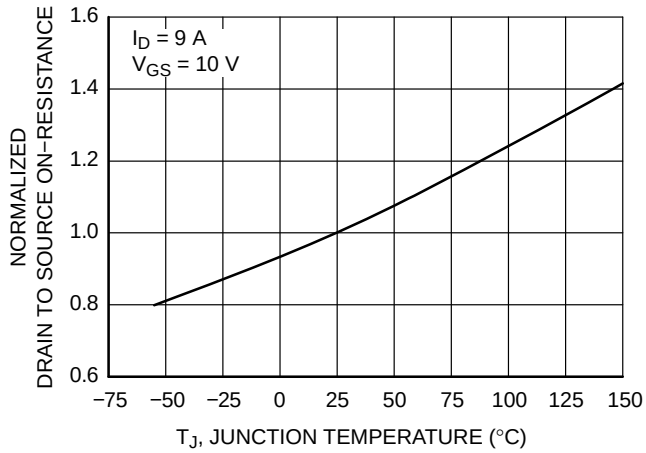


Figure 15. Normalized On Resistance vs. Junction Temperature

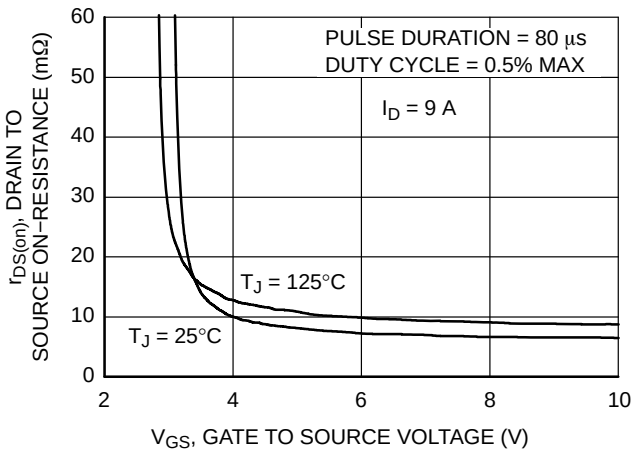


Figure 16. On−Resistance vs. Gate to Source Voltage

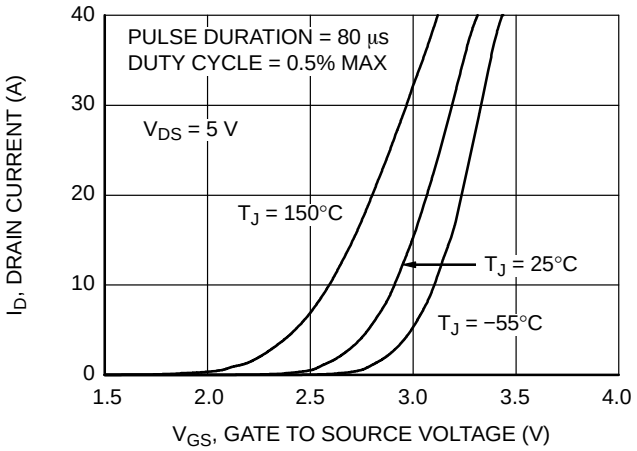


Figure 17. Transfer Characteristics

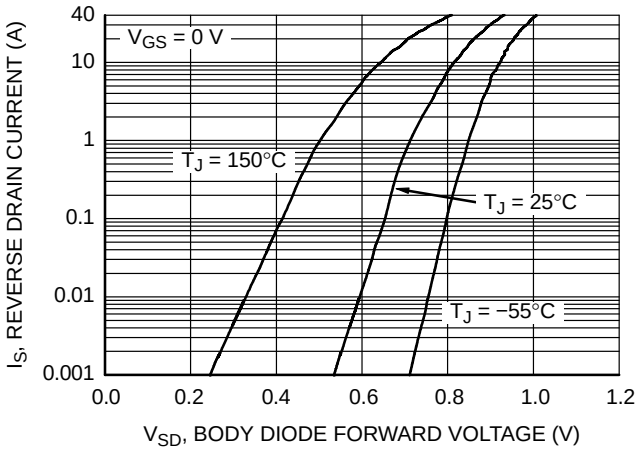


Figure 18. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q2 N−CHANNEL) (T_J = 25°C, unless otherwise noted) (continued)

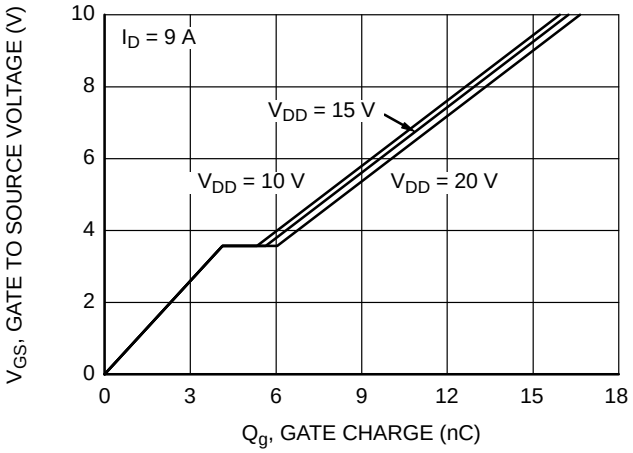


Figure 19. Gate Charge Characteristics

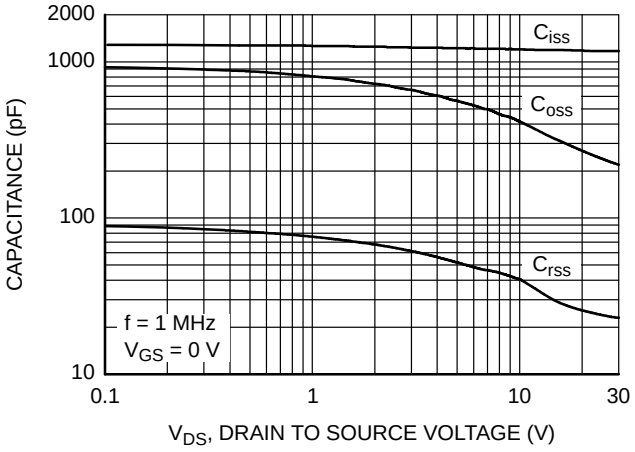


Figure 20. Capacitance vs. Drain to Source Voltage

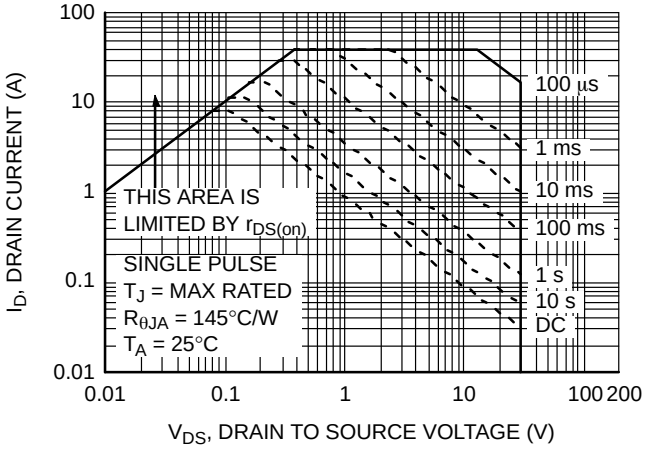


Figure 21. Forward Bias Safe Operating Area

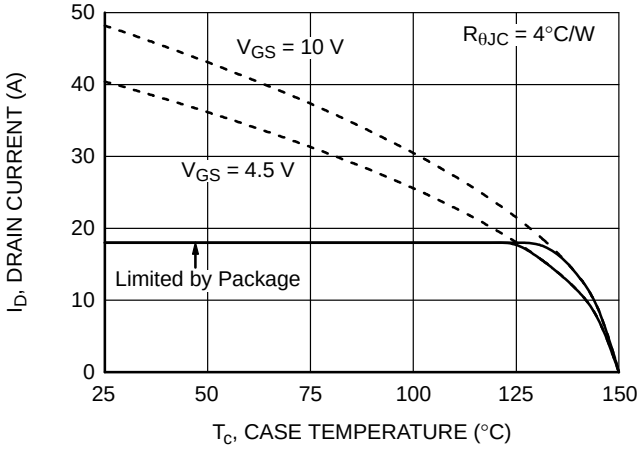


Figure 22. Maximum Continuous Drain Current vs. Case Temperature

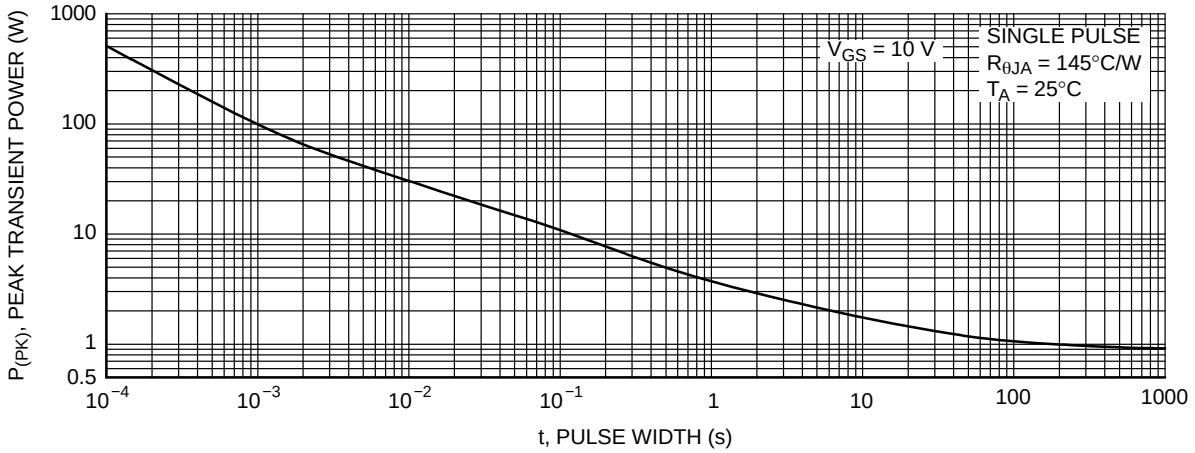


Figure 23. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (Q2 N−CHANNEL) (T_J = 25°C, unless otherwise noted) (continued)

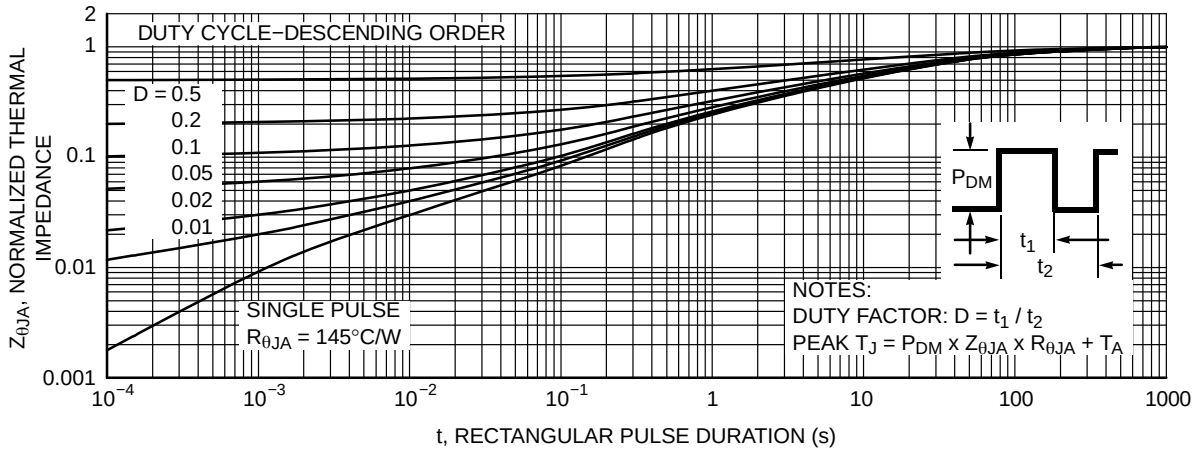


Figure 24. Junction−to−Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

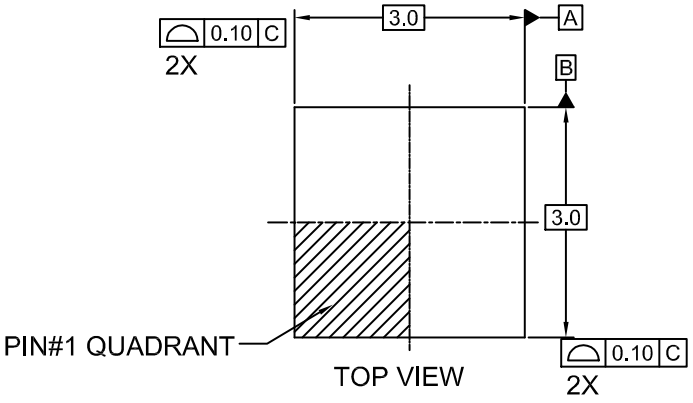
Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMC8200	FDMC8200	WDFN8 3x3, 0.65P (Power 33) (Pb−Free, Halide Free)	13”	12 mm	3000 / Tape & Reel

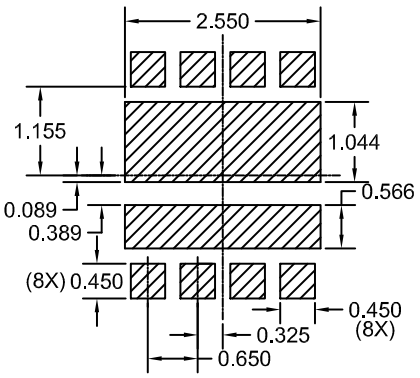
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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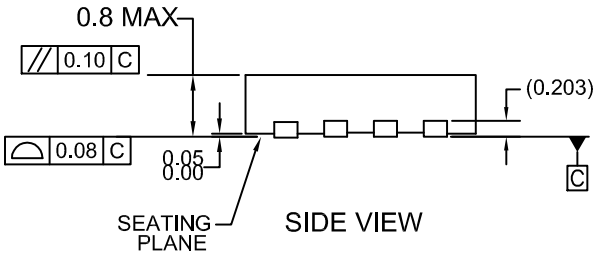
WDFN8 3x3, 0.65P
CASE 511DE
ISSUE O

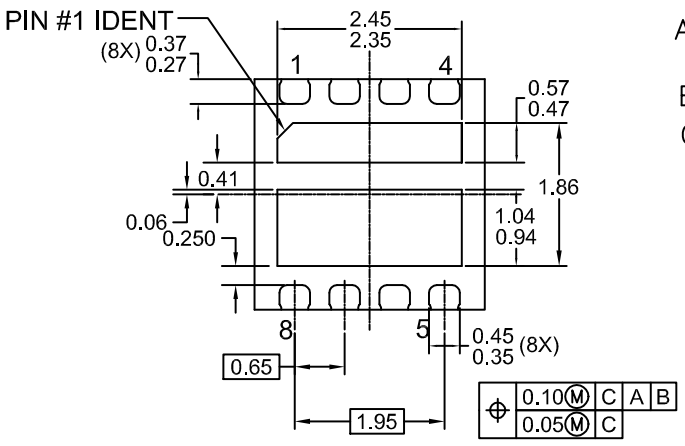
DATE 31 AUG 2016





RECOMMENDED LAND PATTERN





BOTTOM VIEW

NOTES:

A. DOES NOT CONFORM TO JEDEC REGISTRATION MO−229
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994

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DESCRIPTION:	**WDFN8 3X3, 0.65P**	**PAGE 1 OF 1**

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