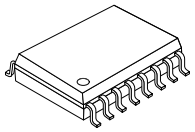
Input LED Drive, 2.5 A Output Current, IGBT Drive Optocoupler with Desaturation Detection, Isolated Fault Sensing, and Active Miller Clamp

FOD8332



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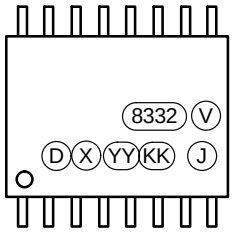
CASE 751EN

MARKING DIAGRAM



8332 = Device number, e.g., '8332' for FOD8332
V = DIN EN/IEC60747−5−5 Option (Only Appears on Component Ordered with This Option)
D = Plant Code
X = Alphabetical Year Code
YY = Two−digit Work Week
KK = Lot Traceability Code
W = Package Assembly Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 28 of this data sheet.

Description

The FOD8332 is an advanced 2.5 A output current IGBT drive optocoupler capable of driving medium−power IGBTs with ratings up to 1,200 V and 150 A. It is suited for fast−switching driving of power IGBTs and MOSFETs in motor−control inverter applications and high−performance power systems. The FOD8332 offers protection features necessary for preventing fault conditions that lead to destructive thermal runaway of IGBTs.

The device utilizes **onsemi**'s proprietary OPTOPLANAR® coplanar packaging technology and optimized IC design to achieve reliable high isolation and high noise immunity, characterized by high common−mode rejection and power supply rejection specifications. The device is housed in a wide−body, 16−pin, small−outline, plastic package.

The gate−driver channel consists of an aluminum gallium arsenide (AlGaAs) light−emitting diode (LED) optically coupled to an integrated high−speed driver circuit with a low−$R_{DS(ON)}$ MOSFET output stage. The fault−sense channel consists of an AlGaAs LED optically coupled to an integrated high−speed feedback circuit for fault sensing.

Features

- Input LED Drive Facilitates Receiving Digitally Encoded Signals from PWM Output
- Optically Isolated Fault−Sensing Feedback
- Active Miller Clamp to Shut Off IGBT During High dv/dt without Negative Supply Voltage
- High Noise Immunity Characterized by Common Mode Rejection − 35 kV/μs Minimum, V_{CM} = 1500 V_{PEAK}
- 2.5 A Peak Output Current Driving Capability for Medium Power IGBT
  - P−Channel MOSFETs at Output Stage Enable Output Voltage Swing Close to Supply Rail (Rail−to−Rail Output)
  - Wide Supply Voltage Range: 15 V to 30 V
- Integrated IGBT Protection
  - Desaturation Detection
  - "Soft" IGBT Turn−Off
  - Under−Voltage Lockout (UVLO) with Hysteresis
- Fast Switching Speed Over Full Operating Temperature Range
  - 250 ns Maximum Propagation Delay
  - 100 ns Maximum Pulse Width Distortion

Features (continued)

- Extended Industrial Temperature Range:
  - −40°C to 100°C
- Safety and Regulatory Approvals
  - UL1577, 4,243 V_{RMS} for 1 Minute
  - DIN−EN/IEC60747−5−5:
    1,414 VPEAK Working Insulation Voltage Rating
    8,000 VPEAK Transient Isolation Voltage Rating
- 8 mm Creepage and Clearance Distances
- These are Pb−Free Devices

Applications

- AC and Brushless DC Motor Drive
- Industrial Inverter
- Uninterruptible Power Supply
- Induction Heating
- Isolated IGBT/Power MOSFET Gate Drive

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Related Resources

- FOD8316 − 2.5 A Output Current, IGBT Drive Optocoupler with Desaturation, Isolated Fault Sensing
- FOD8318 − 2.5 A Output Current, IGBT Drive Optocoupler with Active Miller Clamp, Desaturation Detection, and Isolated Fault Sensing
- FOD8333 − Input LED Drive, 2.5 A Output Current, IGBT Drive Optocoupler with Desaturation Detection, Isolated Fault Sensing, Active Miller Clamp, and Automatic Fault Reset
- AN−3009 − Standard Gate−Driver Optocouplers
- https://www.onsemi.com/products/interfaces/igbt−mosfet−gate−drivers−optocouplers

TRUTH TABLE

LED	UVLO (V_{DD} − V_E)	DESAT Detected?	$\overline{\text{FAULT}}$ (Note 1)	V_O
X	Active	X	HIGH	LOW
On	Not Active	Yes	LOW	LOW
Off	X	X	HIGH	LOW
On	Not Active	No	HIGH	HIGH

1. $\overline{\text{FAULT}}$ pin is connected to a pull−up resistor.

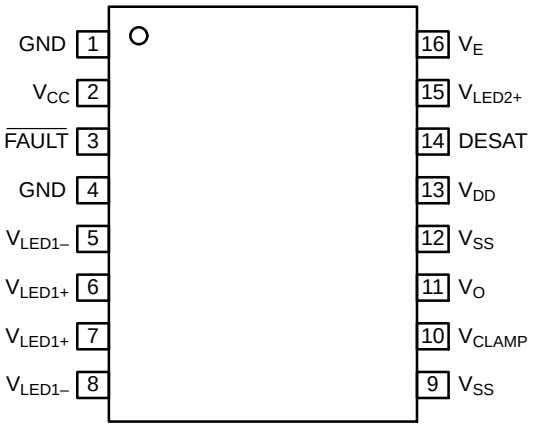

Figure 1. Pin Configuration

PIN DEFINITIONS

Pin No.	Name	Description
1	GND	Ground for Fault−Sense Optocoupler
2	V_{CC}	Positive Supply Voltage (3 V to 15 V) for Fault Sense Optocoupler
3	$\overline{\text{FAULT}}$	Fault−Sense Output
4	GND	Ground for Fault−Sense Optocoupler
5	V_{LED1-}	LED1 Cathode
6	V_{LED1+}	LED1 Anode
7	V_{LED1+}	LED1 Anode
8	V_{LED1-}	LED1 Cathode
9	V_{SS}	Negative Output Supply Voltage
10	V_{CLAMP}	Clamp Supply Voltage
11	V_O	Gate−Drive Output Voltage
12	V_{SS}	Negative Output Supply Voltage
13	V_{DD}	Positive Output Supply Voltage
14	DESAT	Desaturation Voltage Input
15	V_{LED2+}	LED2 Anode (Do not connect. Leave floating.)
16	V_E	Output Supply Voltage/IGBT Emitter

BLOCK DIAGRAM

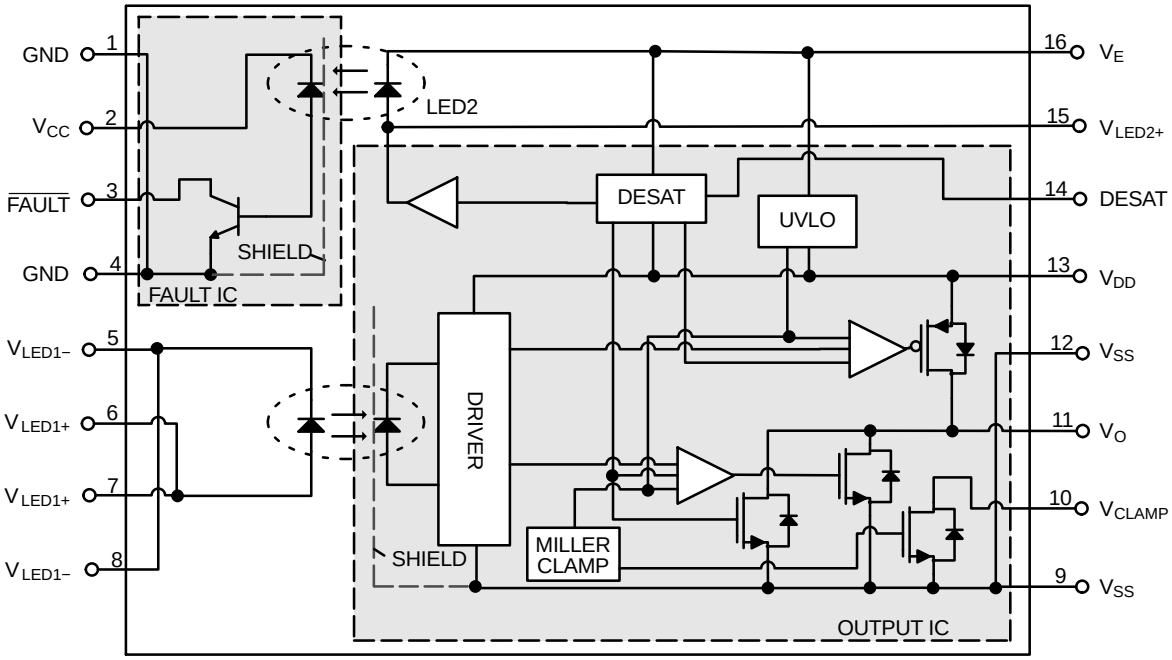

Figure 2. Functional Block Diagram

SAFETY AND INSULATION RATINGS (As per DIN EN/IEC 60747−5−5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings must be ensured by means of protective circuits.)

Symbol	Parameter	Min	Typ	Max	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage < 150 V_{RMS}	−	I−IV	−	
	Rated Mains Voltage < 300 V_{RMS}	−	I−IV	−	
	Rated Mains Voltage < 450 V_{RMS}	−	I−IV	−	
	Rated Mains Voltage < 600 V_{RMS}	−	I−IV	−	
	Rated Mains Voltage < 1000 V_{RMS}	−	I−III	−	
	Climatic Classification	−	40/100/21	−	
	Pollution Degree (DIN VDE 0110/1.89)	−	2	−	
CTI	Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1)	175	−	−	
V_{PR}	Input−to−Output Test Voltage, Method b, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC	2651	−	−	V_{peak}
	Input−to−Output Test Voltage, Method a, V_{IORM} x 1.6 = V_{PR}, Type and Sample Test with t_m = 10 s, Partial Discharge < 5 pC	2262	−	−	V_{peak}
V_{IORM}	Maximum Working Insulation Voltage	1414	−	−	V_{peak}
V_{IOTM}	Highest Allowable Over Voltage	8000	−	−	V_{peak}
	External Creepage	8.0	−	−	mm
	External Clearance	8.0	−	−	mm
	Insulation Thickness	0.5	−	−	mm
T_{Case}	Safety Limit Values − Maximum Values in Failure; Case Temperature	150	−	−	°C
$P_{S,INPUT}$	Safety Limit Values − Maximum Values in Failure; Input Power	100	−	−	mW
$P_{S,OUTPUT}$	Safety Limit Values − Maximum Values in Failure; Output Power	600	−	−	mW
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V	10^9	−	−	Ω

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified.)

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−40 to +125	°C
T_{OPR}	Operating Temperature	−40 to +100	°C
T_J	Junction Temperature	−40 to +125	°C
T_{SOL}	Lead Solder Temperature (Not Certified for Wave Immersion) *Refer to Reflow Temperature Profile on Page 27*	260 for 10 s	°C
PD_I	Input Power Dissipation (Note 2, 3)	45	mW
PD_O	Output Power Dissipation (Note 3, 4)	600	mW
GATE DRIVE CHANNEL			
$I_{F(AVG)}$	Average Input Current	25	mA
$I_{F(PEAK)}$	Peak Transient Forward Current (Pulse Width < 1 μs)	1.0	A
$I_{OH(PEAK)}$	Peak Output High Current (Note 5)	3.0	A
$I_{OL(PEAK)}$	Peak Output Low Current (Note 5)	3.0	A
V_R	Reverse Input Voltage	5.0	V
$V_E - V_{SS}$	Negative Output Supply Voltage (Note 6)	−0.5 to 15	V
$V_{DD} - VE$	Positive Output Supply Voltage	−0.5 to 35 − ($V_E - V_{SS}$)	V
$V_{O(PEAK)} - V_{SS}$	Gate Drive Output Voltage	−0.5 to 35	V
$V_{DD} - V_{SS}$	Output Supply Voltage	−0.5 to 35	V
V_{DESAT}	Desaturation Voltage	V_E to V_E + 25	V
I_{DESAT}	Desaturation Current	60	mA
$V_{CLAMP} - V_{SS}$	Active Miller Clamping Voltage	−0.5 to 35	V
I_{CLAMP}	Peaking Clamping Sinking Current	1.7	A
$t_{R(IN)}$, $t_{F(IN)}$	Input Signal Rise and Fall Time	500	ns
FAULT SENSE CHANNEL			
V_{CC}	Positive Input Supply Voltage	−0.5 to 20	V
$V_{\overline{FAULT}}$	$\overline{FAULT}$ Output Voltage	−0.5 to 20	V
$I_{\overline{FAULT}}$	$\overline{FAULT}$ Output Current	16.0	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. No derating required across temperature range.
3. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.
4. Derate linearly above 25°C, free air temperature at a rate of 6.2 mW/°C.
5. Maximum pulse width = 10 μs.
6. This negative output supply voltage is optional. It is only needed when negative gate drive is implemented.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
T_A	Ambient Operating Temperature	−40	+100	°C
$I_{F(ON)}$	Input Current (ON)	7	16	mA
$V_{F(OFF)}$	Input Voltage (OFF)	−3.6	0.8	V
V_{CC}	Supply Voltage	3	15	V
$V_{DD} - V_{SS}$	Total Output Supply Voltage	15	30	V
$V_{DD} - V_E$	Positive Output Supply Voltage (Note 7)	15	30 − ($V_E - V_{SS}$)	V
$V_E - V_{SS}$	Negative Output Supply Voltage	0	15	V
t_{PW}	Input Pulse Width	500	−	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

7. During power up or down, ensure that both the input and output supply voltages reach the proper recommended operating voltages to avoid any momentary instability at the output state.

ISOLATION CHARACTERISTICS (Apply over all recommended conditions; typical value is measured at T_A = 25°C.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{ISO}	Input−Output Isolation Voltage	T_A = 25°C, Relative Humidity < 50%, t = 1.0 minute, I_{I-O} ≤ 10 μA, 50 Hz (Note 8, 9, 10)	4,243	−	−	V_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V (Note 8)	−	10^{11}	−	
C_{ISO}	Isolation Capacitance	V_{I-O} = 0 V, Frequency = 1.0 MHz (Note 8)	−	1	−	pF

8. Device is considered a two−terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together.
9. 4,243 V_{RMS} for 1−minute duration is equivalent to 5,091 V_{RMS} for 1−second duration.
10. The input−output isolation voltage is a dielectric voltage rating per UL1577. It should not be regarded as an input−output continuous voltage rating. For the continuous working voltage rating, refer to equipment−level safety specification or DIN EN/IEC 60747−5−5 Safety and Insulation Ratings Table.

ELECTRICAL CHARACTERISTICS (Apply over all recommended conditions; typical value is measured at V_{CC} = 5 V, V_{DD} − V_{SS} = 30 V, V_E − V_{SS} = 0 V, and T_A = 25°C; unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Figure
GATE DRIVE CHANNEL							
V_F	Input Forward Voltage	I_F = 10 mA	1.10	1.45	1.80	V	5
$\Delta(V_F/T_A)$	Temperature Coefficient of Forward Voltage		−	−1.5	−	mV/°C	
BV_R	Input Reverse Breakdown Voltage	I_R = 10 μA	5	−	−	V	
C_{IN}	Input Capacitance	f = 1 MHz, V_F = 0 V	−	60		pF	
I_{FLH}	Threshold Input Current, Low−to−High	I_O = 0 mA, V_O > 5 V	−	2.5	7.0	mA	30
V_{FHL}	Threshold Input Voltage, High−to−Low	I_O = 0 mA, V_O < 5 V	0.8	−	−	V	31
I_{OH}	High Level Output Current	V_O = V_{DD} − 3 V, I_F = 10 mA	−1.0	−2.5	−	A	6, 10, 32
		V_O = V_{DD} − 6 V, I_F = 10 mA (Note 11)	−2.5	−	−	A	
I_{OL}	Low Level Output Current	V_O = V_{SS} + 3 V, I_F = 0 mA	1	3	−	A	7, 11, 33
		V_O = V_{SS} + 6 V, I_F = 0 mA (Note 12)	2.5	−	−	A	
I_{OLF}	Low Level Output Current During Fault Condition	V_O − V_{SS} = 14 V	70	125	170	mA	34
V_{OH}	High Level Output Voltage	I_F = 10 mA, I_O = −100 mA (Note 13, 14, 15)	V_{DD} − 1.0	V_{DD} − 0.2	−	V	8, 10, 35
V_{OL}	Low Level Output Voltage	I_F = 0 mA, I_O = 100 mA	−	0.1	0.5	V	9, 11, 36
I_{DDH}	High Level Supply Current	V_O = Open (Note 15), I_O = 0 mA	−	2.5	5.0	mA	12, 13, 37
I_{DDL}	Low Level Supply Current	V_O = Open, I_O = 0 mA	−	2.5	5.0	mA	12, 13, 38
I_{EL}	V_E Low Level Supply Current		−0.8	−0.5	−	mA	38
I_{EH}	V_E High Level Supply Current		−0.50	−0.25	−	mA	37
I_{CHG}	Blanking Capacitor Charge Current	V_{DESAT} = 2 V (Note 15, 16)	−0.33	−0.25	−0.13	mA	14, 39
I_{DSCHG}	Blanking Capacitor Discharge Current	V_{DESAT} = 7 V	10	40	−	mA	39
V_{UVLO+}	Under−Voltage Lockout Threshold (Note 14)	I_F = 10 mA, V_O > 5 V	10.8	11.7	12.7	V	40
V_{UVLO-}		I_F = 10 mA, V_O < 5 V	9.8	10.7	11.7	V	
$UVLO_{HYS}$	Under−Voltage Lockout Threshold Hysteresis		−	1.0	−	V	
V_{DESAT}	DESAT Threshold (Note 14)	V_{DD} − V_E > V_{ULVO-}	6.0	6.5	7.2	V	15, 39
V_{CLAMP_THRES}	Clamping Threshold Voltage		−	2.0	−	V	41
I_{CLAMPL}	Clamp Low Level Sinking Current	V_O = V_{SS} + 2.5 V	0.35	1.10	−	A	16, 42

ELECTRICAL CHARACTERISTICS (Apply over all recommended conditions; typical value is measured at V_{CC} = 5 V, $V_{DD} - V_{SS}$ = 30 V, $V_E - V_{SS}$ = 0 V, and T_A = 25°C; unless otherwise specified.) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Figure
FAULT FEEDBACK CHANNEL							
I_{CCH}	$\overline{FAULT}$ High Level Supply Current	I_{F2} = 0 mA, $V_{\overline{FAULT}}$ = Open, V_{CC} = 15 V	−	0.0004	2	μA	43
I_{CCL}	$\overline{FAULT}$ Low Level Supply Current	I_{F2} = 16 mA, $V_{\overline{FAULT}}$ = Open, V_{CC} = 15 V	−	150	200	μA	44
$I_{\overline{FAULTH}}$	$\overline{FAULT}$ Logic High Output Current	$V_{\overline{FAULT}} = V_{CC}$ = 5.5 V	−	0.02	0.50	μA	45
$I_{\overline{FAULTL}}$	$\overline{FAULT}$ Logic Low Output Current	$V_{\overline{FAULT}}$ = 0.4 V, V_{CC} = 5.5 V	1.1	−	−	mA	17, 46

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

11. Maximum pulse width = 10 μs, maximum duty cycle = 0.2%.
12. Minimum pulse width = 4.99 ms, minimum duty cycle = 99.8%.
13. V_{OH} is measured with the DC load current in this testing (maximum pulse width = 1 ms, maximum duty cycle = 20%). When driving capacitive loads, V_{OH} approaches V_{DD} as I_{OH} approaches zero units.
14. Positive output supply voltage ($V_{DD} - V_E$) should be at least 15 V to ensure adequate margin in excess of the maximum under−voltage lockout threshold, V_{UVLO+}, of 12.7 V.
15. When $V_{DD} - V_E > V_{UVLO}$ and the output state V_O is allowed to go HIGH, the DESAT−detection feature is active and provides the primary source of IGBT protection. UVLO is needed to ensure DESAT detection is functional.
16. The blanking time, t_{BLANK}, is adjustable by an external capacitor (C_{BLANK}), where $t_{BLANK} = C_{BLANK} \times (V_{DESAT} / I_{CHG})$.

SWITCHING CHARACTERISTICS (Apply over all recommended conditions; typical value is measured at V_{CC} = 5 V, V_{DD} − V_{SS} = 30 V, V_E − V_{SS} = 0 V, and T_A = 25°C; unless otherwise specified.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	Figure
t_{PHL}	Propagation Delay to Logic Low Output (Note 18)	Rg = 10 Ω, Cg =10 nF, f = 10 kHz, Duty Cycle = 50%, I_F = 10 mA, V_{DD} − V_{SS} = 30 V (Note 17)	100	135	250	ns	18, 19, 20, 21, 47
t_{PLH}	Propagation Delay to Logic High Output (Note 19)		100	150	250	ns	
PWD	Pulse Width Distortion, | t_{PHL} − t_{PLH}| (Note 20)		−	15	100	ns	47
PDD Skew	Propagation Delay Difference Between Any Two Parts or Channels, (t_{PHL} − t_{PLH}) (Note 21)		−150	−	150	ns	
t_R	Output Rise Time (10% to 90%)		−	50	−	ns	47
t_F	Output Fall Time (90% to 10%)		−	50	−	ns	
$t_{DESAT(LOW)}$	DESAT Sense to DESAT Low Propagation Delay (Note 24)	Rg = 10 Ω, Cg = 10 nF, V_{DD} − V_{SS} = 30 V (C_{DESAT} = 100 pF, R_F = 4.7 kΩ, V_{CC} = 5.5 V)	−	0.25	−	µs	
$t_{DESAT(90\%)}$	DESAT Sense to 90% V_O Delay (Note 22)		−	0.45	0.70	µs	22, 48
$t_{DESAT(10\%)}$	DESAT Sense to 10% V_O Delay (Note 22)		−	2.8	4.0	µs	23, 24, 25, 48
$t_{DESAT(FAULT)}$	DESAT Sense to Low Level FAULT Signal Delay (Note 23)		−	0.5	1.5	µs	26, 48
$t_{RESET(FAULT)}$	RESET to High Level FAULT Signal Delay (Note 25)		0.5	2.3	4.5	µs	27, 48
$t_{DESAT(MUTE)}$	DESAT Input Mute		10.0	22.0	35.0	µs	48
$t_{UVLO\ ON}$	UVLO Turn−On Delay (Note 26)	V_{DD} = 20 V in 1.0 ms Ramp	−	4.0	−	µs	49
$t_{UVLO\ OFF}$	UVLO Turn−Off Delay (Note 27)		−	4.0	−	µs	
t_{GP}	Time−to−Good Power (Note 28)	V_{DD} = 0 to 30 V in 10 µs Ramp	−	2.0	−	µs	28, 29, 49
| CM_H |	Common Mode Transient Immunity at Output High	T_A = 25°C, V_{CC} = 5 V, V_{DD} = 25 V, V_{SS} = Ground, C_F = 15 pF, R_F = 4.7 kΩ, V_{CM} = 1500 V_{PEAK} (Note 29)	35	50	−	kV/µs	51, 52
| CM_L |	Common Mode Transient Immunity at Output Low	T_A = 25°C, V_{CC} = 5 V, V_{DD} = 25 V, V_{SS} = Ground, C_F = 15 pF, R_F = 4.7 kΩ, V_{CM} = 1500 V_{PEAK} (Note 30)	35	50	−	kV/µs	50, 53

17. This load condition approximates the gate load of a 1200 V / 150 A IGBT.
18. Propagation delay t_{PHL} is measured from the 50% level on the falling edge of the input pulse to the 50% level of the falling edge of the V_O signal.
19. Propagation delay t_{PLH} is measured from the 50% level on the rising edge of the input pulse to the 50% level of the rising edge of the V_O signal.
20. PWD is defined as | t_{PHL} − t_{PLH} | for any given device.
21. The difference between t_{PHL} and t_{PLH} between any two parts under same operating conditions with equal loads.
22. The length of time the DESAT threshold must be exceeded before V_O begins to go LOW. This is supply voltage dependent.
23. The time from DESAT threshold is exceeded until the FAULT output goes LOW.
24. The length of time the DESAT threshold must be exceeded before V_O begins to go LOW and the FAULT output begins to go LOW.
25. The length of time from when RESET is initiated (via I_F turn−on) until FAULT output goes HIGH.
26. The UVLO turn−on delay, $t_{UVLO\ ON}$, is measured from the V_{UVLO+} threshold level of the rising edge of the output supply voltage (V_{DD}) to the 5 V level of the rising edge of the VO signal.
27. The UVLO turn−off delay, $t_{UVLO\ OFF}$, is measured from the $V_{UVLO−}$ threshold level of the falling edge of the output supply voltage (V_{DD}) to the 5 V level of the falling edge of the V_O signal.
28. The time to good power, t_{GP}, is measured from the V_{UVLO+} threshold level of the rising edge of the output supply voltage (V_{DD}) to the 5 V level of the rising edge of the V_O signal.
29. Common−mode transient immunity at output HIGH state is the maximum tolerable negative dVCM / dt on the trailing edge of the common−mode pulse, V_{CM}, to assure the output remains in HIGH state (i.e., V_O > 15 V or V_{FAULT} > 2 V).
30. Common−mode transient immunity at output LOW state is the maximum positive tolerable dVCM / dt on the leading edge of the common−mode pulse, V_{CM}, to ensure the output remains in LOW state (i.e., V_O < 1.0 V or V_{FAULT} < 0.8 V).

TIMING DIAGRAMS

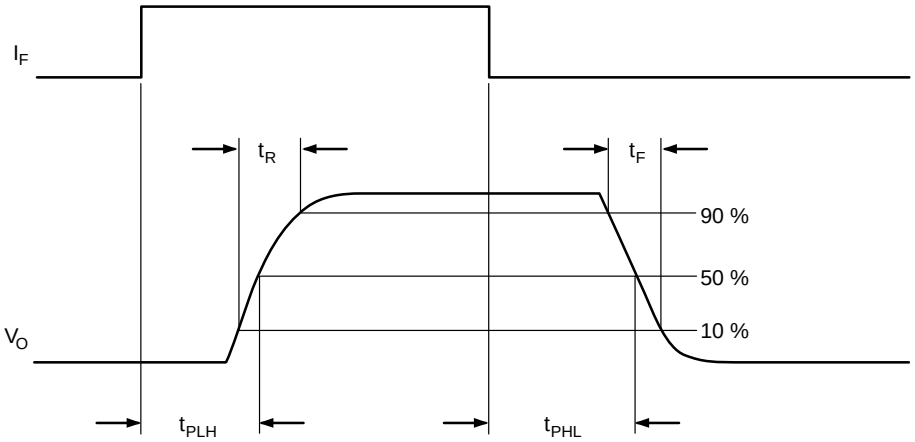

Figure 3. t_{PLH}, t_{PHL}, t_R, and t_F Timing Diagram

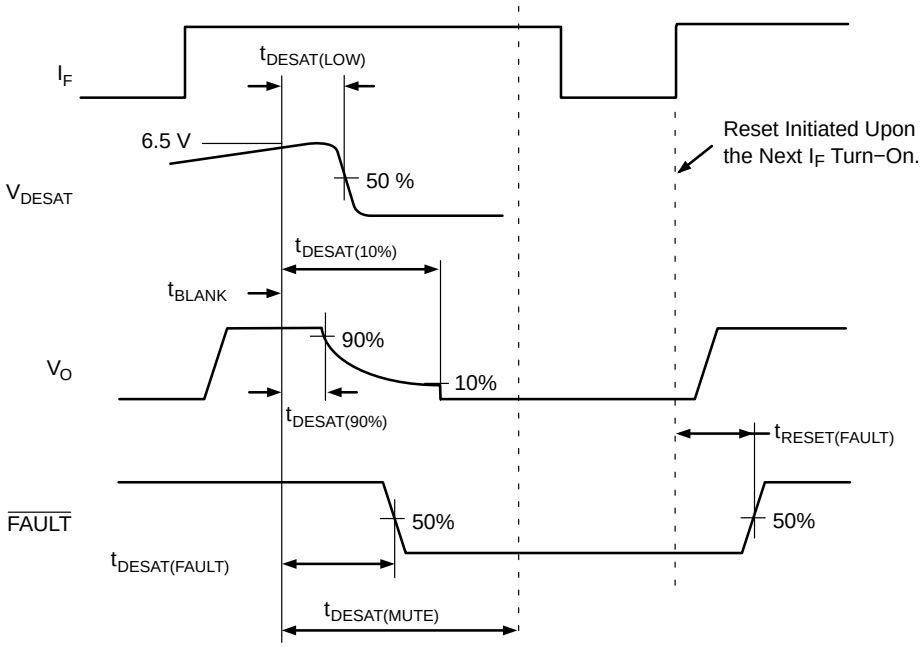

Figure 4. Definitions for DESAT, V_O and $\overline{FAULT}$ Timing Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

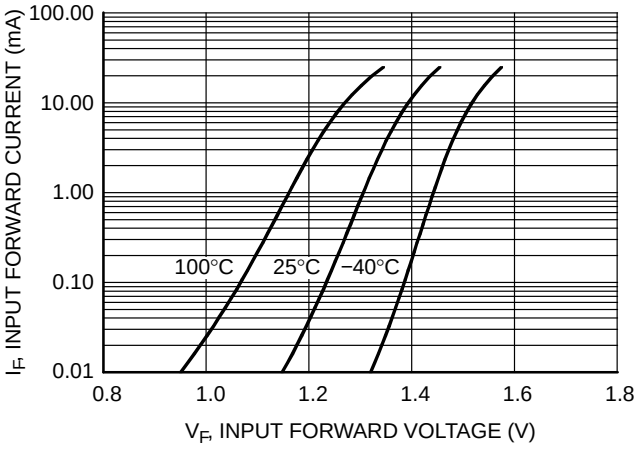

Figure 5. Input Forward Current (I_F) vs. Voltage (V_F)

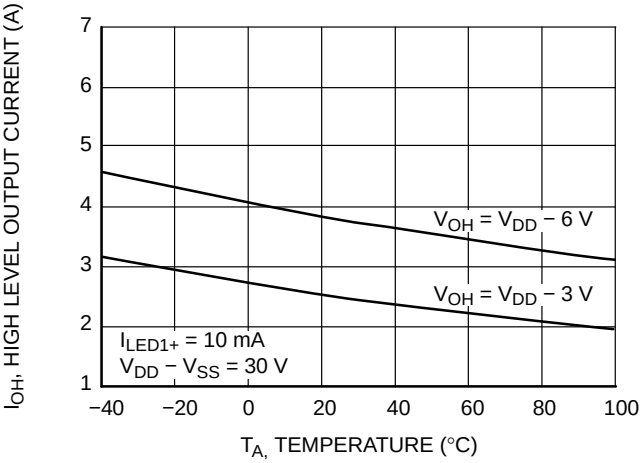

Figure 6. High Level Output Current (I_{OH}) vs. Temperature

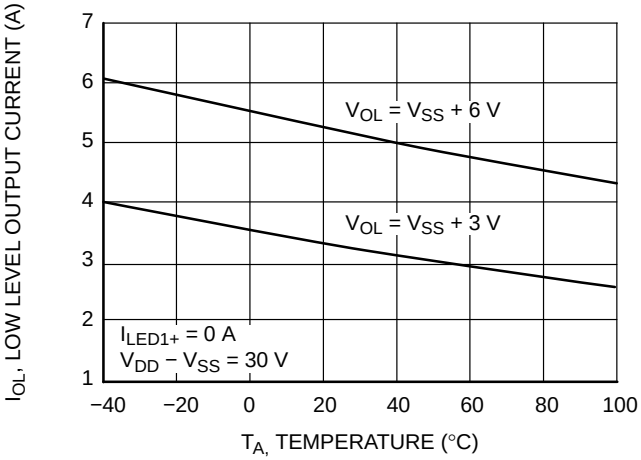

Figure 7. Low Level Output Current (I_{OL}) vs. Temperature

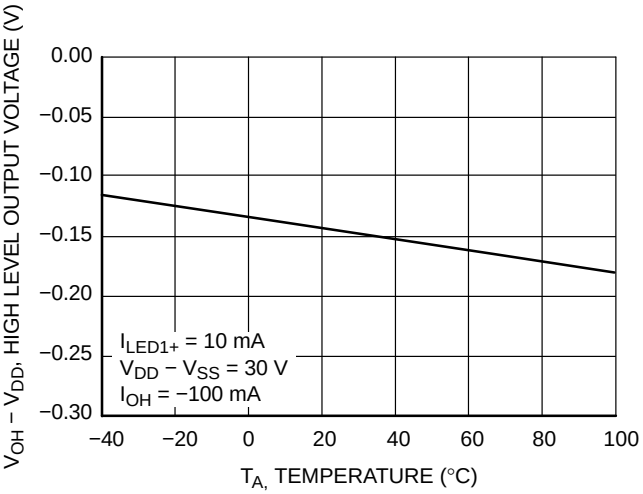

Figure 8. High Level Output Voltage ($V_{OH} - V_{DD}$) vs. Temperature

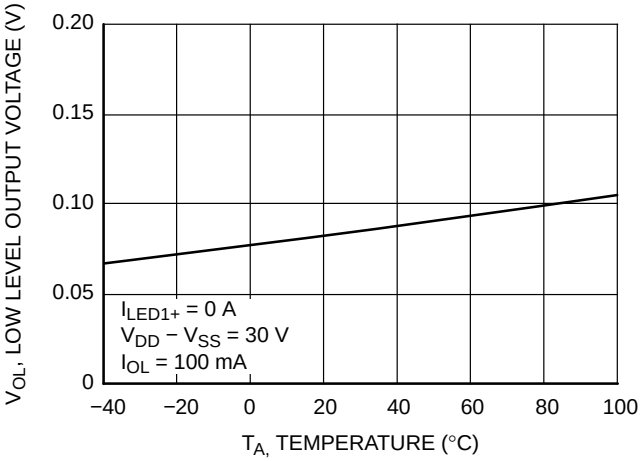

Figure 9. Low Level Output Voltage (V_{OL}) vs. Temperature

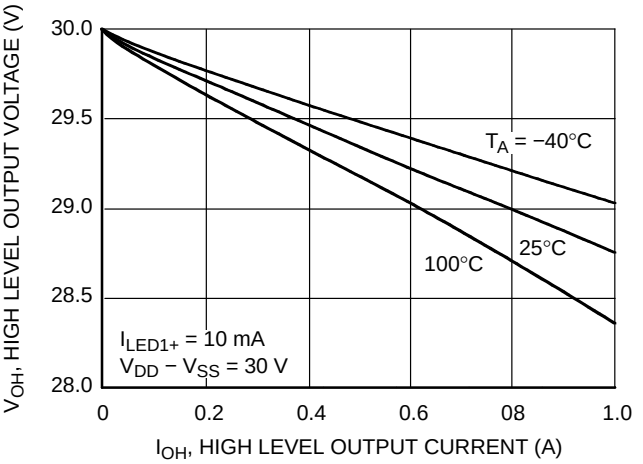

Figure 10. High Level Output Voltage (V_{OH}) vs. High Level Output Current (I_{OH})

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

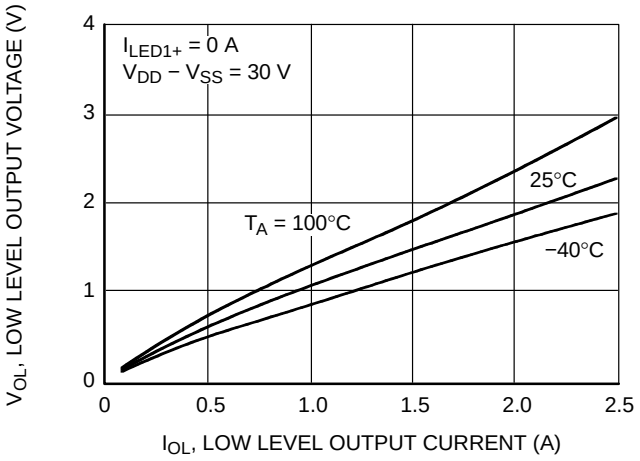

Figure 11. Low Level Output Voltage (V_{OL}) vs. Low Level Output Current (I_{OL})

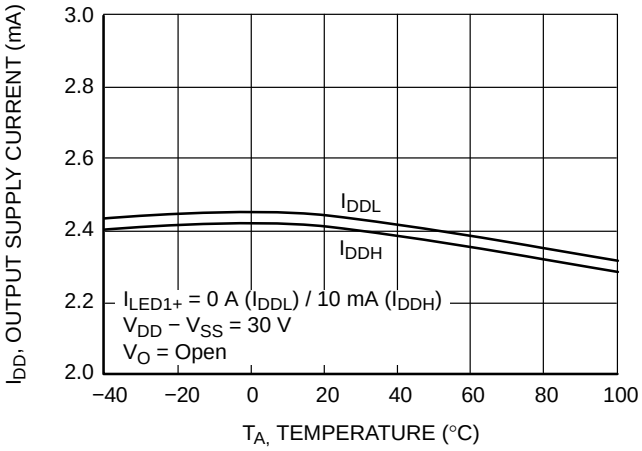

Figure 12. Output Supply Current (I_{DD}) vs. Temperature

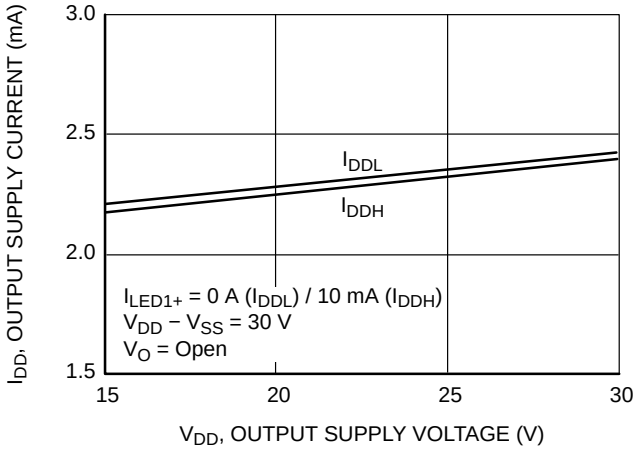

Figure 13. Output Supply Current (I_{DD}) vs. Voltage (V_{DD})

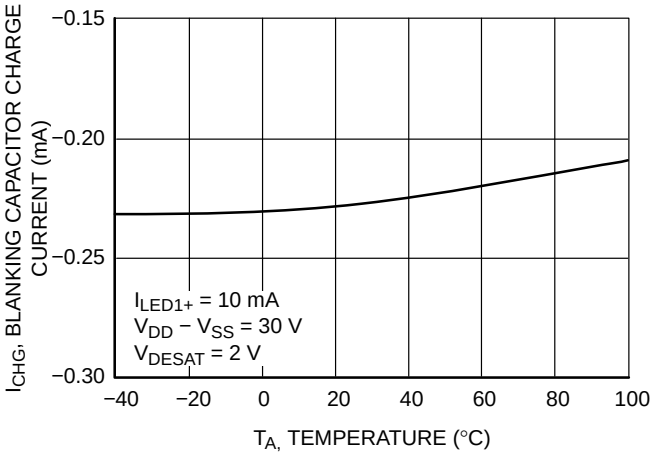

Figure 14. Blanking Capacitor Charge Current (I_{CHG}) vs. Temperature

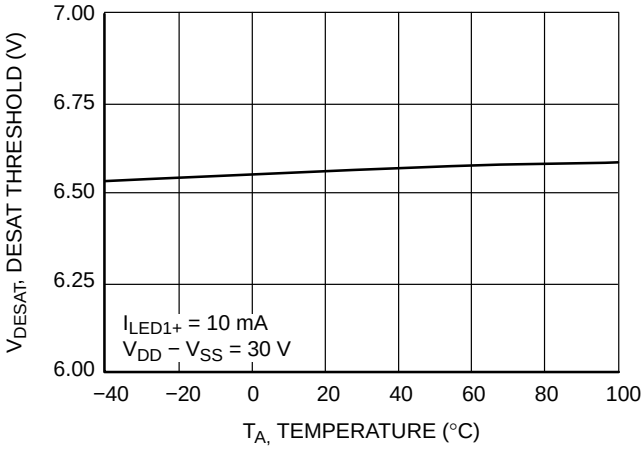

Figure 15. DESAT Threshold (V_{DESAT}) vs. Temperature

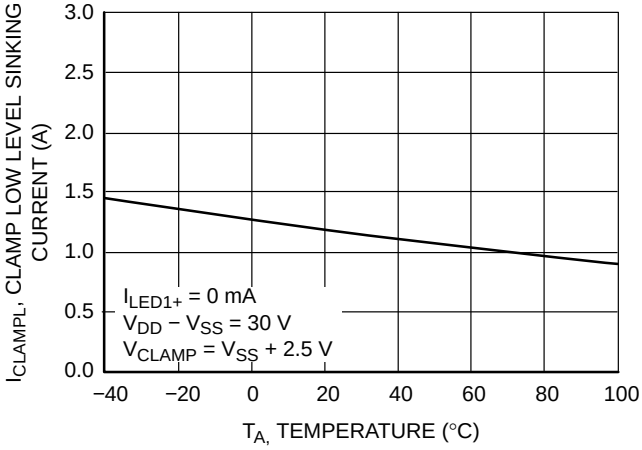

Figure 16. Clamp Low Level Sinking Current (I_{CLAMPL}) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

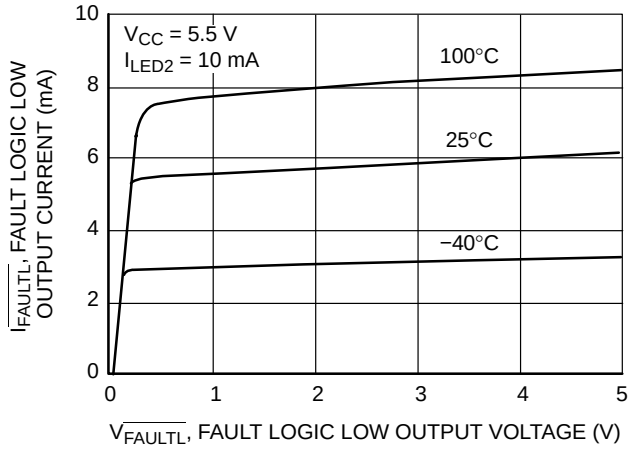

Figure 17. FAULT Logic Low Output Current ($I_{\overline{FAULTL}}$) vs. Voltage ($V_{\overline{FAULTL}}$)

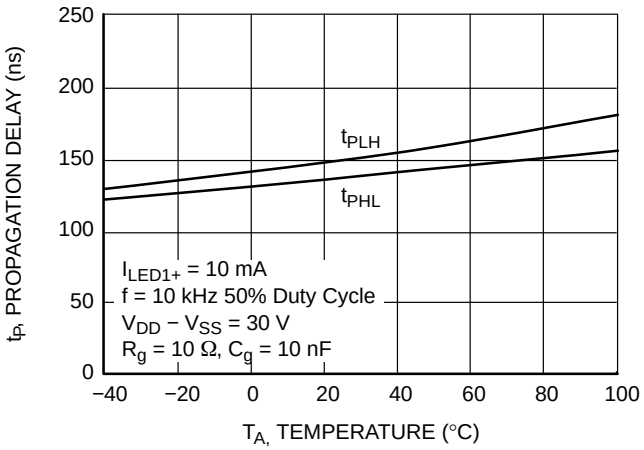

Figure 18. Propagation Delay (t_P) vs. Temperature

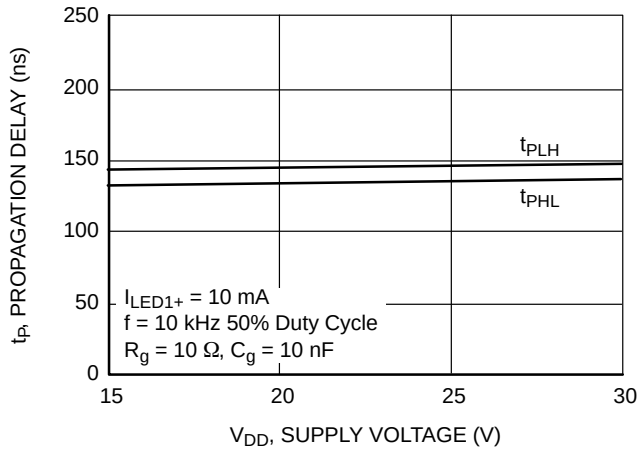

Figure 19. Propagation Delay (t_P) vs. Supply Voltage (V_{DD})

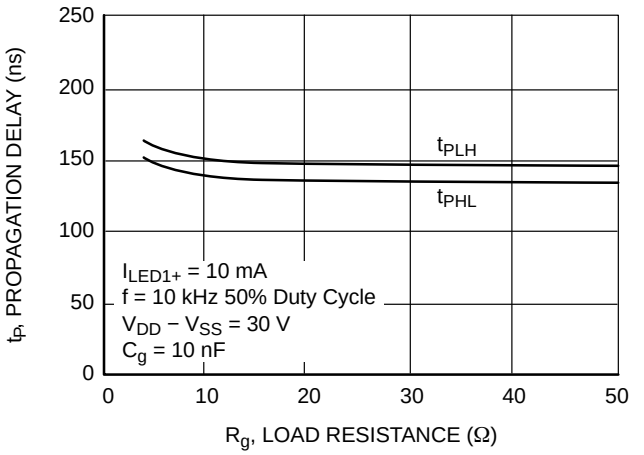

Figure 20. Propagation Delay (t_P) vs. Load Resistance (R_g)

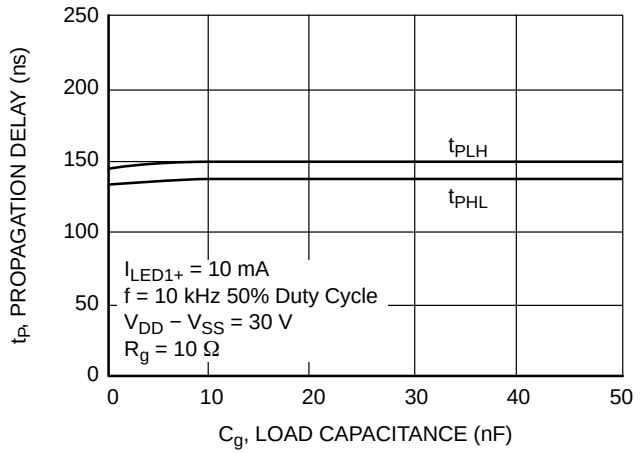

Figure 21. Propagation Delay (t_P) vs. Load Capacitance (C_g)

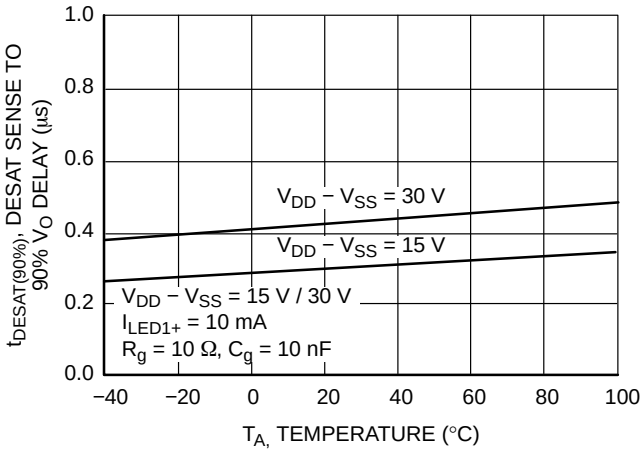

Figure 22. DESAT Sense to 90% V_O Delay ($t_{DESAT(90\%)}$) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

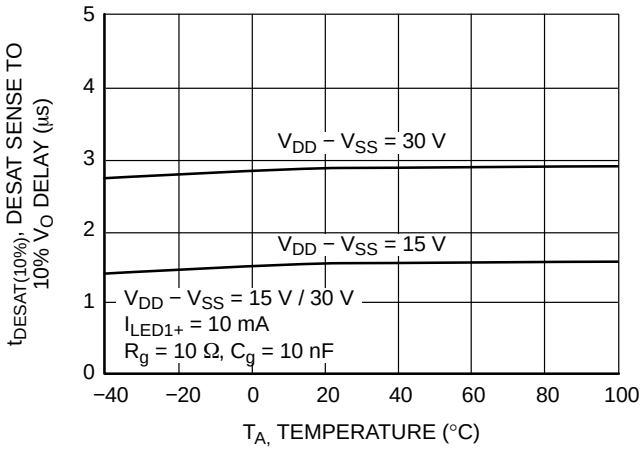

Figure 23. DESAT Sense to 10% V_O Delay ($t_{DESAT(10\%)}$) vs. Temperature

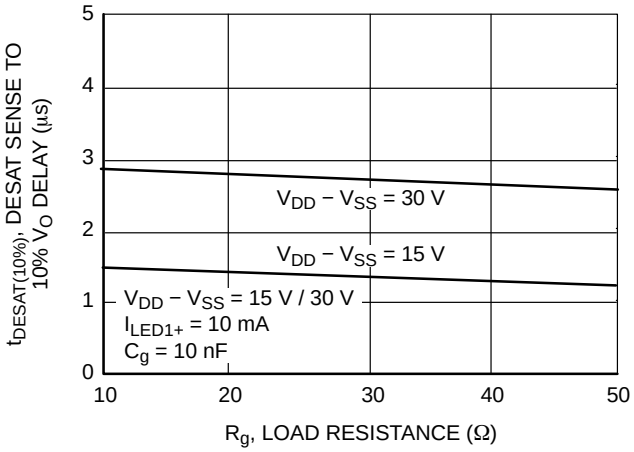

Figure 24. DESAT Sense to 10% V_O Delay ($t_{DESAT(10\%)}$) vs. Load Resistance (R_g)

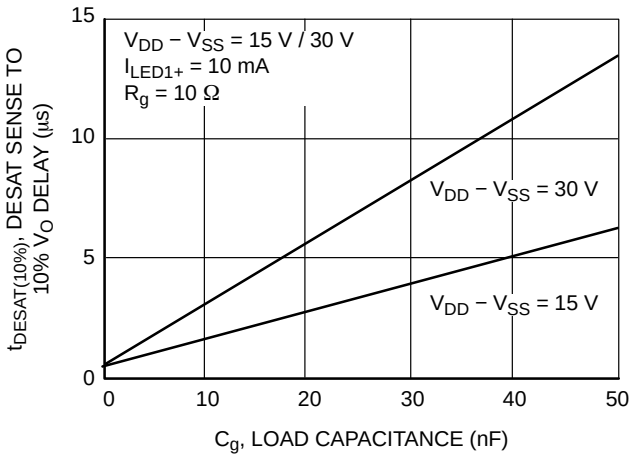

Figure 25. DESAT Sense to 10% V_O Delay ($t_{DESAT(10\%)}$) vs. Load Capacitance (C_g)

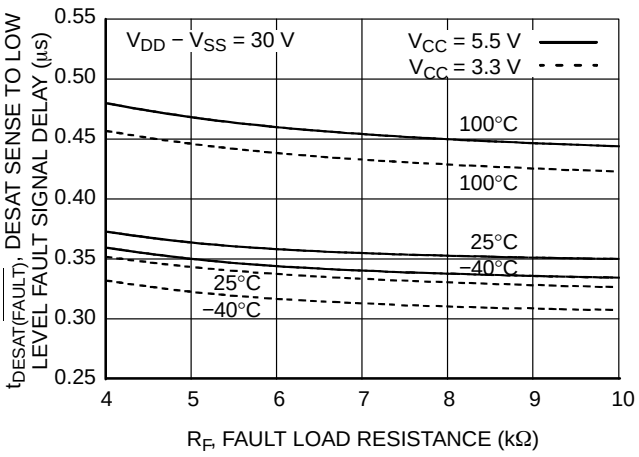

Figure 26. DESAT Sense to Low Level Fault Signal Delay ($t_{DESAT(\overline{FAULT})}$) vs. Fault Load Resistance (R_F)

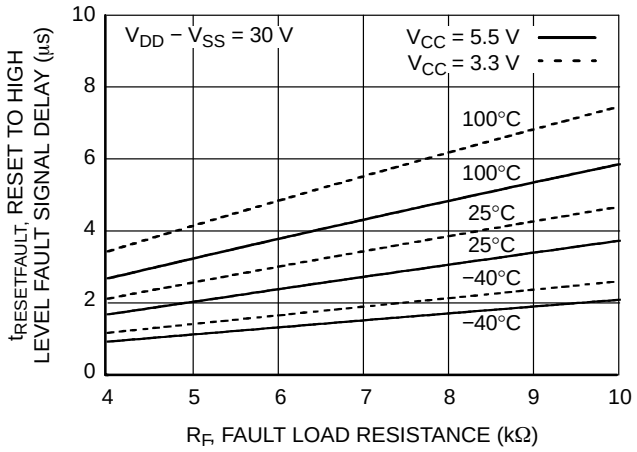

Figure 27. $\overline{\text{RESET}}$ to High Level Fault Signal Delay ($t_{RESET(\overline{FAULT})}$) vs. Fault Load Resistance (R_F)

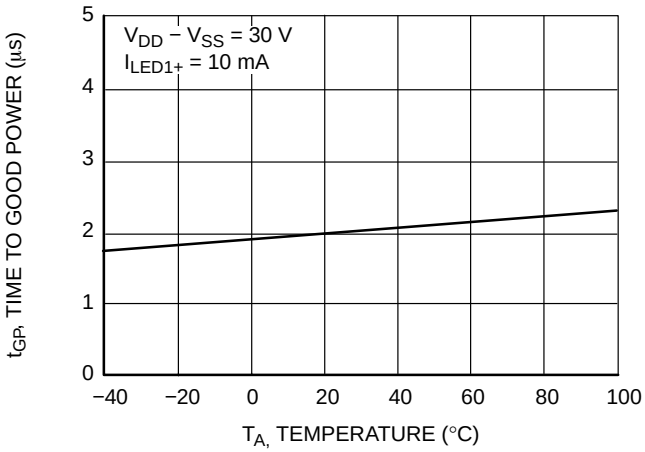

Figure 28. Time−to−Good Power (t_{GP}) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

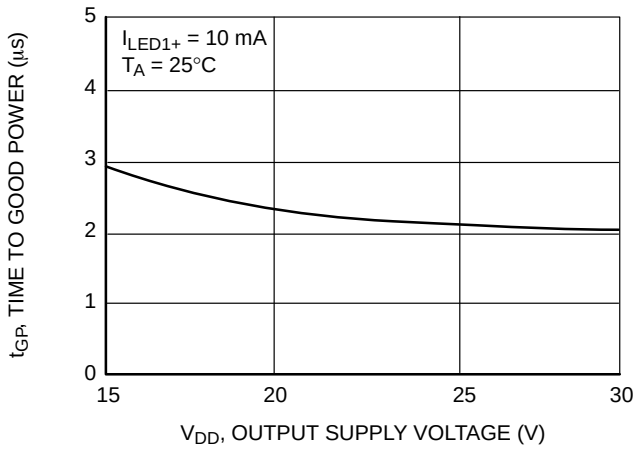

Figure 29. Time−to−Good Power (t_{GP}) vs. Output Supply Voltage (V_{DD})

TEST CIRCUITS

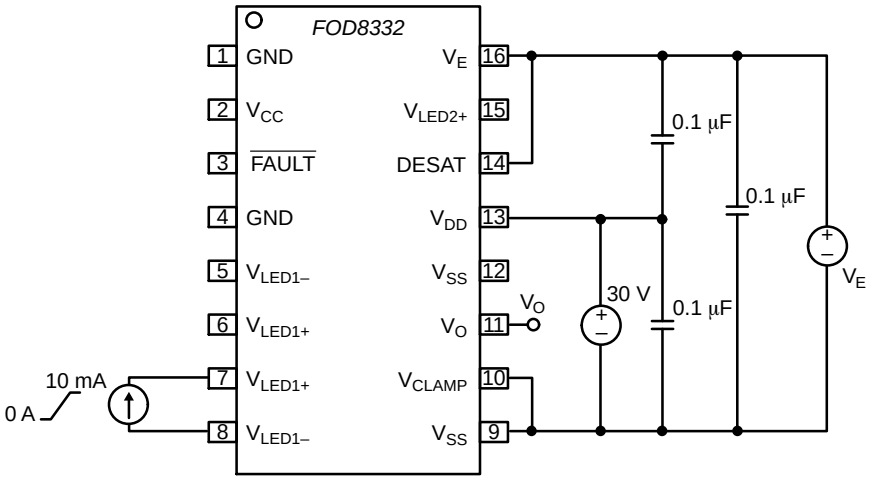

Figure 30. Threshold Input Current Low−to−High (I_{FLH}) Test Circuit

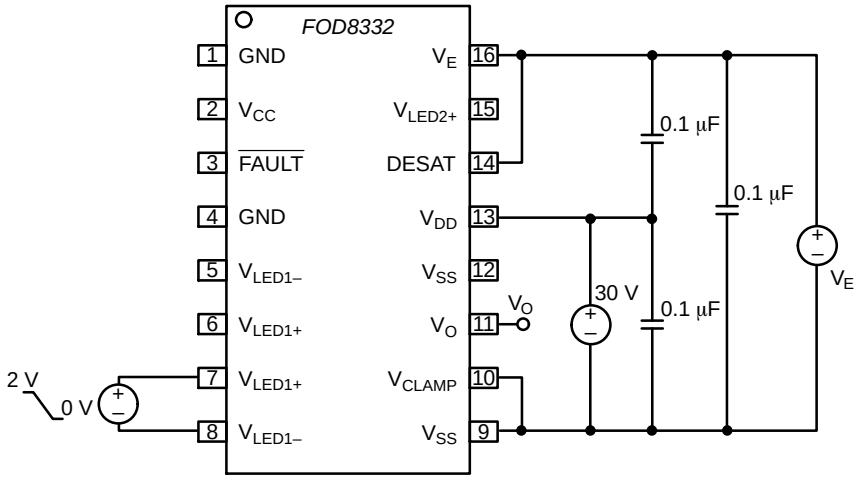

Figure 31. Threshold Input Voltage High−to−Low (V_{FHL}) Test Circuit

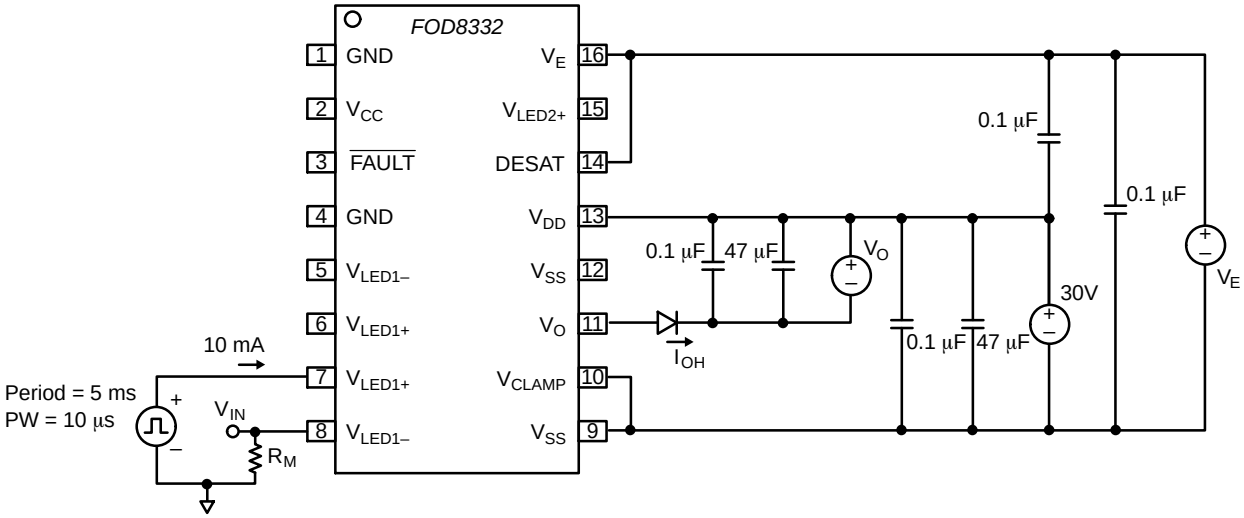

Figure 32. High Level Output Current (I_{OH}) Test Circuit

TEST CIRCUITS (continued)

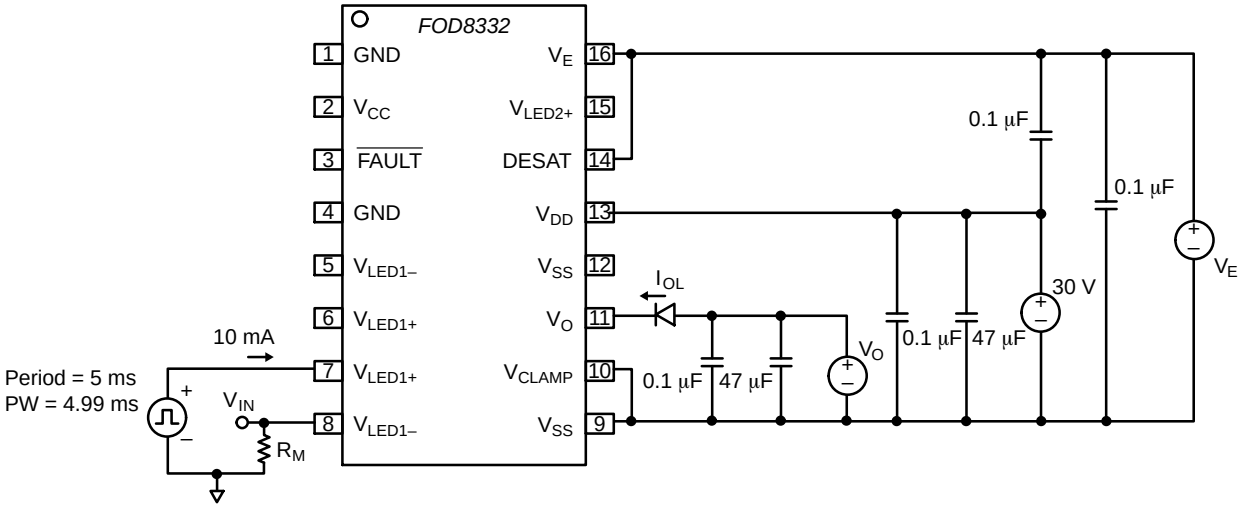

Figure 33. Low Level Output Current (I_{OL}) Test Circuit

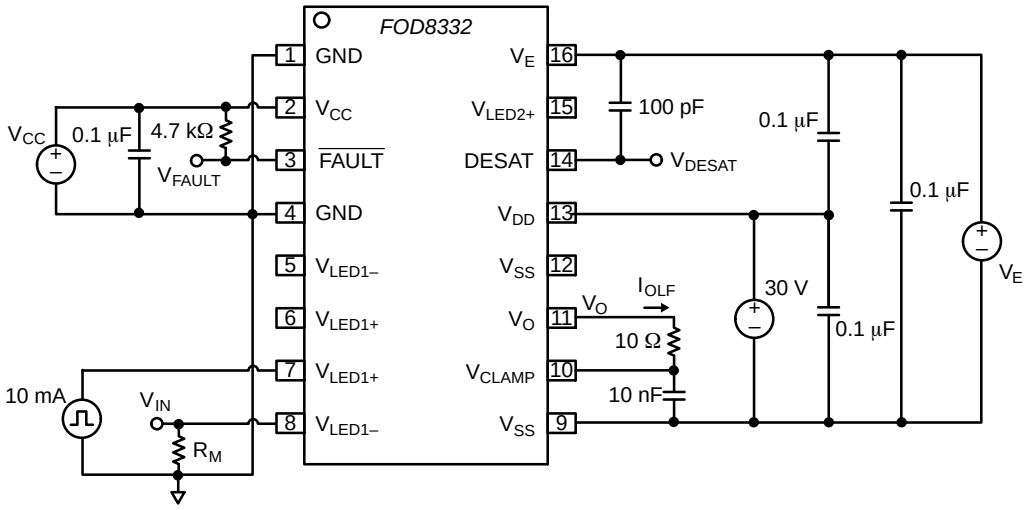

Figure 34. Low Level Output Current During Fault Condition (I_{OLF}) Test Circuit

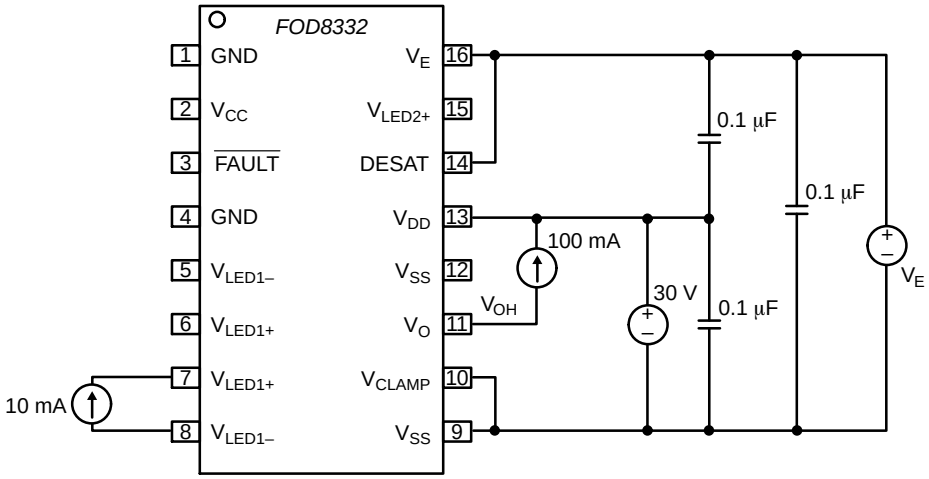

Figure 35. High Level Output Voltage (V_{OH}) Test Circuit

TEST CIRCUITS (continued)

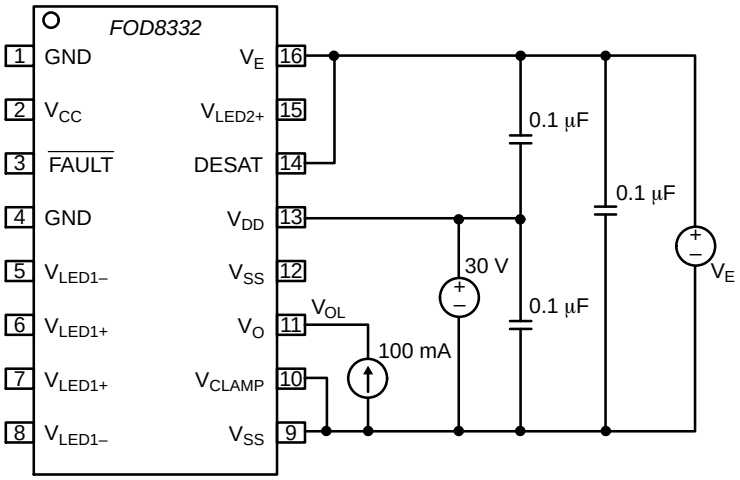

Figure 36. Low Level Output Voltage (V_{OL}) Test Circuit

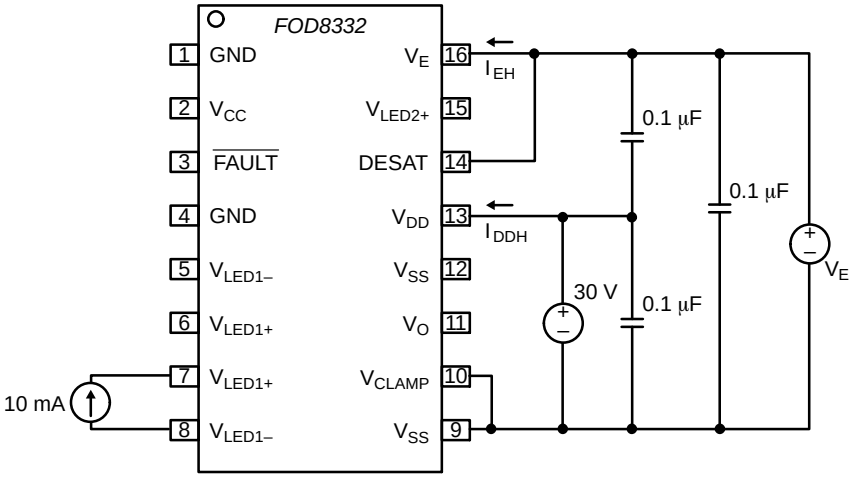

Figure 37. High Level Supply Current (I_{DDH}), VE High Level Supply Current (I_{EH}) Test Circuit

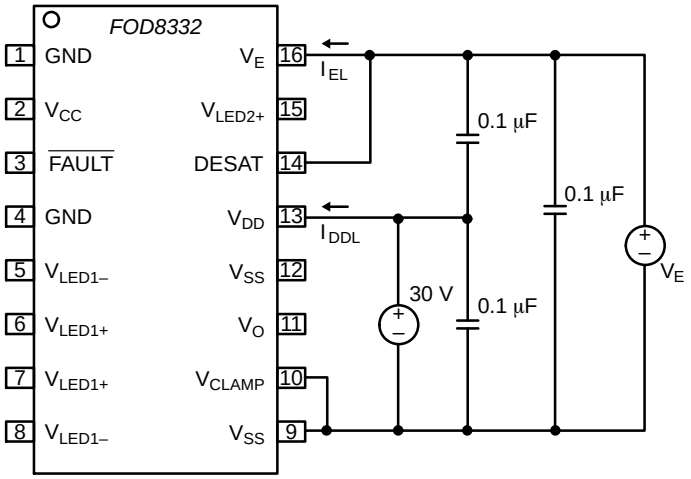

Figure 38. Low Level Supply Current (I_{DDL}), V_E Low Level Supply Current (I_{EL}) Test Circuit

TEST CIRCUITS (continued)

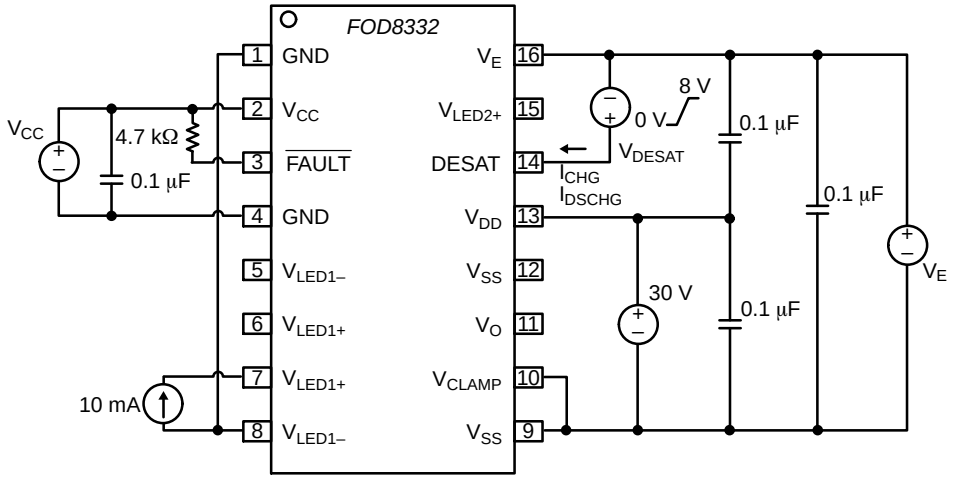

Figure 39. DESAT Threshold (V_{DESAT}), Blanking Capacitor Charge Current (I_{CHG}), Blanking Capacitor Discharge Current (I_{DSCHG}) Test Circuit

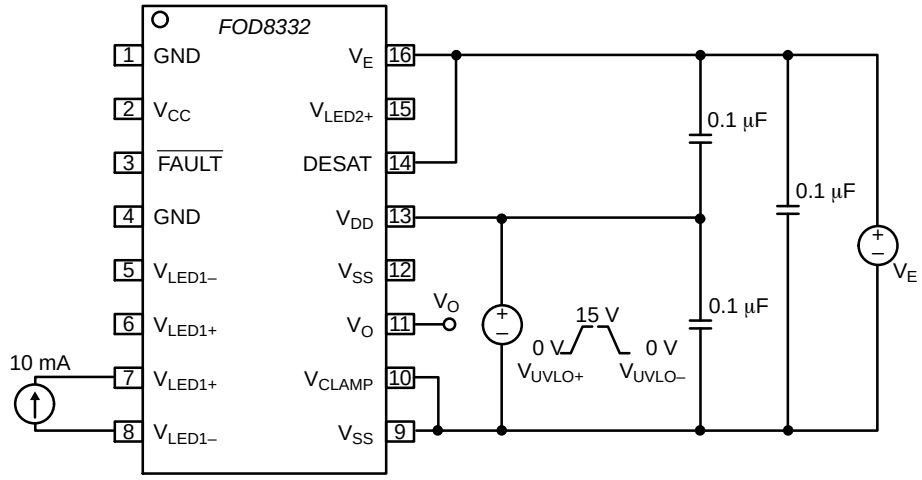

Figure 40. Under−Voltage Lockout Threshold (V_{UVLO+} / V_{UVLO-}), Under−Voltage Lockout Threshold Hysteresis ($UVLO_{HYS}$) Test Circuit

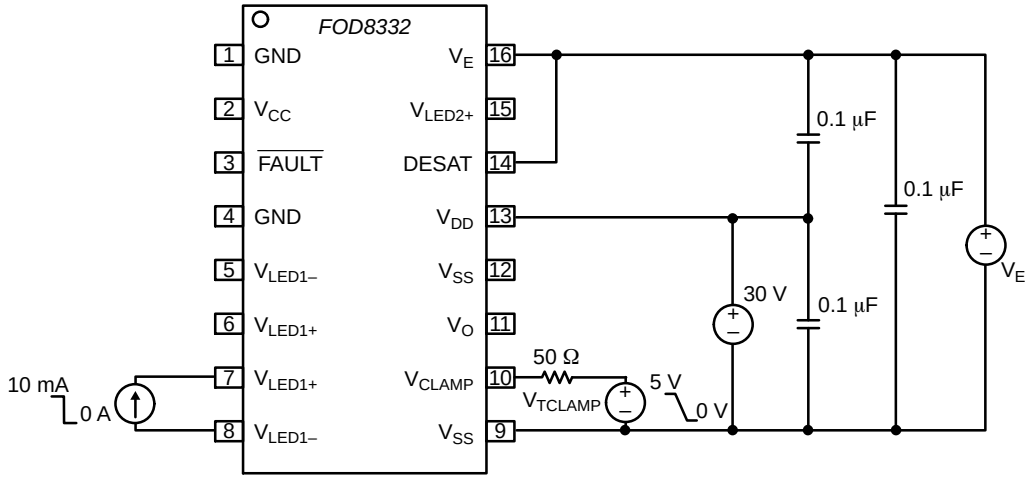

Figure 41. Clamping Threshold Voltage (V_{CLAMP_THRES}) Test Circuit

TEST CIRCUITS (continued)

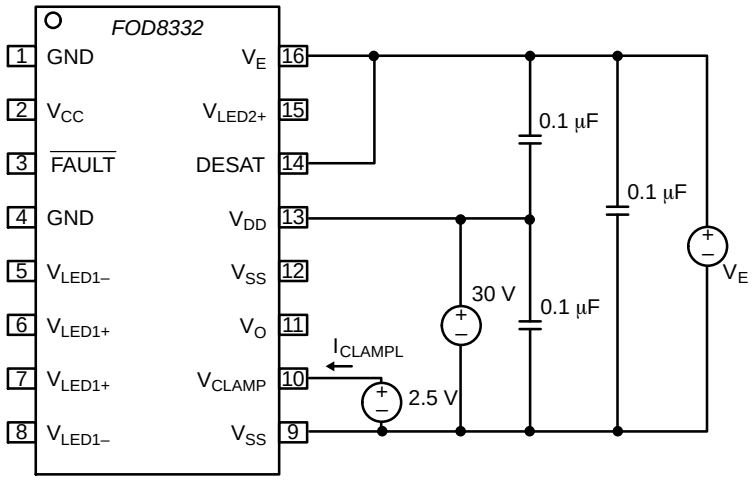

Figure 42. Clamp Low Level Sinking Current (I_{CLAMPL}) Test Circuit

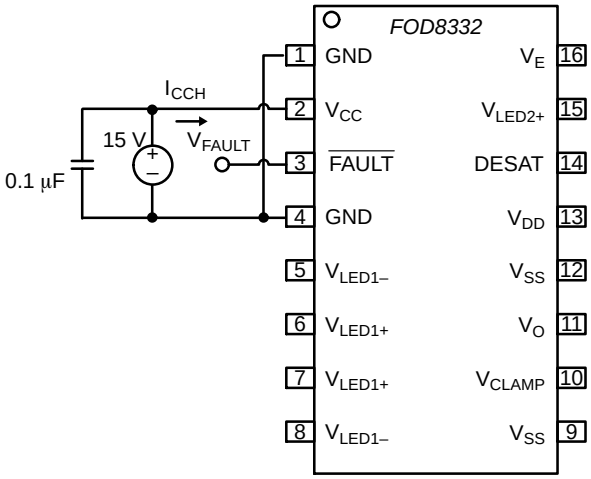

Figure 43. FAULT High Level Supply Current (I_{CCH}) Test Circuit

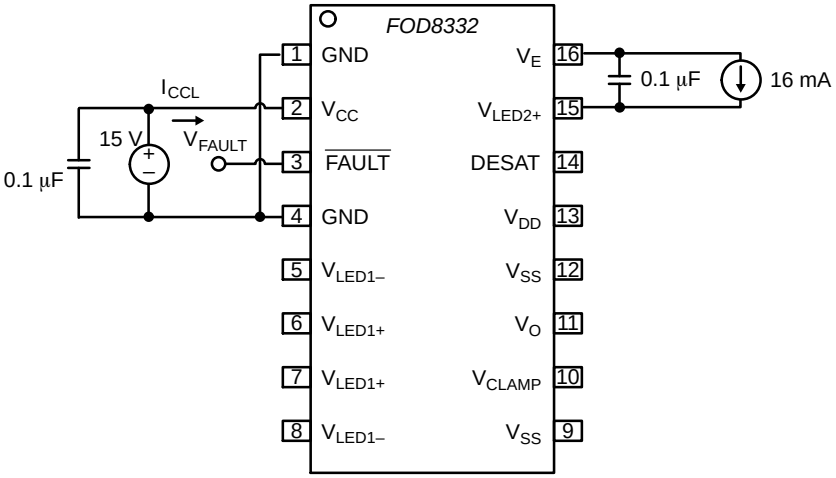

Figure 44. FAULT Low Level Supply Current (I_{CCL}) Test Circuit

TEST CIRCUITS (continued)

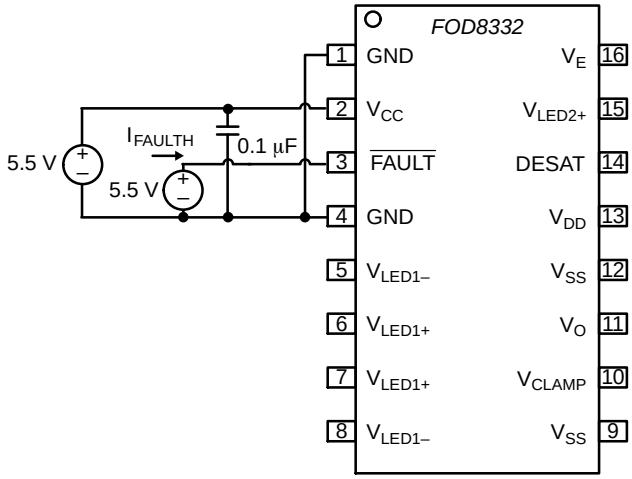

Figure 45. FAULT High Level Output Current ($I_{\overline{FAULTH}}$) Test Circuit

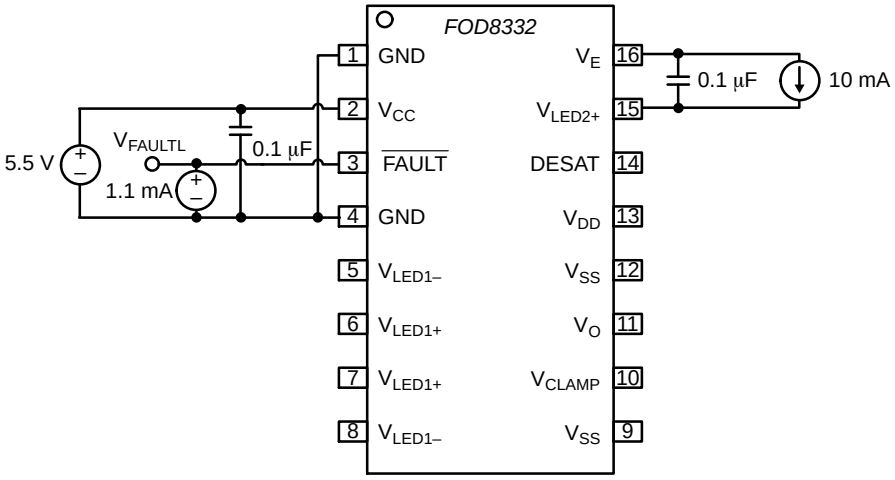

Figure 46. FAULT Low Level Output Voltage (V_{FAULTL}) Test Circuit

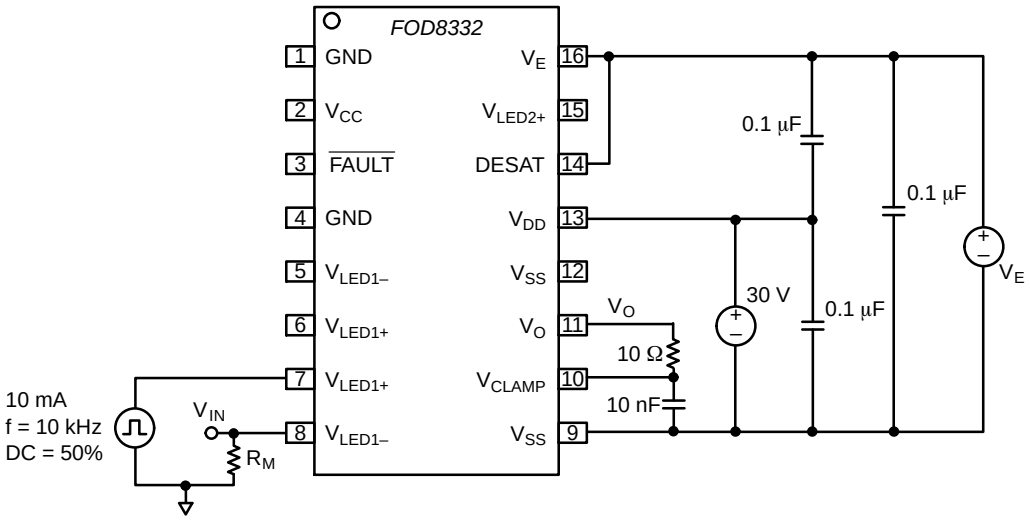

Figure 47. Propagation Delay (t_{PLH}, t_{PHL}), Rise Time (t_R), Fall Time (t_F), Pulse Width Distortion (PWD) Test Circuit

TEST CIRCUITS (continued)

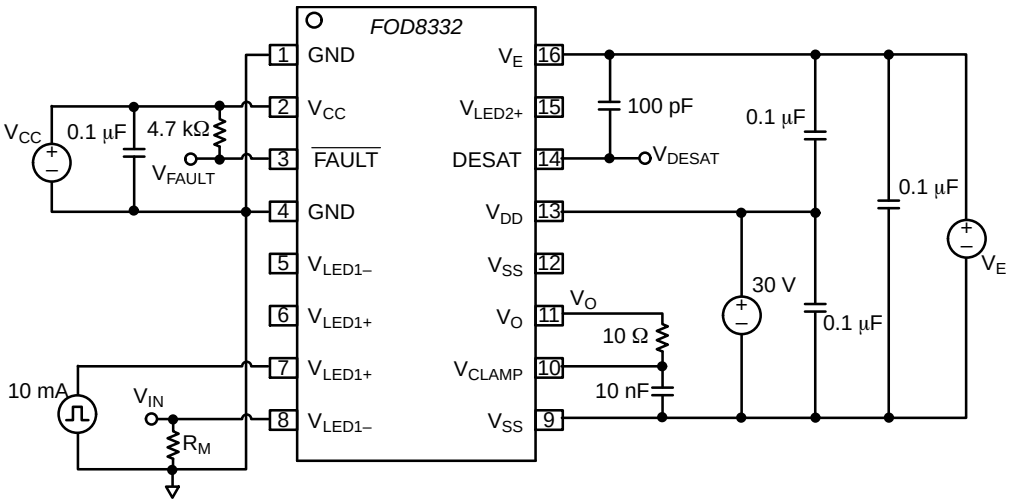

Figure 48. DESAT Sense Delay ($t_{DESAT(90\%)}$), $t_{DESAT(10\%)}$), $t_{DESAT(\overline{LOW})}$, DESAT Sense to Low Level FAULT Signal Delay ($t_{DESAT(\overline{FAULT})}$), Reset to High Level FAULT Signal Delay ($t_{RESET(\overline{FAULT})}$), DESAT Input Mute ($t_{DESAT(MUTE)}$) Test Circuit

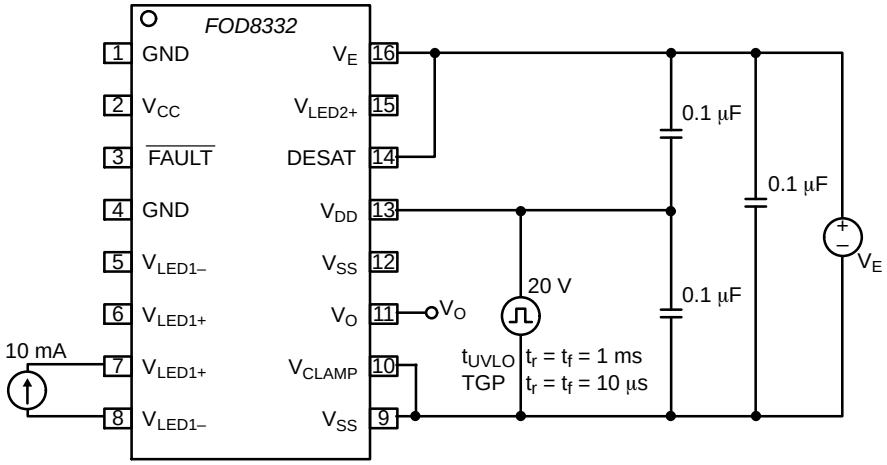

Figure 49. Under−Voltage Lockout Delay (t_{UVLO}), Time−to−Good−Power (t_{GP}) Test Circuit

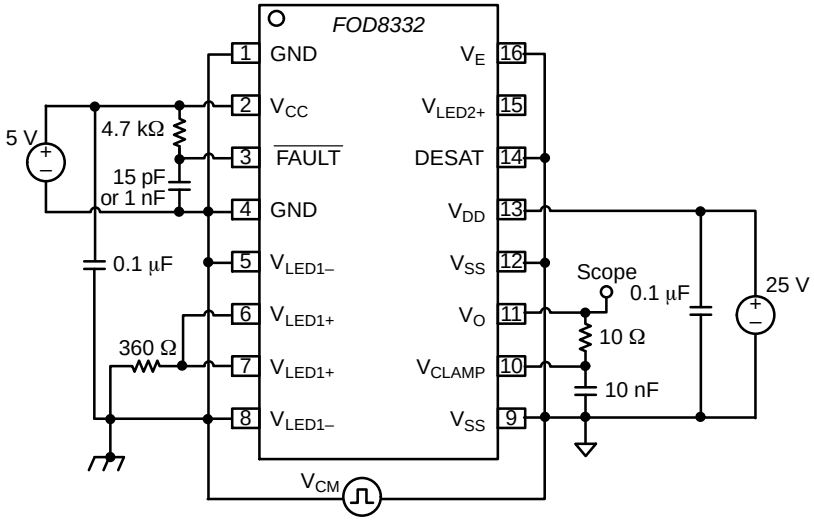

Figure 50. Common−Mode Low (CML) LED1−Off Test Circuit

TEST CIRCUITS (continued)

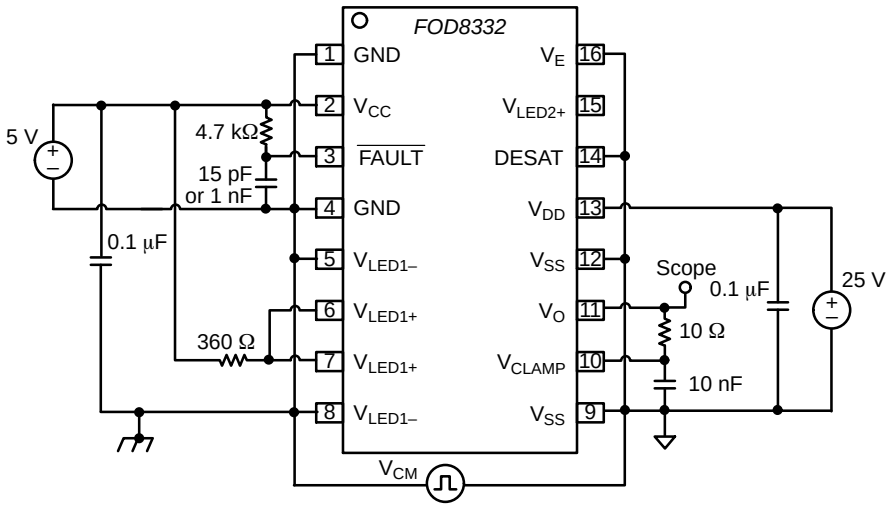

Figure 51. Common−Mode High (CMH) LED1−On Test Circuit

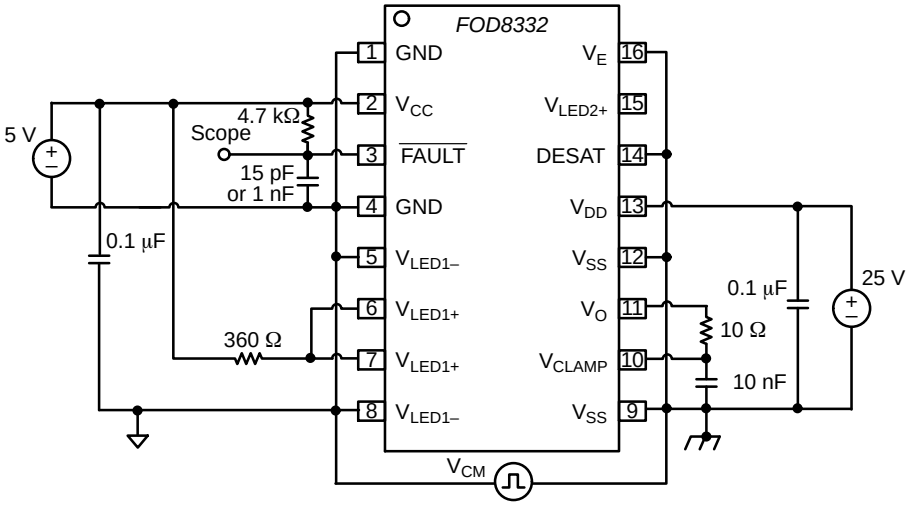

Figure 52. Common−Mode High (CMH) LED2−Off Test Circuit

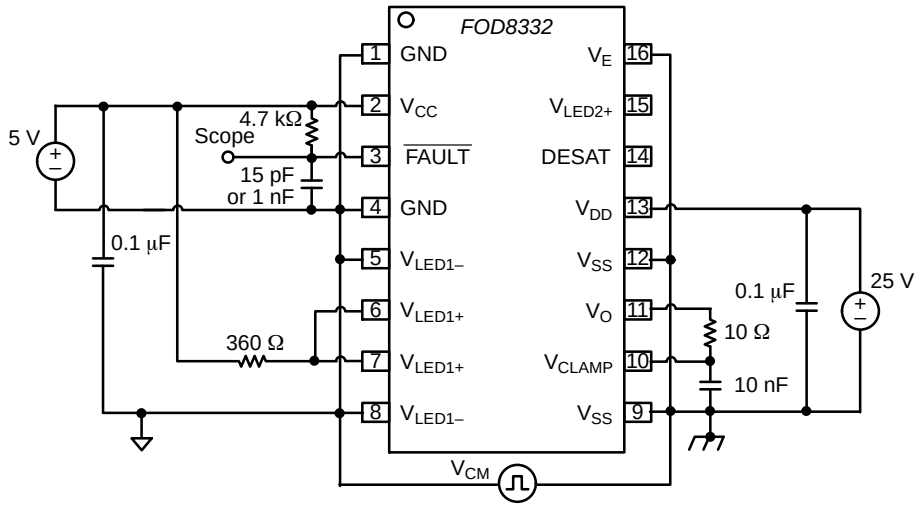

Figure 53. Common−Mode High (CML) LED2−On Test Circuit

APPLICATION INFORMATION

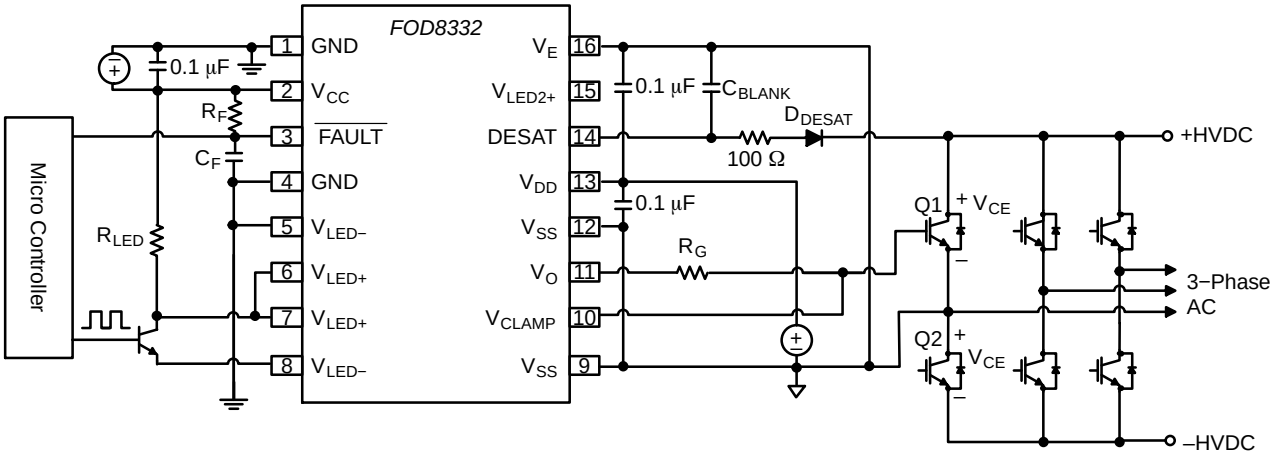

Figure 54. Recommended Application Circuit

Functional Description

The functional behavioral of FOD8332 is illustrated by the detailed internal schematic shown in Figure 55.

Figure 55 and the timing diagrams explain the interaction and sequence of internal and external signals.

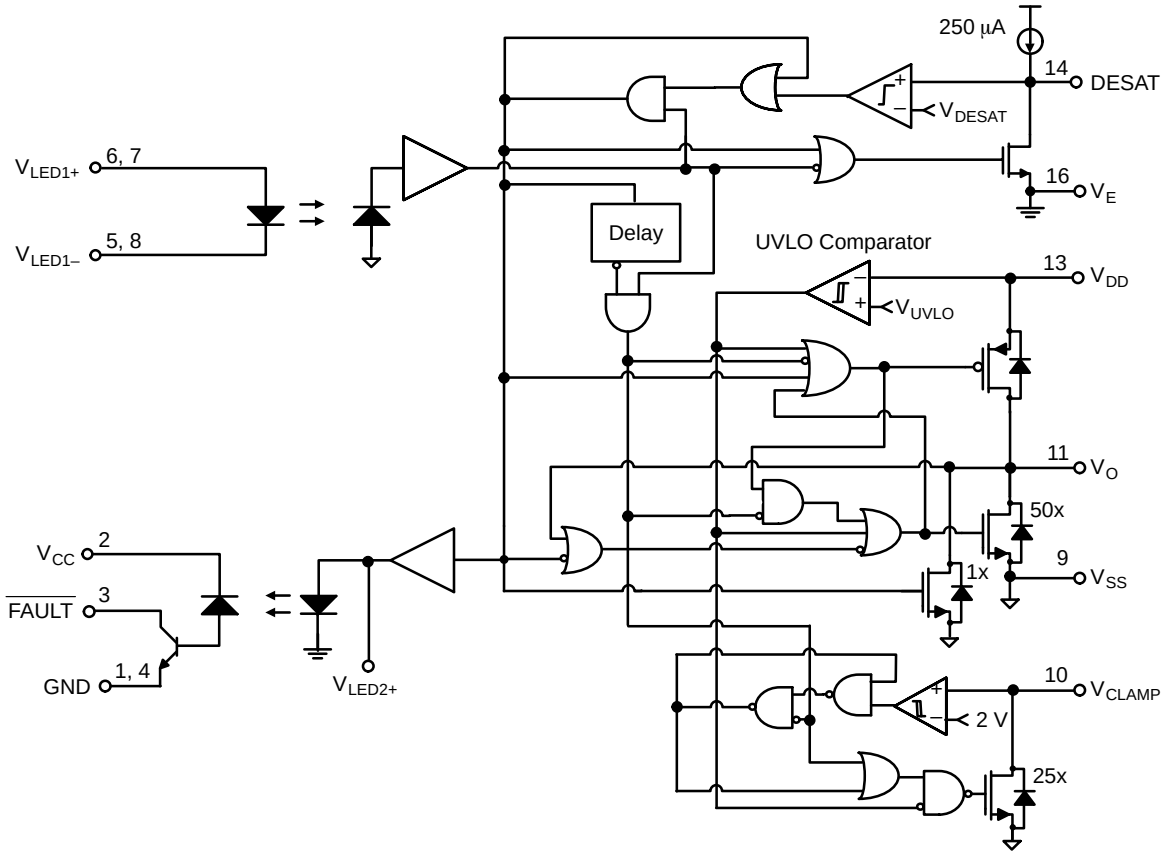

Figure 55. Detailed Internal Behavioral Schematic

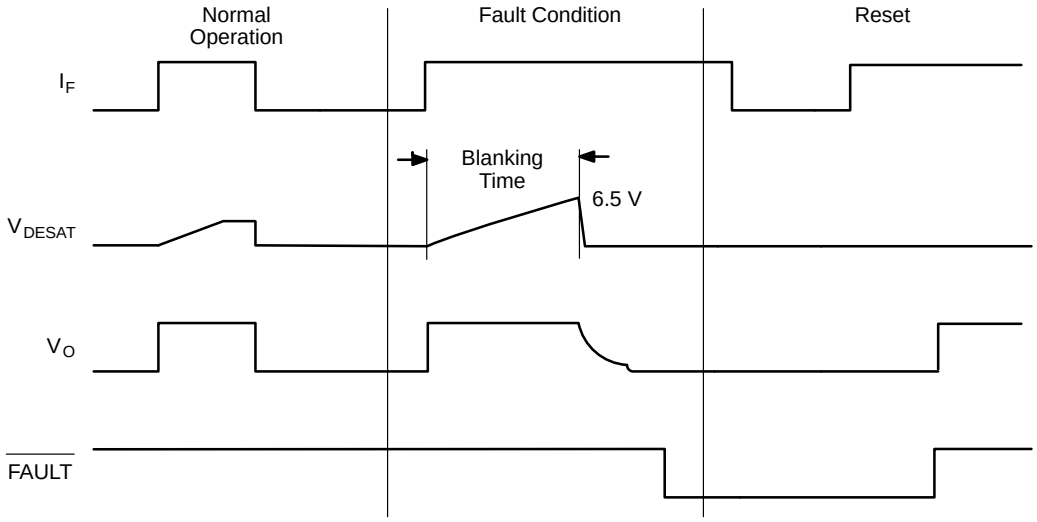

Figure 56. Operating Relationship Among Desaturation Voltage (DESAT), Fault Output (FAULT), and Reset Conditions

LED Input and Operation Explanation

FOD8332 is an advanced IGBT gate−drive optocoupler capable of driving most 1200 V / 150 A IGBTs and power MOSFETs in motor control and inverter applications. The following section describes driving IGBT, but is also applicable to driving MOSFET. Adjust the V_{DD} supply based on the gate threshold voltages. Critical protection features and controls are incorporated to simplify the design and improve reliability. The device includes an IGBT desaturation detection protection and a FAULT status output.

This highly integrated device consists of two high−performance AlGaAs LEDs and two integrated circuits. LED1 directly controls the isolated gate driver IC output, while the returned optical signal path is transmitted by LED2, which reports the fault status through the open−collector fault−sense IC output.

The control LED input and the fault−sense IC output can be connected to a standard 3.3 V / 5 V DSP or microcontroller. The gate driver output can be connected to the gate of the power devices on the high−voltage side. A typical recommended application is shown in Figure 54. A typical shunt LED drive can be used to improve noise immunity. The LED is connected in parallel with the bipolar transistor switch, creating a current shunt drive. Common−mode transients from the load coupling via the packa ge capacitance can be coupled into a low−impedance path, either the conducting LED or the on resistance of the conducting bipolar transistor, increasing its noise immunity.

During normal operation, when no fault is detected, LED1 controls the gate driver output. V_O is set to HIGH when the current flowing from the anode to the cathode (LED1) is greater than I_{FLH} and the forward voltage V_F is greater than V_F(MIN). The timing relationship between the LED input and gate driver output is illustrated in Figure 3. When a fault is detected, the gate driver ouptut IC immediately enters “soft” turn−off mode, where the output voltage changes slowly from HIGH to LOW state. This also disables the gate control input on the gate driver IC side for a minimum mute time of 10 μs.

The FAULT output, which is open−collector configuration, is latched to LOW state to report a fault status to the microcontroller. It is only reset or pulled back to HIGH when LED1 is pulled from LOW to HIGH again.

The active Miller clamp function avoids the need of negative gate driving in most applications and allows the use of a simple bootstrap supply for the high−side driver.

Gate Driver Output

A pair of PMOS and NMOS make up the output driver stage, which facilitates close to rail−to−rail output swing. This feature allows tight control of gate voltage during on−state and short−circuit conditions.

The output driver can typically sink 2.5 A and source 2.5 A at room temperature. Due to the low $R_{DS(ON)}$ of the MOSFETs, the power dissipation is lower than bipolar−type driver output stages. The absolute maximum rating of the output peak current, $I_{O(PEAK)}$, is 3 A. Careful selection of the gate resistor, R_G, is required to avoid violation of this rating. For charging and discharging, the R_G value is approximated by:

$$R_G = V_{CC} - V_{EE} - V_{OL} / I_{OL(PEAK)} \quad \text{(eq. 1)}$$

As shown in Figure 55, the gate driver output is influenced by signals from the photodetector circuitry, the UVLO comparator, and the DESAT signals. Under no−fault condition, normal operation resumes while the supply voltage is above the UVLO threshold and the output of the photodetector drives the MOSFETs of the output stage. The logic circuitry of the output stage ensures that the push−pull devices are never turned ON simultaneously. When the output of the photodetector is HIGH, output V_O is pulled to HIGH state by turning on the PMOS. When the output of the photodetector is LOW, V_O is pulled to LOW state by turning on the 50XNMOS.

When V_{DD} supply goes below V_{UVLO}, which is the designated ULVO threshold at the comparator, V_O is pulled to LOW state regardless of photodetector output.

When V_O is HIGH and desaturation is detected, V_O turns off slowly as it is pulled LOW by the 1XNMOS device. The input to the fault−sense circuitry is latched to HIGH state and turns on the LED2. The fault−sense signal remains in HIGH state until LED1 is switched from LOW to HIGH. When V_O goes below 2 V, the 50XNMOS device turns on, clamping the IGBT gate firmly to V_{SS}.

Desaturation Protection, FAULT Output and FAULT RESET

Desaturation detection protects the IGBT in short circuit by monitoring the collector−emitter voltage of the IGBT when it's turned on. When the DESAT pin voltage goes above the threshold voltage, a short−circuit condition is detected and the driver output stage executes a "soft" IGBT turn−off and is eventually driven LOW. This sequence is illustrated in Figure 56. The FAULT open−collector output is triggered active LOW to report a desaturation error. The gate driver output is muted for minimum of 10 μs. All input LED signals are ignored during the mute period to allow the driver to completely soft shutdown the IGBT. The fault mechanism is reset by the next LED turn−on after the $t_{RESET(\overline{FAULT})}$ (see Figure 56). During OFF state of the IGBT, or if V_O is LOW, the fault sense circuitry is disabled to prevent false fault signals.

The DESAT comparator should be disabled for a short tme period (blanking time) before the IGBT turns on to allow the collector voltage to fall below the DESAT threshold.

This blanking period protects against false triggering of the DESAT while the IGBT is turning on. The blanking time is controlled by the internal DESAT charge current, the DESAT voltage threshold, and the external DESAT capacitor (capacitor between DESAT and V_E pin). The nominal blanking time can be calculated using external capacitance (C_{BLANK}), FAULT threshold voltage (V_{DESAT}), and DESAT charge current (I_{CHG}):

$$t_{BLANK} = C_{BLANK} \times V_{DESAT} / I_{CHG} \quad \text{(eq. 2)}$$

With a recommended 100 pF DESAT capacitor, the nominal blanking time is:

$$100\ pF \times 6.5\ V / 205\ \mu A = 2.6\ \mu s$$

Soft Turn−Off

The soft turn−off feature ensures the safe shutdown of the IGBT under fault condition. The gate−driver voltage V_O turns off the IGBT in a controlled slow manner. This reduces the voltage spike on the collector of the IGBT. Without this, the IGBT would see a heavy spike on the collector, resulting in a permanent damage to the device when it's turned off immediately. The V_O is pulled to LOW slowly in 4 μs.

Under−Voltage Lockout (UVLO)

Under−Voltage detection prevents the application of insufficient gate voltage to the IGBT. This could be dangerous, as it would drive the IGBT out of saturation and into the linear operation where losses are very high and the IGBT quickly overheats. This feature ensures proper operation of the IGBTs. The output voltage, V_O, remains LOW irregardless of the inputs, as long as the supply voltage, $V_{DD} - V_E$, is less than V_{UVLO+} during power up. When the supply voltage falls below $V_{UVLO−}$, V_O goes LOW, as illustrated in Figure 57.

Active Miller Clamp Function

An active Miller clamp feature allows the sinking of the Miller current to ground during a high−dV/dt situation. Instead of driving the IGBT gate to a negative supply voltage to increase the safety margin, the device has a dedicated V_{CLAMP} pin to control the Miller current. During turn−off, the gate voltage of the IGBT is monitored and the V_{CLAMP} output is activated when the gate voltage goes below 2 V (relative to V_{SS}).

The Miller clamp NMOS transistor is then turned on and provides a low resistive path for the Miller current, which helps prevent a self−turn−on due to the parasitic Miller capacitor in power switches. The clamp voltage is V_{SS} + 2.5 V, typical for a Miller current up to 1100 mA.

In this way, the V_{CLAMP} function does not affect the turn−off characteristic. It helps to clamp the gate to the low level throughout the turn−off time. During turn−on, where the input of the driver is activated, the V_{CLAMP} function is disabled or opened.

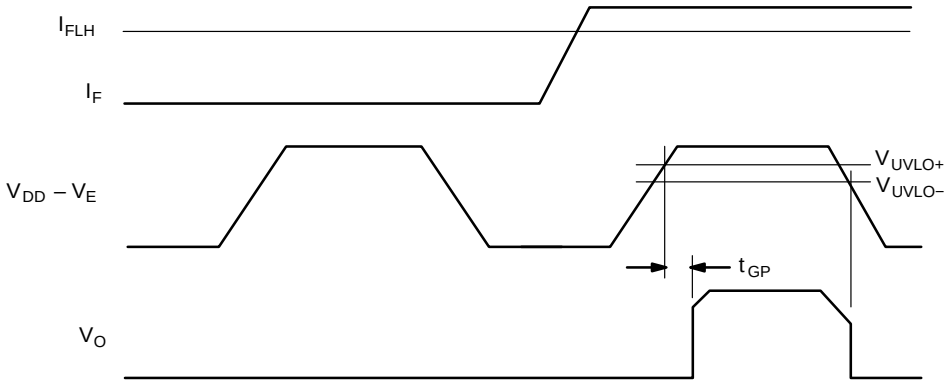

Figure 57. Time to Good Power

Time to Good Power

During fast power up (e.g. bootstrap power supply), the LED is off and the output of the gate driver should be in the LOW or OFF state. Sometimes, race conditions exist that cause the output to follow V_{DD} until all of the circuits in the output IC stabilize. This condition can result in output transitions or transients that are coupled to the driven IGBT. These glitches can cause the high− and low−side IGBTs to conduct shoot−through current that can damage the power semiconductor devices.

onsemi has introduced a initial turn−on delay, called "time to good power." This delay, typically 2.0 μs, is only present during the initial power−up of the device. If the LED is ON during the initial turn−on activation, low−to−high transition at the output of the gate driver only occurs 2.0 μs after the V_{DD} power is applied.

Dual Supply Operation − Negative Bias at V_{SS}

The IGBT's off−state noise immunity can be enhanced by providing a negative gate−to−emitter bias when the IGBT is in OFF state. This static off−state bias can be supplied by connecting a separate negative voltage source between the V_E (pin 16) and V_{SS} (pin 9 and pin 12). The primary ground reference is the IGBT's emitter connection, V_E (pin 16). The under−voltage lockout threshold and desaturation voltage detection are referenced to the IGBT's emitter (V_E) ground.

The negative voltage supply at V_{SS} appears at the gate drive output, V_O, when in LOW state. When the input drives the output HIGH, the output voltage, V_O, has the potential of the V_{DD} and V_{SS}. Proper power supply bypass capacitors are added to provide paths for the instantaneous gate charging and discharging currents. The Schottky diode is recommended connected between V_E and V_{SS} to protect against a reverse voltage greater than 0.5 V. The V_{CLAMP} (pin 10) should be connected to V_{SS} when not in use.

DESAT Pin Protection

During turn off, especially with inductive load, a large instantaneous forward−voltage transient can appear on the freewheeling diode of the IGBT. A large negative voltage spike on the DESAT pin can result and draw substantial current out of the gate driver IC if there is not current−limiting resistor. To limit this current, a 100 Ω to 1 kΩ resistor should be inserted in series with the DESAT diode. The added resistance does not change the DESAT threshold or the DESAT blanking time.

The DESAT diode protects the gate driver IC from high voltages when the IGBT is turning off, while allowing a forward I_{CHG} current of 250 μA to be conducted to sense the IGBT's saturated collector to emitter voltage when the IGBT is turned on. A fast−recovery diode, t_{rr} below 75 ns, with sufficient reverse−voltage rating, should be used. **onsemi** offers many of these ultra−fast diodes/rectifiers, such as ES1J−600V, with t_{rr} at 35 ns.

If two diodes or more are used, the required maximum reverse voltage can be reduced by half or accordingly. This modifies the trigger level for a fault condition. The sum of the DESAT diode forward−voltage and the IGBT collector−emitter V_{CE} voltage form the voltage at the DESAT pin. The trigger level for a fault condition given by:

$$V_{CE@FAULT} = V_{DESAT} - n \times V_F \quad \text{(eq. 3)}$$

where n is the number of the DESAT diodes.

Pull−Up Resistor on FAULT Pin

The FAULT pin is an open−collector output and can be connected as wire−OR operation with other types of protection (e.g., over−temperature, over−voltage, over−current) to alert the microcontroller. Being an open−collector output, it requires a pull−up resistor to provide a normal high output voltage level. This resistor value must be properly considered based on various IC interface requirements. The sinking current capability is given by $I_{\overline{FAULTL}}$.

Increasing the Output Drive Current Using an External Booster Stage

If larger gate drive capability is needed for large IGBT modules or parallel operation, an output booster stage may be added to driver for optimum performance.

A possible implementation is by a discrete NPN/PNP totem−pole configuration. These booster transistors should be fast switching and have sufficient current gain to deliver the desired peak output current.

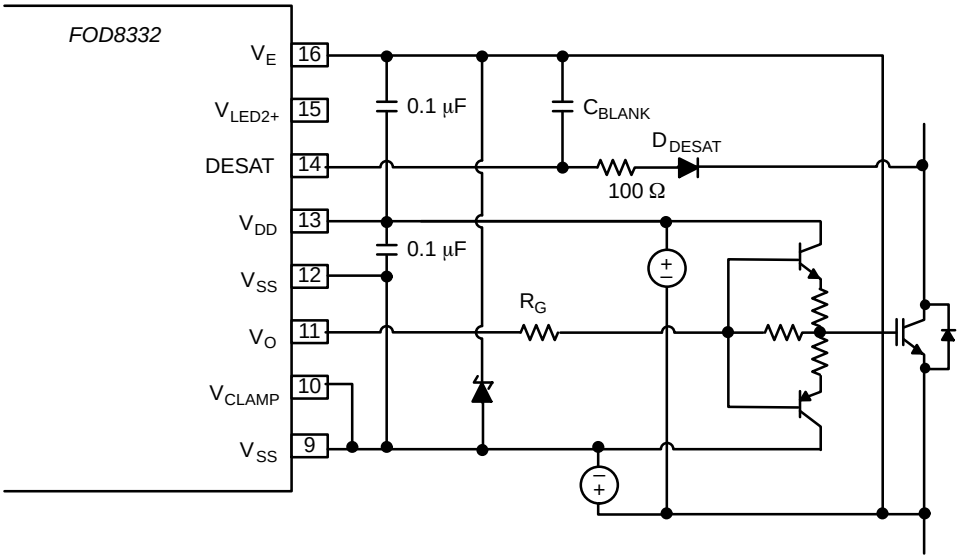

Figure 58. Output Booster Stage for Increased Output Drive Current

REFLOW PROFILE

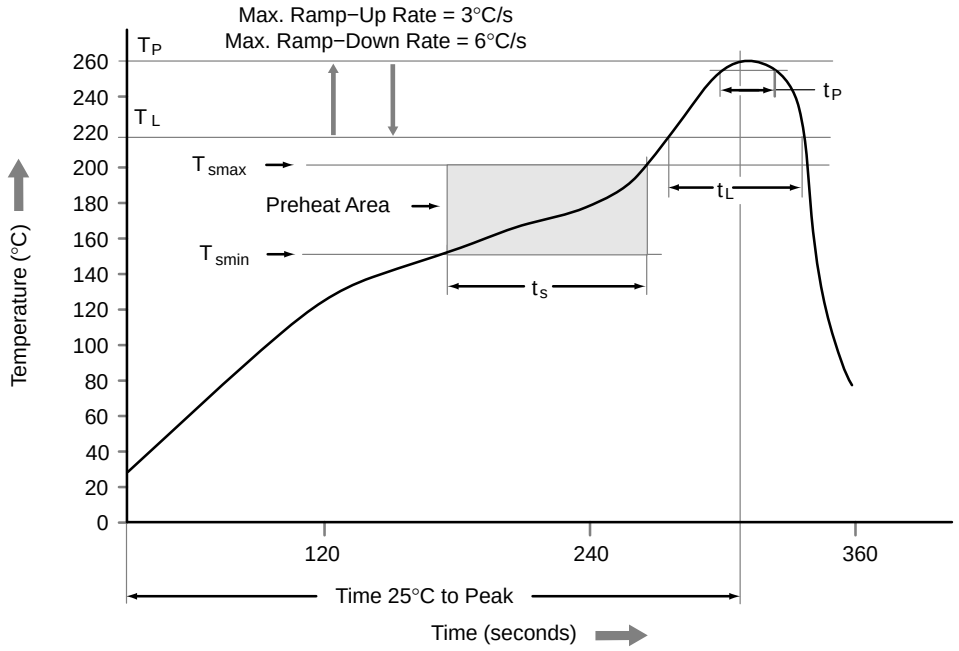

Figure 59. Relow Profile

Profile Freature	Pb−Free Assembly Profile
Temperature Minimum (T_{smin})	150°C
Temperature Maximum (T_{smax})	200°C
Time (t_S) from (T_{smin} to T_{smax})	60−120 seconds
Ramp−up Rate (t_L to t_P)	3°C/second maximum
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60−150 seconds
Peak Body Package Temperature	260°C +0°C / −5°C
Time (t_P) within 5°C of 260°C	30 seconds
Ramp−Down Rate (T_P to T_L)	6°C/second maximum
Time 25°C to Peak Temperature	8 minutes maximum

ORDERING INFORMATION

Part Number	Package	Shipping†
FOD8332	SOIC16 W, SO 16−Pin (Pb−Free)	50 Units / Tube
FOD8332R2	SOIC16 W, SO 16−Pin (Pb−Free)	750 Units / Tape & Reel
FOD8332V	SOIC16 W, SO 16−Pin, DIN EN/IEC 60747−5−5 Option (Pb−Free)	50 Units / Tube
FOD8332R2V	SOIC16 W, SO 16−Pin, DIN EN/IEC 60747−5−5 Option (Pb−Free)	750 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

31. All packages are lead free per JEDEC: J−STD−020B standard.

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PACKAGE DIMENSIONS

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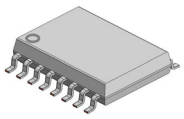
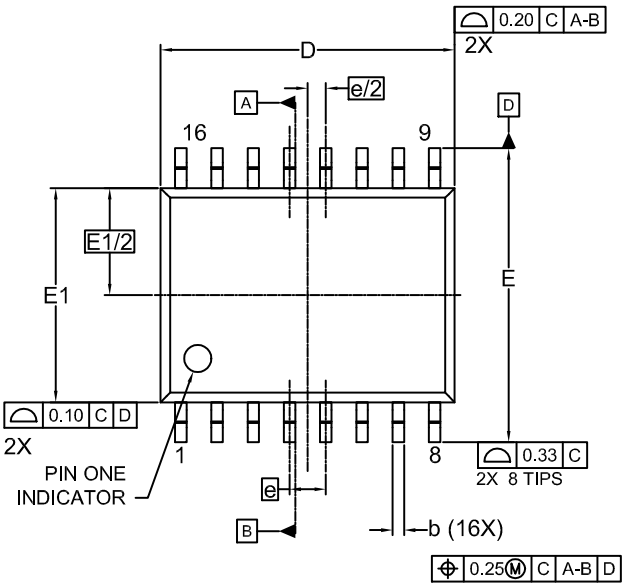
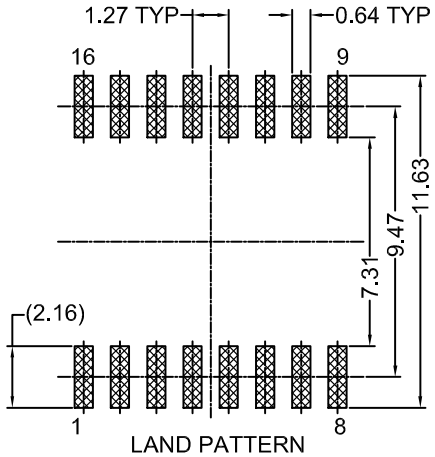


SOIC16 W
CASE 751EN
ISSUE A

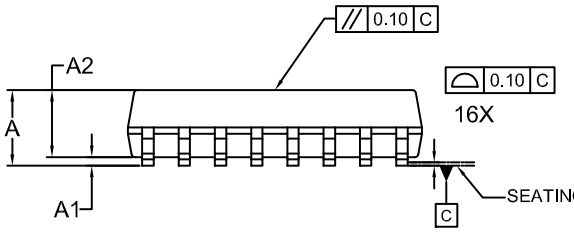
DATE 24 AUG 2021

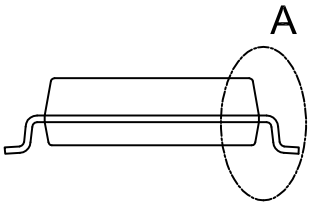


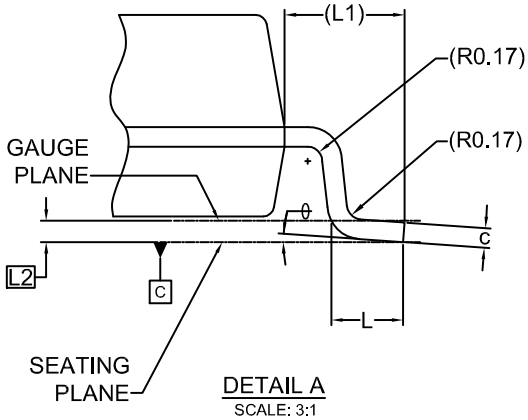


LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.







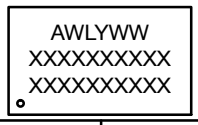
DETAIL A
SCALE: 3:1

DIM	MILLIMETER		
	MIN.	NOM.	MAX.
A	–	–	3.00
A1	0.15	0.30	0.45
A2	2.25	2.35	2.45
b	0.31	0.41	0.51
c	0.19	0.22	0.25
D	10.20	10.30	10.40
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
E1/2	3.75 BSC		
e	1.27 BSC		
e/2	0.635 BSC		
L	0.40	0.84	1.27
L1	1.42 REF		
L2	0.25 BSC		
θ	0°	–	8°

NOTES: UNLESS OTHERWISE SPECIFIED

A) DRAWING REFERS TO JEDEC MS-013, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS
D) DRAWING CONFORMS TO ASME Y14.5M-1994
E) LAND PATTERN STANDARD: SOIC127P1030X275-16N
F) DRAWING FILE NAME: MKT-M16FREV2
G) OPTOCOUPLER COMES IN WHITE MOLD BODY.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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