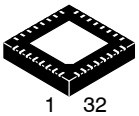
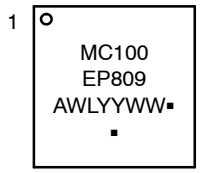
# 3.3 V 2:1:9 Differential HSTL/PECL/LVDS to HSTL Clock Driver with LVTTL Clock Select and Enable

# MC100EP809




**QFN32**
**MN SUFFIX**
**CASE 488AM**

### MARKING DIAGRAM*




A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package
(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

| Device | Package | Shipping |
|---|---|---|
| MC100EP809MNG | QFN32 (Pb−Free) | 74 Units / Rail |

### Description

The MC100EP809 is a low skew 2:1:9 differential clock driver, designed with clock distribution in mind, accepting two clock sources into an input multiplexer. The part is designed for use in low voltage applications which require a large number of outputs to drive precisely aligned low skew signals to their destination. The two clock inputs are one differential HSTL and one differential LVPECL. Both input pairs can accept LVDS levels. They are selected by the CLK_SEL pin which is LVTTL. To avoid generation of a runt clock pulse when the device is enabled/disabled, the Output Enable (OE), which is LVTTL, is synchronous ensuring the outputs will only be enabled/disabled when they are already in LOW state (Figure 8).

The MC100EP809 guarantees low output−to−output skew. The optimal design, layout, and processing minimize skew within a device and from lot to lot. The MC100EP809 output structure uses open emitter architecture and will be terminated with 50 Ω to ground instead of a standard HSTL configuration (Figure 6). To ensure the tight skew specification is realized, both sides of the differential output need to be terminated identically into 50 Ω even if only one output is being used. If an output pair is unused, both outputs may be left open (unterminated) without affecting skew.

Designers can take advantage of the EP809's performance to distribute low skew clocks across the backplane of the board. Both clock inputs may be single−end driven by biasing the non−driven pin in an input pair (Figure 7).

### Features

- 100 ps Typical Device−to−Device Skew
- 15 ps Typical within Device Skew
- HSTL Compatible Outputs Drive 50 Ω to GND with no Offset Voltage
- Maximum Frequency > 750 MHz
- 850 ps Typical Propagation Delay
- Fully Compatible with Micrel SY89809L
- PECL and HSTL Mode Operating Range: $V_{CCI}$ = 3 V to 3.6 V with GND = 0 V, $V_{CCO}$ = 1.6 V to 2.0 V
- Open Input Default State
- This Device is Pb−Free and is RoHS Compliant

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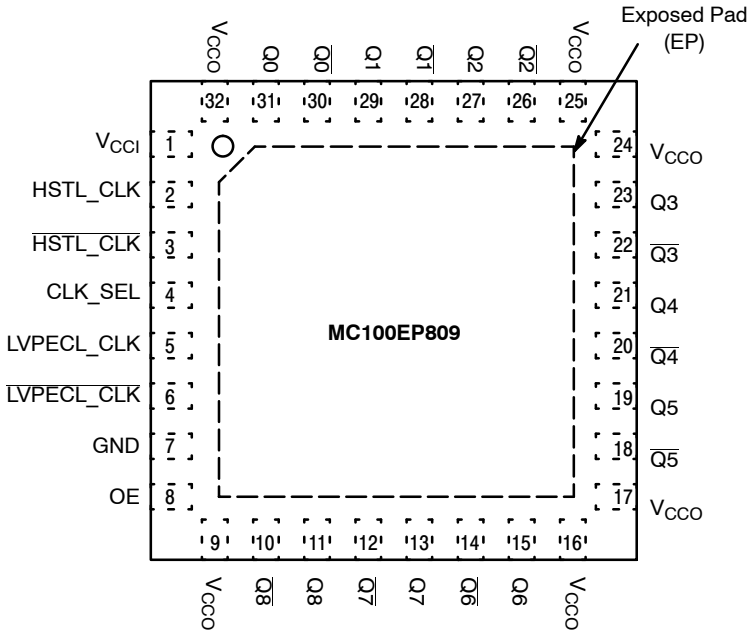



**Figure 1. 32−Lead QFN Pinout** (Top View)

**Table 1. PIN DESCRIPTION**

| PIN | FUNCTION |
|---|---|
| HSTL_CLK*, HSTL_CLK** | HSTL or LVDS Differential Inputs |
| LVPECL_CLK*, LVPECL_CLK** | LVPECL or LVDS Differential Inputs |
| CLK_SEL** | LVCMOS/LVTTL Input CLK Select |
| OE** | LVCMOS/LVTTL Output Enable |
| Q0 − Q8, Q0 − Q8 | HSTL Differential Outputs |
| $V_{CC1}$ | Positive Supply_Core (3.0 V − 3.6 V) |
| $V_{CC0}$ | Positive Supply_HSTL Outputs (1.6 V − 2.0 V) |
| GND | Ground |
| EP | The exposed pad (EP) on the QFN−32 package bottom is thermally connected to the die for improved heat transfer out of the package. THe exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to GND. |

* Pins will default LOW when left open.
** Pins will default HIGH when left open.

**Table 2. TRUTH TABLE**

| OE* | CLK_SEL | Q0 − Q8 | Q0 − Q8 |
|---|---|---|---|
| L | L | L | H |
| L | H | L | H |
| H | L | HSTL_CLK | HSTL_CLK |
| H | H | LVPECL_CLK | LVPECL_CLK |

*The OE (Output Enable) signal is synchronized with the rising edge of the HSTL_CLK and LVOCL_CLK signals.

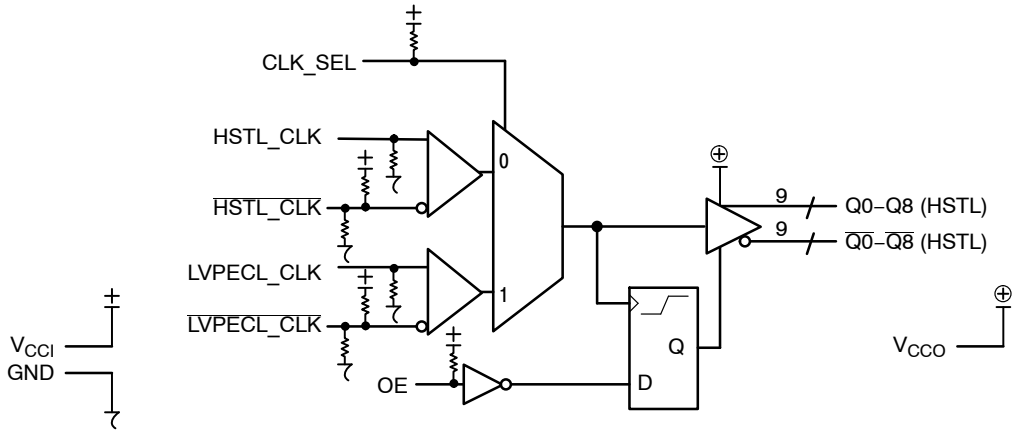



**Figure 2. Logic Diagram**

**Table 3. ATTRIBUTES**

| Characteristics | Value |
|---|---|
| Internal Input Pulldown Resistor | 75 kΩ |
| Internal Input Pullup Resistor | 37.5 kΩ |
| ESD Protection<br>Human Body Model<br>Machine Model<br>Charged Device Model | <br>> 2 kV<br>> 200 V<br>> 2 kV |
| Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1) | Pb−Free Pkg |
| QFN−32 | Level 1 |
| Flammability Rating<br>Oxygen Index: 28 to 34 | <br>UL 94 V−0 @ 0.125 in |
| Transistor Count | 478 Devices |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | |

1. For additional information, see Application Note AND8003/D.

**Table 4. MAXIMUM RATINGS**

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---|---|---|---|---|---|
| $V_{CC1}$ | Core Power Supply | GND = 0 V | $V_{CC0}$ = 1.6 to 2.0 V | 4 | V |
| $V_{CC0}$ | HSTL Output Power Supply | GND = 0 V | $V_{CC1}$ = 3.0 to 3.6 V | 4 | V |
| $V_I$ | Input Voltage | GND = 0 V | $V_I \le V_{CC1}$ | 4 | V |
| $I_{out}$ | Output Current | Continuous<br>Surge | | 50<br>100 | mA<br>mA |
| $T_A$ | Operating Temperature Range | | | 0 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) | 0 lfpm<br>500 lfpm | | 31<br>27 | °C/W<br>°C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) | 2S2P | | 12 | °C/W |
| $T_{sol}$ | Wave Solder | | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

**Table 5. LVPECL DC CHARACTERISTICS** $V_{CCI}$ = 3.0 V to 3.6 V; $V_{CCO}$ = 1.6 V to 2.0 V, GND = 0 V

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $I_{CC}$ | Core Power Supply Current | 75 | 95 | 115 | 75 | 95 | 115 | 75 | 95 | 115 | mA |
| $V_{IH}$ | Input HIGH Voltage (Single−Ended) | $V_{CCI}$ − 1.165 | | $V_{CCI}$ − 0.88 | $V_{CCI}$ − 1.165 | | $V_{CCI}$ − 0.88 | $V_{CCI}$ − 1.165 | | $V_{CCI}$ − 0.88 | V |
| $V_{IL}$ | Input LOW Voltage (Single−Ended) | $V_{CCI}$ − 1.945 | | $V_{CCI}$ − 1.6 | $V_{CCI}$ − 1.945 | | $V_{CCI}$ − 1.6 | $V_{CCI}$ − 1.945 | | $V_{CCI}$ − 1.6 | V |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 2) (Figure 4) LVPECL_CLK/$\overline{\text{LVPECL_CLK}}$ | 1.2 | | $V_{CCI}$ | 1.2 | | $V_{CCI}$ | 1.2 | | $V_{CCI}$ | V |
| $I_{IH}$ | Input HIGH Current | −150 | | 150 | −150 | | 150 | −150 | | 150 | μA |
| $I_{IL}$ | Input LOW Current | −150 | | 150 | −150 | | 150 | −150 | | 150 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

2. $V_{IHCMR}$ max varies 1:1 with $V_{CCI}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 6. LVTTL/LVCMOS DC CHARACTERISTICS** $V_{CCI}$ = 3.0 V to 3.6 V; $V_{CCO}$ = 1.6 V to 2.0 V, GND = 0 V

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{IH}$ | Input HIGH Voltage | 2.0 | | | 2.0 | | | 2.0 | | | V |
| $V_{IL}$ | Input LOW Voltage | | | 0.8 | | | 0.8 | | | 0.8 | V |
| $I_{IH}$ | Input HIGH Current | −150 | | 150 | −150 | | 150 | −150 | | 150 | μA |
| $I_{IL}$ | Input LOW Current | −300 | | 300 | −300 | | 300 | −300 | | 300 | μA |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

**Table 7. HSTL DC CHARACTERISTICS** $V_{CCI}$ = 3.0 V to 3.6 V; $V_{CCO}$ = 1.6 V to 2.0 V, GND = 0 V

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{OH}$ | Output HIGH Voltage (Note 3) | 1.0 | | 1.2 | 1.0 | | 1.2 | 1.0 | | 1.2 | V |
| $V_{OL}$ | Output LOW Voltage (Note 3) | 0.1 | | 0.4 | 0.1 | | 0.4 | 0.1 | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage (Figure 5) | $V_X$ + 0.1 | | 1.6 | $V_X$ + 0.1 | | 1.6 | $V_X$ + 0.1 | | 1.6 | V |
| $V_{IL}$ | Input LOW Voltage (Figure 5) | −0.3 | | $V_X$ − 0.1 | −0.3 | | $V_X$ − 0.1 | −0.3 | | $V_X$ − 0.1 | V |
| $V_X$ | HSTL Input Crossover Voltage | 0.68 | − | 0.9 | 0.68 | − | 0.9 | 0.68 | − | 0.9 | V |
| $I_{IH}$ | Input HIGH Current | −150 | | 150 | −150 | | 150 | −150 | | 150 | μA |
| $I_{IL}$ | Input LOW Current | −300 | | 300 | −300 | | 300 | −300 | | 300 | μA |
| $V_{IHCMR}$ | Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 4) HSTL_CLK/$\overline{\text{HSTL_CLK}}$ | 0.6 | | $V_{CCI}$ − 1.2 | 0.6 | | $V_{CCI}$ − 1.2 | 0.6 | | $V_{CCI}$ − 1.2 | V |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. All outputs loaded with 50 Ω to GND (Figure 6).
4. $V_{IHCMR}$ max varies 1:1 with $V_{CCI}$. The $V_{IHCMR}$ range is referenced to the most positive side of the differential input signal.

**Table 8. AC CHARACTERISTICS** $V_{CCI}$ = 3.0 V to 3.6 V; $V_{CCO}$ = 1.6 V to 2.0 V, GND = 0 V (Note 5)

| Symbol | Characteristic | 0°C | | | 25°C | | | 85°C | | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | Min | Typ | Max | |
| $V_{Opp}$ | Differential Output Voltage (Figure 3)<br>$f_{out}$ < 100 MHz<br>$f_{out}$ < 500 MHz<br>$f_{out}$ < 750 MHz | <br>600<br>600<br>450 | <br>850<br>750<br>575 | | <br>600<br>600<br>450 | <br>850<br>750<br>575 | | <br>600<br>600<br>450 | <br>850<br>750<br>575 | | <br>mV<br>mV<br>mV |
| $t_{PLH}$<br>$t_{PHL}$ | Propagation Delay<br>(Differential Configuration)<br>LVPECL_CLK to Q<br>HSTL_CLK to Q | <br><br>680<br>690 | <br><br>800<br>830 | <br><br>930<br>990 | <br><br>700<br>700 | <br><br>820<br>850 | <br><br>950<br>1000 | <br><br>780<br>790 | <br><br>920<br>950 | <br><br>1070<br>1110 | <br><br>ps<br>ps |
| $t_{skew}$ | Within−Device Skew (Note 6)<br>Device−to−Device Skew (Note 7) | | 15<br>100 | 50<br>200 | | 15<br>100 | 50<br>200 | | 15<br>100 | 50<br>200 | ps<br>ps |
| $t_{JITTER}$ | Random Clock Jitter (Figure 3) (RMS) | | 1.4 | 3.0 | | 1.4 | 3.0 | | 1.4 | 3.0 | ps |
| $V_{PP}$ | Input Swing (Differential Configuration)<br>(Note 8) (Figure 4)<br>LVPECL<br>HSTL | <br><br>200<br>200 | | | <br><br>200<br>200 | | | <br><br>200<br>200 | | | <br><br>mV<br>mV |
| $t_S$ | OE Set Up Time (Note 9) | 0.5 | | | 0.5 | | | 0.5 | | | ns |
| $t_H$ | OE Hold Time | 0.5 | | | 0.5 | | | 0.5 | | | ns |
| $t_r/t_f$ | Output Rise/Fall Time<br>(20% − 80%) | <br>350 | | <br>600 | <br>350 | <br>450 | <br>600 | <br>350 | | <br>600 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

5. Measured with 750 mV (LVPECL) source or 1 V (HSTL) source, 50% duty cycle clock source. All outputs loaded with 50 Ω to GND (Figure 6).
6. Skew is measured between outputs under identical transitions and conditions on any one device.
7. Device−to−Device skew for identical transitions and conditions.
8. $V_{PP}$ is the Differential Input Voltage swing required to maintain AC characteristics listed herein.
9. OE Set Up Time is defined with respect to the rising edge of the clock. OE High−to−Low transition ensures outputs remain disabled during the next clock cycle. OE Low−to−High transition enables normal operation of the next input clock (Figure 8).

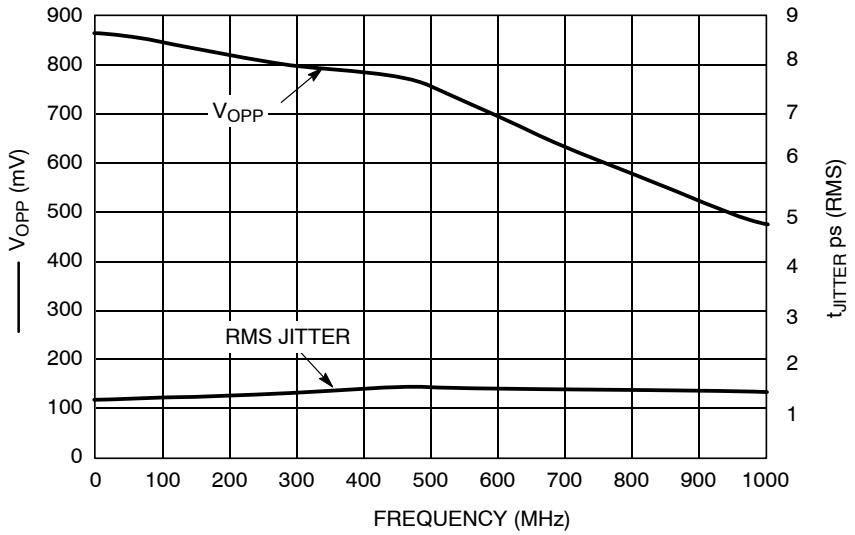



**Figure 3. Output Frequency ($F_{OUT}$) versus Output Voltage ($V_{OPP}$) and Random Clock Jitter ($t_{JITTER}$)**

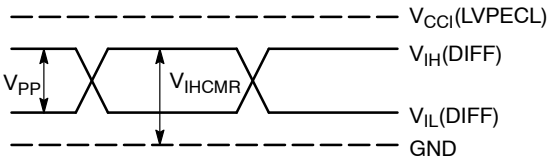



**Figure 4. LVPECL Differential Input Levels**

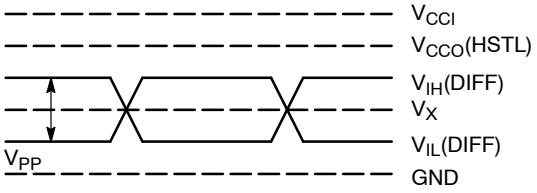



**Figure 5. HSTL Differential Input Levels**

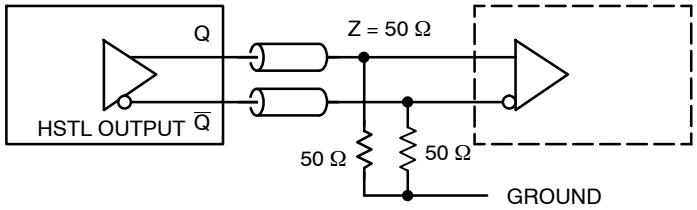
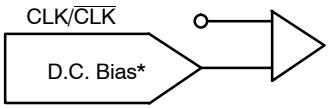



**Figure 6. HSTL Output Termination and AC Test Reference**




*Must be CLK/$\overline{\text{CLK}}$ common mode voltage: $((V_{IH} + V_{IL})/2)$.

**Figure 7. Single−Ended CLK/$\overline{\text{CLK}}$ Input Configuration**

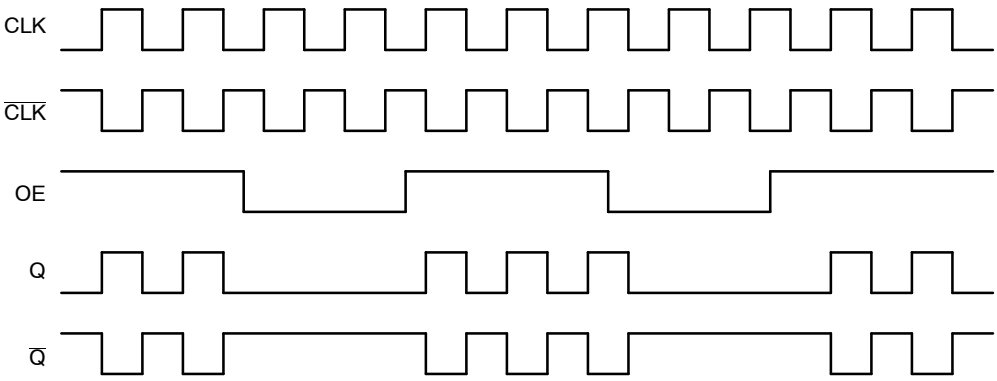



**Figure 8. Output Enable (OE) Timing Diagram**

### Resource Reference of Application Notes

**AN1405/D** – ECL Clock Distribution Techniques

**AN1406/D** – Designing with PECL (ECL at +5.0 V)

**AN1503/D** – ECLinPS™ I/O SPiCE Modeling Kit

**AN1504/D** – Metastability and the ECLinPS Family

**AN1568/D** – Interfacing Between LVDS and ECL

**AN1672/D** – The ECL Translator Guide

**AND8001/D** – Odd Number Counters Design

**AND8002/D** – Marking and Date Codes

**AND8020/D** – Termination of ECL Logic Devices

**AND8066/D** – Interfacing with ECLinPS

**AND8090/D** – AC Characteristics of ECL Devices

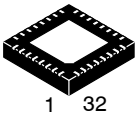
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# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

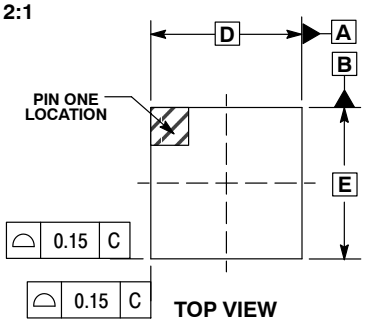
ON Semiconductor®

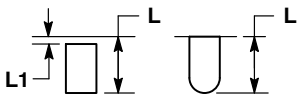
**QFN32 5x5, 0.5P**
CASE 488AM
ISSUE A

DATE 23 OCT 2013

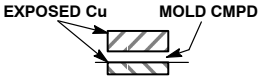



**SCALE 2:1**

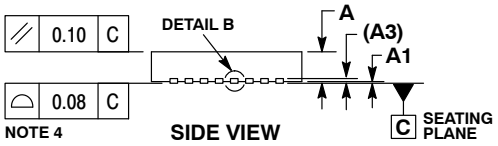


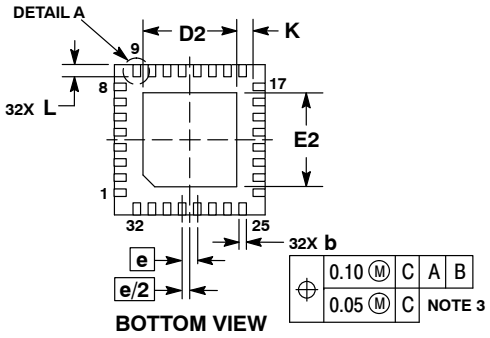




**DETAIL A**
**ALTERNATE TERMINAL CONSTRUCTIONS**




**DETAIL B**
**ALTERNATE CONSTRUCTION**

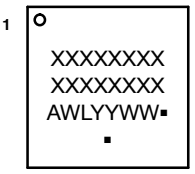



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | --- | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 5.00 BSC | |
| D2 | 2.95 | 3.25 |
| E | 5.00 BSC | |
| E2 | 2.95 | 3.25 |
| e | 0.50 BSC | |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | --- | 0.15 |

### GENERIC MARKING DIAGRAM*

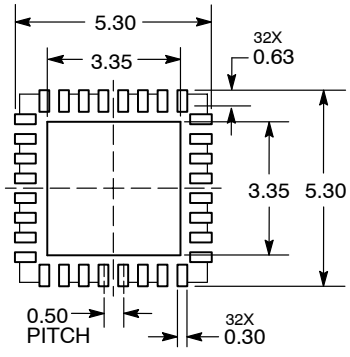



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, "G" or microdot " ▪", may or may not be present.

### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **QFN32 5x5 0.5P** | **PAGE 1 OF 1** |

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