MC100EPT24

3.3 V LVTTL/LVCMOS to Differential LVECL Translator

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Description

The MC100EPT24 is a LVTTL/LVCMOS to differential LVECL translator. Because LVECL levels and LVTTL/LVCMOS levels are used, a −3.3 V, +3.3 V and ground are required. The small outline 8-lead package and the single gate of the EPT24 makes it ideal for those applications where space, performance, and low power are at a premium.

Features

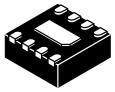
- 350 ps Typical Propagation Delay
- Maximum Input Clock Frequency = > 1.0 GHz Typical
- The 100 Series Contains Temperature Compensation
- Operating Range:
  V_{CC} = 3.0 V to 3.6 V; V_{EE} = −3.6 V to −3.0 V; GND = 0 V
- PNP LVTTL Input for Minimal Loading
- Q Output will Default HIGH with Input Open
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant



SOIC−8 NB
D SUFFIX
CASE 751−07

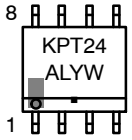


TSSOP−8
DT SUFFIX
CASE 948R−02

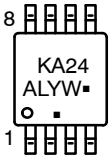


DFN8
MN SUFFIX
CASE 506AA

MARKING DIAGRAMS*



SOIC−8 NB



TSSOP−8



DFN8

A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
M	= Date Code
▪	= Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
MC100EPT24DG	SOIC−8 NB (Pb-Free)	98 Units / Tube
MC100EPT24DR2G	SOIC−8 NB (Pb-Free)	2500 Tape & Reel
MC100EPT24DTG	TSSOP−8 (Pb-Free)	100 Units / Tube
MC100EPT24MNR4G	DFN8 (Pb-Free)	1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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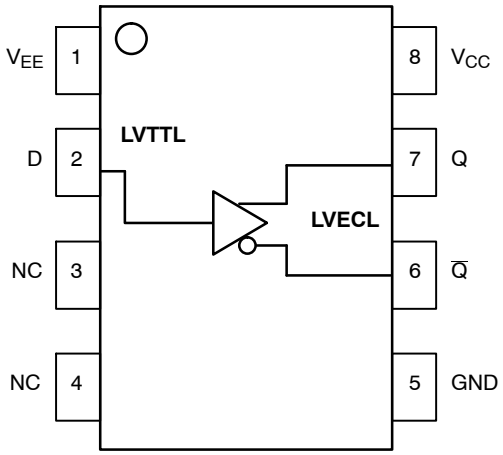

Figure 1. 8-Lead Pinout (Top View) **and Logic Diagram**

Table 1. PIN DESCRIPTION

PIN	FUNCTION
Q, $\overline{Q}$	Differential LVECL Outputs
D	LVTTL Input
V_{CC}	Positive Supply
GND	Ground
V_{EE}	Negative Supply
NC	No Connect
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

Table 2. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	N/A
Internal Input Pullup Resistor	N/A
ESD Protection Human Body Model Machine Model Charged Device Model	 > 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb-Free Pkg
SOIC−8 NB TSSOP−8 DFN8	Level 1 Level 3 Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in
Transistor Count	181 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V	V_{EE} = −3.3V	3.8	V
V_{EE}	Negative Power Supply	GND = 0 V	V_{CC} = 3.3V	−3.8	V
V_{IN}	Input Voltage	GND = 0 V	$V_I \le V_{CC}$	0 to V_{CC}	V
I_{out}	Output Current	Continuous Surge		50 100	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−65 to +150	°C
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 50 lfpm	SOIC−8 NB SOIC−8 NB	190 130	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC−8 NB	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 50 lfpm	TSSOP−8 TSSOP−8	185 140	°C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP−8	41 to 44	°C/W
θ_{JA}	Thermal Resistance (Junction-to-Ambient)	0 lfpm 50 lfpm	DFN8 DFN8	129 84	°C/W
T_{sol}	Wave Solder (Pb-Free)			265	°C
θ_{JC}	Thermal Resistance (Junction-to-Case)	(Note 1)	DFN8	35 to 40	°C/W

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. JEDEC standard multilayer board − 2S2P (2 signal, 2 power)

Table 4. LVTTL INPUT DC CHARACTERISTICS (V_{CC} = 3.3 V, V_{EE} = −3.6 V to −3.0 V, GND = 0.0 V; T_A = −40°C to 85°C)

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
I_{IH}	Input HIGH Current	V_{IN} = 2.7 V			20	μA
I_{IHH}	Input HIGH Current HIGH Voltage	V_{CC} = V_{IN} = 3.8 V			100	μA
I_{IL}	Input LOW Current	V_{IN} = 0.5 V			−0.6	mA
V_{IK}	Input Clamp Voltage	I_{IN} = −18 mA			−1.0	V
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 50 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. NECL OUTPUT DC CHARACTERISTICS (V_{CC} = 3.3 V, V_{EE} = −3.3 V, GND = 0.0 V (Note 1))

		−40°C			25°C			85°C			
Symbol	Characteristic	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
V_{OH}	Output HIGH Voltage (Note 2)	-1145	−1020	-895	-1145	−1020	-895	-1145	−1030	-895	mV
V_{OL}	Output LOW Voltage (Note 2)	-1945	−1820	-1695	-1945	−1820	-1695	-1945	−1820	-1695	mV
I_{CC}	Positive Power Supply Current		2.0	4.0		2.0	4.0		2.0	4.0	mA
I_{EE}	Negative Power Supply Current	20	30	38	20	30	38	20	30	38	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 50 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Output levels will vary 1:1 with GND. V_{EE} can vary ± 0.3 V.
2. Outputs are terminated through a 50 Ω resistor to GND − 2 V.

Table 6. AC CHARACTERISTICS (V_{CC} = 0 V; V_{EE} = −3.0 V to −5.5 V or V_{CC} = 3.0 V to 5.5 V; V_{EE} = 0 V (Note 1))

Symbol	Characteristic	−40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{max}	Maximum Input Clock Frequency (Figure 2)		> 1			> 1			> 1		GHz
t_{PLH}, t_{PHL}	Propagation Delay to Output Differential (Note 2)	300	500	800	300	530	800	300	560	800	ps
t_{JITTER}	RMS Random Clock Jitter (Figure 2)		0.2	< 1		0.2	< 1		0.2	< 1	ps
t_r t_f	Output Rise/Fall Times Q, $\overline{Q}$ (20% − 80%) @ 50 MHz	70	125	170	80	130	180	100	150	200	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 50 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Measured using a LVTTL source, 50% duty cycle clock source. All loading with 50 Ω to GND − 2.0 V.
2. Specifications for standard TTL input signal.

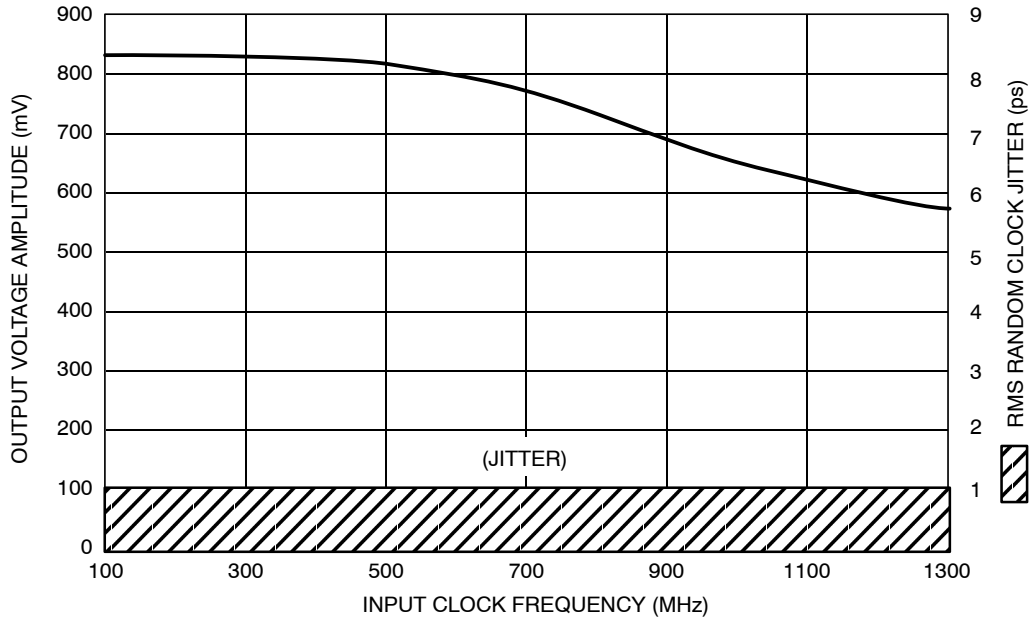

Figure 2. Output Voltage Amplitude (V_{OUTpp})/RMS Jitter vs. Input Clock Frequency at Ambient Temperature

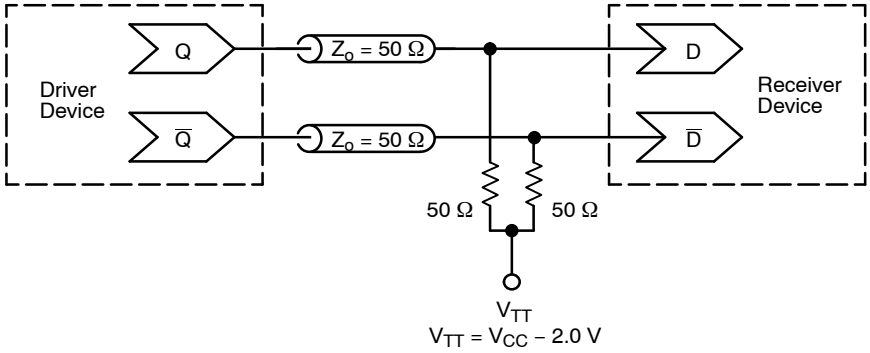

Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D – Termination of ECL Logic Devices)

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

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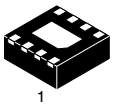
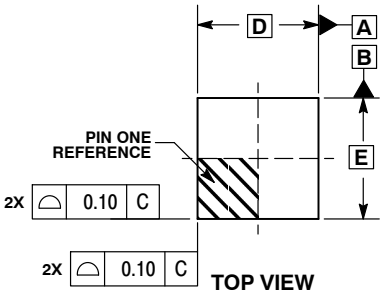
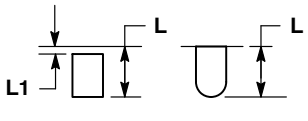


SCALE 4:1

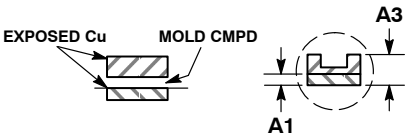
DFN8 2x2, 0.5P
CASE 506AA
ISSUE F

DATE 04 MAY 2016





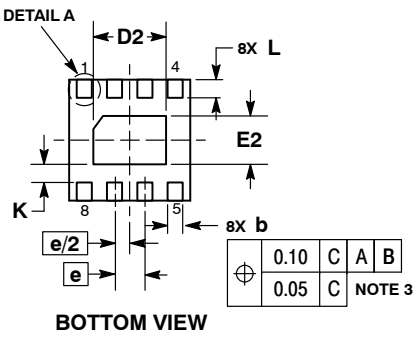
DETAIL A
OPTIONAL CONSTRUCTIONS



DETAIL B
ALTERNATE CONSTRUCTIONS

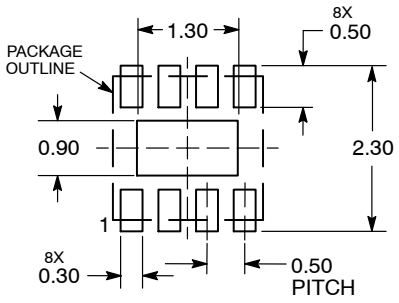
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.00 BSC	
D2	1.10	1.30
E	2.00 BSC	
E2	0.70	0.90
e	0.50 BSC	
K	0.30 REF	
L	0.25	0.35
L1	---	0.10



BOTTOM VIEW

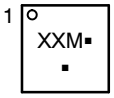
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Device

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98AON18658D**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**DFN8, 2.0X2.0, 0.5MM PITCH**		**PAGE 1 OF 1**

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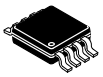
TSSOP 8
CASE 948R–02
ISSUE A

DATE 04/07/2000



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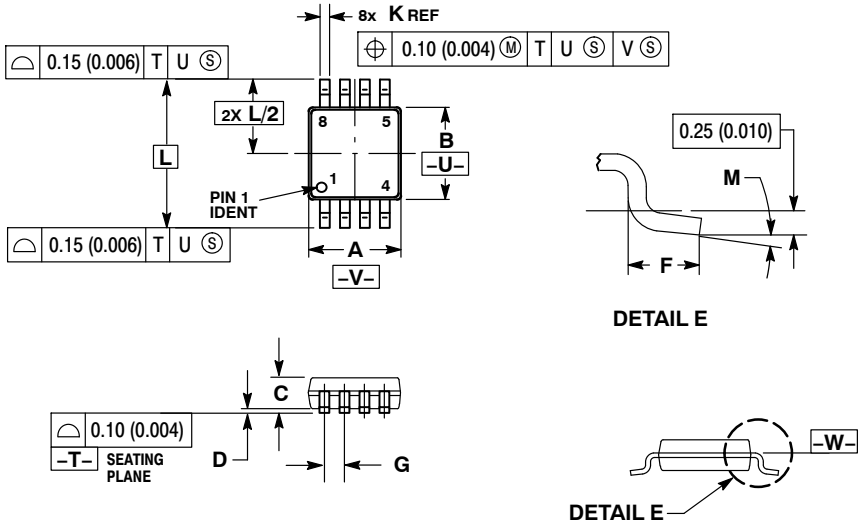

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

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