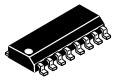
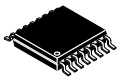
Hex Level Shifter for TTL to CMOS or CMOS to CMOS

MC14504B



SOIC−16
D SUFFIX
CASE 751B



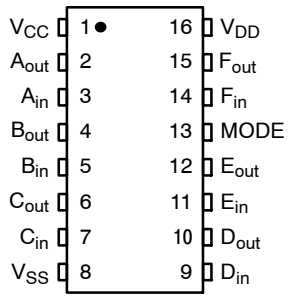
TSSOP−16
DT SUFFIX
CASE 948F

The MC14504B is a hex non−inverting level shifter using CMOS technology. The level shifter will shift a TTL signal to CMOS logic levels for any CMOS supply voltage between 5 and 15 volts. A control input also allows interface from CMOS to CMOS at one logic level to another logic level: Either up or down level translating is accomplished by selection of power supply levels V_{DD} and V_{CC}. The V_{CC} level sets the input signal levels while V_{DD} selects the output voltage levels.

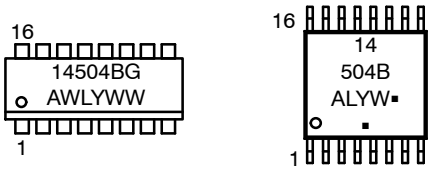
Features

- UP Translates from a Low to a High Voltage or DOWN Translates from a High to a Low Voltage
- Input Threshold Can Be Shifted for TTL Compatibility
- No Sequencing Required on Power Supplies or Inputs for Power Up or Power Down
- 3 to 18 Vdc Operation for V_{DD} and V_{CC}
- Diode Protected Inputs to V_{SS}
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load Over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC−16 TSSOP−16

A = Assembly Location
WL, L = Wafer Lot
Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Indicator

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}	Input Voltage Range (DC or Transient)	−0.5 to +18.0	V
V_{out}	Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Packages: −7.0 mW/°C From 65°C To 125°C.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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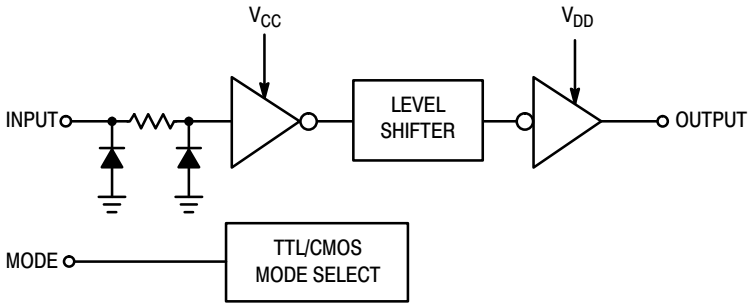
LOGIC DIAGRAM



Mode Select	Input Logic Levels	Output Logic Levels
1 (V_{CC})	TTL	CMOS
0 (V_{SS})	CMOS	CMOS

1/6 of package shown.

ORDERING INFORMATION

Device	Package	Shipping†
MC14504BDG	SOIC−16 (Pb−Free)	48 Units / Rail
MC14504BDR2G	SOIC−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14504BDR2G*		
MC14504BDTG	TSSOP−16 (Pb−Free)	96 Units / Rail
MC14504BDTR2G	TSSOP−16 (Pb−Free)	2500 Units / Tape & Reel
NLV14504BDTR2G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{CC} Vdc	V_{DD} Vdc	– 55°C Min	– 55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level	V_{OL}	–	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = 0 V		–	10	–	0.05	–	0	0.05	–	0.05	
		–	1 5	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	–	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = V_{CC}		–	10	9.95	–	9.95	10	–	9.95	–	
		–	15	14.95	–	14.95	15	–	14.95	–	
Input Voltage "0" Level	V_{IL}										Vdc
(V_{OL} = 1.0 Vdc) TTL–CMOS		5.0	10	–	0.8	–	1.3	0.8	–	0.8	
(V_{OL} = 1.5 Vdc) TTL–CMOS		5.0	15	–	0.8	–	1.3	0.8	–	0.8	
(V_{OL} = 1.0 Vdc) CMOS–CMOS		5.0	10	–	1.5	–	2.25	1.5	–	1.4	
(V_{OL} = 1.5 Vdc) CMOS–CMOS		5.0	15	–	1.5	–	2.25	1.5	–	1.5	
(V_{OL} = 1.5 Vdc) CMOS–CMOS		10	15	–	3.0	–	4.5	3.0	–	2.9	
Input Voltage "1" Level	V_{IH}										Vdc
(V_{OH} = 9.0 Vdc) TTL–CMOS		5.0	10	2.0	–	2.0	1.5	–	2.0	–	
(V_{OH} = 13.5 Vdc) TTL–CMOS		5.0	15	2.0	–	2.0	1.5	–	2.0	–	
(V_{OH} = 9.0 Vdc) CMOS–CMOS		5.0	10	3.6	–	3.5	2.75	–	3.5	–	
(V_{OH} = 13.5 Vdc) CMOS–CMOS		5.0	15	3.6	–	3.5	2.75	–	3.5	–	
(V_{OH} = 13.5 Vdc) CMOS–CMOS		10	15	7.1	–	7.0	5.5	–	7.0	–	
Output Drive Current	I_{OH}										mAdc
(V_{OH} = 2.5 Vdc) Source		–	5.0	– 3.0	–	– 2.4	– 4.2	–	– 1.7	–	
(V_{OH} = 4.6 Vdc)		–	5.0	–0.64	–	–0.51	– 0.88	–	–0.36	–	
(V_{OH} = 9.5 Vdc)		–	10	– 1.6	–	– 1.3	– 2.25	–	– 0.9	–	
(V_{OH} = 13.5 Vdc)		–	15	– 4.2	–	– 3.4	– 8.8	–	– 2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	–	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		–	10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		–	15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I_{in}	–	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD} or	–	5.0	–	0.05	–	0.0005	0.05	–	1.5	μAdc
(Per Package)	I_{CC}	–	10	–	0.10	–	0.0010	0.10	–	3.0	
CMOS–CMOS Mode		–	15	–	0.20	–	0.0015	0.20	–	6.0	
Quiescent Current	I_{DD}	5.0	5.0	–	0.5	–	0.0005	0.5	–	3.8	μAdc
(Per Package)		5.0	10	–	1.0	–	0.0010	1.0	–	7.5	
TTL–CMOS Mode		5.0	15	–	2.0	–	0.0015	2.0	–	15	
Quiescent Current	I_{CC}	5.0	5.0	–	5.0	–	2.5	5.0	–	6.0	mAdc
(Per Package)		5.0	10	–	5.0	–	2.5	5.0	–	6.0	
TTL–CMOS Mode		5.0	15	–	5.0	–	2.5	5.0	–	6.0	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	Shifting Mode	V_{CC} Vdc	V_{DD} Vdc	Limits Min	Limits Typ (Note 3)	Limits Max	Unit
Propagation Delay, High to Low	t_{PHL}	TTL – CMOS $V_{DD} > V_{CC}$	5.0 5.0	10 15	– –	140 140	280 280	ns
		CMOS – CMOS $V_{DD} > V_{CC}$	5.0 5.0 10	10 15 15	– – –	120 120 70	240 240 140	
		CMOS – CMOS $V_{CC} > V_{DD}$	10 15 15	5.0 5.0 10	– – –	185 185 175	370 370 350	
Propagation Delay, Low to High	t_{PLH}	TTL – CMOS $V_{DD} > V_{CC}$	5.0 5.0	10 15	– –	170 160	340 320	ns
		CMOS – CMOS $V_{DD} > V_{CC}$	5.0 5.0 10	10 15 15	– – –	170 170 100	340 340 200	
		CMOS – CMOS $V_{CC} > V_{DD}$	10 15 15	5.0 5.0 10	– – –	275 275 145	550 550 290	
Output Rise and Fall Time	t_{TLH}, t_{THL}	ALL	– – –	5.0 10 15	– – –	100 50 40	200 100 80	ns

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

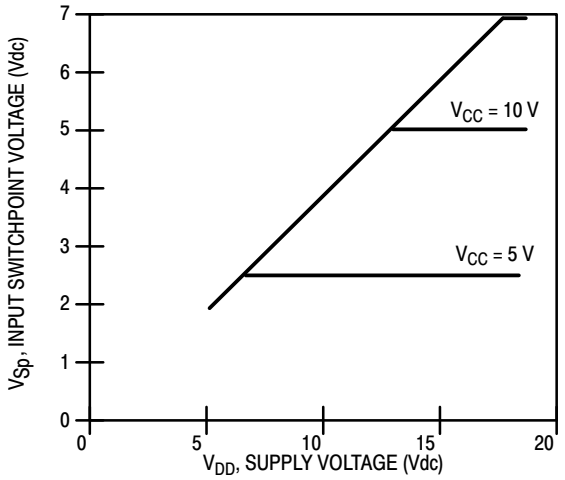


Figure 1. Input Switchpoint CMOS to CMOS Mode

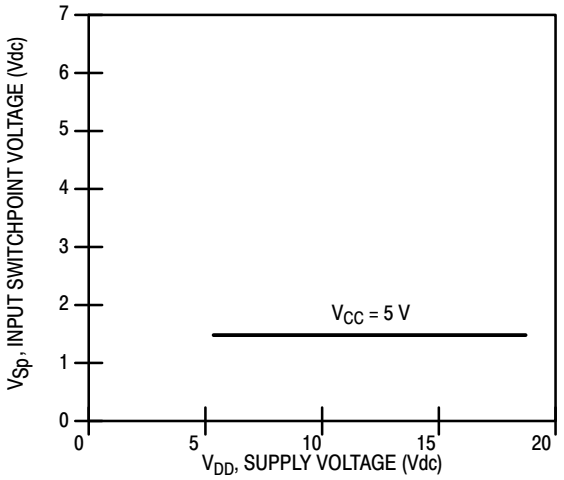


Figure 2. Input Switchpoint TTL to CMOS Mode

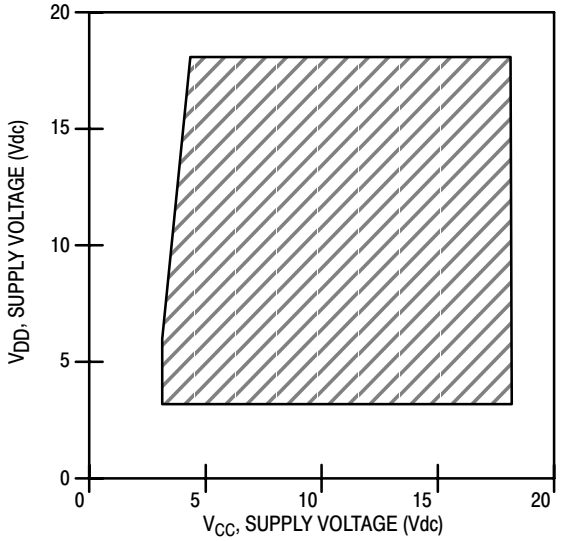


Figure 3. Operating Boundary CMOS to CMOS Mode

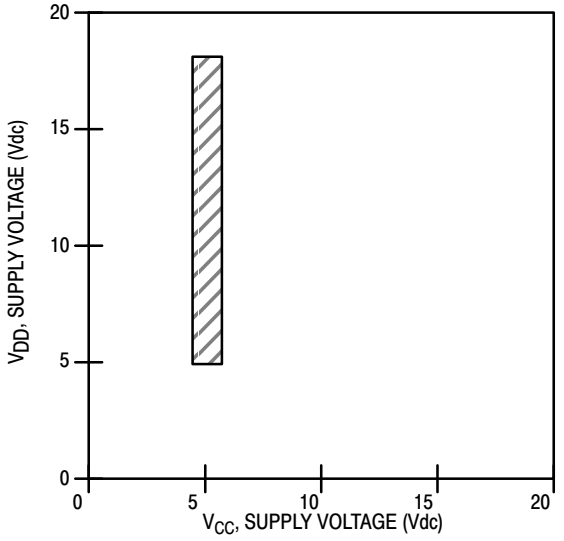
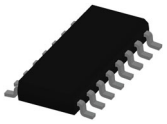


Figure 4. Operating Boundary TTL to CMOS Mode

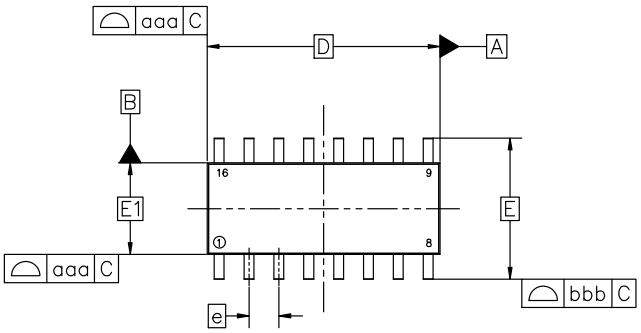
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



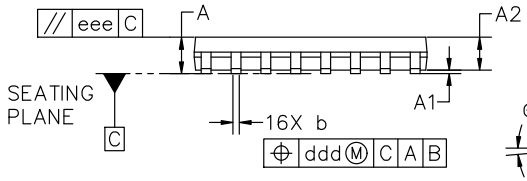
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

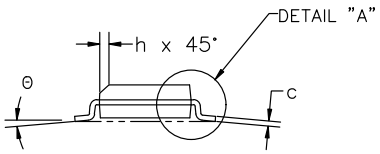
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

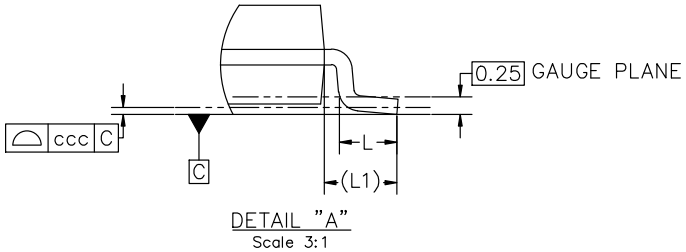


SIDE VIEW

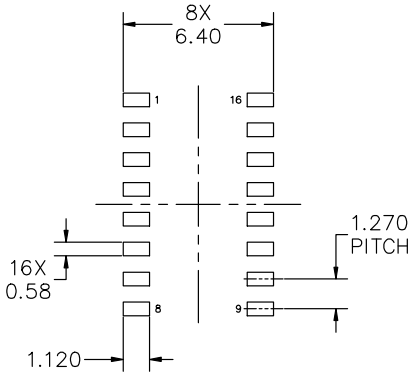


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P	PAGE 1 OF 2

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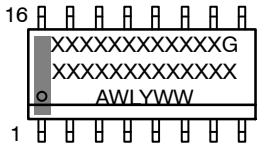
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:	
PIN 1.	COLLECTOR	PIN 1.	CATHODE	PIN 1.	COLLECTOR, DYE #1	PIN 1.	COLLECTOR, DYE #1
2.	BASE	2.	ANODE	2.	BASE, #1	2.	COLLECTOR, #1
3.	EMITTER	3.	NO CONNECTION	3.	EMITTER, #1	3.	COLLECTOR, #2
4.	NO CONNECTION	4.	CATHODE	4.	COLLECTOR, #1	4.	COLLECTOR, #2
5.	EMITTER	5.	CATHODE	5.	COLLECTOR, #2	5.	COLLECTOR, #3
6.	BASE	6.	NO CONNECTION	6.	BASE, #2	6.	COLLECTOR, #3
7.	COLLECTOR	7.	ANODE	7.	EMITTER, #2	7.	COLLECTOR, #4
8.	COLLECTOR	8.	CATHODE	8.	COLLECTOR, #2	8.	COLLECTOR, #4
9.	BASE	9.	CATHODE	9.	COLLECTOR, #3	9.	BASE, #4
10.	EMITTER	10.	ANODE	10.	BASE, #3	10.	EMITTER, #4
11.	NO CONNECTION	11.	NO CONNECTION	11.	EMITTER, #3	11.	BASE, #3
12.	EMITTER	12.	CATHODE	12.	COLLECTOR, #3	12.	EMITTER, #3
13.	BASE	13.	CATHODE	13.	COLLECTOR, #4	13.	BASE, #2
14.	COLLECTOR	14.	NO CONNECTION	14.	BASE, #4	14.	EMITTER, #2
15.	EMITTER	15.	ANODE	15.	EMITTER, #4	15.	BASE, #1
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1

STYLE 5:		STYLE 6:		STYLE 7:	
PIN 1.	DRAIN, DYE #1	PIN 1.	CATHODE	PIN 1.	SOURCE N-CH
2.	DRAIN, #1	2.	CATHODE	2.	COMMON DRAIN (OUTPUT)
3.	DRAIN, #2	3.	CATHODE	3.	COMMON DRAIN (OUTPUT)
4.	DRAIN, #2	4.	CATHODE	4.	GATE P-CH
5.	DRAIN, #3	5.	CATHODE	5.	COMMON DRAIN (OUTPUT)
6.	DRAIN, #3	6.	CATHODE	6.	COMMON DRAIN (OUTPUT)
7.	DRAIN, #4	7.	CATHODE	7.	COMMON DRAIN (OUTPUT)
8.	DRAIN, #4	8.	CATHODE	8.	SOURCE P-CH
9.	GATE, #4	9.	ANODE	9.	SOURCE P-CH
10.	SOURCE, #4	10.	ANODE	10.	COMMON DRAIN (OUTPUT)
11.	GATE, #3	11.	ANODE	11.	COMMON DRAIN (OUTPUT)
12.	SOURCE, #3	12.	ANODE	12.	COMMON DRAIN (OUTPUT)
13.	GATE, #2	13.	ANODE	13.	GATE N-CH
14.	SOURCE, #2	14.	ANODE	14.	COMMON DRAIN (OUTPUT)
15.	GATE, #1	15.	ANODE	15.	COMMON DRAIN (OUTPUT)
16.	SOURCE, #1	16.	ANODE	16.	SOURCE N-CH

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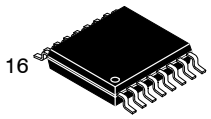
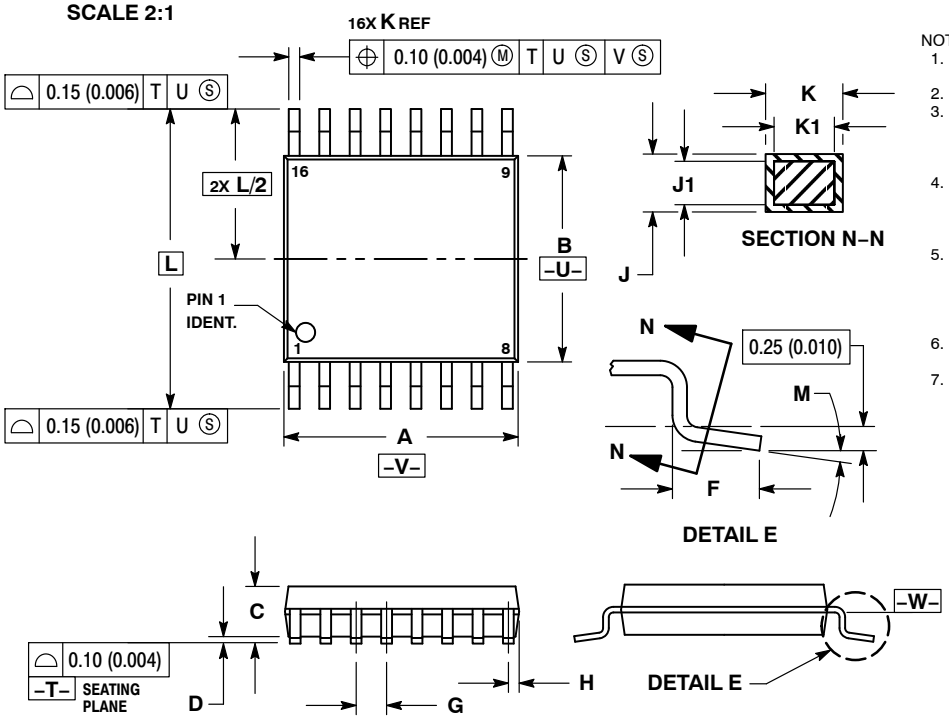
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006



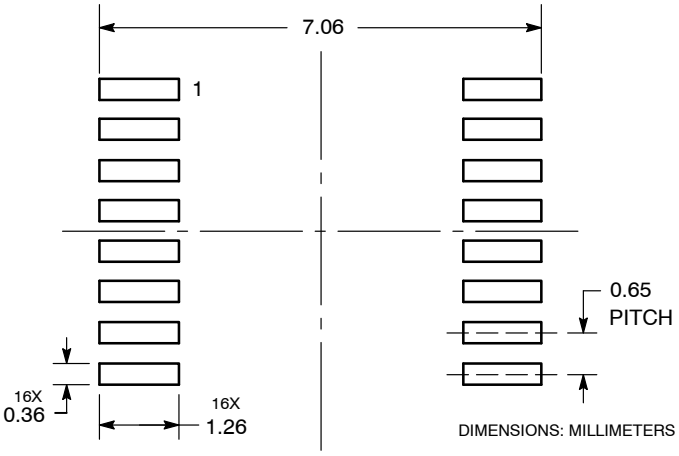
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

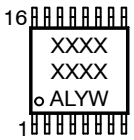
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSSOP−16**		**PAGE 1 OF 1**

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