MC14518B, MC14520B

Dual Up Counters

The MC14518B dual BCD counter and the MC14520B dual binary counter are constructed with MOS P−channel and N−channel enhancement mode devices in a single monolithic structure. Each consists of two identical, independent, internally synchronous 4−stage counters. The counter stages are type D flip−flops, with interchangeable Clock and Enable lines for incrementing on either the positive−going or negative−going transition as required when cascading multiple stages. Each counter can be cleared by applying a high level on the Reset line. In addition, the MC14518B will count out of all undefined states within two clock periods. These complementary MOS up counters find primary use in multi−stage synchronous or ripple counting applications requiring low power dissipation and/or high noise immunity.

Features

- Diode Protection on All Inputs
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Internally Synchronous for High Internal and External Speeds
- Logic Edge−Clocked Design − Incremented on Positive Transition of Clock or Negative Transition on Enable
- Capable of Driving Two Low−power TTL Loads or One Low−power Schottky TTL Load Over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1)

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	−0.5 to V_{DD} + 0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	±10	mA
P_D	Power Dissipation, per Package (Note 2)	500	mW
T_A	Operating Temperature Range	−55 to +125	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C
T_L	Lead Temperature (8−Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum Ratings are those values beyond which damage to the device may occur.
2. Temperature Derating: “D/DW” Package: –7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

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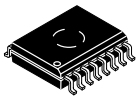
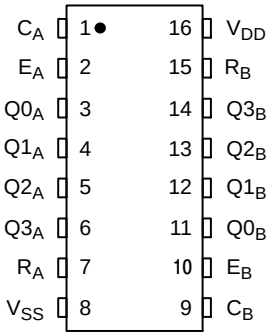
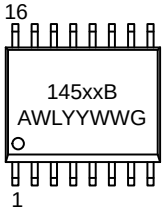


SOIC−16 WB
DW SUFFIX
CASE 751G

PIN ASSIGNMENT



MARKING DIAGRAM



xx = 18 or 20
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Indicator

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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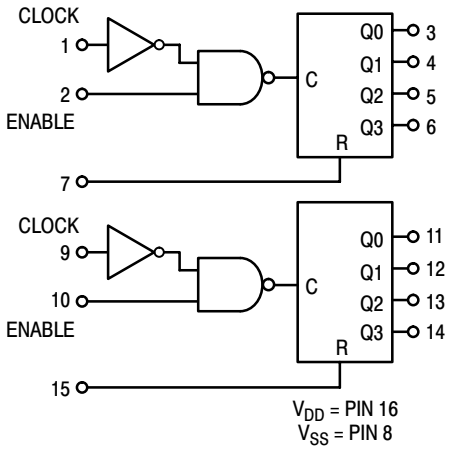
BLOCK DIAGRAM



TRUTH TABLE

Clock	Enable	Reset	Action
↗	1	0	Increment Counter
0	↘	0	Increment Counter
↘	X	0	No Change
X	↗	0	No Change
↗	0	0	No Change
1	↘	0	No Change
X	X	1	Q0 thru Q3 = 0

X = Don't Care

ORDERING INFORMATION

Device	Package	Shipping†
MC14518BDWG	SOIC−16 WB (Pb−Free)	47 Units / Rail
MC14518BDWR2G	SOIC−16 WB (Pb−Free)	1000 Units / Tape & Reel
NLV14518BDWR2G*	SOIC−16 WB (Pb−Free)	1000 Units / Tape & Reel
MC14520BDWG	SOIC−16 WB (Pb−Free)	47 Units / Rail
MC14520BDWR2G	SOIC−16 WB (Pb−Free)	1000 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	− 55°C Min	− 55°C Max	25°C Min	25°C Typ (Note 3)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage “0” Level	V_{OL}	5.0	−	0.05	−	0	0.05	−	0.05	Vdc
V_{in} = V_{DD} or 0		10	−	0.05	−	0	0.05	−	0.05	
		15	−	0.05	−	0	0.05	−	0.05	
“1” Level	V_{OH}	5.0	4.95	−	4.95	5.0	−	4.95	−	Vdc
V_{in} = 0 or V_{DD}		10	9.95	−	9.95	10	−	9.95	−	
		15	14.95	−	14.95	15	−	14.95	−	
Input Voltage “0” Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	−	1.5	−	2.25	1.5	−	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	−	3.0	−	4.50	3.0	−	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	−	4.0	−	6.75	4.0	−	4.0	
“1” Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	−	3.5	2.75	−	3.5	−	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	−	7.0	5.50	−	7.0	−	
(V_O = 1.5 or 13.5 Vdc)		15	11	−	11	8.25	−	11	−	
Output Drive Current	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	–3.0	−	–2.4	–4.2	−	–1.7	−	
(V_{OH} = 4.6 Vdc)		5.0	–0.64	−	–0.51	–0.88	−	–0.36	−	
(V_{OH} = 9.5 Vdc)		10	–1.6	−	–1.3	–2.25	−	–0.9	−	
(V_{OH} = 13.5 Vdc)		15	–4.2	−	–3.4	–8.8	−	–2.4	−	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	−	0.51	0.88	−	0.36	−	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	−	1.3	2.25	−	0.9	−	
(V_{OL} = 1.5 Vdc)		15	4.2	−	3.4	8.8	−	2.4	−	
Input Current	I_{in}	15	−	±0.1	−	±0.00001	±0.1	−	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package)	I_{DD}	5.0	−	5.0	−	0.005	5.0	−	150	μAdc
		10	−	10	−	0.010	10	−	300	
		15	−	20	−	0.015	20	−	600	
Total Supply Current (Notes 4, 5) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	I_T = (0.6 μA/kHz) f + I_{DD}							μAdc
		10	I_T = (1.2 μA/kHz) f + I_{DD}							
		15	I_T = (1.7 μA/kHz) f + I_{DD}							

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
4. The formulas given are for the typical characteristics only at 25°C.
5. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

SWITCHING CHARACTERISTICS (Note 6) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	All Types			Unit
			Min	Typ (Note 7)	Max	
Output Rise and Fall Time	t_{TLH},					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns	t_{THL}	5.0	–	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q/Enable to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	280	560	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	115	230	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	80	160	
Reset to Q	t_{PHL}					ns
t_{PHL} = (1.7 ns/pF) C_L + 265 ns		5.0	–	330	650	
t_{PHL} = (0.66 ns/pF) C_L + 117 ns		10	–	130	230	
t_{PHL} = (0.66 ns/pF) C_L + 95 ns		15	–	90	170	
Clock Pulse Width	$t_{w(H)}$	5.0	200	100	–	ns
	$t_{w(L)}$	10	100	50	–	
		15	70	35	–	
Clock Pulse Frequency	f_{cl}	5.0	–	2.5	1.5	MHz
		10	–	6.0	3.0	
		15	–	8.0	4.0	
Clock or Enable Rise and Fall Time	t_{THL}, t_{TLH}	5.0	–	–	15	μs
		10	–	–	5	
		15	–	–	4	
Enable Pulse Width	$t_{WH(E)}$	5.0	440	220	–	ns
		10	200	100	–	
		15	140	70	–	
Reset Pulse Width	$t_{WH(R)}$	5.0	280	125	–	ns
		10	120	55	–	
		15	90	40	–	
Reset Removal Time	t_{rem}	5.0	– 5	– 45	–	ns
		10	15	– 15	–	
		15	20	– 5	–	

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

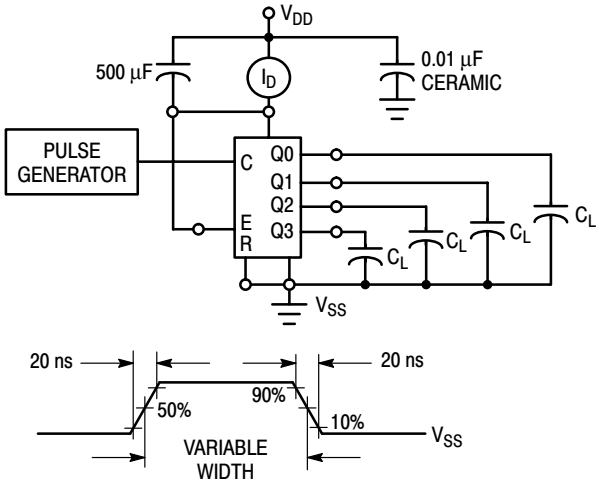


Figure 1. Power Dissipation Test Circuit and Waveform

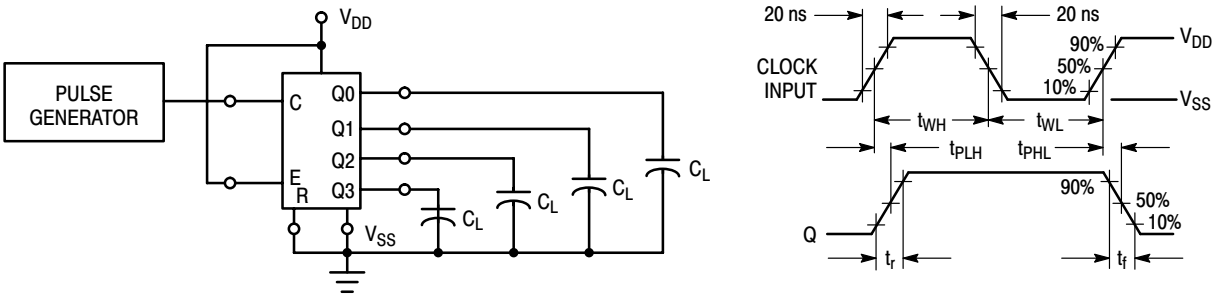


Figure 2. Switching Time Test Circuit and Waveforms

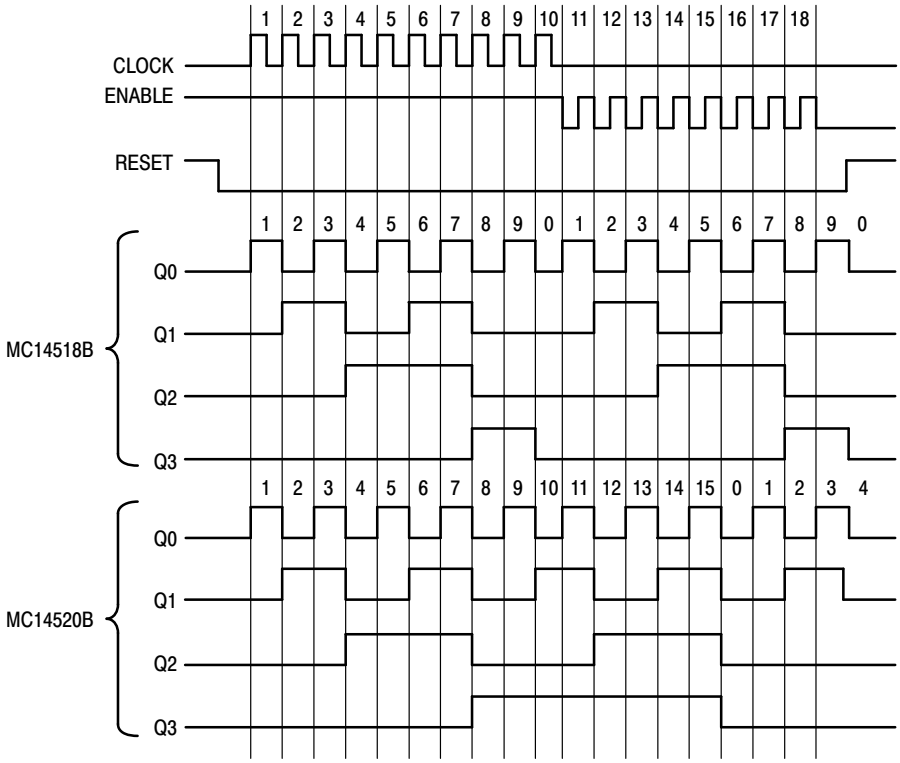


Figure 3. Timing Diagram

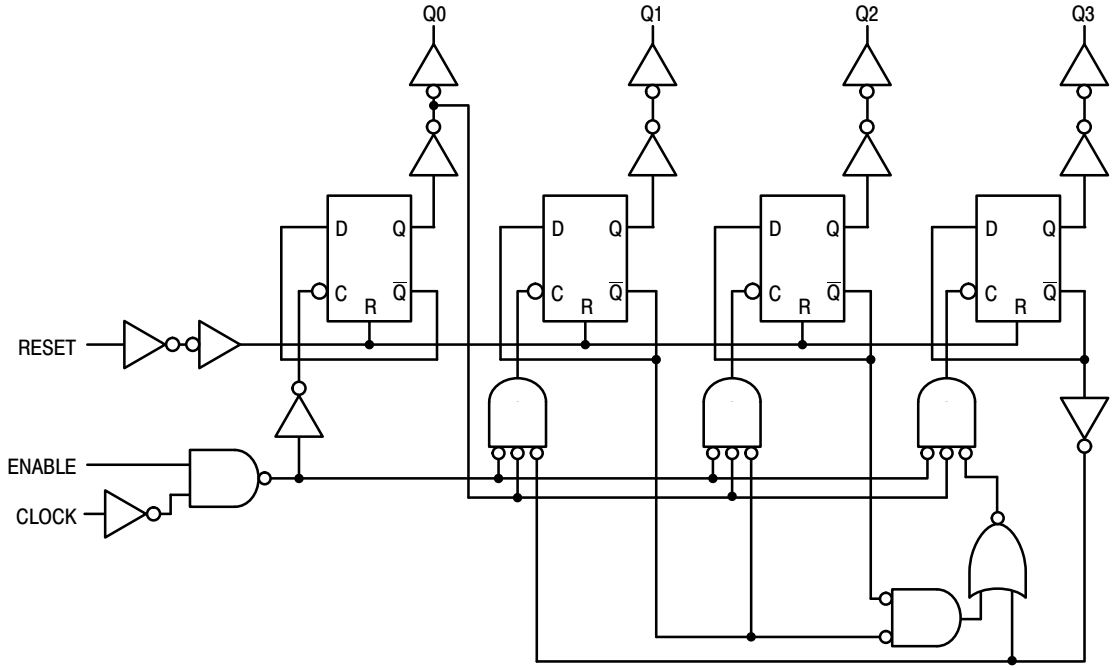


Figure 4. Decade Counter (MC14518B) Logic Diagram
(1/2 of Device Shown)

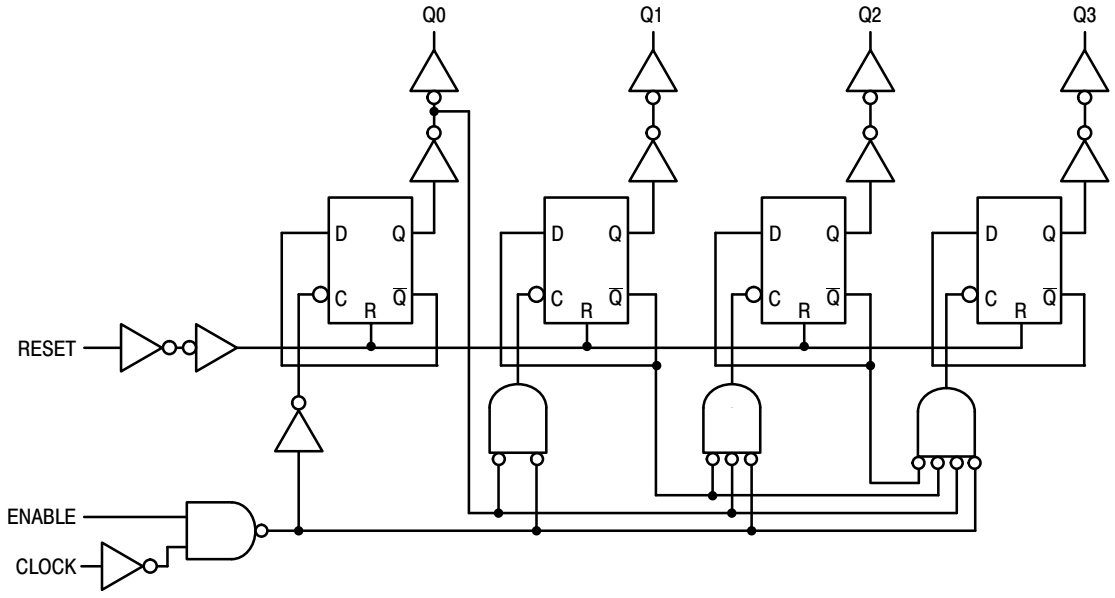
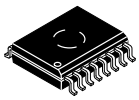


Figure 5. Binary Counter (MC14520B) Logic Diagram
(1/2 of Device Shown)

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−16 WB
CASE 751G
ISSUE E

DATE 08 OCT 2021



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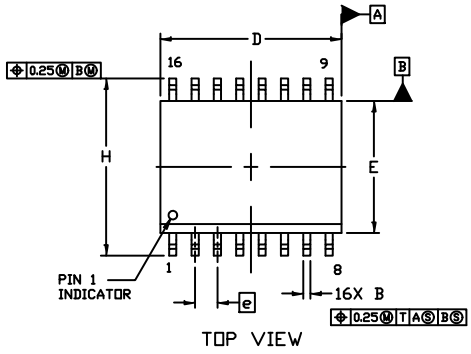
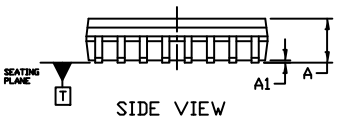
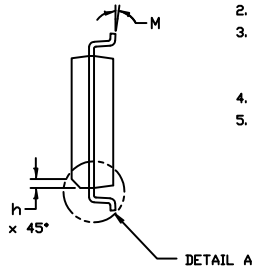
SCALE 1:1



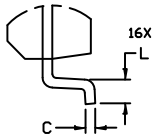
TOP VIEW



SIDE VIEW



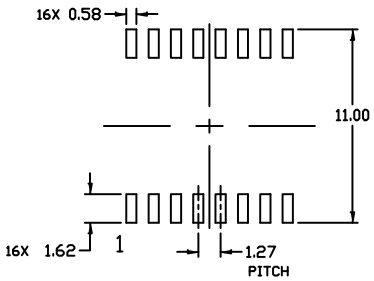
END VIEW



DETAIL A
2X SCALE

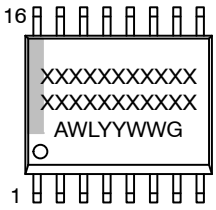
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOIC−16 WB**		**PAGE 1 OF 1**

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