# MC14521B

# 24-Stage Frequency Divider

The MC14521B consists of a chain of 24 flip−flops with an input circuit that allows three modes of operation. The input will function as a crystal oscillator, an RC oscillator, or as an input buffer for an external oscillator. Each flip−flop divides the frequency of the previous flip−flop by two, consequently this part will count up to $2^{24} = 16{,}777{,}216$. The count advances on the negative going edge of the clock. The outputs of the last seven−stages are available for added flexibility.

### Features

- All Stages are Resettable
- Reset Disables the RC Oscillator for Low Standby Power Drain
- RC and Crystal Oscillator Outputs Are Capable of Driving External Loads
- Test Mode to Reduce Test Time
- $V_{DD}$′ and $V_{SS}$′ Pins Brought Out on Crystal Oscillator Inverter to Allow the Connection of External Resistors for Low−Power Operation
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low−Power TTL Loads or One Low−Power Schottky TTL Load over the Rated Temperature Range
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- This Device is Pb−Free and is RoHS Compliant

**MAXIMUM RATINGS** (Voltages Referenced to $V_{SS}$)

| Parameter | Symbol | Value | Unit |
|---|---|---|---|
| DC Supply Voltage Range | $V_{DD}$ | −0.5 to +18.0 | V |
| Input or Output Voltage Range (DC or Transient) | $V_{in}$, $V_{out}$ | −0.5 to $V_{DD}$ +0.5 | V |
| Input or Output Current (DC or Transient) per Pin | $I_{in}$, $I_{out}$ | ±10 | mA |
| Power Dissipation, per Package (Note 1) | $P_D$ | 500 | mW |
| Ambient Temperature Range | $T_A$ | −55 to +125 | °C |
| Storage Temperature Range | $T_{stg}$ | −65 to +150 | °C |
| Lead Temperature (8−Second Soldering) | $T_L$ | 260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

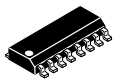
1. Temperature Derating: “D/DW” Package: –7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either $V_{SS}$ or $V_{DD}$). Unused outputs must be left open.

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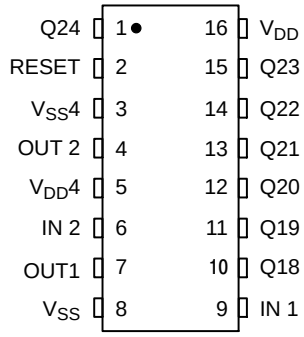
**http://onsemi.com**



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**SOIC−16**
**D SUFFIX**
**CASE 751B**

### PIN ASSIGNMENT




### MARKING DIAGRAMS



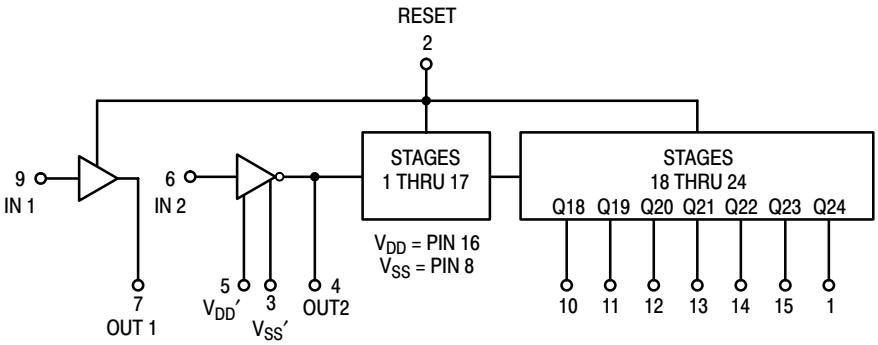

A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb−Free Package

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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## BLOCK DIAGRAM




| Output | Count Capacity |
|---|---|
| Q18 | $2^{18}$ = 262,144 |
| Q19 | $2^{19}$ = 524,288 |
| Q20 | $2^{20}$ = 1,048,576 |
| Q21 | $2^{21}$ = 2,097,152 |
| Q22 | $2^{22}$ = 4,194,304 |
| Q23 | $2^{23}$ = 8,388,608 |
| Q24 | $2^{24}$ = 16,777,216 |

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| MC14521BDG | SOIC−16<br>(Pb−Free) | 48 Units / Rail |
| NLV14521BDG* | SOIC−16<br>(Pb−Free) | 48 Units / Rail |
| MC14521BDR2G | SOIC−16<br>(Pb−Free) | 2500 / Tape & Reel |
| NLV14521BDR2G* | SOIC−16<br>(Pb−Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

**ELECTRICAL CHARACTERISTICS** (Voltages Referenced to $V_{SS}$)

| Characteristic | Symbol | $V_{DD}$ Vdc | − 55°C Min | − 55°C Max | 25°C Min | 25°C Typ (Note 2) | 25°C Max | 125°C Min | 125°C Max | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| Output Voltage “0” Level<br>$V_{in}$ = $V_{DD}$ or 0 | $V_{OL}$ | 5.0<br>10<br>15 | −<br>−<br>− | 0.05<br>0.05<br>0.05 | −<br>−<br>− | 0<br>0<br>0 | 0.05<br>0.05<br>0.05 | −<br>−<br>− | 0.05<br>0.05<br>0.05 | Vdc |
| “1” Level<br>$V_{in}$ = 0 or $V_{DD}$ | $V_{OH}$ | 5.0<br>10<br>15 | 4.95<br>9.95<br>14.95 | −<br>−<br>− | 4.95<br>9.95<br>14.95 | 5.0<br>10<br>15 | −<br>−<br>− | 4.95<br>9.95<br>14.95 | −<br>−<br>− | Vdc |
| Input Voltage “0” Level<br>($V_O$ = 4.5 or 0.5 Vdc)<br>($V_O$ = 9.0 or 1.0 Vdc)<br>($V_O$ = 13.5 or 1.5 Vdc) | $V_{IL}$ | 5.0<br>10<br>15 | −<br>−<br>− | 1.5<br>3.0<br>4.0 | −<br>−<br>− | 2.25<br>4.50<br>6.75 | 1.5<br>3.0<br>4.0 | −<br>−<br>− | 1.5<br>3.0<br>4.0 | Vdc |
| “1” Level<br>($V_O$ = 0.5 or 4.5 Vdc)<br>($V_O$ = 1.0 or 9.0 Vdc)<br>($V_O$ = 1.5 or 13.5 Vdc) | $V_{IH}$ | 5.0<br>10<br>15 | 3.5<br>7.0<br>11 | −<br>−<br>− | 3.5<br>7.0<br>11 | 2.75<br>5.50<br>8.25 | −<br>−<br>− | 3.5<br>7.0<br>11 | −<br>−<br>− | Vdc |
| Output Drive Current<br>($V_{OH}$ = 4.5 Vdc) Source<br>($V_{OH}$ = 9.0 Vdc) Pin 4<br>($V_{OH}$ = 13 Vdc) | $I_{OH}$ | 5.0<br>10<br>15 | –0.25<br>–0.62<br>–1.8 | −<br>−<br>− | –0.2<br>–0.5<br>–1.5 | –0.36<br>–0.9<br>–3.5 | −<br>−<br>− | –0.14<br>–0.35<br>–1.1 | −<br>−<br>− | mAdc |
| ($V_{OH}$ = 2.5 Vdc) Source<br>($V_{OH}$ = 4.6 Vdc) Pins 1, 7, 10,<br>($V_{OH}$ = 9.5 Vdc) 11, 12, 13, 14<br>($V_{OH}$ = 13.5 Vdc) and 15 | | 5.0<br>5.0<br>10<br>15 | –3.0<br>–0.64<br>–1.6<br>–4.2 | −<br>−<br>−<br>− | –2.4<br>–0.51<br>–1.3<br>–3.4 | –4.2<br>–0.88<br>–2.25<br>–8.8 | −<br>−<br>−<br>− | –1.7<br>–0.36<br>–0.9<br>–2.4 | −<br>−<br>−<br>− | mAdc |
| ($V_{OL}$ = 0.4 Vdc) Sink<br>($V_{OL}$ = 0.5 Vdc)<br>($V_{OL}$ = 1.5 Vdc) | $I_{OL}$ | 5.0<br>10<br>15 | 0.64<br>1.6<br>4.2 | −<br>−<br>− | 0.51<br>1.3<br>3.4 | 0.88<br>2.25<br>8.8 | −<br>−<br>− | 0.36<br>0.9<br>2.4 | −<br>−<br>− | mAdc |
| Input Current | $I_{in}$ | 15 | − | ±0.1 | − | ±0.00001 | ±0.1 | − | ±1.0 | μAdc |
| Input Capacitance<br>($V_{in}$ = 0) | $C_{in}$ | − | − | − | − | 5.0 | 7.5 | − | − | pF |
| Quiescent Current<br>(Per Package) | $I_{DD}$ | 5.0<br>10<br>15 | −<br>−<br>− | 5.0<br>10<br>20 | −<br>−<br>− | 0.005<br>0.010<br>0.015 | 5.0<br>10<br>20 | −<br>−<br>− | 150<br>300<br>600 | μAdc |
| Total Supply Current (Note 3, 4)<br>(Dynamic plus Quiescent,<br>Per Package)<br>($C_L$ = 50 pF on all outputs, all<br>buffers switching) | $I_T$ | 5.0<br>10<br>15 | $I_T$ = (0.42 μA/kHz) f + $I_{DD}$<br>$I_T$ = (0.85 μA/kHz) f + $I_{DD}$<br>$I_T$ = (1.40 μA/kHz) f + $I_{DD}$ | | | | | | | μAdc |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25°C.
4. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + (C_L - 50)\ Vfk$ where: $I_T$ is in μA (per package), $C_L$ in pF, $V = (V_{DD} - V_{SS})$ in volts, f in kHz is input frequency, and k = 0.003.

**SWITCHING CHARACTERISTICS** (Note 5) ($C_L$ = 50 pF, $T_A$ = 25°C)

| Characteristic | Symbol | $V_{DD}$ Vdc | Min | Typ (Note 6) | Max | Unit |
|---|---|---|---|---|---|---|
| Output Rise and Fall Time (Counter Outputs)<br>$t_{TLH}$, $t_{THL}$ = (1.5 ns/pF) $C_L$ + 25 ns<br>$t_{TLH}$, $t_{THL}$ = (0.75 ns/pF) $C_L$ + 12.5 ns<br>$t_{TLH}$, $t_{THL}$ = (0.55 ns/pF) $C_L$ + 12.5 ns | $t_{TLH}$, $t_{THL}$ | <br>5.0<br>10<br>15 | <br>–<br>–<br>– | <br>100<br>50<br>40 | <br>200<br>100<br>80 | ns |
| Propagation Delay Time<br>Clock to Q18<br>$t_{PHL}$, $t_{PLH}$ = (1.7 ns/pF) $C_L$ + 4415 ns<br>$t_{PHL}$, $t_{PLH}$ = (0.66 ns/pF) $C_L$ + 1667 ns<br>$t_{PHL}$, $t_{PLH}$ = (0.5 ns/pF) $C_L$ + 1275 ns<br>Clock to Q24<br>$t_{PHL}$, $t_{PLH}$ = (1.7 ns/pF) $C_L$ + 5915 ns<br>$t_{PHL}$, $t_{PLH}$ = (0.66 ns/pF) $C_L$ + 2167 ns<br>$t_{PHL}$, $t_{PLH}$ = (0.5 ns/pF) $C_L$ + 1675 ns | $t_{PHL}$, $t_{PLH}$ | <br><br>5.0<br>10<br>15<br><br><br>5.0<br>10<br>15 | <br><br>–<br>–<br>–<br><br><br>–<br>–<br>– | <br><br>4.5<br>1.7<br>1.3<br><br><br>6.0<br>2.2<br>1.7 | <br><br>9.0<br>3.5<br>2.7<br><br><br>12<br>4.5<br>3.5 | µs |
| Propagation Delay Time<br>Reset to $Q_n$<br>$t_{PHL}$ = (1.7 ns/pF) $C_L$ + 1215 ns<br>$t_{PHL}$ = (0.66 ns/pF) $C_L$ + 467 ns<br>$t_{PHL}$ = (0.5 ns/pF) $C_L$ + 350 ns | $t_{PHL}$ | <br><br>5.0<br>10<br>15 | <br><br>–<br>–<br>– | <br><br>1300<br>500<br>375 | <br><br>2600<br>1000<br>750 | ns |
| Clock Pulse Width | $t_{WH(cl)}$ | 5.0<br>10<br>15 | 385<br>150<br>120 | 140<br>55<br>40 | –<br>–<br>– | ns |
| Clock Pulse Frequency | $f_{cl}$ | 5.0<br>10<br>15 | –<br>–<br>– | 3.5<br>9.0<br>12 | 2.0<br>5.0<br>6.5 | MHz |
| Clock Rise and Fall Time | $t_{TLH}$, $t_{THL}$ | 5.0<br>10<br>15 | –<br>–<br>– | –<br>–<br>– | 15<br>5.0<br>4.0 | µs |
| Reset Pulse Width | $t_{WH(R)}$ | 5.0<br>10<br>15 | 1400<br>600<br>450 | 700<br>300<br>225 | –<br>–<br>– | ns |
| Reset Removal Time | $t_{rem}$ | 5.0<br>10<br>15 | 30<br>0<br>– 40 | –200<br>–160<br>–110 | –<br>–<br>– | ns |

5. The formulas given are for the typical characteristics only at 25°C.
6. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.

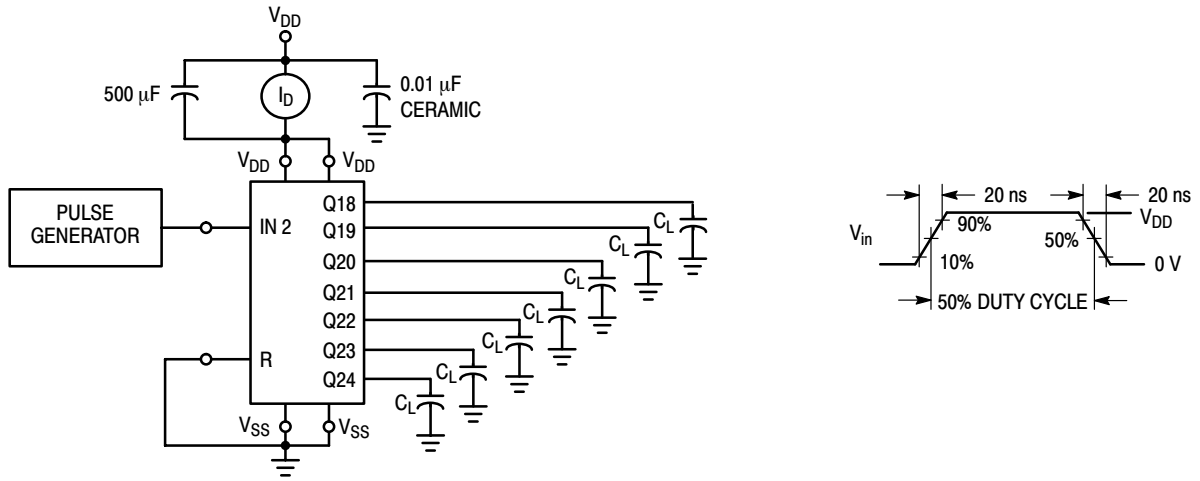



**Figure 1. Power Dissipation Test Circuit and Waveform**

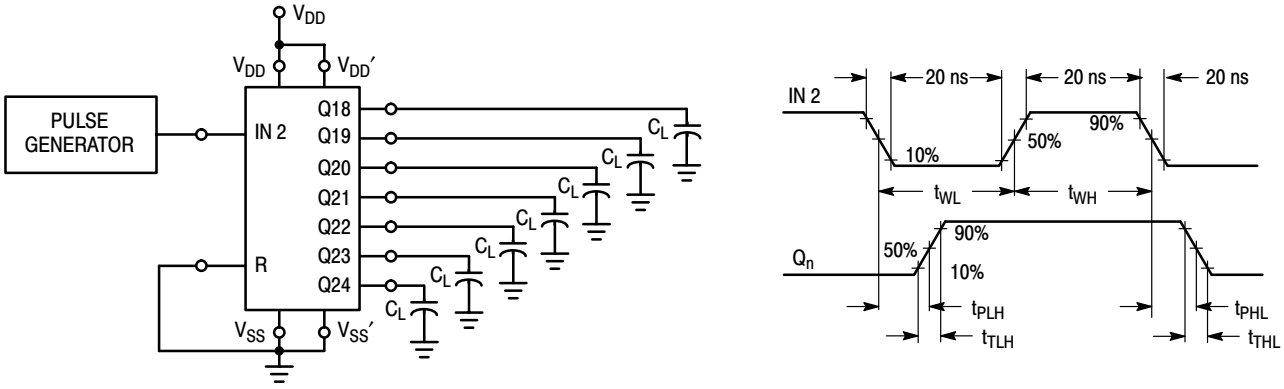
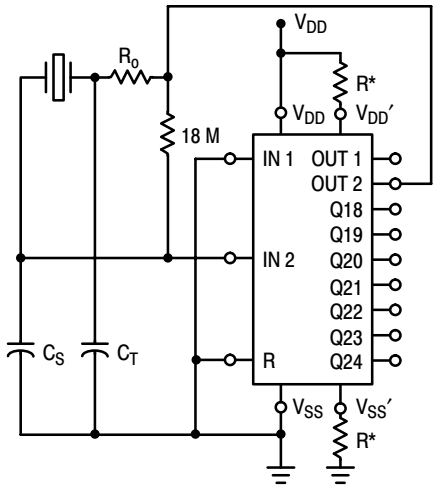



**Figure 2. Switching Time Test Circuit and Waveforms**




*Optional for low power operation,
10 kΩ ≤ R ≤ 70 kΩ.

**Figure 3. Crystal Oscillator Circuit**

| Characteristic | 500 kHz Circuit | 50 kHz Circuit | Unit |
|---|---|---|---|
| Crystal Characteristics | | | |
| Resonant Frequency | 500 | 50 | kHz |
| Equivalent Resistance, $R_S$ | 1.0 | 6.2 | kΩ |
| External Resistor/Capacitor Values | | | |
| $R_o$ | 47 | 750 | kΩ |
| $C_T$ | 82 | 82 | pF |
| $C_S$ | 20 | 20 | pF |
| Frequency Stability | | | |
| Frequency Change as a Function of $V_{DD}$ ($T_A$ = 25°C) | | | |
| $V_{DD}$ Change from 5.0 V to 10 V | + 6.0 | + 2.0 | ppm |
| $V_{DD}$ Change from 10 V to 15 V | + 2.0 | + 2.0 | ppm |
| Frequency Change as a Function of Temperature ($V_{DD}$ = 10 V) | – 4.0 | – 2.0 | ppm |
| $T_A$ Change from – 55°C to + 25°C | + 100 | + 120 | ppm |
| MC14521 only | | | |
| Complete Oscillator* | | | |
| $T_A$ Change from + 25°C to + 125°C | – 2.0 | – 2.0 | ppm |
| MC14521 only | – 160 | – 560 | ppm |
| Complete Oscillator* | | | |

*Complete oscillator includes crystal, capacitors, and resistors.

**Figure 4. Typical Data for Crystal Oscillator Circuit**

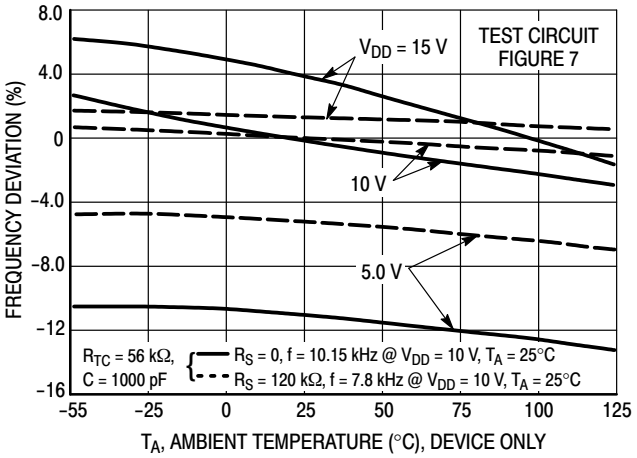



**Figure 5. RC Oscillator Stability**

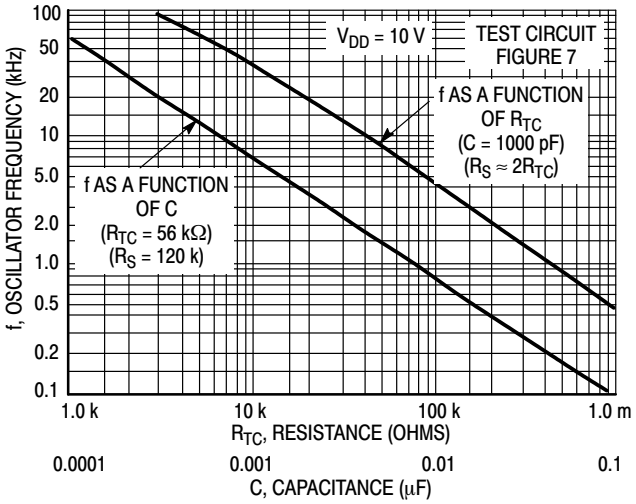



**Figure 6. RC Oscillator Frequency as a Function of $R_{TC}$ and C**

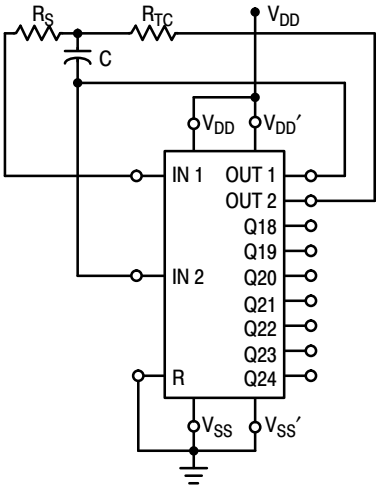



**Figure 7. RC Oscillator Circuit**

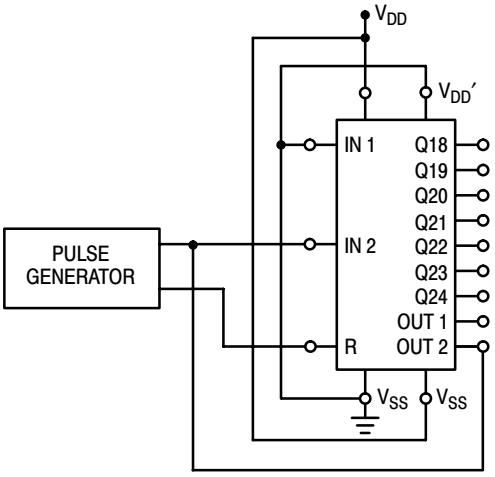


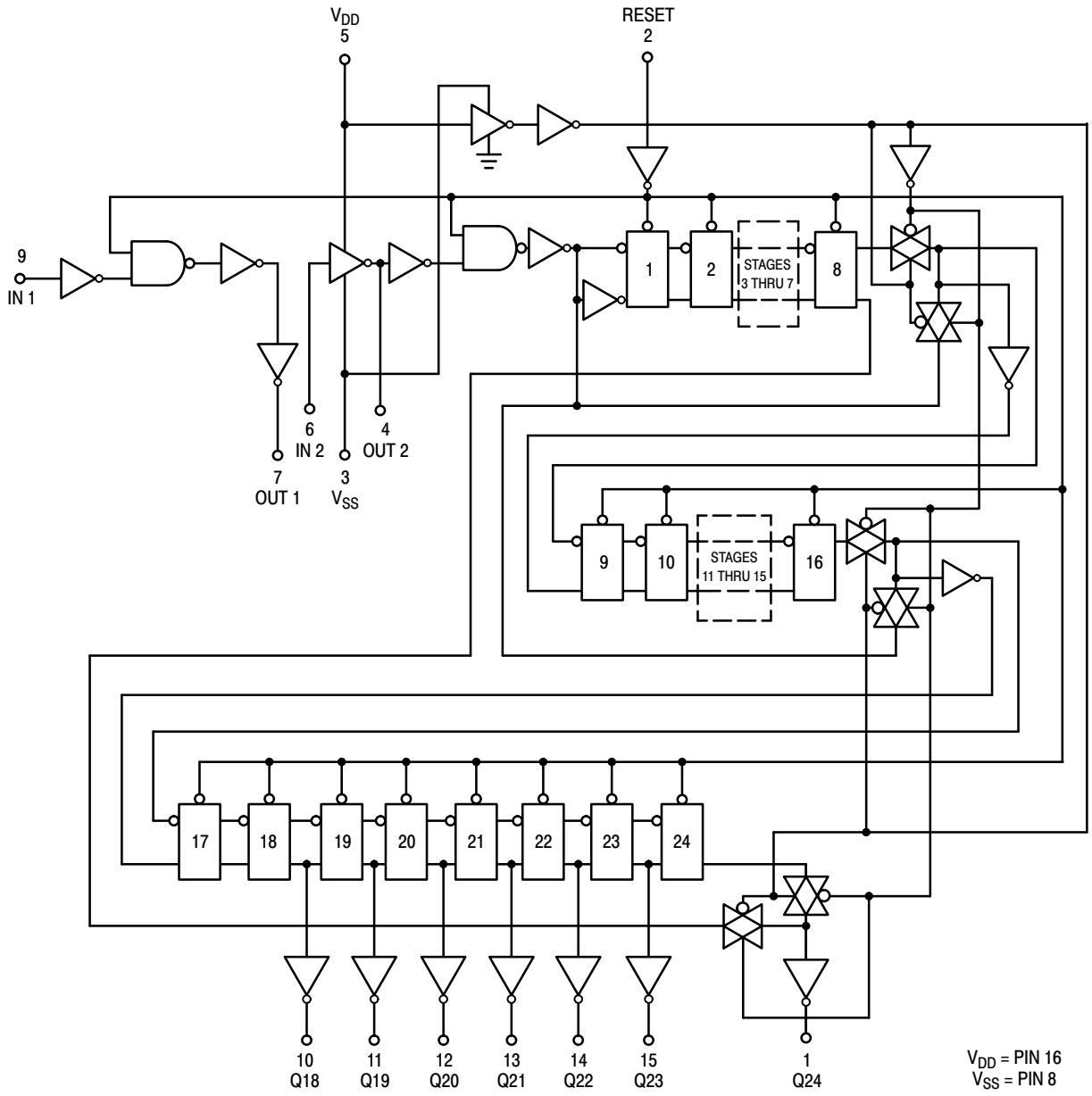

**Figure 8. Functional Test Circuit**

**FUNCTIONAL TEST SEQUENCE**

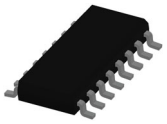
A test function (see Figure 8) has been included for the reduction of test time required to exercise all 24 counter stages. This test function divides the counter into three 8−stage sections, and 255 counts are loaded in each of the 8−stage sections in parallel. All flip−flops are now at a logic “1”. The counter is now returned to the normal 24−stages in series configuration. One more pulse is entered into Input 2 (In 2) which will cause the counter to ripple from an all “1” state to an all “0” state.

| Inputs | | Outputs | | | | Comments |
|---|---|---|---|---|---|---|
| Reset | In 2 | Out 2 | $V_{SS}'$ | $V_{DD}'$ | Q18 thru Q24 | Counter is in three 8−stage sections in parallel mode Counter is reset. In 2 and Out 2 are connected together. |
| 1 | 0 | 0 | $V_{DD}$ | GND | 0 | |
| 0 | 1 | 1 | | | | First “0” to “1” transition on In 2, Out 2 node. |
| | 0<br>1<br>–<br>–<br>– | 0<br>1<br>–<br>–<br>– | | | | 255 “0” to “1” transitions are clocked into this In 2, Out 2 node. |
| | 1 | 1 | | | 1 | The 255th “0” to “1” transition. |
| | 0<br>0 | 0<br>0 | | | 1<br>1 | |
| | 1 | 0 | GND | $V_{DD}$ | 1 | Counter converted back to 24−stages in series mode. |
| | 1 | 0 | | | 1 | Out 2 converts back to an output. |
| | 0 | 1 | | | 0 | Counter ripples from an all “1” state to an all “0” stage. |

## LOGIC DIAGRAM



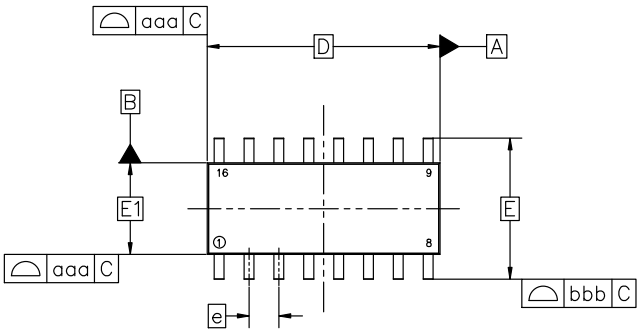
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



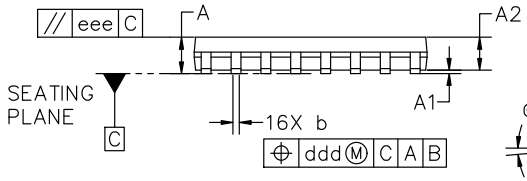
**SOIC−16 9.90x3.90x1.50 1.27P**
CASE 751B
ISSUE L

DATE 29 MAY 2024

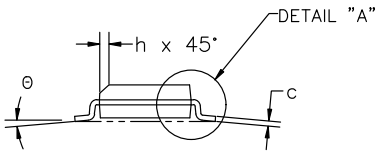
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.




TOP VIEW

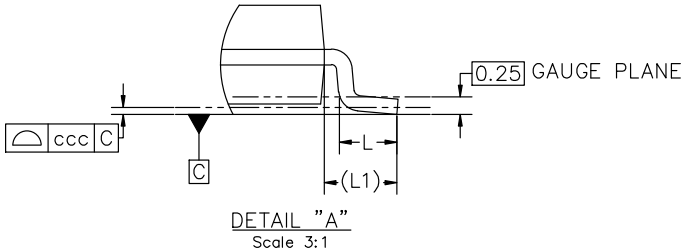



SIDE VIEW

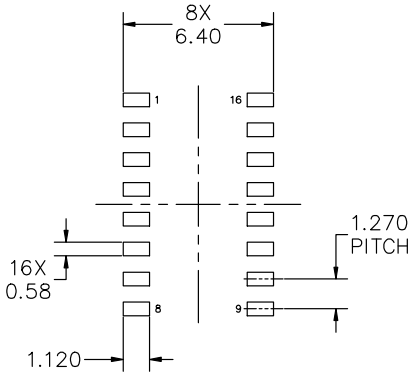



END VIEW

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 1.35 | 1.55 | 1.75 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | 1.35 | 1.50 | 1.65 |
| b | 0.35 | 0.42 | 0.49 |
| c | 0.19 | 0.22 | 0.25 |
| D | 9.90 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27 BSC | | |
| h | 0.25 | −−− | 0.50 |
| L | 0.40 | 0.83 | 1.25 |
| L1 | 1.05 REF | | |
| θ | 0° | −−− | 7° |
| TOLERANCE OF FORM AND POSITION | | | |
| aaa | 0.10 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.25 | | |
| eee | 0.10 | | |




DETAIL "A"
Scale 3:1




RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

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| DESCRIPTION: | SOIC−16 9.90X3.90X1.50 1.27P | PAGE 1 OF 2 |

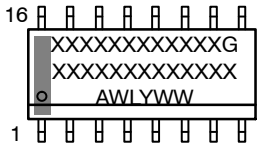
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**SOIC−16 9.90x3.90x1.50 1.27P**
CASE 751B
ISSUE L

DATE 29 MAY 2024

**GENERIC**
**MARKING DIAGRAM***




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| STYLE 1: | | STYLE 2: | | STYLE 3: | | STYLE 4: | |
|---|---|---|---|---|---|---|---|
| PIN 1. | COLLECTOR | PIN 1. | CATHODE | PIN 1. | COLLECTOR, DYE #1 | PIN 1. | COLLECTOR, DYE #1 |
| 2. | BASE | 2. | ANODE | 2. | BASE, #1 | 2. | COLLECTOR, #1 |
| 3. | EMITTER | 3. | NO CONNECTION | 3. | EMITTER, #1 | 3. | COLLECTOR, #2 |
| 4. | NO CONNECTION | 4. | CATHODE | 4. | COLLECTOR, #1 | 4. | COLLECTOR, #2 |
| 5. | EMITTER | 5. | CATHODE | 5. | COLLECTOR, #2 | 5. | COLLECTOR, #3 |
| 6. | BASE | 6. | NO CONNECTION | 6. | BASE, #2 | 6. | COLLECTOR, #3 |
| 7. | COLLECTOR | 7. | ANODE | 7. | EMITTER, #2 | 7. | COLLECTOR, #4 |
| 8. | COLLECTOR | 8. | CATHODE | 8. | COLLECTOR, #2 | 8. | COLLECTOR, #4 |
| 9. | BASE | 9. | CATHODE | 9. | COLLECTOR, #3 | 9. | BASE, #4 |
| 10. | EMITTER | 10. | ANODE | 10. | BASE, #3 | 10. | EMITTER, #4 |
| 11. | NO CONNECTION | 11. | NO CONNECTION | 11. | EMITTER, #3 | 11. | BASE, #3 |
| 12. | EMITTER | 12. | CATHODE | 12. | COLLECTOR, #3 | 12. | EMITTER, #3 |
| 13. | BASE | 13. | CATHODE | 13. | COLLECTOR, #4 | 13. | BASE, #2 |
| 14. | COLLECTOR | 14. | NO CONNECTION | 14. | BASE, #4 | 14. | EMITTER, #2 |
| 15. | EMITTER | 15. | ANODE | 15. | EMITTER, #4 | 15. | BASE, #1 |
| 16. | COLLECTOR | 16. | CATHODE | 16. | COLLECTOR, #4 | 16. | EMITTER, #1 |

| STYLE 5: | | STYLE 6: | | STYLE 7: | |
|---|---|---|---|---|---|
| PIN 1. | DRAIN, DYE #1 | PIN 1. | CATHODE | PIN 1. | SOURCE N-CH |
| 2. | DRAIN, #1 | 2. | CATHODE | 2. | COMMON DRAIN (OUTPUT) |
| 3. | DRAIN, #2 | 3. | CATHODE | 3. | COMMON DRAIN (OUTPUT) |
| 4. | DRAIN, #2 | 4. | CATHODE | 4. | GATE P-CH |
| 5. | DRAIN, #3 | 5. | CATHODE | 5. | COMMON DRAIN (OUTPUT) |
| 6. | DRAIN, #3 | 6. | CATHODE | 6. | COMMON DRAIN (OUTPUT) |
| 7. | DRAIN, #4 | 7. | CATHODE | 7. | COMMON DRAIN (OUTPUT) |
| 8. | DRAIN, #4 | 8. | CATHODE | 8. | SOURCE P-CH |
| 9. | GATE, #4 | 9. | ANODE | 9. | SOURCE P-CH |
| 10. | SOURCE, #4 | 10. | ANODE | 10. | COMMON DRAIN (OUTPUT) |
| 11. | GATE, #3 | 11. | ANODE | 11. | COMMON DRAIN (OUTPUT) |
| 12. | SOURCE, #3 | 12. | ANODE | 12. | COMMON DRAIN (OUTPUT) |
| 13. | GATE, #2 | 13. | ANODE | 13. | GATE N-CH |
| 14. | SOURCE, #2 | 14. | ANODE | 14. | COMMON DRAIN (OUTPUT) |
| 15. | GATE, #1 | 15. | ANODE | 15. | COMMON DRAIN (OUTPUT) |
| 16. | SOURCE, #1 | 16. | ANODE | 16. | SOURCE N-CH |



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