MC14549B, MC14559B

Successive Approximation Registers

The MC14549B and MC14559B successive approximation registers are 8−bit registers providing all the digital control and storage necessary for successive approximation analog−to−digital conversion systems. These parts differ in only one control input. The Master Reset (MR) on the MC14549B is required in the cascaded mode when more than 8 bits are desired. The Feed Forward (FF) of the MC14559B is used for register shortening where End−of−Conversion (EOC) is required after less than eight cycles.

Applications for the MC14549B and MC14559B include analog−to−digital conversion, with serial and parallel outputs.

Features

- Totally Synchronous Operation
- All Outputs Buffered
- Single Supply Operation
- Serial Output
- Retriggerable
- Compatible with a Variety of Digital and Analog Systems such as the MC1408 8−Bit D/A Converter
- All Control Inputs Positive−Edge Triggered
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving 2 Low−Power TTL Loads, 1 Low−Power Schottky TTL Load or 2 HTL Loads Over the Rated Temperature Range
- Chip Complexity: 488 FETs or 122 Equivalent Gates
- This Device is Pb−Free and is RoHS Compliant

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V_{DD}	−0.5 to +18.0	V
Input Voltage Range, All Inputs	V_{in}	−0.5 to V_{DD} + 0.5	V
DC Input Current per Pin	I_{in}	±10	mA
Power Dissipation per Package (Note 1)	P_D	500	mW
Operating Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Temperature Derating: “D/DW” Package: –7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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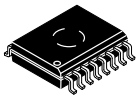
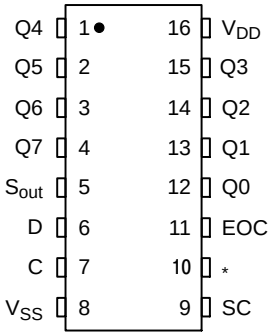


1

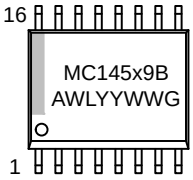
SOIC−16 WB
DW SUFFIX
CASE 751G

PIN ASSIGNMENT



*For MC14549B Pin 10 is MR input.
For MC14559B Pin 10 is FF input.

MARKING DIAGRAM



x = 4 or 5
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

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TRUTH TABLES

MC14549B

SC	$SC_{(t-1)}$	MR	$MR_{(t-1)}$	Clock	Action
X	X	X	X	↘	None
X	X	1	X	↗	Reset
1	0	0	0	↗	Start Conversion
1	X	0	1	↗	Start Conversion
1	1	0	0	↗	Continue Conversion
0	X	0	X	↗	Continue Previous Operation

X = Don't Care t−1 = State at Previous Clock ↗

MC14559B

SC	$SC_{(t-1)}$	EOC	Clock	Action
X	X	X	↘	None
1	0	0	↗	Start Conversion
X	1	0	↗	Continue Conversion
0	0	0	↗	Continue Conversion
0	X	1	↗	Retain Conversion Result
1	X	1	↗	Start Conversion

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	−55°C Min	−55°C Max	25°C Min	25°C Typ (Note 2)	25°C Max	125°C Min	125°C Max	Unit
Output Voltage "0" Level V_{in} = V_{DD} or 0	V_{OL}	5.0 10 15	− − −	0.05 0.05 0.05	− − −	0 0 0	0.05 0.05 0.05	− − −	0.05 0.05 0.05	Vdc
"1" Level V_{in} = 0 or V_{DD}	V_{OH}	5.0 10 15	4.95 9.95 14.95	− − −	4.95 9.95 14.95	5.0 10 15	− − −	4.95 9.95 14.95	− − −	Vdc
Input Voltage (Note 2) "0" Level (V_O = 4.5 or 0.5 Vdc) (V_O = 9.0 or 1.0 Vdc) (V_O = 13.5 or 1.5 Vdc)	V_{IL}	 5.0 10 15	 − − −	 1.5 3.0 4.0	 − − −	 2.25 4.50 6.75	 1.5 3.0 4.0	 − − −	 1.5 3.0 4.0	Vdc
"1" Level (V_O = 0.5 or 4.5 Vdc) (V_O = 1.0 or 9.0 Vdc) (V_O = 1.5 or 13.5 Vdc)	V_{IH}	 5.0 10 15	 3.5 7.0 11	 − − −	 3.5 7.0 11	 2.75 5.50 8.25	 − − −	 3.5 7.0 11	 − − −	Vdc
Output Drive Current (V_{OH} = 2.5 Vdc) Source (V_{OH} = 4.6 Vdc) (V_{OH} = 9.5 Vdc) (V_{OH} = 13.5 Vdc)	I_{OH}	 5.0 5.0 10 15	 –1.2 –0.25 –0.62 –1.8	 − − − −	 –1.0 –0.2 −0.5 –1.5	 –1.7 –0.36 –0.9 –3.5	 − − − −	 –0.7 –0.14 –0.35 –1.1	 − − − −	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) Q Outputs (V_{OL} = 1.5 Vdc)	I_{OL}	5.0 10 15	1.28 3.2 8.4	− − −	1.02 2.6 6.8	1.76 4.5 17.6	− − −	0.72 1.8 4.8	− − −	mAdc
(V_{OL} = 0.4 Vdc) Sink (V_{OL} = 0.5 Vdc) Pin 5, 11 only (V_{OL} = 1.5 Vdc)		5.0 10 15	0.64 1.6 4.2	− − −	0.51 1.3 3.4	0.88 2.25 8.8	− − −	0.36 0.9 2.4	− − −	mAdc
Input Current	I_{in}	15	−	±0.1	−	±0.00001	±0.1	−	±1.0	μAdc
Input Capacitance	C_{in}	−	−	−	−	5.0	7.5	−	−	pF
Quiescent Current (Per Package) (Clock = 0 V, Other Inputs = V_{DD} or 0 V, I_{out} = 0 μA)	I_{DD}	5.0 10 15	− − −	5.0 10 20	− − −	0.005 0.010 0.015	5.0 10 20	− − −	150 300 600	μAdc
Total Supply Current (Note 3, 4) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0 10 15	I_T = (0.8 μA/kHz) f + I_{DD} I_T = (1.6 μA/kHz) f + I_{DD} I_T = (2.4 μA/kHz) f + I_{DD}							μAdc

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Noise immunity specified for worst−case input combination.
   Noise Margin for both "1" and "0" level = 1.0 V min @ V_{DD} = 5.0 V
   = 2.0 V min @ V_{DD} = 10 V
   = 2.5 V min @ V_{DD} = 15 V
3. To calculate total supply current at loads other than 50 pF: $I_T(C_L) = I_T(50\ pF) + 3.5 \times 10^{-3} (C_L = 50) V_{DD} f$ where: I_T is in μA (per package), C_L in pF, V_{DD} in V, and f in kHz is input frequency.
4. The formulas given are for the typical characteristics only at 25°C.

SWITCHING CHARACTERISTICS (Note 5) (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD}	Min	Typ	Max	Unit
Output Rise Time	t_{TLH}					ns
t_{TLH} = (3.0 ns/pF) C_L + 30 ns		5.0	–	180	360	
t_{TLH} = (1.5 ns/pF) C_L + 15 ns		10	–	90	180	
t_{TLH} = (1.1 ns/pF) C_L + 10 ns		15	–	65	130	
Output Fall Time	t_{THL}					ns
t_{THL} = (1.5 ns/pF) C_L + 25 ns		5.0	–	100	200	
t_{THL} = (0.75 ns/pF) C_L + 12.5 ns		10	–	50	100	
t_{THL} = (0.55 ns/pF) C_L + 9.5 ns		15	–	40	80	
Propagation Delay Time	t_{PLH},					ns
Clock to Q	t_{PHL}					
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 415 ns		5.0	–	500	1000	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 177 ns		10	–	210	420	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 130 ns		15	–	155	310	
Clock to S_{out}						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 665 ns		5.0	–	750	1500	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 277 ns		10		310	620	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 195 ns		15	–	220	440	
Clock to EOC						
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 215 ns		5.0	–	300	600	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 97 ns		10	–	130	260	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 75 ns		15	–	100	200	
SC, D, FF or MR Setup Time	t_{su}	5.0	250	125	–	ns
		10	100	50	–	
		15	80	40	–	
Clock Pulse Width	$t_{WH(cl)}$	5.0	700	350	–	ns
		10	270	135	–	
		15	200	100	–	
Pulse Width — D, SC, FF or MR	t_{WH}	5.0	500	250	–	ns
		10	200	100	–	
		15	160	80	–	
Clock Rise and Fall Time	t_{TLH},	5.0	–		15	μs
	t_{THL}	10	–		1.0	
		15	–	–	0.5	
Clock Pulse Frequency	f_{cl}	5.0	–	1.5	0.8	MHz
		10	–	3.0	1.5	
		15	–	4.0	2.0	

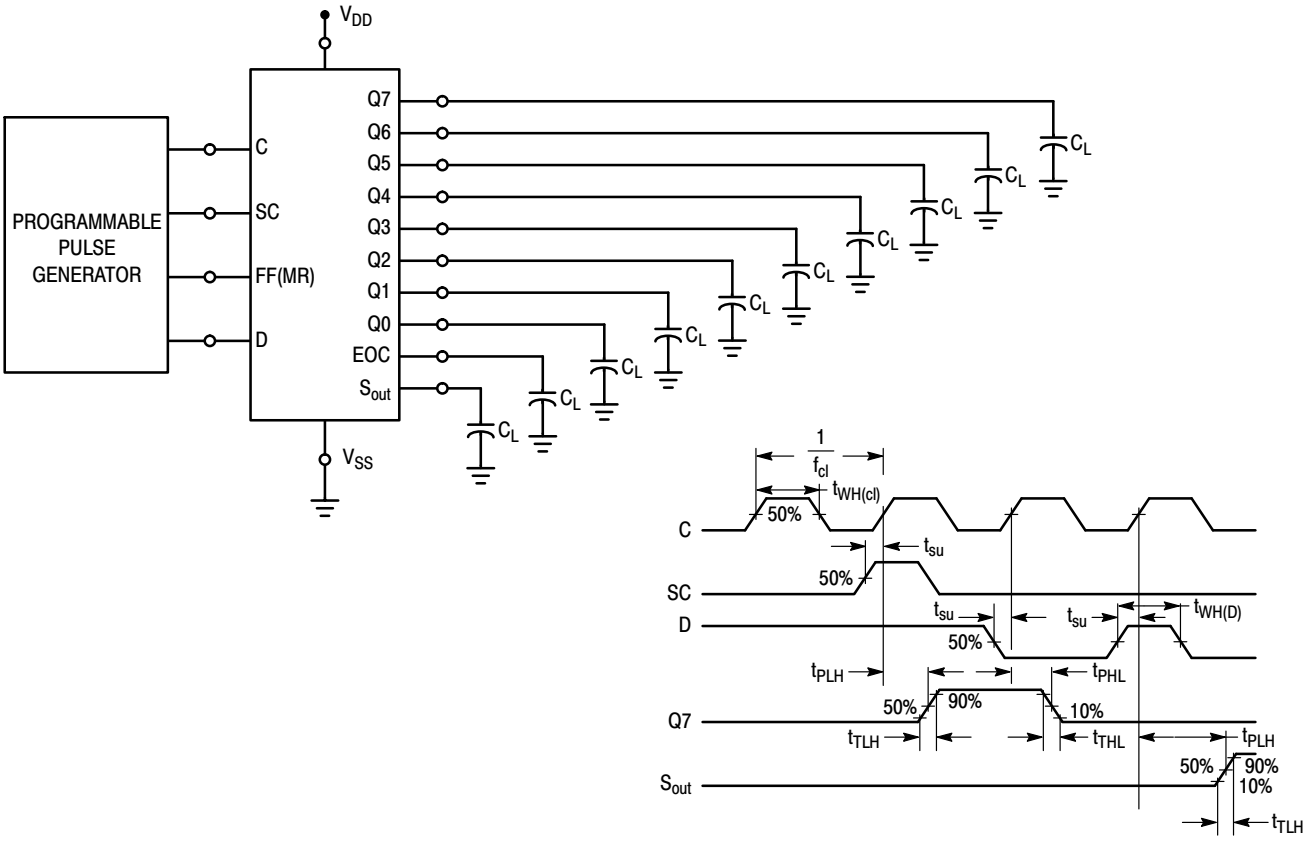
5. The formulas given are for the typical characteristics only.

ORDERING INFORMATION

Device	Package	Shipping†
MC14549BDWR2G	SOIC−16 WB (Pb−Free)	1000 / Tape & Reel
MC14559BDWR2G	SOIC−16 WB (Pb−Free)	1000 / Tape & Reel

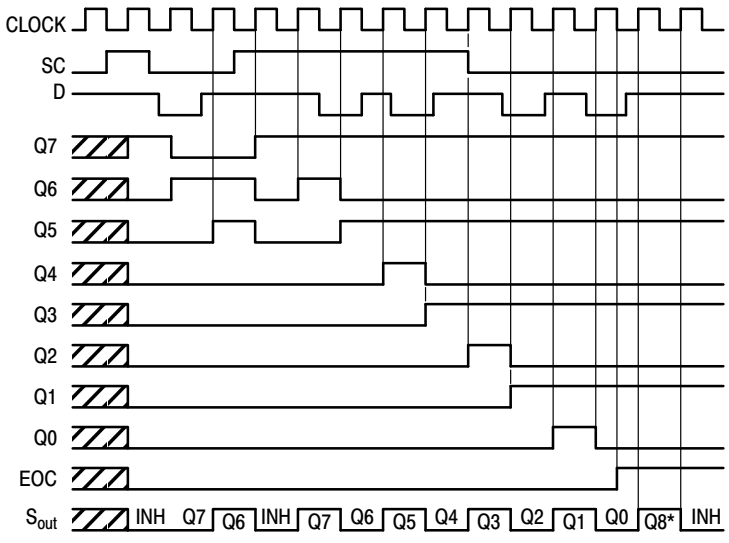
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS



NOTE: Pin 10 = V_{SS}

TIMING DIAGRAM



— Don't care condition

INH — Indicates Serial Out is inhibited low.

* — Q8 is ninth−bit of serial information available from 8−bit register.

NOTE: Pin 10 = V_{SS}

OPERATING CHARACTERISTICS

Both the MC14549B and MC14559B can be operated in either the “free run” or “strobed operation” mode for conversion schemes with any number of bits. Reliable cascading and/or recirculating operation can be achieved if the End of Convert (EOC) output is used as the controlling function, since with EOC = 0 (and with SC = 1 for MC14549B but either 1 or 0 for MC14559B) no stable state exists under continual clocked operation. The MC14559B will automatically recirculate after EOC = 1 during externally strobed operation, provided SC = 1.

All data and control inputs for these devices are triggered into the circuit on the positive edge of the clock pulse.

Operation of the various terminals is as follows:

C = Clock — A positive−going transition of the Clock is required for data on any input to be strobed into the circuit.

SC = Start Convert — A conversion sequence is initiated on the positive−going transition of the SC input on succeeding clock cycles.

D = Data in — Data on this input (usually from a comparator in A/D applications) is also entered into the circuit on a positive−going transition of the clock. This input is Schmitt triggered and synchronized to allow fast response and guaranteed quality of serial and parallel data.

MR = Master Reset (MC14549B Only) — Resets all output to 0 on positive−going transitions of the clock. If removed while SC = 0, the circuit will remain reset until SC = 1. This allows easy cascading of circuits.

FF = Feed Forward (MC14559B Only) — Provides register shortening by removing unwanted bits from a system.

For operation with less than 8 bits, tie the output *following* the least significant bit of the circuit to EOC. E.g., for a 6−bit conversion, tie Q1 to FF; the part will respond as shown in the timing diagram less two bit times. Not that Q1 and Q0 will still operate and must be disregarded.

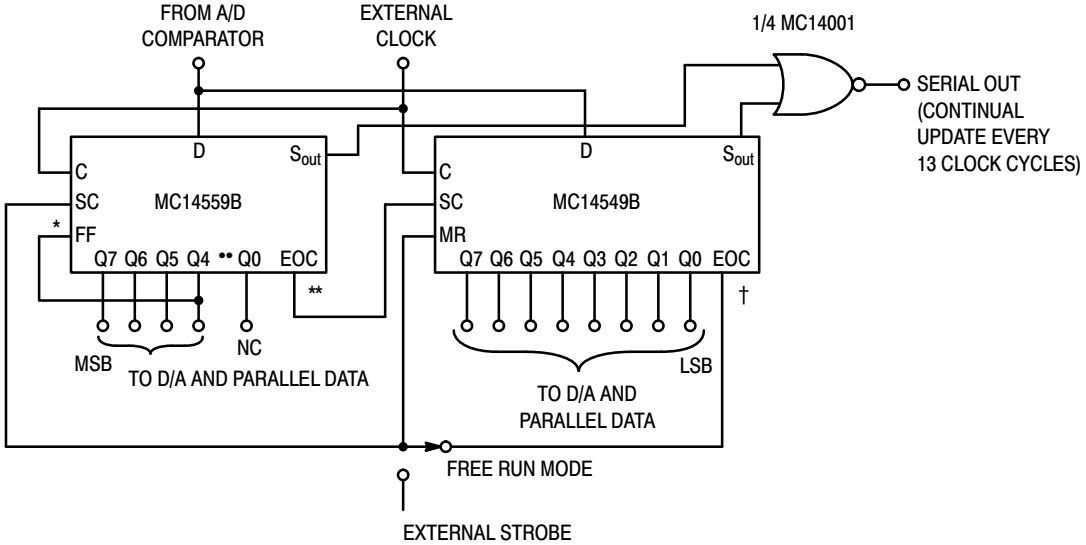
For 8−bit operation, FF is tied to V_{SS}.

For applications with more than 8 but less than 16 bits, use the basic connections shown in Figure 1. The FF input of the MC14559B is used to shorten the setup. Tying FF directly to the least significant bit used in the MC14559B allows EOC to provide the cascading signal, and results in smooth transition of serial information from the MC14559B to the MC14549B. The Serial Out (S_{out}) inhibit structure of the MC14559B remains inactive one cycle after EOC goes high, while S_{out} of the MC14549B remains inhibited until the second clock cycle of its operation.

Q_n = Data Outputs — After a conversion is initiated the Q’s on succeeding cycles go high and are then conditionally reset dependent upon the state of the D input. Once conditionally reset they remain in the proper state until the circuit is either reset or reinitiated.

EOC = End of Convert — This output goes high on the negative−going transition of the clock following FF = 1 (for the MC14559B) or the conditional reset of Q0. This allows settling of the digital circuitry prior to the End of Conversion indication. Therefore either level or edge triggering can indicate complete conversion.

S_{out} = Serial Out — Transmits conversion in serial fashion. Serial data occurs during the clock period when the corresponding parallel data bit is conditionally reset. Serial Out is inhibited on the initial period of a cycle, when the circuit is reset, and on the second cycle after EOC goes high. This provides efficient operation when cascaded.



* FF allows EOC to activate as if in 4−stage register.

** Cascading using EOC guaranteed; no stable unfunctional state.

† Completion of conversion automatically re−initiates cycle in free run mode.

Figure 1. 12−Bit Conversion Scheme

TYPICAL APPLICATIONS

Externally Controlled 6−Bit ADC (Figure 2)

Several features are shown in this application:

- Shortening of the register to six bits by feeding the seventh output bit into the FF input.
- Continuous conversion, if a continuous signal is applied to SC.
- Externally controlled updating (the start pulse must be shorter than the conversion cycle).
- The EOC output indicating that the parallel data are valid and that the serial output is complete.

Continuously Cycling 8−Bit ADC (Figure 3)

This ADC is running continuously because the EOC signal is fed back to the SC input, immediately initiating a new cycle on the next clock pulse.

Continuously Cycling 12−Bit ADC (Figure 4)

Because each successive approximation register (SAR) has a capability of handling only an eight−bit word, two must be cascaded to make an ADC with more than eight bits.

When it is necessary to cascade two SAR's, the second SAR must have a stable resettable state to remain in while awaiting a subsequent start signal. However, the first stage must not have a stable resettable state while recycling, because during switch−on or due to outside influences, the first stage has entered a reset state, the entire ADC will remain in a stable non−functional condition.

This 12−bit ADC is continuously recycling. The serial as well as the parallel outputs are updated every thirteenth clock pulse. The EOC pulse indicates the completion of the 12−bit conversion cycle, the end of the serial output word, and the validity of the parallel data output.

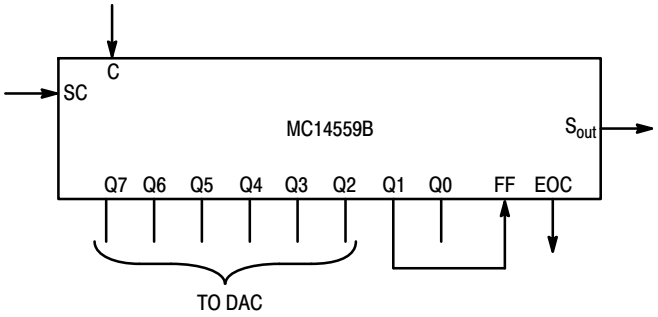


Figure 2. Externally Controlled 6−Bit ADC

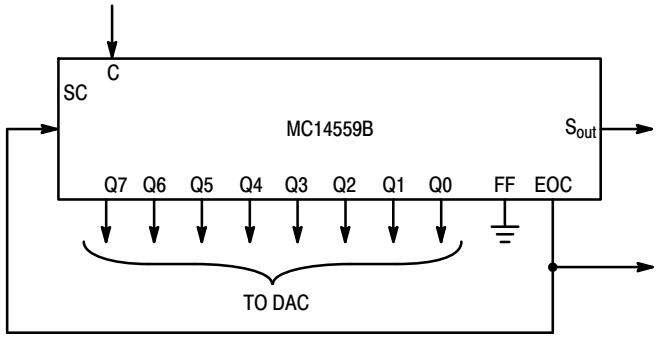


Figure 3. Continuously Cycling 8−Bit ADC

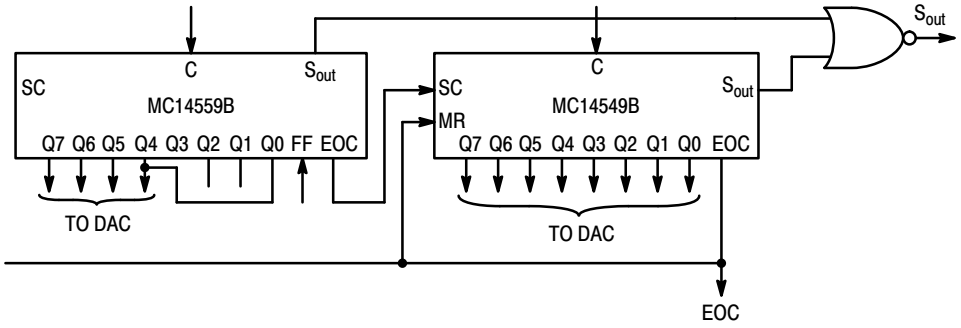


Figure 4. Continuously Cycling 12−Bit ADC

Externally Controlled 12−Bit ADC (Figure 5)

In this circuit the external pulse starts the first SAR and simultaneously resets the cascaded second SAR. When Q4 of the first SAR goes high, the second SAR starts conversion, and the first one stops conversion. EOC indicates that the parallel data are valid and that the serial output is complete. Updating the output data is started with every external control pulse.

Additional Motorola Parts for Successive Approximation ADC

Monolithic digital−to−analog converters — The MC1408/1508 converter has eight−bit resolution and is available with 6, 7, and 8−bit accuracy. **The amplifier−comparator block** — The MC1407/1507 contains a high speed operational amplifier and a high speed comparator with adjustable window.

With these two linear parts it is possible to construct SA−ADCs with an accuracy of up to eight bits, using as the register one MC14549B or one MC14559B. An additional CMOS block will be necessary to generate the clock frequency.

Additional information on successive approximation ADC is found in Motorola Application Note AN−716.

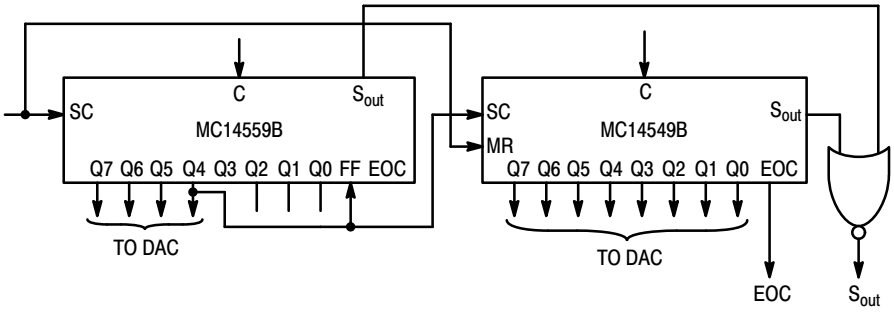
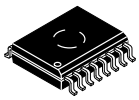


Figure 5. Externally Controlled 12−Bit ADC

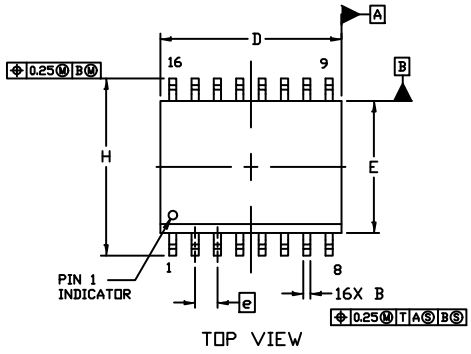
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−16 WB
CASE 751G
ISSUE E

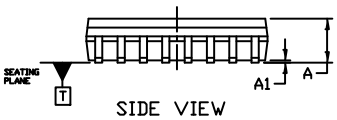
DATE 08 OCT 2021



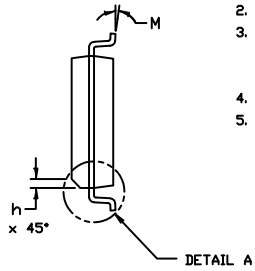
1
SCALE 1:1



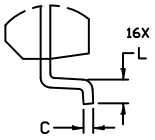
TOP VIEW



SIDE VIEW



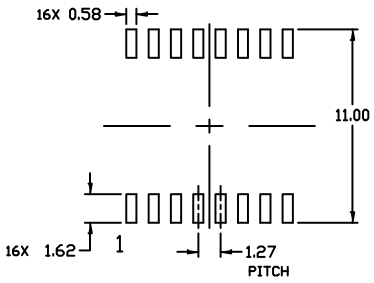
END VIEW



DETAIL A
2X SCALE

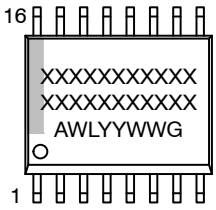
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
5. MAXIMUM MOLD PROTRUSION OR FLASH TO BE 0.15 PER SIDE.

	MILLIMETERS	
DIM	MIN.	MAX.
A	2.35	2.65
A1	0.10	0.25
B	0.35	0.49
C	0.23	0.32
D	10.15	10.45
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.53 REF	
L	0.50	0.90
M	0°	7°



RECOMMENDED
MOUNTING FOOTPRINT

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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