# MC74HC368A

# Hex 3-State Inverting Buffer with Separate 2-Bit and 4-Bit Sections

## High−Performance Silicon−Gate CMOS

The MC74HC368A is identical in pinout to the LS368. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device is arranged into 2−bit and 4−bit sections, each having its own active−low Output Enable. When either of the enables is high, the affected buffer outputs are placed into high−impedance states. The HC368A has inverting outputs.

### Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- These are Pb−Free Devices

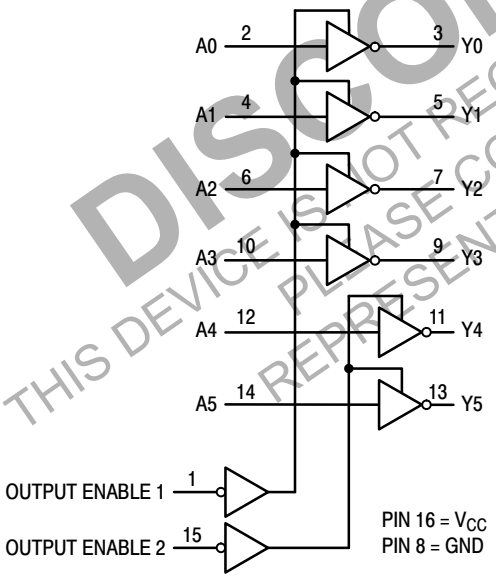
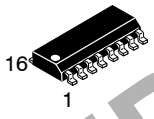



**Figure 1. Logic Diagram**

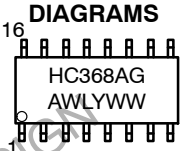
**ON Semiconductor®**

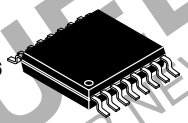
**http://onsemi.com**

### MARKING DIAGRAMS

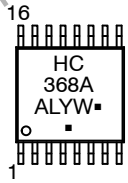



**SOIC−16**
**D SUFFIX**
**CASE 751B**



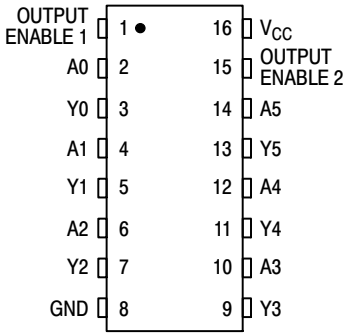




**TSSOP−16**
**DT SUFFIX**
**CASE 948F**




A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G or ▪ = Pb−Free Package
(Note: Microdot may be in either location)

### PIN ASSIGNMENT




### FUNCTION TABLE

| Inputs | | Output |
|---|---|---|
| Enable 1, Enable 2 | A | Y |
| L | L | H |
| L | H | L |
| H | X | Z |

X = don't care
Z = high−impedance

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

© Semiconductor Components Industries, LLC, 2013

## MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | −0.5 to + 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | −0.5 to $V_{CC}$ + 0.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | −0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ±20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ±25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ±50 | mA |
| $P_D$ | Power Dissipation in Still Air, Plastic DIP†<br>SOIC Package†<br>TSSOP Package† | 750<br>500<br>450 | mW |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high−impedance circuit. For proper operation, $V_{in}$ and $V_{out}$ should be constrained to the range GND ≤ ($V_{in}$ or $V_{out}$) ≤ $V_{CC}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{CC}$). Unused outputs must be left open.

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | −55 | +125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time (Figure 2) $V_{CC}$ = 2.0 V<br>$V_{CC}$ = 4.5 V<br>$V_{CC}$ = 6.0 V | 0<br>0<br>0 | 1000<br>500<br>400 | ns |

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

**DC ELECTRICAL CHARACTERISTICS** (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | − 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $V_{IH}$ | Minimum High−Level Input Voltage | $V_{out}$ = 0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 2.0<br>4.5<br>6.0 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V |
| $V_{IL}$ | Maximum Low−Level Input Voltage | $V_{out} = V_{CC}$ − 0.1 V<br>$\|I_{out}\| \le 20\ \mu A$ | 2.0<br>4.5<br>6.0 | 0.3<br>0.9<br>1.2 | 0.3<br>0.9<br>1.2 | 0.3<br>0.9<br>1.2 | V |
| $V_{OH}$ | Minimum High−Level Output Voltage | $V_{in} = V_{IL}$<br>$\|I_{out}\| \le 20\ \mu A$ | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | V |
| | | $V_{in} = V_{IL}$ $\|I_{out}\| \le 6.0$ mA<br>$\|I_{out}\| \le 7.8$ mA | 4.5<br>6.0 | 3.98<br>5.48 | 3.84<br>5.34 | 3.70<br>5.20 | |
| $V_{OL}$ | Maximum Low−Level Output Voltage | $V_{in} = V_{IH}$<br>$\|I_{out}\| \le 20\ \mu A$ | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V |
| | | $V_{in} = V_{IH}$ $\|I_{out}\| \le 6.0$ mA<br>$\|I_{out}\| \le 7.8$ mA | 4.5<br>6.0 | 0.26<br>0.26 | 0.33<br>0.33 | 0.40<br>0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in} = V_{CC}$ or GND | 6.0 | ±0.1 | ±1.0 | ±1.0 | μA |
| $I_{OZ}$ | Maximum Three−State Leakage Current | Output in High−Impedance State<br>$V_{in} = V_{IL}$ or $V_{IH}$<br>$V_{out} = V_{CC}$ or GND | 6.0 | ±0.5 | ±5.0 | ±10 | μA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in} = V_{CC}$ or GND<br>$I_{out}$ = 0 μA | 6.0 | 8 | 80 | 160 | μA |

**AC ELECTRICAL CHARACTERISTICS** ($C_L$ = 50 pF, Input $t_r = t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | − 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{PLH}$,<br>$t_{PHL}$ | Maximum Propagation Delay, Input A to Output Y (Figures 2 and 4) | 2.0<br>4.5<br>6.0 | 95<br>19<br>16 | 120<br>24<br>20 | 145<br>29<br>25 | ns |
| $t_{PLZ}$,<br>$t_{PHZ}$ | Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5) | 2.0<br>4.5<br>6.0 | 175<br>35<br>30 | 220<br>44<br>37 | 265<br>53<br>45 | ns |
| $t_{PZL}$,<br>$t_{PZH}$ | Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 5) | 2.0<br>4.5<br>6.0 | 190<br>38<br>32 | 240<br>48<br>41 | 285<br>57<br>48 | ns |
| $t_{TLH}$,<br>$t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 2 and 4) | 2.0<br>4.5<br>6.0 | 60<br>12<br>10 | 75<br>15<br>13 | 90<br>18<br>15 | ns |
| $C_{in}$ | Maximum Input Capacitance | − | 10 | 10 | 10 | pF |
| $C_{out}$ | Maximum Three−State Output Capacitance (Output in High−Impedance State | − | 15 | 15 | 15 | pF |

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Buffer)* | 40 | pF |

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

## SWITCHING WAVEFORMS

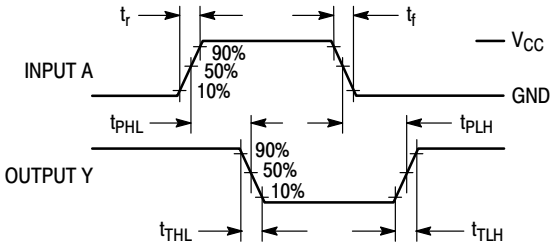



**Figure 2.**

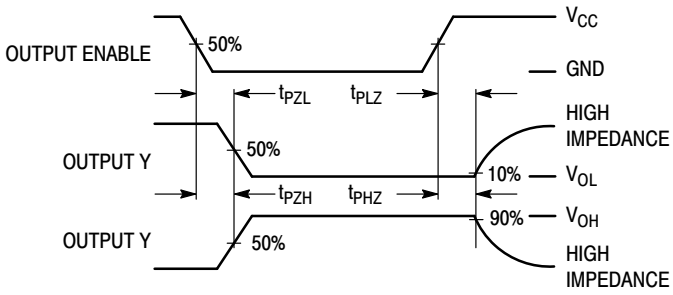
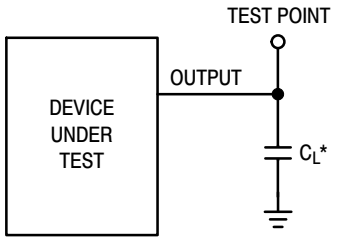


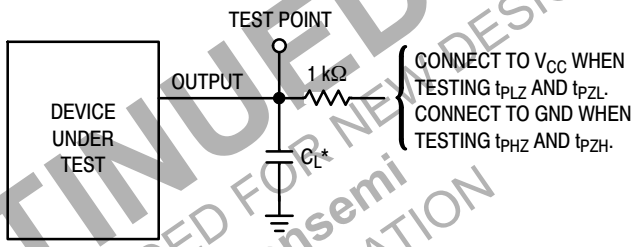

**Figure 3.**

## TEST CIRCUITS




*Includes all probe and jig capacitance

**Figure 4.**




*Includes all probe and jig capacitance

**Figure 5.**

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

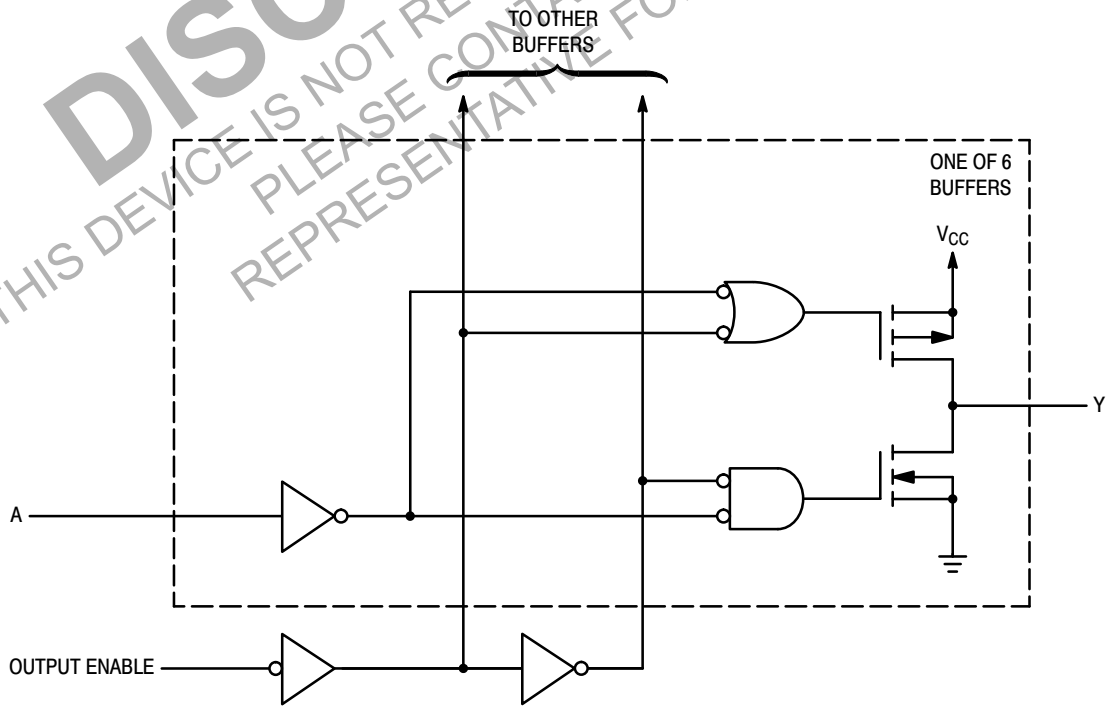



**Figure 6. Logic Detail**

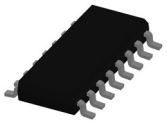
**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| MC74HC368ADG | SOIC−16<br>(Pb−Free) | 48 Units / Rail |
| MC74HC368ADR2G | SOIC−16<br>(Pb−Free) | 2500 Tape & Reel |
| MC74HC368ADTG | TSSOP−16<br>(Pb−Free) | 96 Units / Tube |
| MC74HC368ADTR2G | TSSOP−16<br>(Pb−Free) | 2500 Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DISCONTINUED
THIS DEVICE IS NOT RECOMMENDED FOR NEW DESIGN
PLEASE CONTACT YOUR onsemi
REPRESENTATIVE FOR INFORMATION

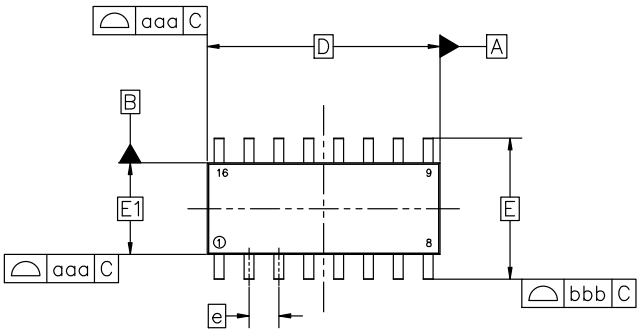
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



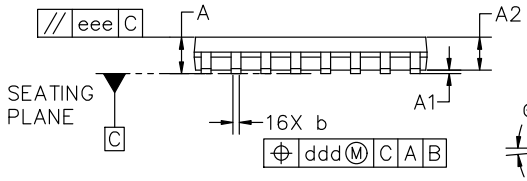
**SOIC−16 9.90x3.90x1.50 1.27P**
CASE 751B
ISSUE L

DATE 29 MAY 2024

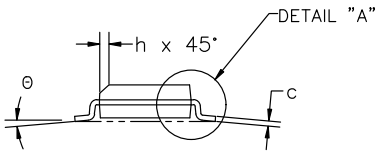
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.




TOP VIEW

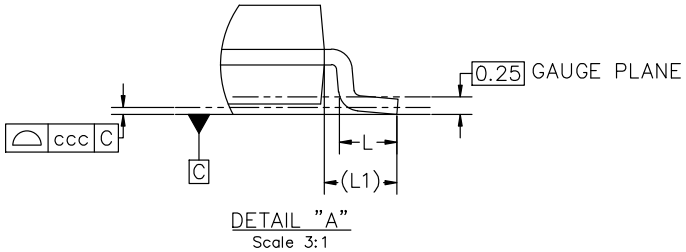



SIDE VIEW

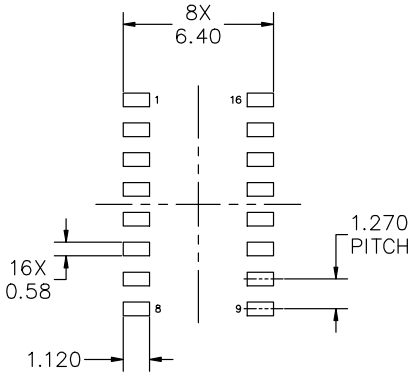



END VIEW

| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 1.35 | 1.55 | 1.75 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | 1.35 | 1.50 | 1.65 |
| b | 0.35 | 0.42 | 0.49 |
| c | 0.19 | 0.22 | 0.25 |
| D | 9.90 BSC | | |
| E | 6.00 BSC | | |
| E1 | 3.90 BSC | | |
| e | 1.27 BSC | | |
| h | 0.25 | −−− | 0.50 |
| L | 0.40 | 0.83 | 1.25 |
| L1 | 1.05 REF | | |
| θ | 0° | −−− | 7° |
| TOLERANCE OF FORM AND POSITION | | | |
| aaa | 0.10 | | |
| bbb | 0.20 | | |
| ccc | 0.10 | | |
| ddd | 0.25 | | |
| eee | 0.10 | | |




DETAIL "A"
Scale 3:1




RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

| DOCUMENT NUMBER: | 98ASB42566B | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
|---|---|---|
| DESCRIPTION: | SOIC−16 9.90X3.90X1.50 1.27P | PAGE 1 OF 2 |

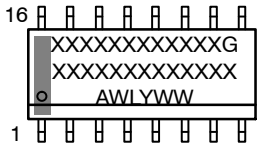
**onsemi** and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

**SOIC−16 9.90x3.90x1.50 1.27P**
CASE 751B
ISSUE L

DATE 29 MAY 2024

**GENERIC**
**MARKING DIAGRAM***




XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

| STYLE 1: | | STYLE 2: | | STYLE 3: | | STYLE 4: | |
|---|---|---|---|---|---|---|---|
| PIN 1. | COLLECTOR | PIN 1. | CATHODE | PIN 1. | COLLECTOR, DYE #1 | PIN 1. | COLLECTOR, DYE #1 |
| 2. | BASE | 2. | ANODE | 2. | BASE, #1 | 2. | COLLECTOR, #1 |
| 3. | EMITTER | 3. | NO CONNECTION | 3. | EMITTER, #1 | 3. | COLLECTOR, #2 |
| 4. | NO CONNECTION | 4. | CATHODE | 4. | COLLECTOR, #1 | 4. | COLLECTOR, #2 |
| 5. | EMITTER | 5. | CATHODE | 5. | COLLECTOR, #2 | 5. | COLLECTOR, #3 |
| 6. | BASE | 6. | NO CONNECTION | 6. | BASE, #2 | 6. | COLLECTOR, #3 |
| 7. | COLLECTOR | 7. | ANODE | 7. | EMITTER, #2 | 7. | COLLECTOR, #4 |
| 8. | COLLECTOR | 8. | CATHODE | 8. | COLLECTOR, #2 | 8. | COLLECTOR, #4 |
| 9. | BASE | 9. | CATHODE | 9. | COLLECTOR, #3 | 9. | BASE, #4 |
| 10. | EMITTER | 10. | ANODE | 10. | BASE, #3 | 10. | EMITTER, #4 |
| 11. | NO CONNECTION | 11. | NO CONNECTION | 11. | EMITTER, #3 | 11. | BASE, #3 |
| 12. | EMITTER | 12. | CATHODE | 12. | COLLECTOR, #3 | 12. | EMITTER, #3 |
| 13. | BASE | 13. | CATHODE | 13. | COLLECTOR, #4 | 13. | BASE, #2 |
| 14. | COLLECTOR | 14. | NO CONNECTION | 14. | BASE, #4 | 14. | EMITTER, #2 |
| 15. | EMITTER | 15. | ANODE | 15. | EMITTER, #4 | 15. | BASE, #1 |
| 16. | COLLECTOR | 16. | CATHODE | 16. | COLLECTOR, #4 | 16. | EMITTER, #1 |

| STYLE 5: | | STYLE 6: | | STYLE 7: | |
|---|---|---|---|---|---|
| PIN 1. | DRAIN, DYE #1 | PIN 1. | CATHODE | PIN 1. | SOURCE N-CH |
| 2. | DRAIN, #1 | 2. | CATHODE | 2. | COMMON DRAIN (OUTPUT) |
| 3. | DRAIN, #2 | 3. | CATHODE | 3. | COMMON DRAIN (OUTPUT) |
| 4. | DRAIN, #2 | 4. | CATHODE | 4. | GATE P-CH |
| 5. | DRAIN, #3 | 5. | CATHODE | 5. | COMMON DRAIN (OUTPUT) |
| 6. | DRAIN, #3 | 6. | CATHODE | 6. | COMMON DRAIN (OUTPUT) |
| 7. | DRAIN, #4 | 7. | CATHODE | 7. | COMMON DRAIN (OUTPUT) |
| 8. | DRAIN, #4 | 8. | CATHODE | 8. | SOURCE P-CH |
| 9. | GATE, #4 | 9. | ANODE | 9. | SOURCE P-CH |
| 10. | SOURCE, #4 | 10. | ANODE | 10. | COMMON DRAIN (OUTPUT) |
| 11. | GATE, #3 | 11. | ANODE | 11. | COMMON DRAIN (OUTPUT) |
| 12. | SOURCE, #3 | 12. | ANODE | 12. | COMMON DRAIN (OUTPUT) |
| 13. | GATE, #2 | 13. | ANODE | 13. | GATE N-CH |
| 14. | SOURCE, #2 | 14. | ANODE | 14. | COMMON DRAIN (OUTPUT) |
| 15. | GATE, #1 | 15. | ANODE | 15. | COMMON DRAIN (OUTPUT) |
| 16. | SOURCE, #1 | 16. | ANODE | 16. | SOURCE N-CH |



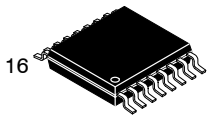
**onsemi** and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

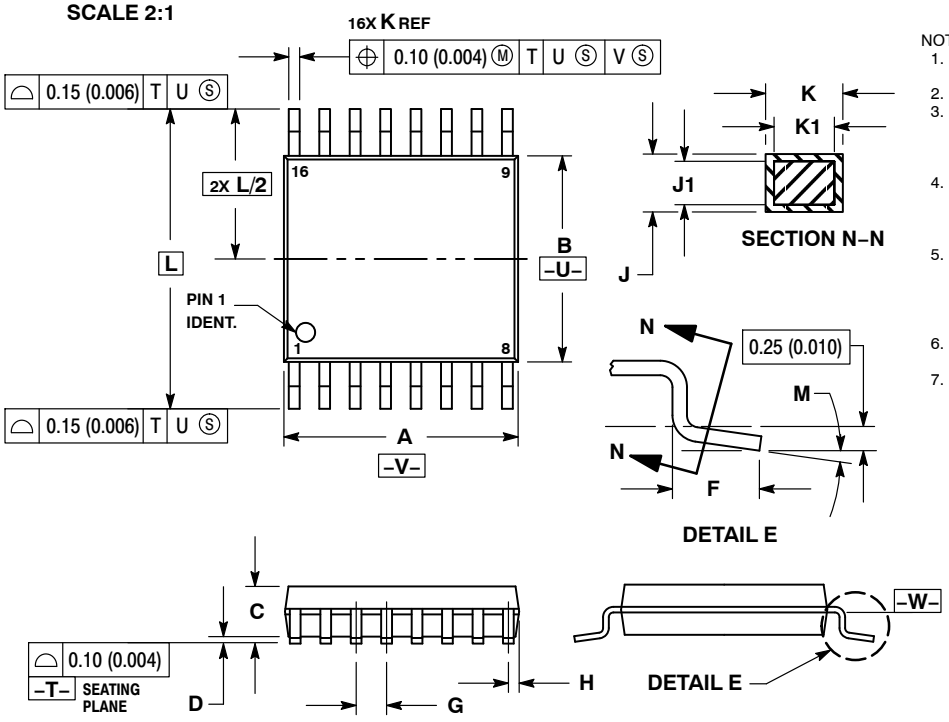
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

**TSSOP−16 WB**
CASE 948F
ISSUE B

DATE 19 OCT 2006



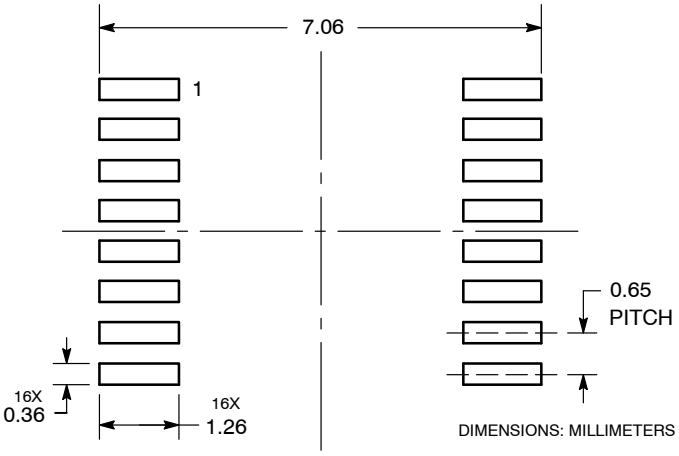

**SCALE 2:1**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

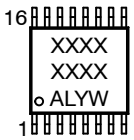
| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | −−− | 1.20 | −−− | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.18 | 0.28 | 0.007 | 0.011 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0 ° | 8 ° | 0 ° | 8 ° |

### RECOMMENDED SOLDERING FOOTPRINT*




*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




| | |
|---|---|
| XXXX | = Specific Device Code |
| A | = Assembly Location |
| L | = Wafer Lot |
| Y | = Year |
| W | = Work Week |
| G or ▪ | = Pb−Free Package |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASH70247A** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| **DESCRIPTION:** | **TSSOP−16** | | **PAGE 1 OF 1** |

**onsemi** and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

**onsemi**, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales