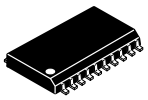
Octal 3-State Non-Inverting Transparent Latch

High−Performance Silicon−Gate CMOS

MC74HC373A, MC74HCT373A



SOIC−20
DW SUFFIX
CASE 751D



TSSOP−20
DT SUFFIX
CASE 948E

The MC74HC373A/MC74HCT373A is identical in pinout to the LS373. The MC74HC373A inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs. The MC74HCT373A may be used as a level converter for interfacing TTL or NMOS outputs to High−Speed CMOS inputs.

The eight latches of this device are transparent D−type latches. While Latch Enable is high, the Q outputs follow the Data Inputs. When Latch Enable goes low, data meeting the setup and hold time becomes latched.

The Output Enable input does not affect the state of the latches, but when Output Enable is high, all outputs are forced to the high−impedance state. Thus, data may be latched even when the outputs are not enabled.

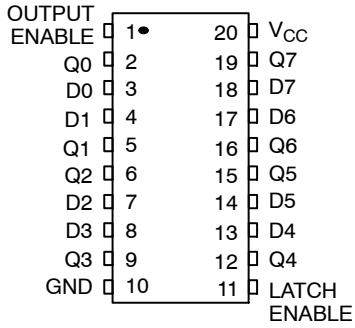
The HC373A/HCT373A is identical in function to the HC573A/HCT573A which has the data inputs on the opposite side of the package from the outputs to facilitate PC board layout.

The HC373A/HCT373A is the non−inverting version of the HC533A/HCT533A.

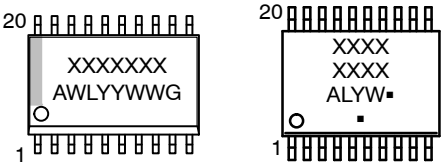
Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS and TTL
- Operating Voltage Range: 2.0 to 6.0 V (HC), 4.5 to 5.5 V (HCT)
- Low Input Current: 1.0 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 196 FETs or 49 Equivalent Gates
- These Devices are Pb−Free and are RoHS Compliant

PIN ASSIGNMENT



MARKING DIAGRAMS



SOIC−20 TSSOP−20

XXXXXXXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
YY, Y	= Year
WW, W	= Work Week
G or ▪	= Pb−Free Package

(Note: Microdot may be in either location)

FUNCTION TABLE

Inputs			Output
Output Enable	Latch Enable	D	Q
L	H	H	H
L	H	L	L
L	L	X	No Change
H	X	X	Z

X = Don't Care
Z = High Impedance

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

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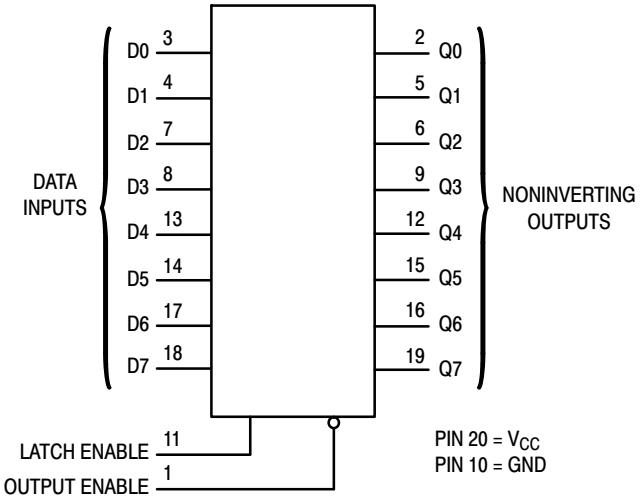


Figure 1. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to V_{CC}+0.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC}+0.5	V
I_{IN}	DC Input Diode Current, per Pin		±20	mA
I_{OUT}	DC Input Diode Current, Per Pin		±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{CC})		±20	mA
I_{OK}	Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{CC})		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC−20W WQFN20 QFN20 TSSOP−20	96 99 111 150	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC−20W WQFN20 QFN20 TSSOP−20	1302 1256 1127 833	mW
MSL	Moisture Sensitivity	SOIC−20W All Other Packages	Level 3 Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	> 2000 > 1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
MC74HC					
V_{CC}	DC Supply Voltage		2.0	6.0	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Note 3)		0	V_{CC}	V
T_A	Operating Free−Air Temperature		−55	+125	°C
t_r, t_f	Input Rise or Fall Time	V_{CC} = 2.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0	1000 500 400	ns
MC74HCT					
V_{CC}	DC Supply Voltage		4.5	5.5	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Note 3)		0	V_{CC}	V
T_A	Operating Free−Air Temperature		−55	+125	°C
t_r, t_f	Input Rise or Fall Time		0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (MC74HC373A)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = V_{CC} − 0.1 V $\|I_{out}\| \le$ 20 μA	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V $\|I_{out}\| \le$ 20 μA	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\| \le$ 20 μA	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} $\|I_{out}\| \le$ 2.4 mA $\|I_{out}\| \le$ 6.0 mA $\|I_{out}\| \le$ 7.8 mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.2 3.7 5.2	
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IL} $\|I_{out}\| \le$ 20 μA	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IL} $\|I_{out}\| \le$ 2.4 mA $\|I_{out}\| \le$ 6.0 mA $\|I_{out}\| \le$ 7.8 mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.4 0.4 0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three−State Leakage Current	Output in High−Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	4.0	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS (MC74HC373A) (See Figures 2 and 3)

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			–55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH} t_{PHL}	Maximum Propagation Delay, Input D to Q	2.0 3.0 4.5 6.0	125 80 25 21	155 110 31 26	190 130 38 32	ns
t_{PLH} t_{PHL}	Maximum Propagation Delay, Latch Enable to Q	2.0 3.0 4.5 6.0	140 90 28 24	175 120 35 30	210 140 42 36	ns
t_{PLZ} t_{PHZ}	Maximum Propagation Delay, Output Enable to Q	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{PZL} t_{PZH}	Maximum Propagation Delay, Output Enable to Q	2.0 3.0 4.5 6.0	150 100 30 26	190 125 38 33	225 150 45 38	ns
t_{TLH} t_{THL}	Maximum Output Transition Time, Any Output	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 32 18 15	ns
C_{in}	Maximum Input Capacitance		10	10	10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High−Impedance State)		15	15	15	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	36	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (MC74HC373A) (See Figures 2 and 3)

Symbol	Parameter	V_{CC} Volts	Guaranteed Limit						Unit
			–55 to 25°C		≤ 85°C		≤ 125°C		
			Min	Max	Min	Max	Min	Max	
t_{su}	Minimum Setup Time, Input D to Latch Enable	2.0 3.0 4.5 6.0	25 20 5.0 5.0		30 25 6.0 6.0		40 30 8.0 7.0		ns
t_h	Minimum Hold Time, Latch Enable to Input D	2.0 3.0 4.5 6.0	5.0 5.0 5.0 5.0		5.0 5.0 5 0 5.0		5.0 5.0 5.0 5.0		ns
t_w	Minimum Pulse Width, Latch Enable	2.0 3.0 4.5 6.0	60 23 12 10		75 27 15 13		90 32 18 15		ns
t_r, t_f	Maximum Input Rise and Fall Times	2.0 3.0 4.5 6.0		1000 800 500 400		1000 800 500 400		1000 800 500 400	ns

DC ELECTRICAL CHARACTERISTICS (MC74HCT373A)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				−55 to 25°C	≤ 85°C	≤ 125°C	
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20$ μA	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 6.0$ mA	4.5	3.98	3.84	3.7	
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20$ μA	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 6.0$ mA	4.5	0.26	0.33	0.4	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	5.5	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three−State Leakage Current	Output in High−Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	5.5	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	5.5	4.0	40	160	μA

ΔI_{CC}	Additional Quiescent Supply Current	V_{in} = 2.4 V, Any One Input V_{in} = V_{CC} or GND, Other Inputs I_{out} = 0 μA	5.5	≥ −55°C	25°C to 125°C		mA
				2.9	2.4		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Total Supply Current = $I_{CC} + \Sigma\Delta I_{CC}$.

AC ELECTRICAL CHARACTERISTICS (MC74HCT373A)

Symbol	Parameter	Guaranteed Limit			Unit
		–55 to 25°C	≤ 85°C	≤ 125°C	
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Input D to Q	28	35	42	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Enable to Q	32	40	48	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q	30	38	45	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q	35	44	53	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output	12	15	18	ns
C_{in}	Maximum Input Capacitance	10	10	10	pF
C_{out}	Maximum Three–State Output Capacitance	15	15	15	pF

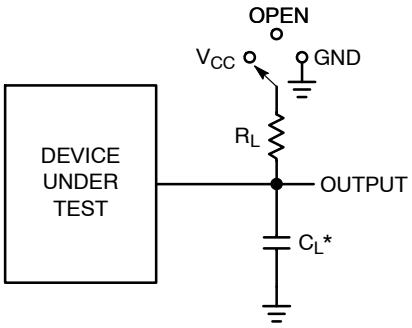
		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Latch)*	65	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (MC74HCT373A)

Symbol	Parameter	Guaranteed Limit			Unit
		–55 to 25°C	≤ 85°C	≤ 125°C	
t_{su}	Minimum Setup Time, Input D to Latch Enable	10	13	15	ns
t_h	Minimum Hold Time, Latch Enable to Input D	10	13	15	ns
t_w	Minimum Pulse Width, Latch Er	12	15	18	ns
t_r, t_f	Maximum Input Rise and Fall Times	500	500	500	ns

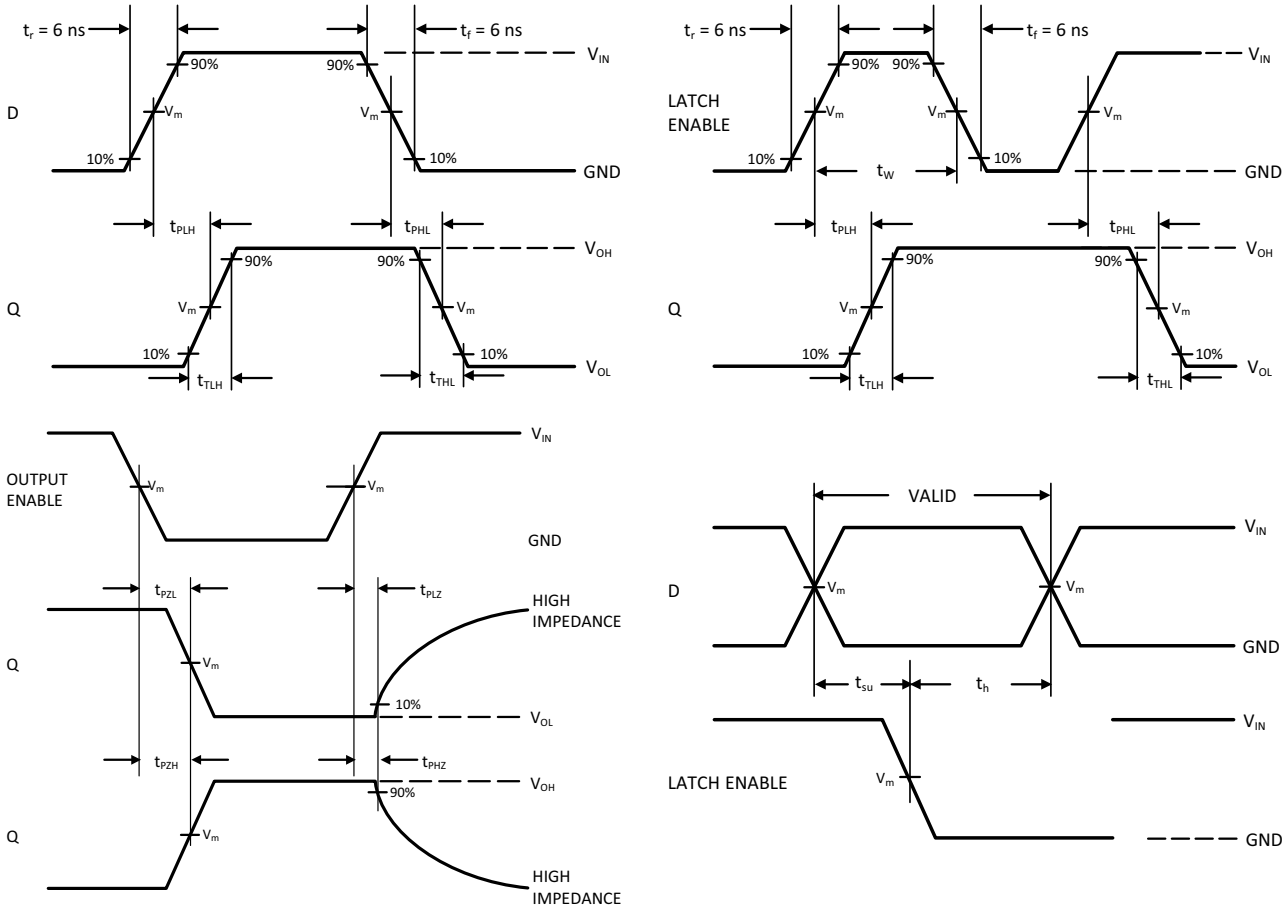
SWITCHING WAVEFORMS



*C_L Includes probe and jig capacitance

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	50 pF	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

Figure 2. Test Circuit



Device	V_{IN}, V	V_m, V
MC74HC373A	V_{CC}	50% x V_{CC}
MC74HCT373A	3 V	1.3 V

Figure 3. Switching Waveforms

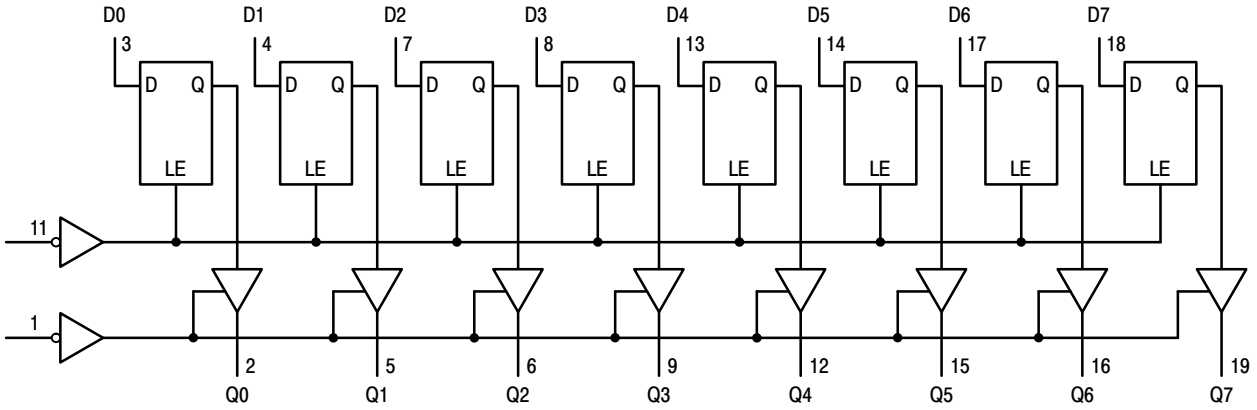


Figure 4. Expanded Logic Diagram

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74HC373ADWG	HC373A	SOIC−20 Wide	38 Units / Rail
MC74HC373ADWR2G	HC373A	SOIC−20 Wide	1000 / Tape & Reel
MC74HC373ADWR2G−Q*	HC373A	SOIC−20 Wide	1000 / Tape & Reel
MC74HC373ADTG	HC 373A	TSSOP−20	75 Units / Rail
MC74HC373ADTR2G	HC 373A	TSSOP−20	2500 / Tape & Reel
MC74HCT373ADWG	HCT373A	SOIC−20 Wide	38 Units / Rail
MC74HCT373ADWR2G	HCT373A	SOIC−20 Wide	1000 / Tape & Reel
MC74HCT373ADWR2G−Q*	HCT373A	SOIC−20 Wide	1000 / Tape & Reel
MC74HCT373ADTR2G	HCT 373A	TSSOP−20	2500 / Tape & Reel

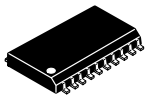
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

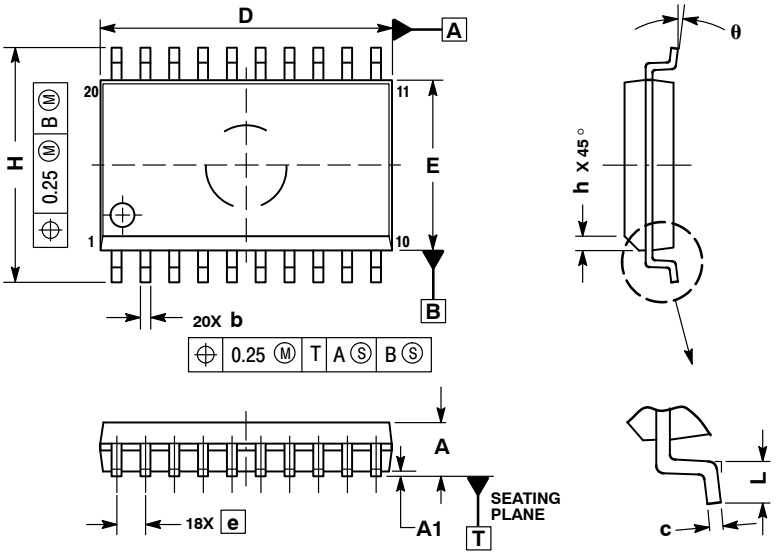
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

SOIC−20 WB
CASE 751D−05
ISSUE H

DATE 22 APR 2015



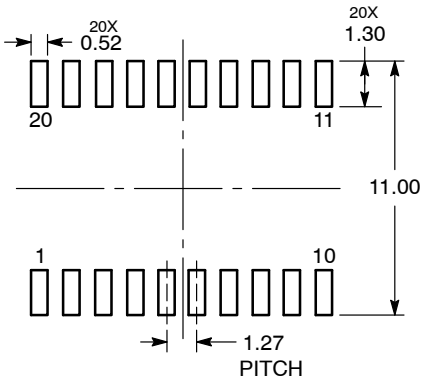
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NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF B DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS	
DIM	MIN	MAX
A	2.35	2.65
A1	0.10	0.25
b	0.35	0.49
c	0.23	0.32
D	12.65	12.95
E	7.40	7.60
e	1.27 BSC	
H	10.05	10.55
h	0.25	0.75
L	0.50	0.90
θ	0°	7°

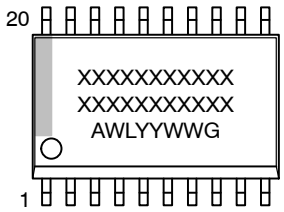
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**SOIC−20 WB**	**PAGE 1 OF 1**

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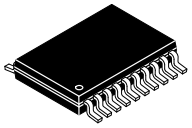
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

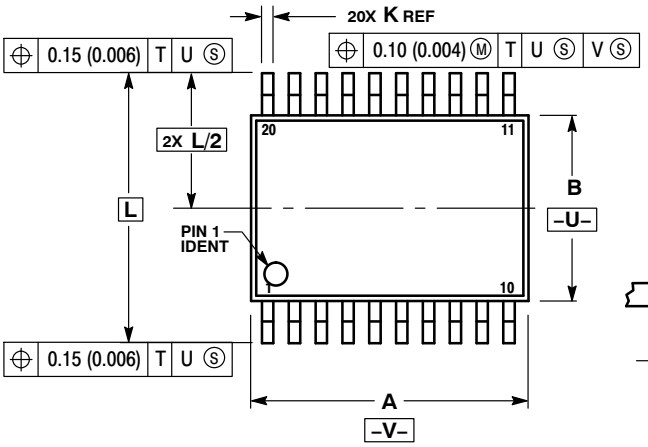
ON Semiconductor®

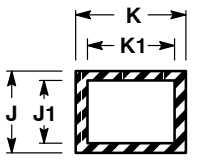
TSSOP−20 WB
CASE 948E
ISSUE D

DATE 17 FEB 2016

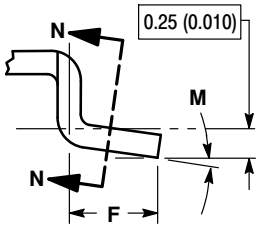


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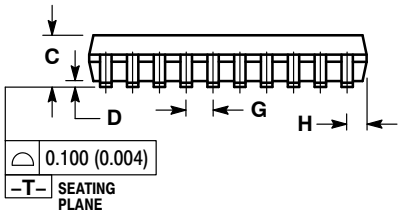


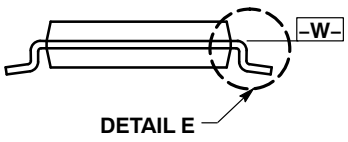


SECTION N−N



DETAIL E

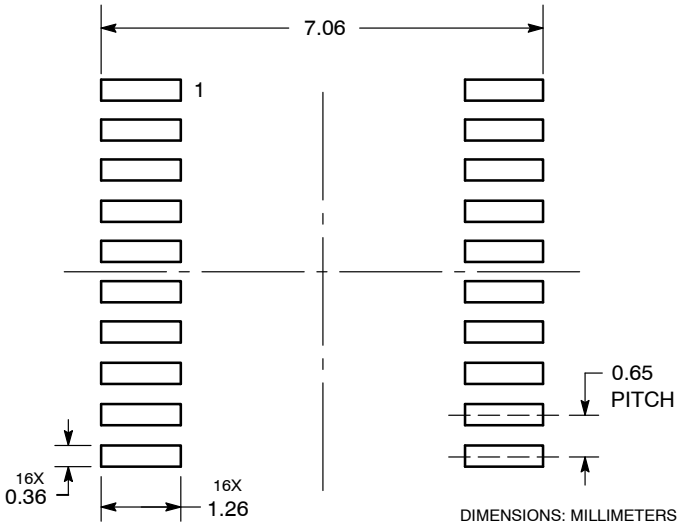




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

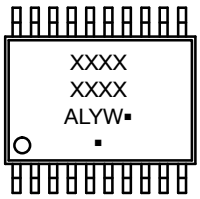
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

SOLDERING FOOTPRINT



DIMENSIONS: MILLIMETERS

GENERIC MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	TSSOP−20 WB	PAGE 1 OF 1

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