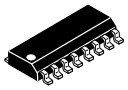
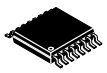
8-Bit Serial or Parallel-Input/Serial-Output Shift Register with 3-State Output

High−Performance Silicon−Gate CMOS

MC74HC589A



SOIC−16
D SUFFIX
CASE 751B



TSSOP−16
DT SUFFIX
CASE 948F



QFN16
MN SUFFIX
CASE 485AW

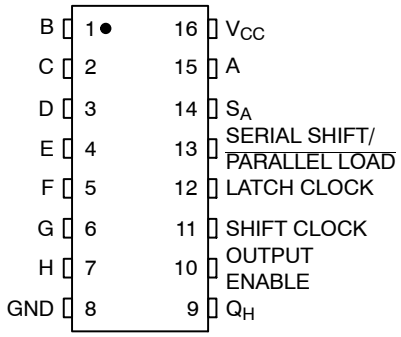
The MC74HC589A device consists of an 8−bit storage latch which feeds parallel data to an 8−bit shift register. Data can also be loaded serially (see the Function Table). The shift register output, Q_H, is a 3−state output, allowing this device to be used in bus−oriented systems.

The HC589A directly interfaces with the SPI serial data port on CMOS MPUs and MCUs.

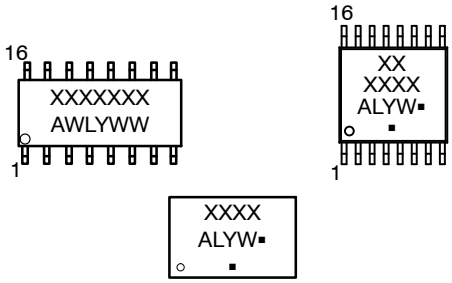
Features

- Output Drive Capability: 15 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1 μA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7 A
- Chip Complexity: 526 FETs or 131.5 Equivalent Gates
- −Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable
- These Devices are Pb−Free, Halogen Free and are RoHS Compliant

PIN ASSIGNMENT



MARKING DIAGRAMS



A	=	Assembly Location
WL, L	=	Wafer Lot
YY, Y	=	Year
WW, W	=	Work Week
G or ▪	=	Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 12 of this data sheet.

© Semiconductor Components Industries, LLC, 2014

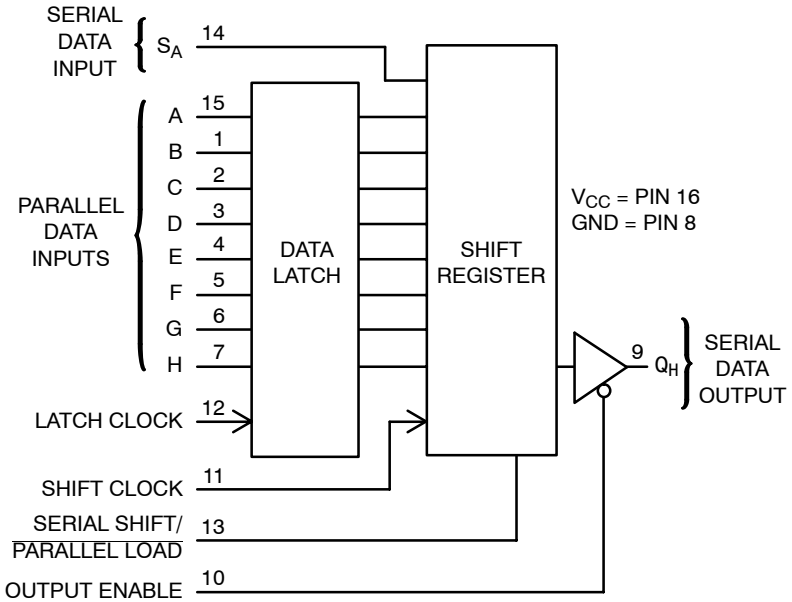


Figure 1. Logic Diagram

FUNCTION TABLE

Operation	Inputs						Resulting Function		
	Output Enable	Serial Shift/ Parallel Load	Latch Clock	Shift Clock	Serial Input S_A	Parallel Inputs A–H	Data Latch Contents	Shift Register Contents	Output Q_H
Force Output into High Impedance State	H	X			X	X	X	X	X Z X
Load Parallel Data into Data Latch	L	H	↗	L, H, ↘	X	a–h	a–h	U	U
Transfer Latch Contents to Shift Register	L	L	L, H, ↘	X	X	X	U	$LR_N \rightarrow$ [SR_N	LR_H
Contents of Input Latch and Shift Register are Unchanged	L	H	L, H, ↘	L, H, ↘	X	X	U	U	U
Load Parallel Data into Data Latch and Shift Register	L	L	↗		X	a–h	a–h	a–h	h X
Shift Serial Data into Shift Register	L	H		↗	D	X	*	SR_A = D, $SR_N \rightarrow$ [SR_{N+1}	X$SR_G \rightarrow$ [SR_H
Load Parallel Data in Data Latch and Shift Serial Data into Shift Register	L	H	↗	↗	D	a–h	a–h	SR_A = D, $SR_N \rightarrow$ [SR_{N+1}	$SR_G \rightarrow$ [SR_H

LR	=	latch register contents	U	=	remains unchanged
SR	=	shift register contents	X	=	don't care
a–h	=	data at parallel data inputs A–H	Z	=	high impedance
D	=	data (L, H) at serial data input S_A	*	=	depends on Latch Clock input

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to V_{CC}+0.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC}+0.5	V
I_{IN}	DC Input Diode Current, per Pin		±20	mA
I_{OUT}	DC Input Diode Current, Per Pin		±35	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current (V_{IN} < 0 or V_{IN} > V_{CC})		±20	mA
I_{OK}	Output Clamp Current (V_{OUT} < 0 or V_{OUT} > V_{CC})		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 1)	SOIC−16 QFN16 TSSOP−16	126 118 159	°C/W
P_D	Power Dissipation in Still Air at 25°C	SOIC−16 QFN16 TSSOP−16	995 1062 787	mW
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.125 in	−
V_{ESD}	ESD Withstand Voltage (Note 2)	Human Body Model Charged Device Model	> 4000 N/A	V
$I_{LATCHUP}$	Latchup Performance (Note 3)		±100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
2. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.
3. Tested to EIA/JESD78 Class II.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)		2.0	6.0	V
V_{in}, V_{out}	DC Input Voltage, Output Voltage	(Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−55	+ 125	°C
t_r, t_f	Input Rise and Fall Time (Figure 3)	V_{CC} = 2.0 V V_{CC} = 3.0 V V_{CC} = 4.5 V V_{CC} = 6.0 V	0 0 0 0	1000 800 500 400	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs may not be left open. All inputs must be tied to a high−logic voltage level or a low−logic input voltage level.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit −55°C to 25°C	Guaranteed Limit ≤85°C	Guaranteed Limit ≤125°C	Unit
V_{IH}	Minimum High−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$	2.0 3.0 4.5 6.0	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	1.5 2.1 3.15 4.2	V
V_{IL}	Maximum Low−Level Input Voltage	V_{out} = 0.1 V or V_{CC} − 0.1 V $\|I_{out}\| \le 20\ \mu A$	2.0 3.0 4.5 6.0	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	0.5 0.9 1.35 1.8	V
V_{OH}	Minimum High−Level Output Voltage	V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	1.9 4.4 5.9	1.9 4.4 5.9	1.9 4.4 5.9	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 2.4$ mA $\|I_{out}\| \le 6.0$ mA $\|I_{out}\| \le 7.8$ mA	3.0 4.5 6.0	2.48 3.98 5.48	2.34 3.84 5.34	2.20 3.70 5.20	
V_{OL}	Maximum Low−Level Output Voltage	V_{in} = V_{IH} $\|I_{out}\| \le 20\ \mu A$	2.0 4.5 6.0	0.1 0.1 0.1	0.1 0.1 0.1	0.1 0.1 0.1	V
		V_{in} = V_{IH} or V_{IL} $\|I_{out}\| \le 2.4$ mA $\|I_{out}\| \le 6.0$ mA $\|I_{out}\| \le 7.8$ mA	3.0 4.5 6.0	0.26 0.26 0.26	0.33 0.33 0.33	0.40 0.40 0.40	
I_{in}	Maximum Input Leakage Current	V_{in} = V_{CC} or GND	6.0	±0.1	±1.0	±1.0	μA
I_{OZ}	Maximum Three−State Leakage Current	Output in High−Impedance State V_{in} = V_{IL} or V_{IH} V_{out} = V_{CC} or GND	6.0	±0.5	±5.0	±10	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{in} = V_{CC} or GND I_{out} = 0 μA	6.0	4	40	160	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} V	Guaranteed Limit −55°C to 25°C	Guaranteed Limit ≤ 85°C	Guaranteed Limit ≤ 125°C	Unit
f_{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 2 and 4)	2.0 3.0 4.5 6.0	6.0 15 30 35	4.8 10 24 28	4.0 8.0 20 24	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Latch Clock to Q_H (Figures 2 and 3)	2.0 3.0 4.5 6.0	175 100 40 30	225 110 50 40	275 125 60 50	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Shift Clock to Q_H (Figures 2 and 4)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Serial Shift/$\overline{\text{Parallel Load}}$ to Q_H (Figures 2 and 6)	2.0 3.0 4.5 6.0	160 90 30 25	200 130 40 30	240 160 48 40	ns
t_{PLZ}, t_{PHZ}	Maximum Propagation Delay, Output Enable to Q_H (Figures 2 and 5)	2.0 3.0 4.5 6.0	150 80 27 23	170 100 30 25	200 130 40 30	ns
t_{PZL}, t_{PZH}	Maximum Propagation Delay, Output Enable to Q_H (Figures 2 and 5)	2.0 3.0 4.5 6.0	150 80 27 23	170 100 30 25	200 130 40 30	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output Figures 2 and 3)	2.0 3.0 4.5 6.0	60 23 12 10	75 27 15 13	90 31 18 15	ns
C_{in}	Maximum Input Capacitance	–	10	10	10	pF
C_{out}	Maximum Three−State Output Capacitance (Output in High−Impedance State)	–	15	15	15	pF

		Typical @ 25°C, V_{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (per Package)*	50	pF

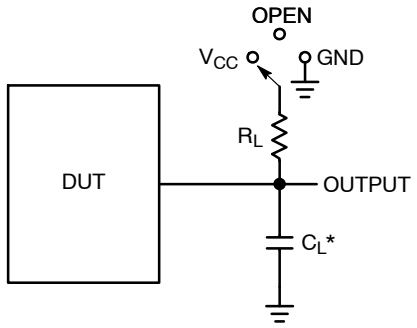
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

*Used to determine the no−load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS

Symbol	Parameter	V_{CC} V	Guaranteed Limit			Unit
			−55°C to 25°C	≤85°C	≤125°C	
t_{su}	Minimum Setup Time, A−H to Latch Clock (Figure 7)	2.0 3.0 4.5 6.0	100 40 20 17	125 50 25 21	150 60 30 26	ns
t_{su}	Minimum Setup Time, Serial Data Input S_A to Shift Clock (Figure 8)	2.0 3.0 4.5 6.0	100 40 20 17	125 50 25 21	150 60 30 26	ns
t_{su}	Minimum Setup Time, Serial Shift/$\overline{\text{Parallel Load}}$ to Shift Clock (Figure 9)	2.0 3.0 4.5 6.0	100 40 20 17	125 50 25 21	150 60 30 26	ns
t_h	Minimum Hold Time, Latch Clock to A−H (Figure 7)	2.0 3.0 4.5 6.0	25 10 5 5	30 12 6 6	40 15 8 7	ns
t_h	Minimum Hold Time, Shift Clock to Serial Data Input S_A (Figure 8)	2.0 3.0 4.5 6.0	5 5 5 5	5 5 5 5	5 5 5 5	ns
t_w	Minimum Pulse Width, Shift Clock (Figure 4)	2.0 3.0 4.5 6.0	75 40 15 13	95 50 19 16	110 60 23 19	ns
t_w	Minimum Pulse Width, Latch Clock (Figure 3)	2.0 3.0 4.5 6.0	80 40 16 14	100 50 20 17	120 60 24 20	ns
t_w	Minimum Pulse Width, Serial Shift/$\overline{\text{Parallel Load}}$ (Figure 6)	2.0 3.0 4.5 6.0	80 40 16 14	100 50 20 17	120 60 24 20	ns
t_r, t_f	Maximum Input Rise and Fall Times (Figure 3)	2.0 3.0 4.5 6.0	1000 800 500 400	1000 800 500 400	1000 800 500 400	ns

SWITCHING WAVEFORMS



*C_L Includes probe and jig capacitance

Test	Switch Position	C_L	R_L
t_{PLH} / t_{PHL}	Open	50 pF	1 kΩ
t_{PLZ} / t_{PZL}	V_{CC}		
t_{PHZ} / t_{PZH}	GND		

Figure 2. Test Circuit

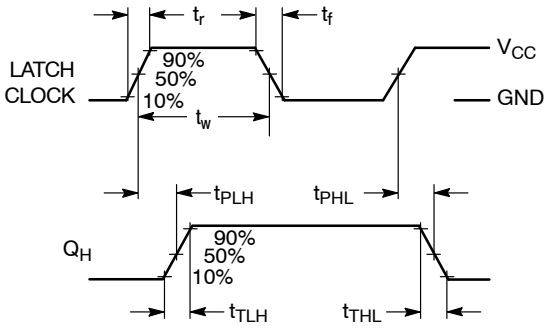


Figure 3. (Serial Shift/$\overline{\text{Parallel Load}}$ = L)

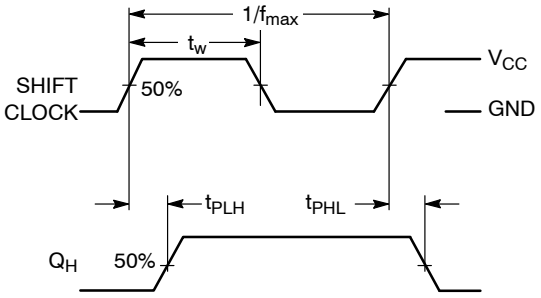


Figure 4. (Serial Shift/$\overline{\text{Parallel Load}}$ = H)

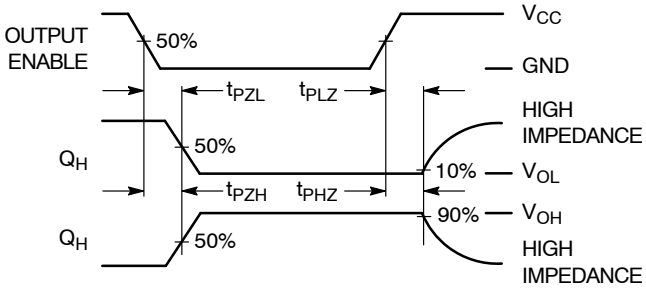


Figure 5.

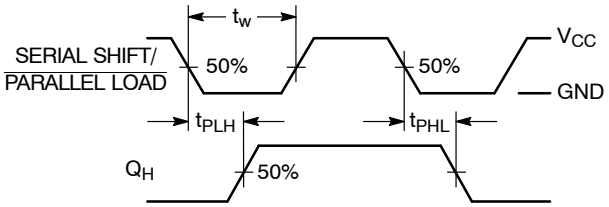


Figure 6.

SWITCHING WAVEFORMS

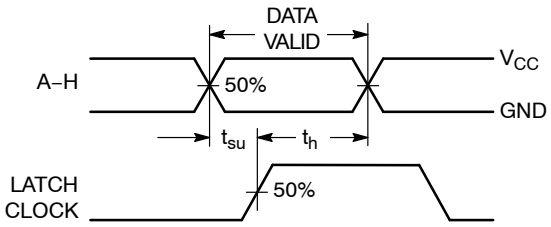


Figure 7.

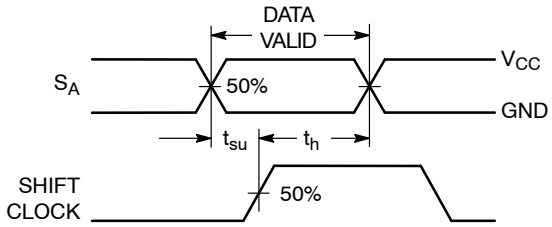


Figure 8.

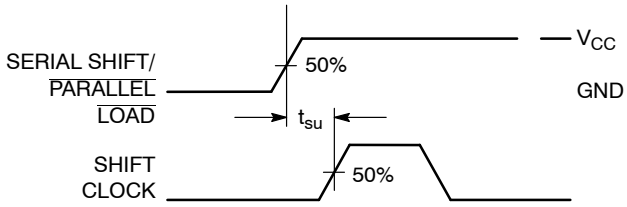


Figure 9.

PIN DESCRIPTIONS

DATA INPUTS

A, B, C, D, E, F, G, H (Pins 15, 1, 2, 3, 4, 5, 6, 7)

Parallel data inputs. Data on these inputs are stored in the data latch on the rising edge of the Latch Clock input.

S_A (Pin 14)

Serial data input. Data on this input is shifted into the shift register on the rising edge of the Shift Clock input if Serial Shift/$\overline{\text{Parallel Load}}$ is high. Data on this input is ignored when Serial Shift/$\overline{\text{Parallel Load}}$ is low.

CONTROL INPUTS

Serial Shift/$\overline{\text{Parallel Load}}$ (Pin 13)

Shift register mode control. When a high level is applied to this pin, the shift register is allowed to serially shift data. When a low level is applied to this pin, the shift register accepts parallel data from the data latch.

Shift Clock (Pin 11)

Serial shift clock. A low−to−high transition on this input shifts data on the serial data input into the shift register and data in stage H is shifted out Q_H, being replaced by the data previously stored in stage G.

Latch Clock (Pin 12)

Data latch clock. A low−to−high transition on this input loads the parallel data on inputs A−H into the data latch.

Output Enable (Pin 10)

Active−low output enable A high level applied to this pin forces the Q_H output into the high impedance state. A low level enables the output. This control does not affect the state of the input latch or the shift register.

OUTPUT

Q_H (Pin 9)

Serial data output. This pin is the output from the last stage of the shift register. This is a 3−state output.

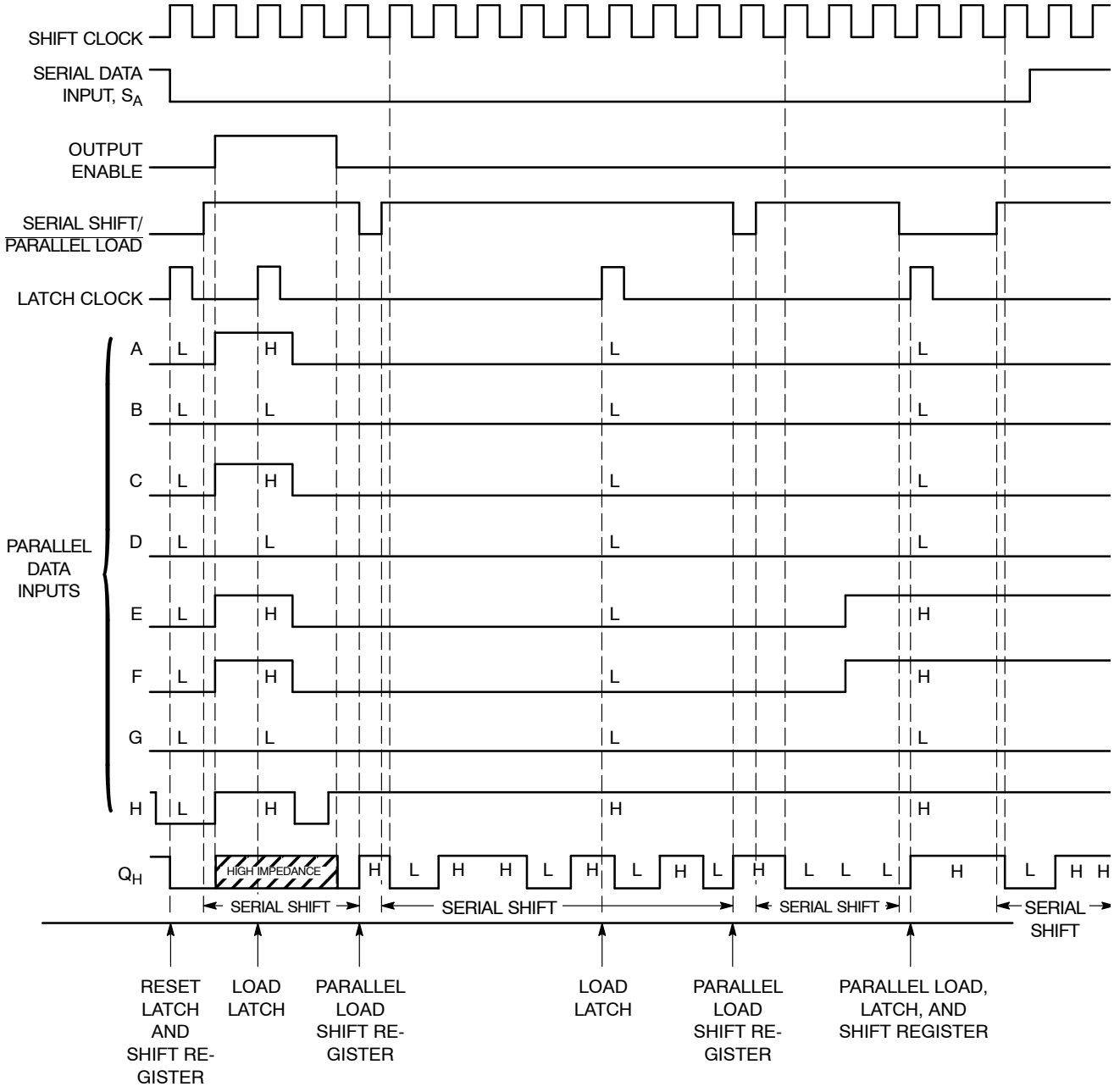
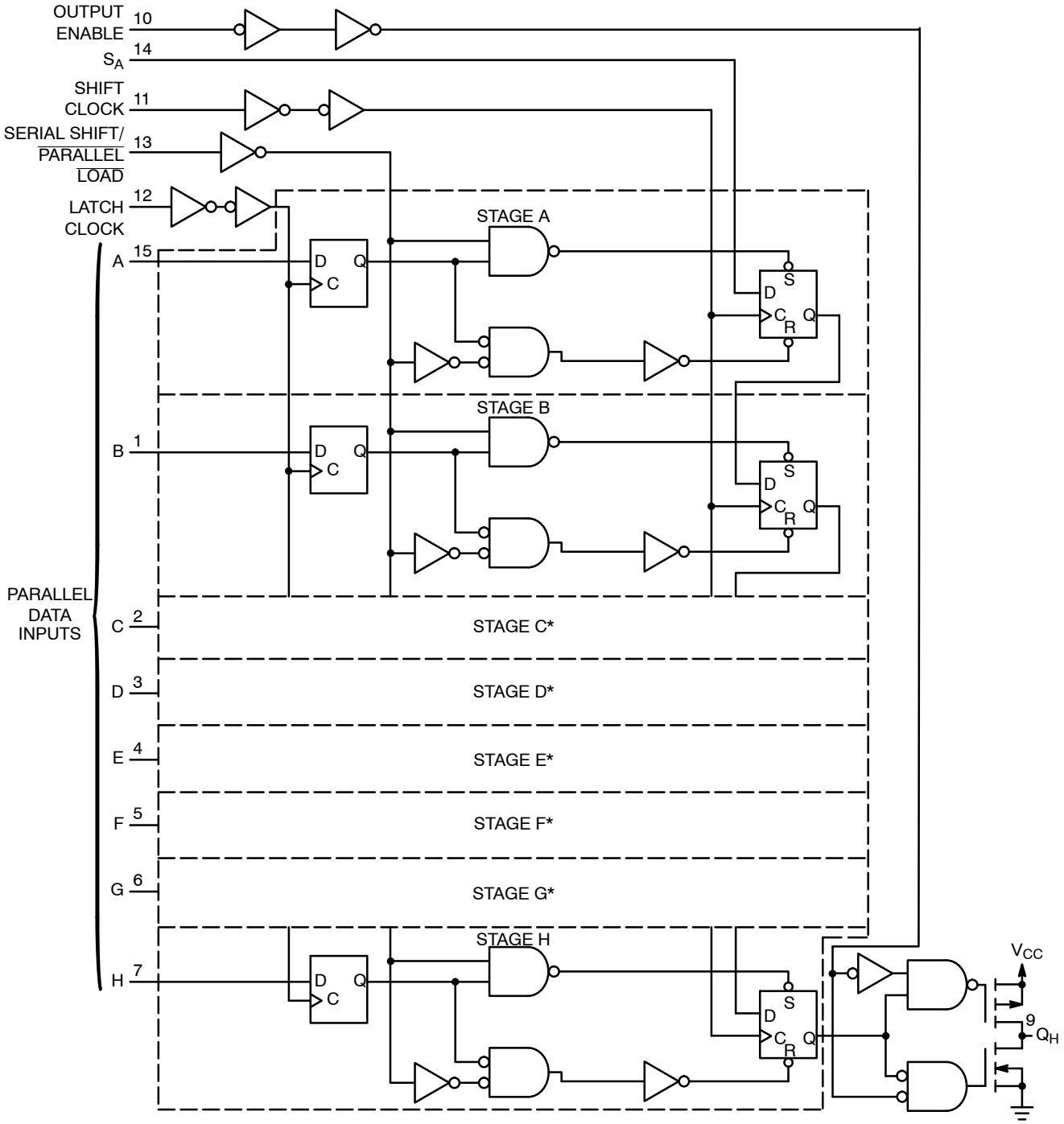


Figure 10. Timing Diagram



*Stages C thru G (not shown in detail) are identical to stages A and B above.

Figure 11. Logic Detail

ORDERING INFORMATION

Device	Marking	Package	Shipping†
MC74HC589ADG	HC589AG	SOIC−16	48 Units / Rail
MC74HC589ADR2G	HC589AG	SOIC−16	2500 / Tape & Reel
MC74HC589ADR2G−Q*	HC589AG	SOIC−16	2500 / Tape & Reel
MC74HC589ADTR2G	HC 589A	TSSOP−16	2500 / Tape & Reel
MC74HC589ADTR2G−Q*	HC 589A	TSSOP−16	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

*−Q Suffix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

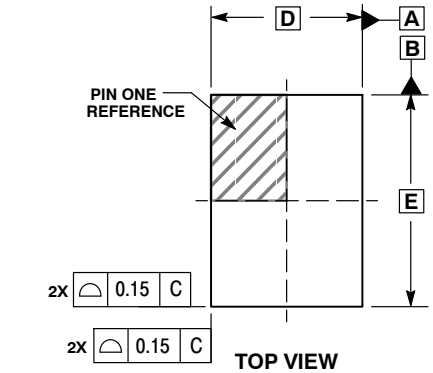
PACKAGE DIMENSIONS

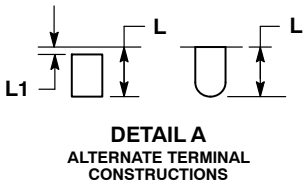
QFN16, 2.5x3.5, 0.5P
CASE 485AW
ISSUE O

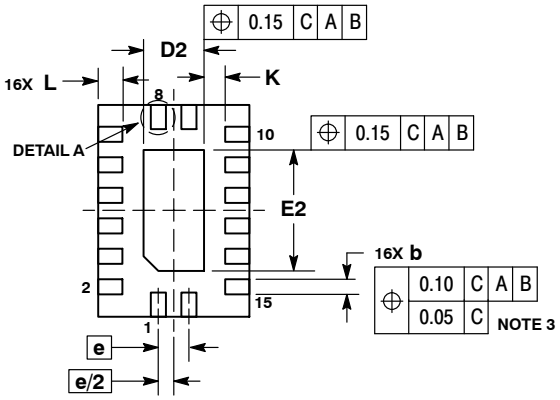
DATE 11 DEC 2008

SCALE 2:1









NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

GENERIC MARKING DIAGRAM*

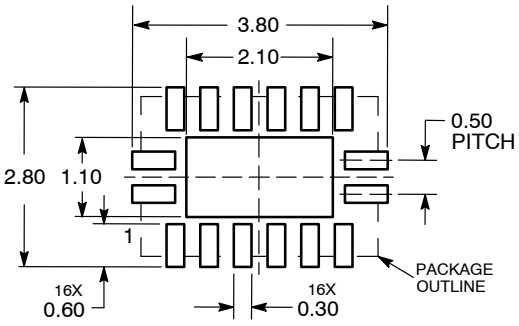


XXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

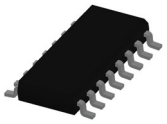
RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

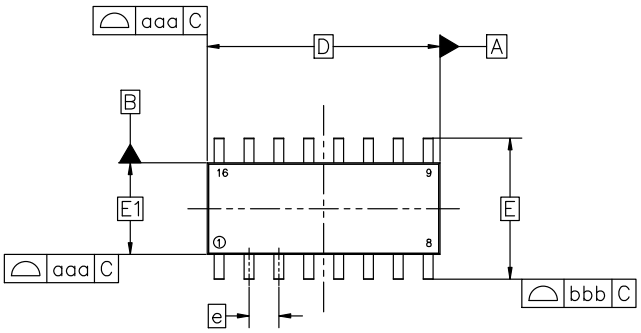
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



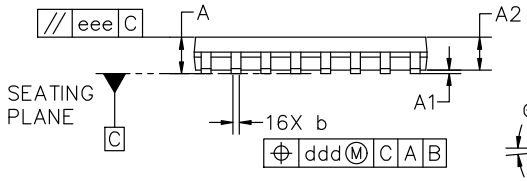
SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

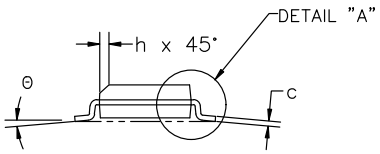
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



TOP VIEW

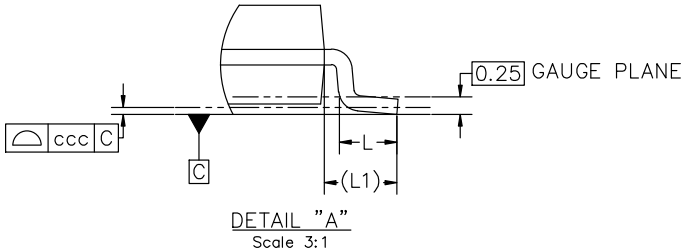


SIDE VIEW

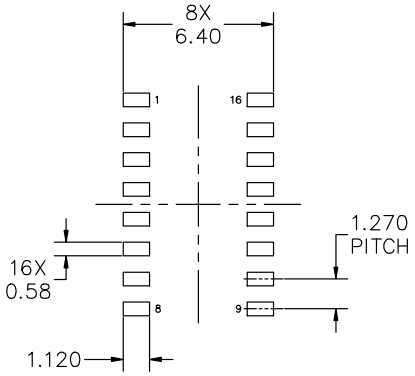


END VIEW

MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.00	0.05	0.10
A2	1.35	1.50	1.65
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	−−−	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	−−−	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



DETAIL "A"
Scale 3:1



RECOMMENDED MOUNTING FOOTPRINT

*FOR ADDITIONAL INFORMATION ON OUR PB−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE onsemi SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D

DOCUMENT NUMBER:	98ASB42566B	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	SOIC−16 9.90X3.90X1.50 1.27P	PAGE 1 OF 2

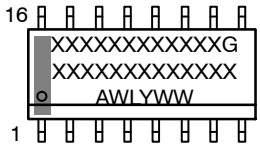
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

SOIC−16 9.90x3.90x1.50 1.27P
CASE 751B
ISSUE L

DATE 29 MAY 2024

GENERIC
MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:	
PIN 1.	COLLECTOR	PIN 1.	CATHODE	PIN 1.	COLLECTOR, DYE #1	PIN 1.	COLLECTOR, DYE #1
2.	BASE	2.	ANODE	2.	BASE, #1	2.	COLLECTOR, #1
3.	EMITTER	3.	NO CONNECTION	3.	EMITTER, #1	3.	COLLECTOR, #2
4.	NO CONNECTION	4.	CATHODE	4.	COLLECTOR, #1	4.	COLLECTOR, #2
5.	EMITTER	5.	CATHODE	5.	COLLECTOR, #2	5.	COLLECTOR, #3
6.	BASE	6.	NO CONNECTION	6.	BASE, #2	6.	COLLECTOR, #3
7.	COLLECTOR	7.	ANODE	7.	EMITTER, #2	7.	COLLECTOR, #4
8.	COLLECTOR	8.	CATHODE	8.	COLLECTOR, #2	8.	COLLECTOR, #4
9.	BASE	9.	CATHODE	9.	COLLECTOR, #3	9.	BASE, #4
10.	EMITTER	10.	ANODE	10.	BASE, #3	10.	EMITTER, #4
11.	NO CONNECTION	11.	NO CONNECTION	11.	EMITTER, #3	11.	BASE, #3
12.	EMITTER	12.	CATHODE	12.	COLLECTOR, #3	12.	EMITTER, #3
13.	BASE	13.	CATHODE	13.	COLLECTOR, #4	13.	BASE, #2
14.	COLLECTOR	14.	NO CONNECTION	14.	BASE, #4	14.	EMITTER, #2
15.	EMITTER	15.	ANODE	15.	EMITTER, #4	15.	BASE, #1
16.	COLLECTOR	16.	CATHODE	16.	COLLECTOR, #4	16.	EMITTER, #1

STYLE 5:		STYLE 6:		STYLE 7:	
PIN 1.	DRAIN, DYE #1	PIN 1.	CATHODE	PIN 1.	SOURCE N-CH
2.	DRAIN, #1	2.	CATHODE	2.	COMMON DRAIN (OUTPUT)
3.	DRAIN, #2	3.	CATHODE	3.	COMMON DRAIN (OUTPUT)
4.	DRAIN, #2	4.	CATHODE	4.	GATE P-CH
5.	DRAIN, #3	5.	CATHODE	5.	COMMON DRAIN (OUTPUT)
6.	DRAIN, #3	6.	CATHODE	6.	COMMON DRAIN (OUTPUT)
7.	DRAIN, #4	7.	CATHODE	7.	COMMON DRAIN (OUTPUT)
8.	DRAIN, #4	8.	CATHODE	8.	SOURCE P-CH
9.	GATE, #4	9.	ANODE	9.	SOURCE P-CH
10.	SOURCE, #4	10.	ANODE	10.	COMMON DRAIN (OUTPUT)
11.	GATE, #3	11.	ANODE	11.	COMMON DRAIN (OUTPUT)
12.	SOURCE, #3	12.	ANODE	12.	COMMON DRAIN (OUTPUT)
13.	GATE, #2	13.	ANODE	13.	GATE N-CH
14.	SOURCE, #2	14.	ANODE	14.	COMMON DRAIN (OUTPUT)
15.	GATE, #1	15.	ANODE	15.	COMMON DRAIN (OUTPUT)
16.	SOURCE, #1	16.	ANODE	16.	SOURCE N-CH

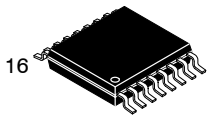
onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

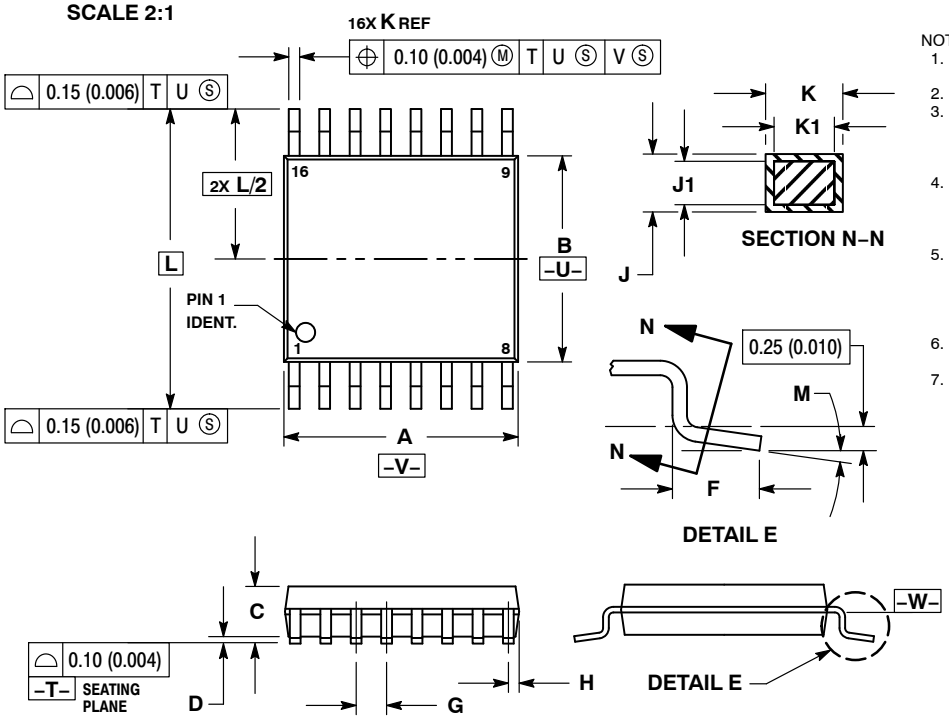
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

TSSOP−16 WB
CASE 948F
ISSUE B

DATE 19 OCT 2006



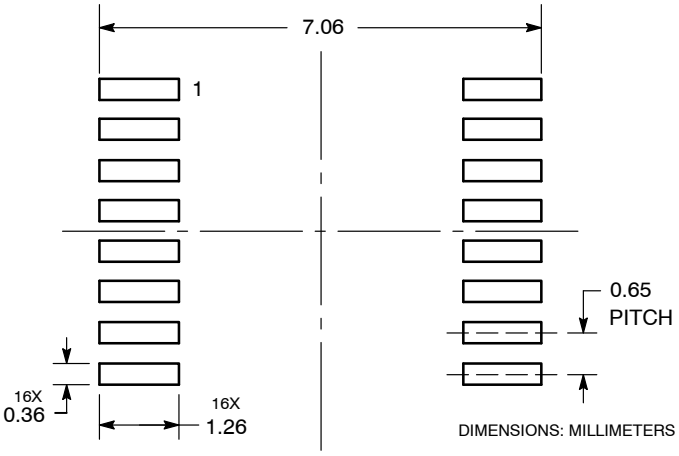
SCALE 2:1



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

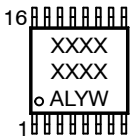
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
G or ▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

DOCUMENT NUMBER:	**98ASH70247A**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**TSSOP−16**		**PAGE 1 OF 1**

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba **onsemi** or its subsidiaries in the United States and/or other countries. **onsemi** reserves the right to make changes without further notice to any products herein. **onsemi** makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. **onsemi** does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

onsemi, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales