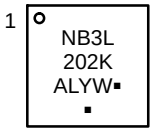
# 2.5 V, 3.3 V Differential 1:2 HCSL Fanout Buffer

# NB3L202K




**QFN16**
**3x3**
**CASE 485FM**

**MARKING DIAGRAM**




NB3L202K = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

## ORDERING INFORMATION

See detailed ordering and shipping information page 13 of this data sheet.

### Description

The NB3L202K is a differential 1:2 Clock fanout buffer with High−speed Current Steering Logic (HCSL) outputs. Inputs can directly accept differential LVPECL, LVDS, and HCSL signals. Single−ended LVPECL, HCSL, LVCMOS, or LVTTL levels are accepted with a proper external Vth reference supply per Figures 4 and 6. The input signal will be translated to HCSL and provides two identical copies operating up to 350 MHz.

The NB3L202K is optimized for ultra−low phase noise, propagation delay variation and low output–to–output skew, and is DB200H compliant. As such, system designers can take advantage of the NB3L202K's performance to distribute low skew clocks across the backplane or the motherboard making it ideal for Clock and Data distribution applications such as PCI Express, FBDIMM, Networking, Mobile Computing, Gigabit Ethernet, etc.

Output drive current is set by connecting a 475 Ω resistor from IREF (Pin 10) to GND per Figure 11. Outputs can also interface to LVDS receivers when terminated per Figure 12.

### Features

- Maximum Input Clock Frequency > 350 MHz
- 2.5 V ±5% / 3.3 V ±10% Supply Voltage Operation
- 2 HCSL Outputs
- DB200H Compliant
- PCIe Gen 3, Gen 4 Compliant
- Individual OE Control Pin for Each Output
- 100 ps Max Output−to−Output Skew Performance
- 1 ns Typical Propagation Delay
- 500 ps Typical Rise and Fall Times
- 80 fs Maximum Additive RMS Phase Jitter
- −40°C to +85°C Ambient Operating Temperature
- QFN 16−pin Package, 3 mm x 3 mm
- These Devices are Pb−Free and are RoHS Compliant

### Typical Applications

- PCI Express
- FBDIMM
- Mobile Computing
- Networking
- Gigabit Ethernet

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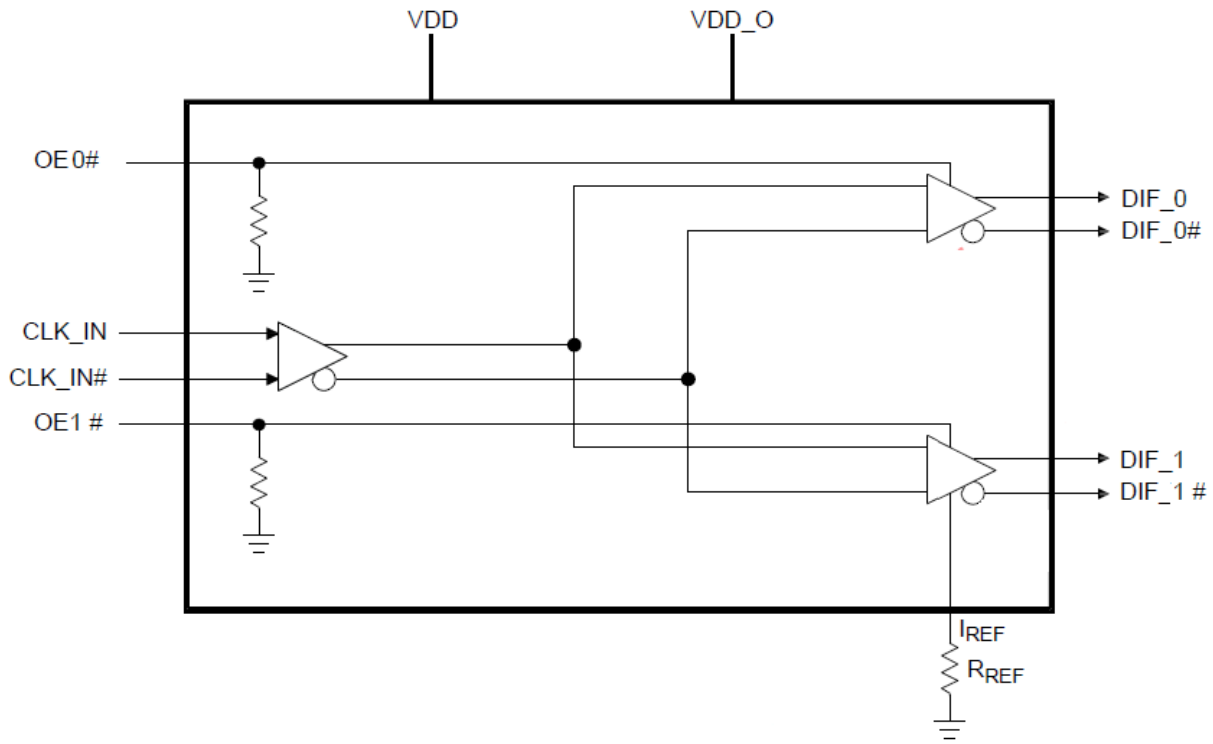



**Figure 1. Simplified Block Diagram**

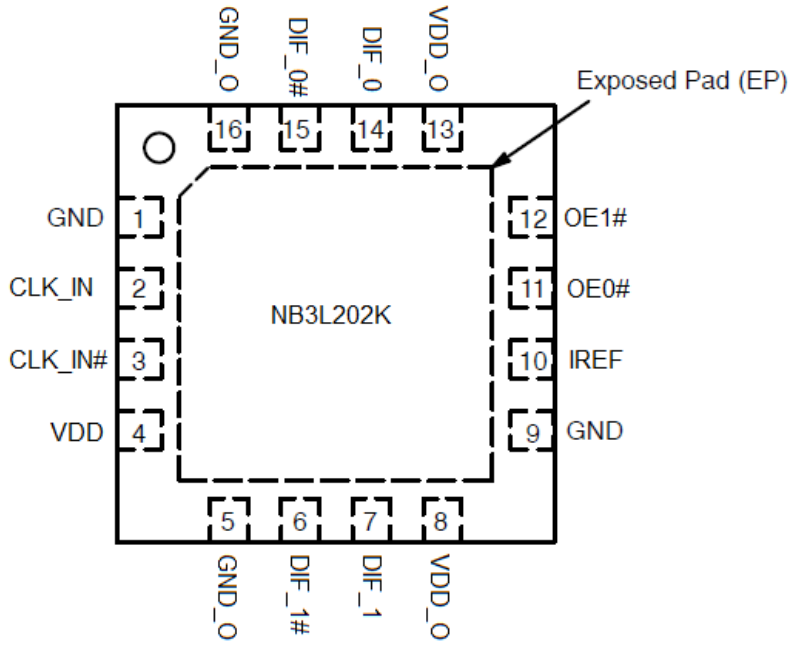



**Figure 2. 16−Pin QFN Pinout**
(Top View)

**Table 1. PIN DESCRIPTION**

| Pin Number | Pin Name | I/O | Description |
|---|---|---|---|
| 1 | GND | Power | Ground |
| 2 | CLK_IN | I, DIF | Differential True input |
| 3 | CLK_IN# | I, DIF | Differential Complementary input |
| 4 | VDD | Power | Core power supply |
| 5 | GND_O | Power | Ground for outputs |
| 6 | DIF_1# | O, DIF | 0.7 V Differential Complementary Output |
| 7 | DIF_1 | O, DIF | 0.7 V Differential True Output |
| 8 | VDD_O | Power | Power supply for outputs |
| 9 | GND | Power | Ground |
| 10 | IREF | I | A precision resistor is attached to this pin to set the differential output current.<br>Use $R_{REF}$ = 475 Ω, 1% for 100 Ω trace, with 50 Ω termination.<br>Use $R_{REF}$ = 412 Ω, 1% for 85 Ω trace, with 43 Ω termination. |
| 11 | OE0# | I, SE | LVTTL / LVCMOS active low input for enabling output DIF_0/0#. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 12 | OE1# | I, SE | LVTTL / LVCMOS active low input for enabling output DIF_1/1#. 0 enables outputs, 1 disables outputs. Internal pull down. |
| 13 | VDD_O | Power | Power supply for outputs |
| 14 | DIF_0 | O, DIF | 0.7 V Differential True Output |
| 15 | DIF_0# | O, DIF | 0.7 V Differential Complementary Output |
| 16 | GND_O | Power | Ground for outputs |
| EP | Exposed Pad | Thermal | The Exposed Pad (EP) on the QFN16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat−sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to GND on the PC board. |

**Table 2. ATTRIBUTES**

| Characteristics | | Value |
|---|---|---|
| ESD Protection | Human Body Model | > 2000 V |
| RPD − Pull−down Resistor | | 50 kΩ |
| Moisture Sensitivity (Note 1) | | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V−0 @ 0.125 in |
| Transistor Count | | 1344 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

1. For additional information, see Application Note AND8003/D.

**Table 3. ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Core Supply Voltage | | − | 4.6 | V |
| $V_{DD_O}$ | I/O Supply Voltage | | − | 4.6 | V |
| $V_{IH}$ | Input High Voltage (Note 2) | | − | 4.6 | V |
| $V_{IL}$ | Input Low Voltage | | −0.5 | − | V |
| $I_{OUT}$ | Maximum Output Current | | − | 24 | mA |
| $T_A$ | Operating Temperature Range | | − | −40 to +85 | °C |
| $T_{stg}$ | Storage Temperature Range | | − | −65 to +150 | °C |
| $\theta_{JA}$ | Thermal Resistance (Junction−to−Ambient) (Note 3) | 0 lfpm<br>500 lfpm | 42<br>35 | | °C/W |
| $\theta_{JC}$ | Thermal Resistance (Junction−to−Case) (Note 3) | | 4 | | °C/W |
| $T_{sol}$ | Wave Solder | | 265 | | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Maximum $V_{IH}$ is not to exceed maximum $V_{DD}$.
3. JEDEC standard multilayer board − 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

**Table 4. DC CHARACTERISTICS** $V_{DD}$ = $V_{DD_O}$ = 3.3 V ±10% or 2.5 V ±5%, $T_A$ = −40°C to 85°C

| Symbol | Characteristics | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **POWER SUPPLY CURRENT** | | | | | | |
| $V_{DD}$ | Core Power Supply Voltage | $V_{DD}$ = 3.3 V ±10%<br>$V_{DD}$ = 2.5 V ±5% | 2.970<br>2.375 | 3.3<br>2.5 | 3.630<br>2.625 | V |
| $V_{DD_O}$ | Output Power Supply Voltage | $V_{DD_O}$ = 3.3 V ±10%<br>$V_{DD_O}$ = 2.5 V ±5% | 2.970<br>2.375 | 3.3<br>2.5 | 3.630<br>2.625 | V |
| $I_{DD}$ + $I_{DD_O}$ | Total Power Supply Current (all outputs active @ 350 MHz, $R_{REF}$ = 412 Ω, $R_L$ = 43 Ω) | | − | 80 | 110 | mA |
| $I_{stdby}$ | Standby Current, all OE pins de−asserted with inputs @ 350 MHz | | − | 50 | 65 | mA |
| $I_{incr}$ | Incremental output current for additional output; One OE Enabled | | − | 15 | 23 | mA |
| $I_{stdby}$ + $I_{incr}$ | Standby Current plus incremental current for one additional differential output; One OE Enabled @ 350 MHz | | − | 65 | 88 | mA |
| **HCSL OUTPUTS** (Notes 4, 5) | | | | | | |
| $V_{OH}$ | Output HIGH Voltage | | 660 | − | 850 | mV |
| $V_{OL}$ | Output LOW Voltage | | −150 | − | − | mV |
| $V_{OUT}$ | Output Swing (Single−Ended)<br>Output Swing (Differential) | | 400<br>800 | 750<br>1500 | −<br>− | mV |
| **DIFFERENTIAL INPUT DRIVEN SINGLE−ENDED** (Note 6) (Figures 4 and 6) | | | | | | |
| $V_{IH}$ | CLK_IN/CLK_IN# Single−ended Input HIGH Voltage | | 0.5 | − | $V_{DD}$ | V |
| $V_{IL}$ | CLK_IN/CLK_IN# Single−ended Input LOW Voltage | | GND | − | $V_{IH}$ − 0.3 | V |
| $V_{th}$ | Input Threshold Reference Voltage Range (Note 7) | | 0.25 | − | $V_{DD}$ − 1.0 | V |
| $V_{ISE}$ | Single−ended Input Voltage ($V_{IH}$ − $V_{IL}$) | | 0.5 | − | VDD | V |
| **DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY** (Note 8) (Figures 5 and 7) | | | | | | |
| $V_{IHD}$ | Differential Input HIGH Voltage | | 0.5 | − | $V_{DD}$ − 0.85 | V |
| $V_{ILD}$ | Differential Input LOW Voltage | | 0 | − | $V_{IHD}$ − 0.25 | V |
| $V_{ID}$ | Differential Input Voltage ($V_{IHD}$ − $V_{ILD}$) | | 0.25 | − | 1.3 | V |
| $V_{IHCMR}$ | Input Common Mode Range (Differential Configuration) (Note 9) (Figure 8) | | 0.5 | − | $V_{DD}$ − 0.85 | V |
| $I_{IL}$ | Input Leakage Current 0 < $V_{IN}$ < $V_{DD}$ (Note 10) | | −5 | − | 5 | μA |
| **LVTTL / LVCMOS INPUTS (OEx#)** | | | | | | |
| $V_{IH}$ | Input HIGH Voltage | | 2.0 | − | $V_{DD}$ + 0.3 | V |
| $V_{IL}$ | Input LOW Voltage | | −0.3 | − | 0.8 | V |
| $I_{IL}$ | Input LOW Current ($V_{IN}$ = GND) | | −10 | − | +10 | μA |
| $I_{IH}$ | Input HIGH Current ($V_{IN}$ = $V_{DD}$) | | − | − | 100 | μA |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Test configuration is $R_S$ = 33.2 Ω, $R_L$ = 49.9, $C_L$ = 2 pF, $R_{REF}$ = 475 Ω.
5. Measurement taken from Single−Ended waveform unless specified otherwise.
6. $V_{IH}$, $V_{IL}$, $V_{th}$ and $V_{ISE}$ parameters must be complied with simultaneously.
7. $V_{th}$ is applied to the complementary input when operating in single−ended mode.
8. $V_{IHD}$, $V_{ILD}$, $V_{ID}$ and $V_{CMR}$ parameters must be complied with simultaneously.
9. The common mode voltage is defined as $V_{IH}$.
10. Does not include inputs with pulldown resistors.

**Table 5. AC TIMING CHARACTERISTICS** $V_{DD}$ = $V_{DD_O}$ = 3.3 V ±10% or 2.5 V ±5%, $T_A$ = −40°C to 85°C (Note 15)

| Symbol | Characteristics | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $F_{max}$ | Maximum Input Frequency | 350 | − | − | MHz |
| $T_{rise}/T_{fall}$ | Rise Time / Fall Time (Notes 13, 17 and 33) (Figure 13) | 175 | 500 | 700 | ps |
| Output Slew Rate | Output Slew Rate (Notes 13 and 17) | 0.5 | − | 2.0 | V/ns |
| $\Delta T_{rise}/\Delta T_{fall}$ | Rise/Fall Time Variation (Notes 17 and 26) | − | − | 125 | ps |
| Slew Rate Matching | (Notes 18, 27 and 28) | − | − | 20% | |
| $V_{high}$ | Voltage High (Notes 17, and 20) (Figure 14) | 660 | 700 | 850 | mV |
| $V_{low}$ | Voltage Low (Notes 17, and 21) (Figure 14) | −150 | 0 | +150 | mV |
| Input Slew Rate | (Note 29 and 32) | 0.35 | − | − | V/ns |
| $V_{cross}$ absolute | Absolute Crossing Point Voltages (Notes 12, 17 and 24)<br>Relative Crossing Point Voltages can be calculated (Notes 16, 17 and 24) (Figure 16) | 250 | − | 550 | mV |
| Total $\Delta V_{cross}$ | Total Variation of Vcross Over All Edges (Notes 17 and 25) | − | − | 140 | mV |
| Duty Cycle | (Note 18) (Figure 15) | 45 | − | 55 | % |
| $V_{ovs}$ | Maximum Voltage (Overshoot) (Notes 17 and 22) (Figure 14) | − | − | $V_{high}$ + 0.3 | V |
| $V_{uds}$ | Maximum Voltage (Undershoot) (Notes 17 and 23) (Figure 14) | − | − | $V_{low}$ − 0.3 | V |
| $V_{rb}$ | Ringback Voltage (Note 17) (Figure 14) | 0.2 | − | N/A | V |
| $T_{oe_lat}$ | OE Latency (Note 11) | 4 | 6 | 12 | Cycles |
| $t_{pd}$ | Input−to−Output Delay CLK_IN, DIF_[1:0] (Note 31) | 0.6 | 1.0 | 1.4 | ns |
| $t_{SKEW}$ | Output−to−Output Skew across 2 outputs DIF_[1:0] (Notes 30 and 31) | 0 | 5.0 | 20 | ps |
| $t_{JITTER\phi}$ | Additive RMS Phase Jitter $f_{carrier}$ = 156.25 MHz, 12 kHz − 20 Mhz Integrated Range | − | 46 | 80 | fs |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

11. Time from deassertion until outputs are >200 mV.
12. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLK#.
13. Measured from $V_{OL}$ = 0.175 V to $V_{OH}$ = 0.525 V. Only valid for Rising Clock and Falling Clock#.
14. This measurement refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing
15. Test configuration is $R_S$ = 33.2 Ω, $R_P$ = 49.9, $C_L$ = 2 pF, $R_{REF}$ = 475 Ω.
16. Vcross(rel) Min and Max are derived using the following, Vcross(rel) Min = 0.250 + 0.5 ($V_{high\ avg}$ − 0.700). Vcross(rel) Max = 0.550 − 0.5 (0.700 – $V_{high\ avg}$), (see Figure 16 for further clarification).
17. Measurement taken from Single Ended waveform.
18. Measurement taken from differential waveform.
19. Unless otherwise noted, all specifications in this table apply to all frequencies.
20. $V_{high}$ is defined as the statistical average High value as obtained by using the Oscilloscope $V_{high}$ Math function.
21. $V_{low}$ is defined as the statistical average Low value as obtained by using the Oscilloscope $V_{low}$ Math function.
22. Overshoot is defined as the absolute value of the maximum voltage.
23. Undershoot is defined as the absolute value of the minimum voltage.
24. The crossing point must meet the absolute and relative crossing point specifications simultaneously.
25. ΔVcross is defined as the total variation of all crossing voltages of Rising CLOCK and Falling CLOCK#. This is the maximum allowed variance in Vcross for any particular system.
26. Measured with oscilloscope, averaging off, using min max statistics. Variation is the delta between min and max.
27. Matching applies to rising edge rate for clock and falling edge rate for Clock#. It is measured using a ±75 mV window centered on the average crosspoint where clock rising meets Clock# falling. The median crosspoint is used to calculate the voltage threshold the oscilloscope is to use for the edge rate calculations.
28. Slew Rate matching is derived using the following, 2 * ($T_{rise}$ – $T_{fall}$) / ($T_{rise}$ + $T_{fall}$).
29. Input slew rate is based on single ended measurement. This is the minimum input slew rate at which the NB3L202K devices are guaranteed to meet all performance specifications.
30. Measured into fixed 2 pF load cap. Input to output skew is measured at the first output edge following the corresponding input.
31. Measured from differential cross−point to differential cross−point with scope averaging on to find mean value.
32. The differential input clock is expected to be sourced from a high performance clock oscillator.
33. Measured at 3.3 V ± 10% with typical HCSL input levels.

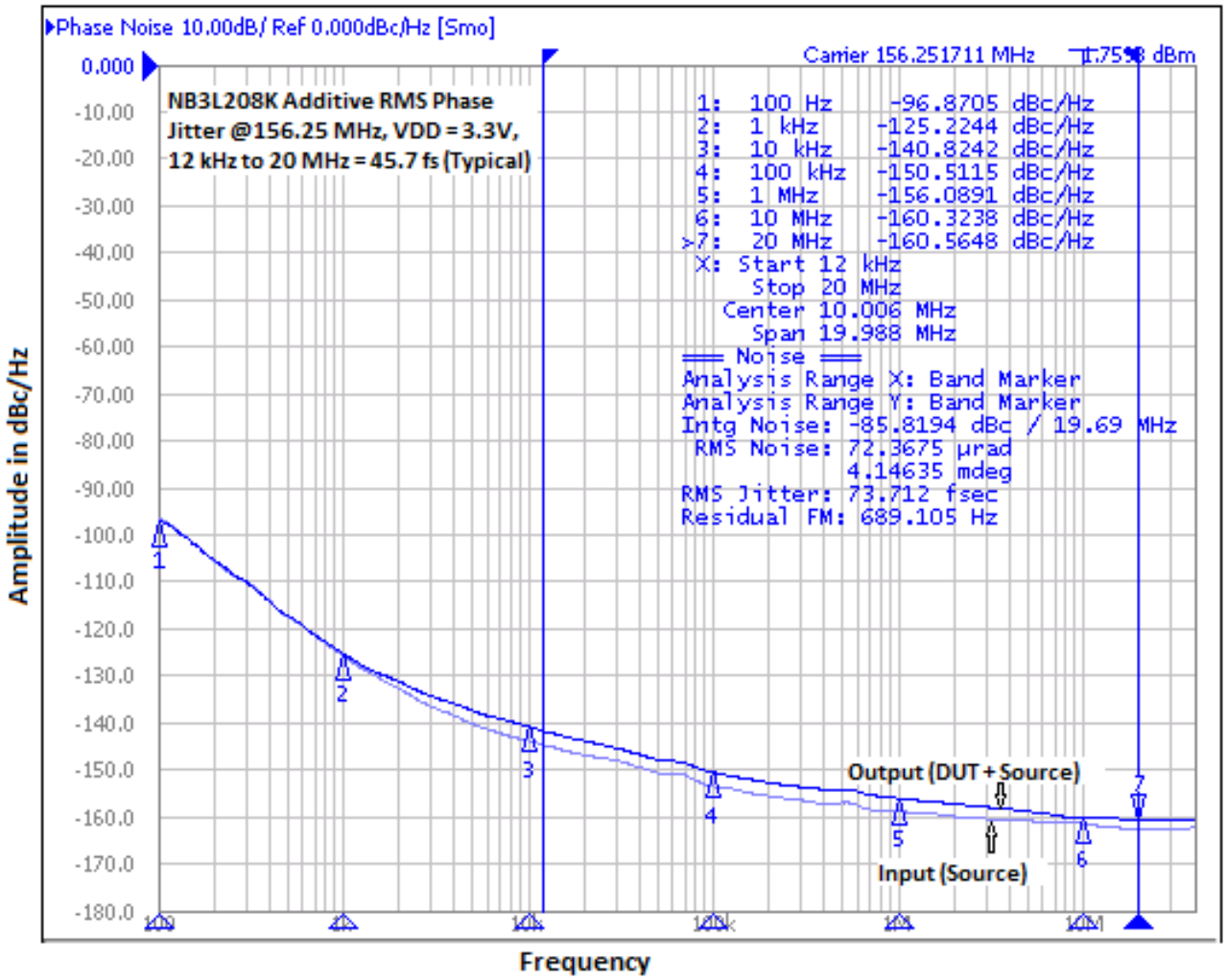



**Figure 3. Typical Phase Noise Plot at $f_{carrier}$ = 156.25 MHz at an Operating Voltage of 3.3 V, Room Temperature**

The above phase noise data was captured using Agilent E5052A/B. The data displays the input phase noise and output phase noise used to calculate the additive phase jitter at a specified integration range. The additive RMS phase jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 45.7 fs.

The additive RMS phase jitter performance of the fanout buffer is highly dependent on the phase noise of the input source.

To obtain the most accurate additive phase noise measurement, it is vital that the source phase noise be notably lower than that of the DUT. If the phase noise of the source is similar or greater than the device under test output, the source noise will dominate the additive phase jitter calculation and lead to an artificially low result for the additive phase noise measurement within the integration range.

$$\text{Additive RMS phase jitter} = \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$$

$$45.7\ \text{fs} = \sqrt{73.7\ \text{fs}^2 - 57.8\ \text{fs}^2}$$

**Table 6. ELECTRICAL CHARACTERISTICS − PHASE JITTER PARAMETERS**
($V_{DD}$ = $V_{DD_O}$ = 3.3 V ±10% or 2.5 V ±5%, $T_A$ = −40°C to 85°C)

| Symbol | Parameter | Conditions (Notes 34 and 39) | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{jphPCIeG1}$ | Additive Phase Jitter | PCIe Gen 1 (Notes 35 and 36) | − | − | 10 | ps (p−p) |
| $t_{jphPCIeG2}$ | | PCIe Gen 2 Lo Band<br>10 kHz < f < 1.5 MHz (Notes 35 and 38) | − | − | 0.3 | ps (rms) |
| | | PCIe Gen 2 High Band<br>1.5 MHz < f < Nyquist (50 MHz)<br>(Notes 35 and 38) | − | − | 0.7 | ps (rms) |
| $t_{jPCIeG3}$ | | PCIe Gen 3<br>(PLL BW= 2−4 MHz or 2−5 MHz, CDR = 10 MHz)<br>(Notes 35 and 38) | − | 0.07 | 0.4 | ps |
| $t_{jPCIeG4}$ | | PCIe Gen 4<br>(PLL BW= 2−4 MHz or 2−5 MHz, CDR = 10 MHz)<br>(Notes 35 and 38) | − | 0.07 | 0.4 | ps |
| $t_{jphQPI_SMI}$ | | QPI & SMI<br>(100.00 MHz or 133.33 MHz, 4.8 Gb/s,<br>6.4 Gb/s 12UI) (Notes 37 and 38) | − | − | 0.3 | ps (rms) |
| | | QPI & SMI<br>(100.00 MHz, 8.0 Gb/s, 12UI) (Notes 37 and 38) | − | − | 0.1 | ps (rms) |
| | | QPI & SMI<br>(100.00 MHz, 9.6 Gb/s, 12UI) (Notes 37 and 38) | − | − | 0.1 | ps (rms) |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

34. Applies to all outputs.
35. See http://www.pcisig.com for complete specs
36. Sample size of at least 100K cycles. This figures extrapolates to 108 ps pk−pk @ 1M cycles for a BER of 1−12.
37. Calculated from Intel−supplied Clock Jitter Tool v 1.6.3.
38. For RMS figures, additive jitter is calculated by solving the following equation: $(\text{Additive jitter})^2 = (\text{total jitter})^2 - (\text{input jitter})^2$
39. Guaranteed by design and characterization, not tested in production

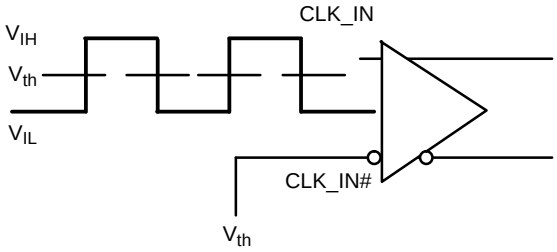



**Figure 4. Differential Input Driven Single−Ended**

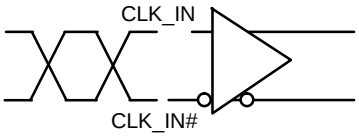



**Figure 5. Differential Inputs Driven Differentially**

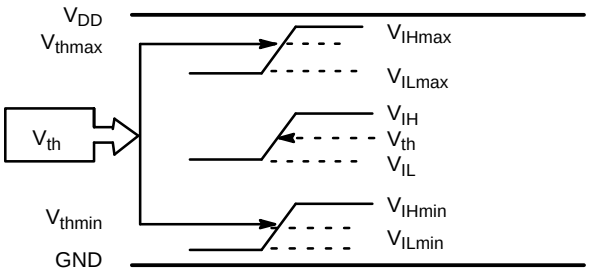



**Figure 6. $V_{th}$ Diagram**

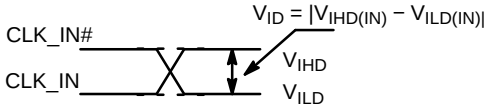



**Figure 7. Differential Inputs Driven Differentially**

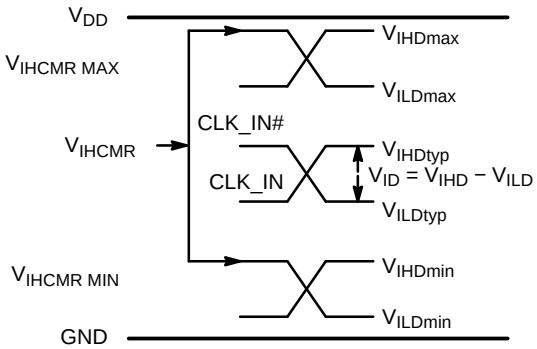



**Figure 8. $V_{IHCMR}$ Diagram**

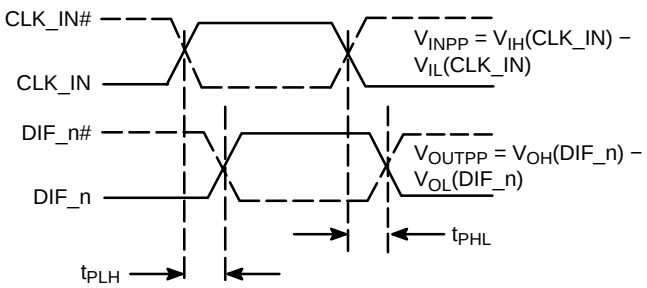
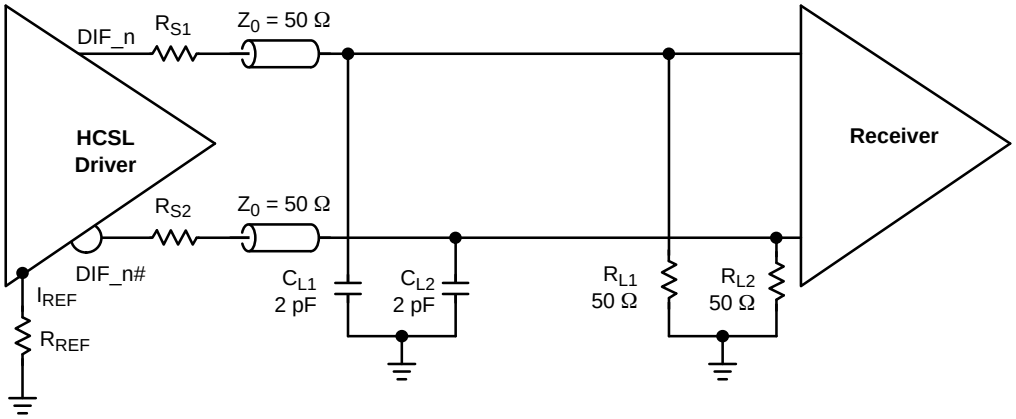



**Figure 9. AC Reference Measurement**




**A**. Connect 475 Ω resistor $R_{REF}$ from $I_{REF}$ pin to GND.
**B**. $R_{S1}$, $R_{S2}$: 33 Ω for Test and Evaluation. Select to Minimizing Ringing.
**C**. $C_{L1}$, $C_{L2}$: Receiver Input Simulation (for test only not added to application circuit.
**D**. $R_{L1}$, $R_{L2}$ Termination and Load Resistors Located at Received Inputs.

**Figure 10. Typical Termination Configuration for Output Driver and Device Evaluation**

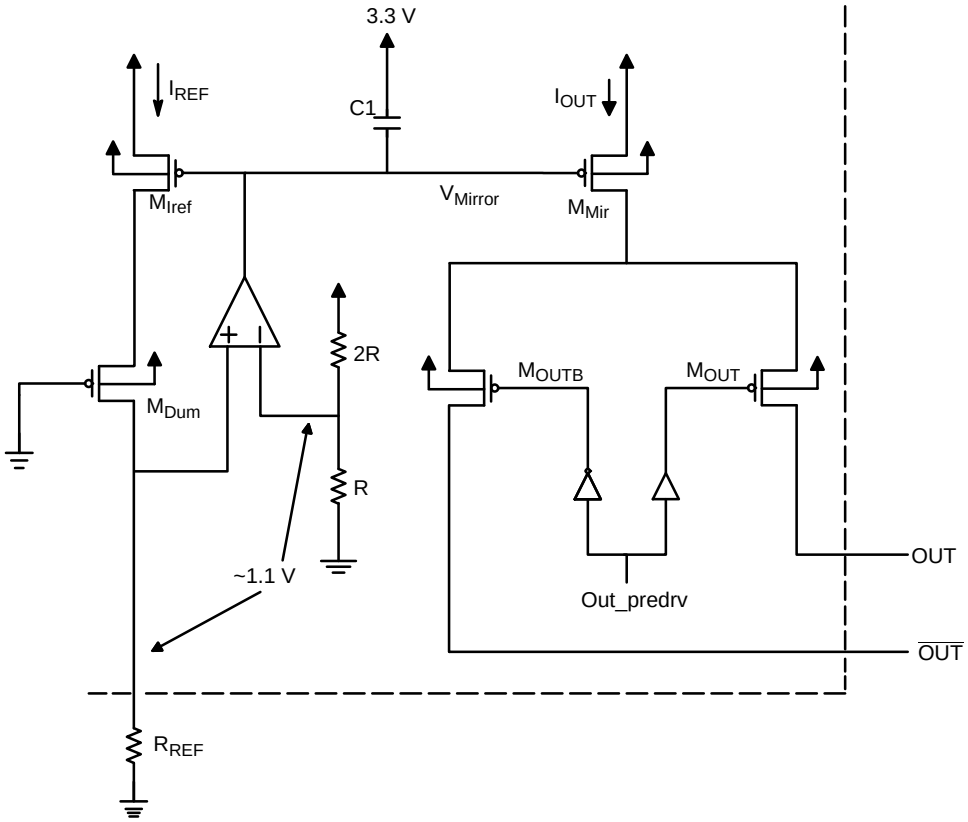



**Figure 11. HCSL Simplified Output Structure**

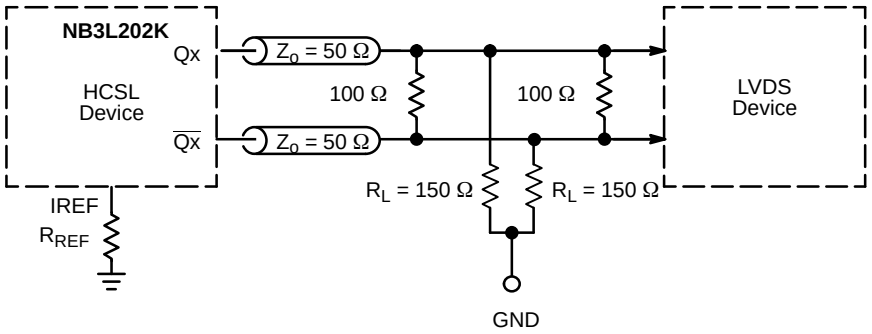



**Figure 12. HCSL Interface Termination to LVDS**

## MEASUREMENT POINTS FOR DIFFERENTIAL

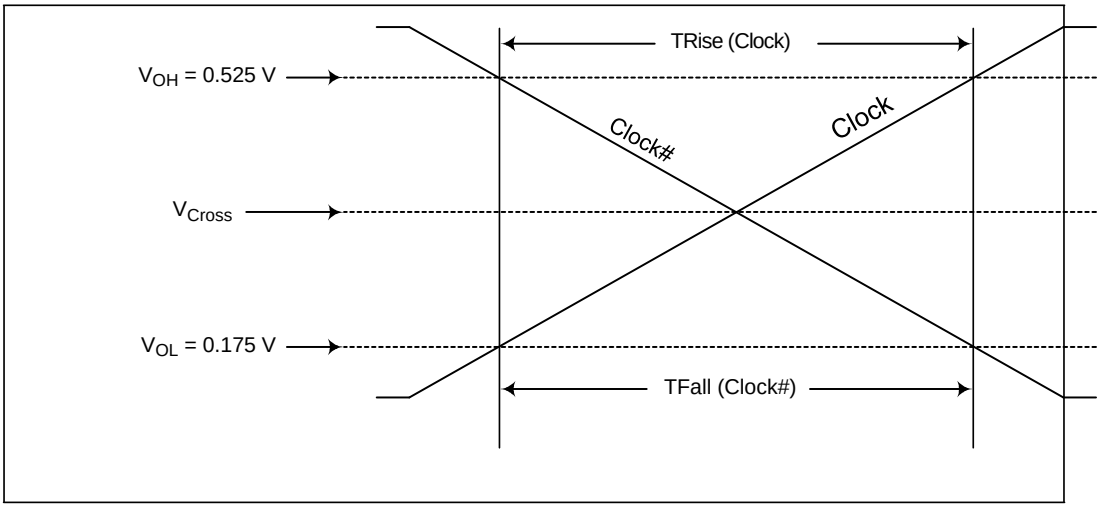



**Figure 13. Single−Ended Measurement Points for Trise, Tfall**

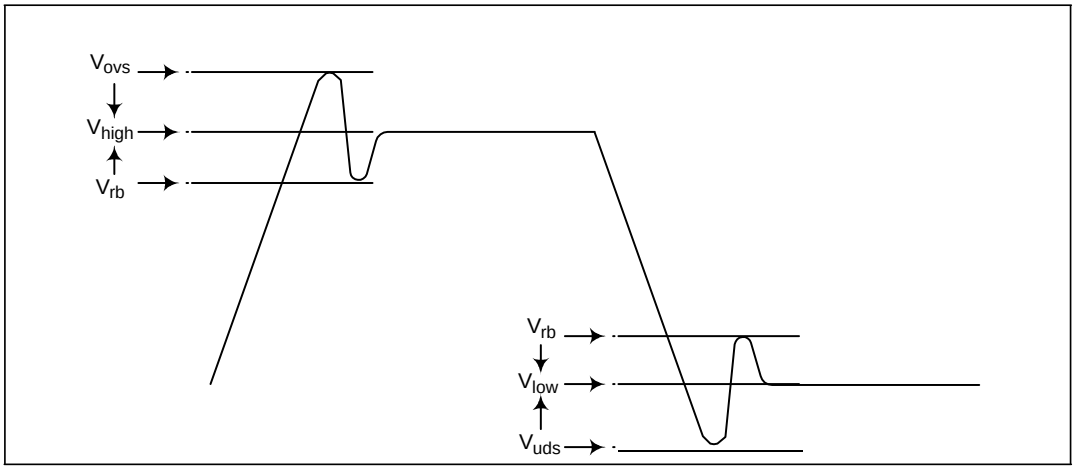



**Figure 14. Single−Ended Measurement Points for $V_{ovs}$, $V_{uds}$, $V_{rb}$**

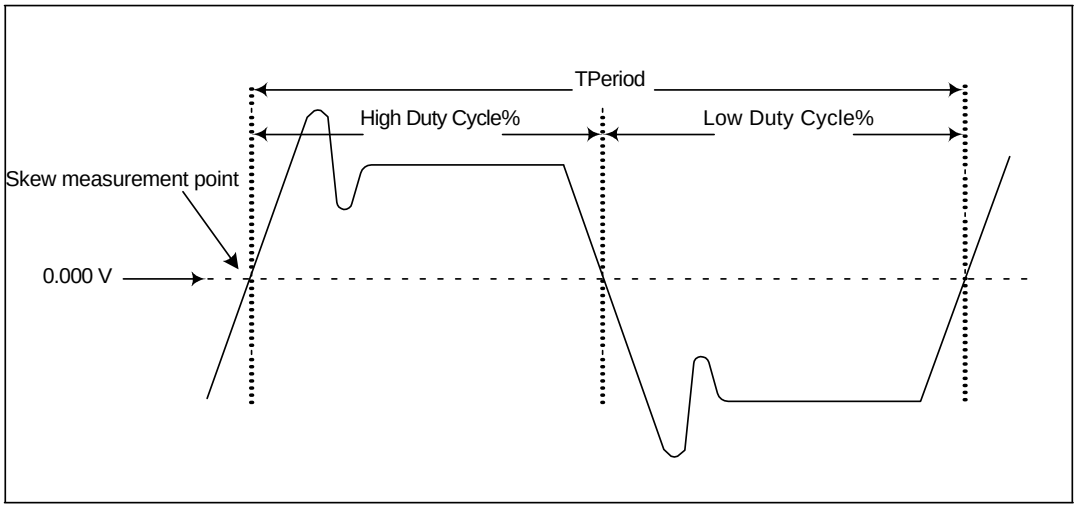



**Figure 15. Differential (CLOCK – CLOCK#) Measurement Points (Tperiod, Duty Cycle)**

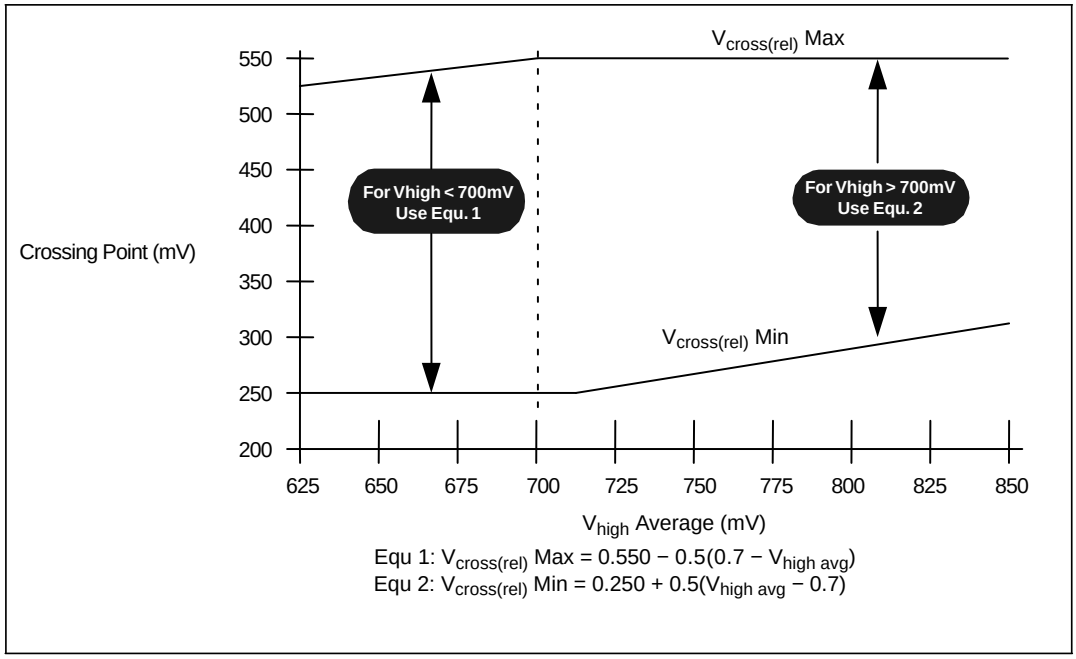



**Figure 16. $V_{cross}$ Range Clarification** (Note 40)

40. The picture above illustrates the effect of $V_{high}$ above and below 700 mV on the $V_{cross}$ range. The purpose of this is to prevent a 250 mV $V_{cross}$ with an 850 mV $V_{high}$. In addition, this prevents the case of a 550 mV $V_{cross}$ with a 660 mV $V_{high}$. The actual specification for $V_{cross}$ is dependent upon the measured amplitude of $V_{high}$.

## Signal and Feature Operation

**Table 7. OE# FUNCTIONALITY** (Notes 41, 42 and 43)

| CLK_IN / CLK_IN# | OE# (Pin) | DIF | DIF # | Notes |
|---|---|---|---|---|
| Running | 1 | Low | Low | 41 |
| Running | 0 | Running | Running | |
| Not Running | x | x | x | |

41. The outputs are tri−stated, but the termination networks pull them low
42. OE# pins are asynchronous asserted−low signals.
43. Each OE# pin controls two pair of DIF outputs.

### OE# Assertion (Transition from ‘1’ to ‘0’)

All differential outputs that were tri−stated (low due to termination pull down) will resume normal operation in a glitch free manner. The latency from the assertion to active outputs is 4 − 12 DIF clock periods.

Note: Input clock must remain running for a minimum of 12 clock cycles.

### OE# De−Assertion (Transition from ‘0’ to ‘1’)

The maximum latency from the de−assertion to tristated (low due to termination pull down) outputs is 12 DIF clock periods.

**Table 8. NB3L202K RESISTIVE LUMPED TEST LOADS FOR DIFFERENTIAL CLOCKS**

| Board Target Trace/Term Z | Reference R, Iref = VDD/(3*$R_{REF}$) | Output Current | $V_{OH}$ @ Z | Rs | Rp |
|---|---|---|---|---|---|
| 100 Ω Differential<br>50 Ω Single−Ended | $R_{REF}$ = 475 Ω 1%,<br>$I_{REF}$ = 2.32 mA | $I_{OH}$ = 6 * $I_{REF}$ | 0.7 V @ 50 | 33 Ω<br>5% | 50 Ω<br>5% |
| 85 Ω Differential<br>43 Ω Single−Ended | $R_{REF}$ = 412 Ω, 1%,<br>$I_{REF}$ = 2.67 mA | $I_{OH}$ = 6 * $I_{REF}$ | 0.7V @ 43.2 | 27 Ω<br>5% | 43 Ω<br>5% |

## ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| NB3L202KMNG | QFN16<br>(Pb−Free) | 123 Units / Rail |
| NB3L202KMNTXG | QFN16<br>(Pb−Free) | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

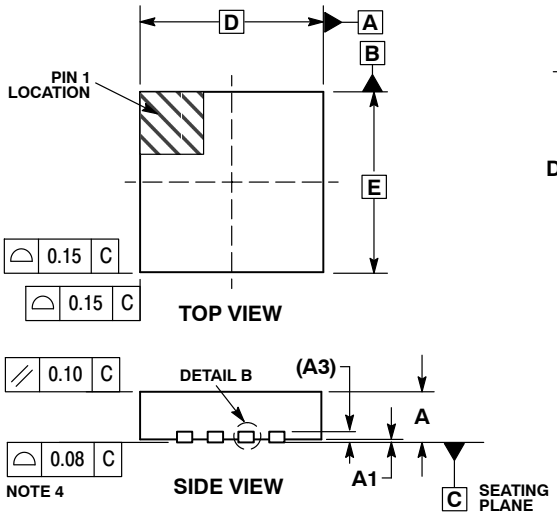
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

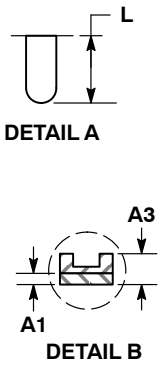
ON Semiconductor®

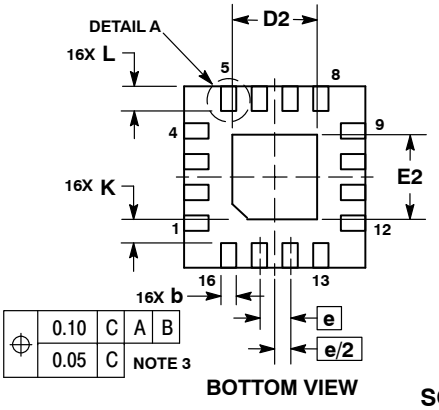
**QFN16 3x3, 0.5P**
CASE 485FM
ISSUE A

DATE 30 JAN 2018

1
**SCALE 2:1**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. OUTLINE MEETS JEDEC DIMENSIONS PER MO−220, VARIATION VEED−6.

| | MILLIMETERS | |
|---|---|---|
| DIM | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 REF | |
| b | 0.18 | 0.30 |
| D | 3.00 BSC | |
| D2 | 1.25 | 1.55 |
| E | 3.00 BSC | |
| E2 | 1.25 | 1.55 |
| e | 0.50 BSC | |
| K | 0.20 | −−− |
| L | 0.30 | 0.50 |

### GENERIC MARKING DIAGRAM*

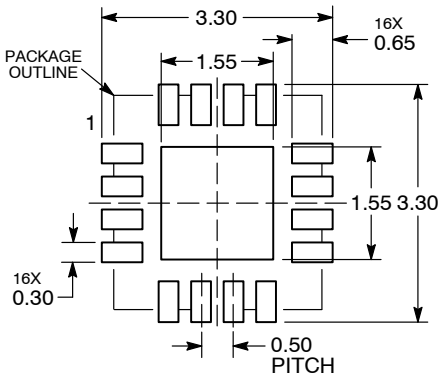



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

### RECOMMENDED SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
|---|---|---|
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| **DESCRIPTION:** | **QFN16 3X3, 0.5P** | **PAGE 1 OF 1** |

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