NBVSBAXXX Series

2.5 V/3.3 V, LVPECL Voltage-Controlled Crystal Oscillator (VCXO) PureEdge™ Product Series

The NBVSBAXXX series voltage−controlled crystal oscillator (VCXO) devices are designed to meet today's requirements for 2.5 V and 3.3 V LVPECL clock generation applications. These devices use a high Q fundamental mode crystal and Phase Locked Loop (PLL) multiplier to provide a wide range of frequencies from 60 MHz to 700 MHz (factory configurable per user specifications) with a pullable range of ±100 ppm and a frequency stability of ±50 ppm. The silicon−based PureEdge™ products design provides users with exceptional frequency stability and reliability. They produce an ultra low jitter and phase noise LVPECL differential output.

The NBVSBAXXX series are members of ON Semiconductor's PureEdge™ clock family that provides accurate and precision clock generation solutions.

Available in the industry standard 5.0 x 7.0 x 1.8 mm and in a new 3.2 x 5.0 x 1.2 mm SMD (CLCC) package on 16 mm tape and reel in quantities of 1,000.

Features

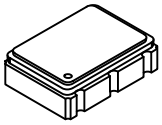
- LVPECL Differential Output
- Operating Range: 2.5 V ±5%, 3.3 V ±10%
- Ultra Low Jitter and Phase Noise − 0.5 ps (12 kHz − 20 MHz)
- Factory Configurable Frequencies from 60 MHz to 700 MHz (see Standard Frequencies in the Ordering Information Table in page 6)
- Pullable Range Minimum of ±100 ppm
- Frequency Stability of ±50 ppm
- Control Voltage with Positive Slope
- Voltage Control Linearity of ±10%
- Uses High Q Fundamental Mode Crystal
- Hermetically Sealed Ceramic SMD Package
- These Devices are Pb−Free and RoHS Compliant

Applications

- Networking
- SONET
- 10 Gigabit Ethernet
- Networking Base Stations
- Broadcasting

ON Semiconductor®

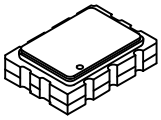
http://onsemi.com



6 PIN CLCC
LN SUFFIX
CASE 848AB

MARKING DIAGRAM





6 PIN CLCC
LU SUFFIX
CASE 848AC



NBVSBAXXX	= NBVSBAXXX (±50 ppm)
XXX.XXXX	= Output Frequency (MHz)
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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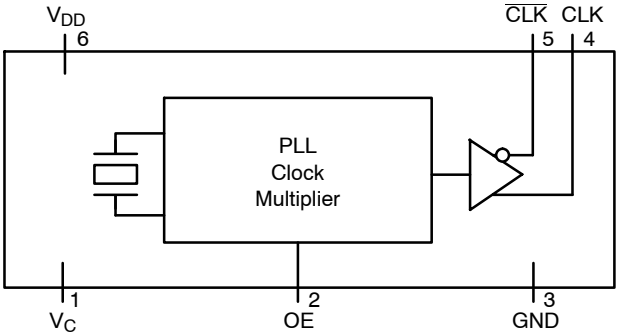


Figure 1. Simplified Logic Diagram

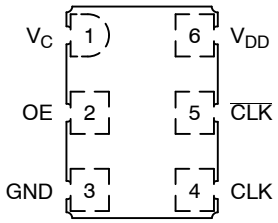


Figure 2. Pin Connections (Top View)

Table 1. PIN DESCRIPTION

Pin No.	Symbol	I/O	Description
1	V_C (Note 1)	Analog Input	Analog control voltage input pin that adjusts output oscillation frequency. f_0 =V_C = 1.65 V
2	OE	LVTTL/LVCMOS Control Input	Output Enable Pin. When left floating pin defaults to logic HIGH and output is active. See OE pin description Table 2.
3	GND	Power Supply	Ground at 0 V. Electrical and Case Ground.
4	CLK	LVPECL Output	Non−Inverted Clock Output. Typically loaded with 50 Ω receiver termination resistor to V_{TT} = V_{DD} − 2 V.
5	$\overline{CLK}$	LVPECL Output	Inverted Clock Output. Typically loaded with 50 Ω receiver termination resistor to V_{TT} = V_{DD} − 2 V.
6	V_{DD}	Power Supply	Positive Power Supply Voltage. Voltage should not exceed 2.5 V ±5% and 3.3 V ±10%.

1. Control voltage has a positive slope with a linearity of ±10%; V_C = 1.65 V ± 1 V.

Table 2. OUTPUT ENABLE TRI−STATE FUNCTION

OE Pin	Output Pins
Open	Active
HIGH Level	Active
LOW Level	High Z

Table 3. ATTRIBUTES

Characteristic		Value
Internal Default State Resistor		170 kΩ
ESD Protection	Human Body Model Machine Model	2 kV 200 V
Meets or Exceeds JEDEC Standard EIA/JESD78 IC Latchup Test		

2. For additional Moisture Sensitivity information, refer to Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V_{DD}	Positive Power Supply	GND = 0 V		4.6	V
V_{IN}	Control Input (V_C and OE)		$V_{IN} \le V_{DD}$ + 200 mV $V_{IN} \ge$ GND − 200 mV		V
I_{out}	LVPECL Output Current	Continuous Surge		25 50	mA
T_A	Operating Temperature Range			−40 to +85	°C
T_{stg}	Storage Temperature Range			−55 to +120	°C
T_{sol}	Wave Solder	See Figure 4		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Table 5. DC CHARACTERISTICS (V_{DD} = 2.5 V ± 5%; 3.3 V ± 10%, GND = 0 V, T_A = −40°C to +85°C) (Note 3)

Symbol	Characteristic		Conditions	Min.	Typ.	Max.	Units
I_{DD}	Power Supply Current				90	110	mA
V_{IH}	Input HIGH Voltage	OE		2000		V_{DD}	mV
V_{IL}	Input LOW Voltage	OE		GND − 200		800	mV
I_{IH}	Input HIGH Current	OE		−100		+100	μA
I_{IL}	Input LOW Current	OE		−100		+100	μA
V_{OH}	Output HIGH Voltage			V_{DD}−1195		V_{DD}−945	mV
V_{OL}	Output LOW Voltage			V_{DD}−1945		V_{DD}−1600	mV
V_{OUTPP}	Output Voltage Amplitude				700		mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

3. Measurement taken with outputs terminated with 50 Ω to V_{DD} − 2.0 V. See Figure 3.

Table 6. AC CHARACTERISTICS (V_{DD} = 2.5 ±5%, V_{DD} = 3.3 ±10%, GND = 0 V, T_A = -40°C to +85°C)

Symbol	Characteristic	Conditions	Min.	Typ.	Max.	Units
f_{CLKOUT}	Output Clock Frequency	NBVSBA011		122.88		MHz
		NBVSBA027		148.50		
		NBVSBA018		155.52		
		NBVSBA017		156.25		
		NBVSBA015		200.00		
		NBVSBA024		622.08		
		NBVSBA026		644.53		
		NBVSBA041		693.48		
		NBVSBA037		707.35		
Δf	Frequency Stability	(Note 5)			±50	ppm
$t_{jit}(\phi)$	RMS Phase Jitter	12 kHz to 20 MHz		0.5	0.9	ps
t_{jitter}	Cycle to Cycle, RMS	1000 Cycles		2	8	ps
	Cycle to Cycle, Peak-to-Peak	1000 Cycles		10	30	ps
	Period, RMS	10,000 Cycles		1	4	ps
	Period, Peak-to-Peak	10,000 Cycles		6	20	ps
$t_{OE/OD}$	Output Enable/Disable Time				200	ns
F_P	Crystal Pullability (Note 4)	$0 \le V_C \le 3.3$ V	±100			ppm
$V_{C(bw)}$	Control Voltage Bandwidth	- 3 dB	20			KHz
t_{DUTY_CYCLE}	Output Clock Duty Cycle (Measured at Cross Point)		45	50	55	%
t_R	Output Rise Time (20% and 80%)			245	400	ps
t_F	Output Fall Time (80% and 20%)			245	400	ps
t_{start}	Start-up Time			1	5	ms
	Aging	1st Year			3	ppm
		Every Year After 1st			1	

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Gain transfer is positive with a rate of 130 ppm/V.
5. Parameter guarantees 10 years of aging. Includes initial stability at 25°C, shock, vibration and first year aging.

Table 7. PHASE NOISE PERFORMANCE

Parameter	Characteristic	Condition	011 122.88 MHZ	027 148.50 MHz	018 155.52 MHz	017 156.25 MHZ	015 200.00 MHz	Units
ϕ_{NOISE}	Output Phase−Noise Performance	100 Hz offset	−90	−90	−90	−90	−87	dBc/Hz
		1 kHz offset	−118	−118	−116	−116	−114	dBc/Hz
		10 kHz offset	−127	−127	−126	−126	−125	dBc/Hz
		100 kHz offset	−127	−127	−126	−126	−125	dBc/Hz
		1 MHz offset	−134	−134	−134	−134	−132	dBc/Hz
		10 MHz offset	−160	−160	−160	−160	−158	dBc/Hz

Table 8. PHASE NOISE PERFORMANCE (continued)

Parameter	Characteristic	Condition	024 622.08 MHZ	026 644.53 MHZ	041 693.48 MHZ	037 707.35 MHZ	Units
ϕ_{NOISE}	Output Phase−Noise Performance	100 Hz offset	−80	−86	−78	−78	dBc/Hz
		1 kHz offset	−106	−107	−105	−105	dBc/Hz
		10 kHz offset	−117	−116	−115	−115	dBc/Hz
		100 kHz offset	−117	−116	−115	−115	dBc/Hz
		1 MHz offset	−122	−125	−124	−124	dBc/Hz
		10 MHz offset	−150	−150	−149	−149	dBc/Hz

Table 9. RELIABILITY COMPLIANCE

Parameter	Standard	Method
Shock	Mechanical	MIL−STD−833, Method 2002, Condition B
Solderability	Mechanical	MIL−STD−833, Method 2003
Vibration	Mechanical	MIL−STD−833, Method 2007, Condition A
Solvent Resistance	Mechanical	MIL−STD−202, Method 215
Thermal Shock	Environment	MIL−STD−833, Method 1011, Condition A
Moisture Level Sensitivity	Environment	MSL1 260°C per IPC/JEDEC J−STD−020D

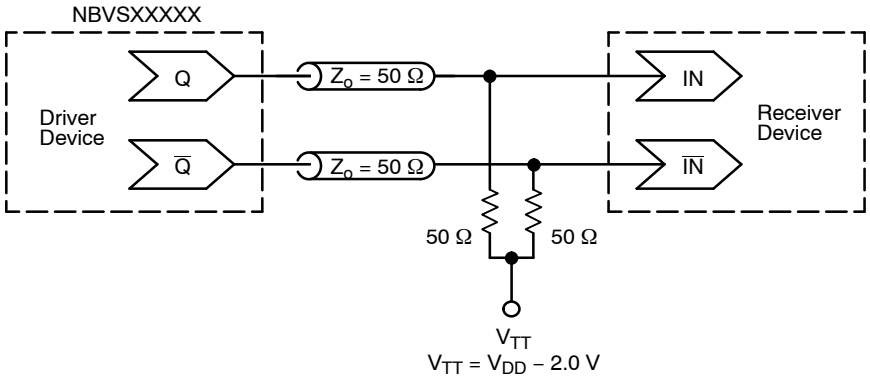


Figure 3. Typical Termination for Output Driver and Device Evaluation (See Application Note AND8020/D − Termination of ECL Logic Devices.)

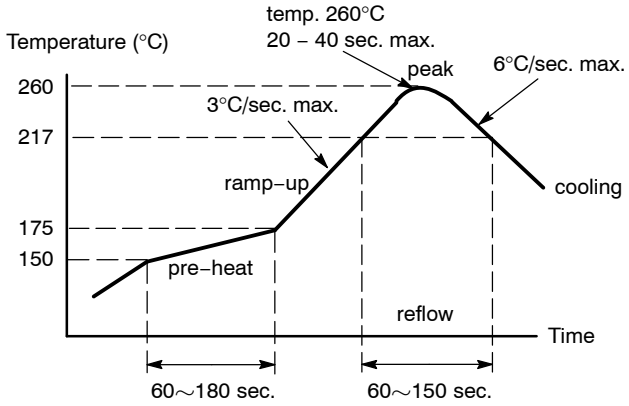


Figure 4. Recommended Reflow Soldering Profile

Table 10. ORDERING INFORMATION

Device	Output Frequency (MHz)	Package	Shipping†
5.0 x 7.0 x 1.8 mm			
NBVSBA011LN1TAG	122.88	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSBA027LN1TAG	148.50	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSBA018LN1TAG	155.52	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSBA017LN1TAG	156.25	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSBA015LN1TAG	200.00	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSBA024LN1TAG	622.08	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSBA026LN1TAG	644.53	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSBA037LN1TAG	707.35	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSBA041LN1TAG	693.48	CLCC−6, Pb−Free	1000 / Tape & Reel
5.0 x 7.0 x 1.8 mm			
NBVSBA011LNHTAG	122.88	CLCC−6, Pb−Free	100 / Tape & Reel
NBVSBA027LNHTAG	148.50	CLCC−6, Pb−Free	100 / Tape & Reel
NBVSBA018LNHTAG	155.52	CLCC−6, Pb−Free	100 / Tape & Reel
NBVSBA017LNHTAG	156.25	CLCC−6, Pb−Free	100 / Tape & Reel
NBVSBA015LNHTAG	200.00	CLCC−6, Pb−Free	100 / Tape & Reel
NBVSBA024LNHTAG	622.08	CLCC−6, Pb−Free	100 / Tape & Reel
NBVSBA026LNHTAG	644.53	CLCC−6, Pb−Free	100 / Tape & Reel
NBVSBA037LNHTAG	707.35	CLCC−6, Pb−Free	100 / Tape & Reel
NBVSBA041LNHTAG	693.48	CLCC−6, Pb−Free	100 / Tape & Reel
3.2 x 5.0 x 1.2 mm			
NBVSBA011LU1TAG*	122.88	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSBA027LU1TAG*	148.50	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSBA018LU1TAG*	155.52	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSBA017LU1TAG*	156.25	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSBA015LU1TAG*	200.00	CLCC−6, Pb−Free	1000 / Tape & Reel

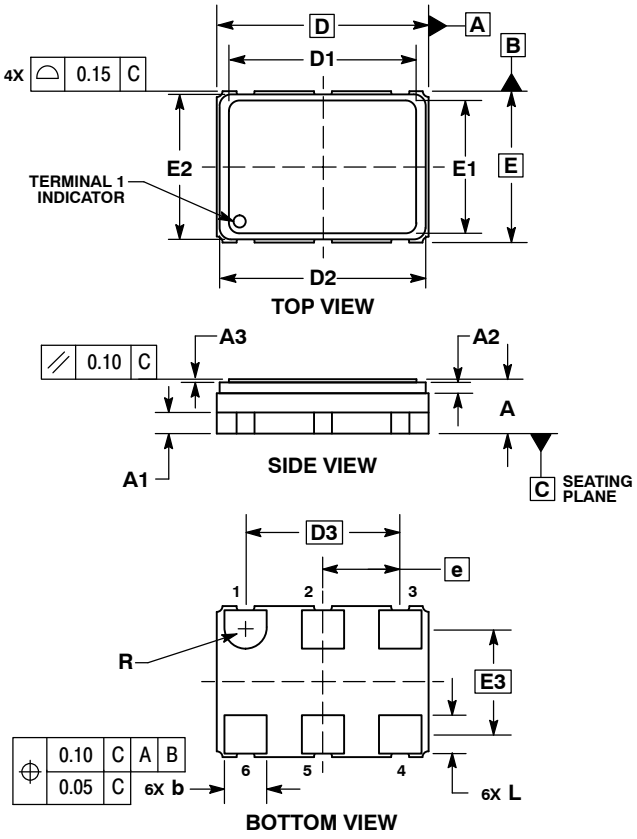
Table 10. ORDERING INFORMATION

Device	Output Frequency (MHz)	Package	Shipping†
3.2 x 5.0 x 1.2 mm			
NBVSBA024LU1TAG*	622.08	CLCC−6, Pb−Free	1000 / Tape & Reel
NBVSBA026LU1TAG*	644.53	CLCC−6, Pb−Free	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our tape and Reel Packaging Specification Brochure, BRD8011/D.
*Consult factory for availability.

PACKAGE DIMENSIONS

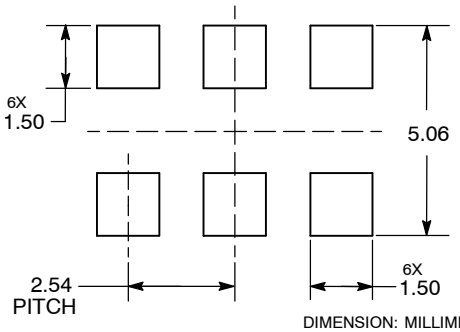
6 PIN CLCC, 7x5, 2.54P
CASE 848AB−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	1.70	1.80	1.90
A1		0.70 REF	
A2		0.36 REF	
A3	0.08	0.10	0.12
b	1.30	1.40	1.50
D		7.00 BSC	
D1	6.17	6.20	6.23
D2	6.66	6.81	6.96
D3		5.08 BSC	
E		5.00 BSC	
E1	4.37	4.40	4.43
E2	4.65	4.80	4.95
E3		3.49 BSC	
e		2.54 BSC	
L	1.17	1.27	1.37
R		0.70 REF	

SOLDERING FOOTPRINT*

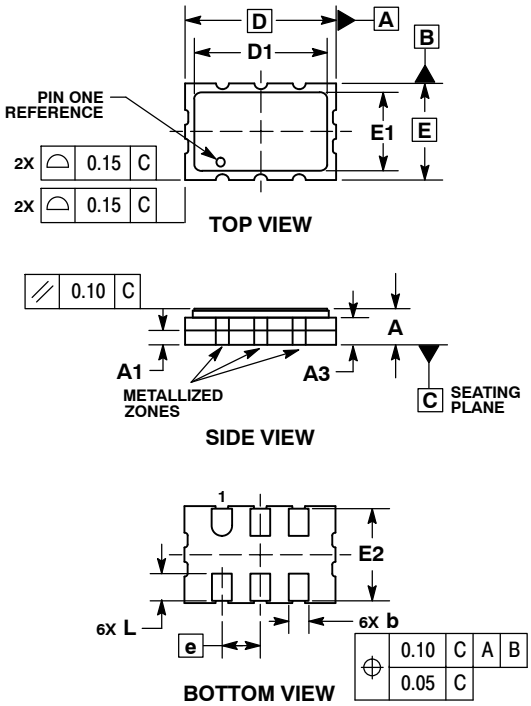


DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

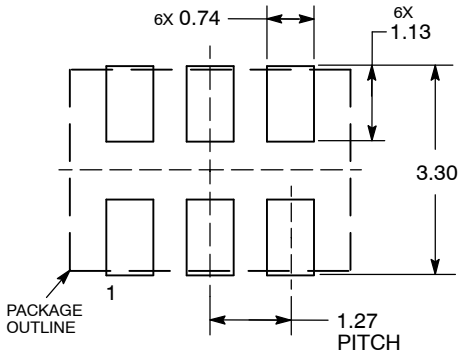
6 PIN CLCC, 5x3.2, 1.27P
CASE 848AC−01
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

	MILLIMETERS	
DIM	MIN	MAX
A	1.05	1.35
A1	0.35	0.65
A3	0.90 REF	
b	0.50	0.80
D	5.00 BSC	
D1	4.25	4.55
E	3.20 BSC	
E1	2.45	2.75
E2	2.90	3.20
e	1.27 BSC	
L	0.75	1.05

SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

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