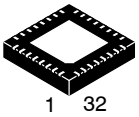
10Mb/s Industrial Ethernet 10BASE-T1S Transceiver (802.3cg Compliant)

NCN26000



QFNW32 5x5
CASE 484AB

The NCN26000 device is an IEEE 802.3cg compliant Ethernet Transceiver (PHY) designed for industrial multi−drop Ethernet. It provides all physical layer functions needed to transmit and receive data over a single unshielded twisted−pair. The NCN26000 communicates to existing half−duplex 10 Mb/s capable Ethernet MAC controllers via a standard MII interface.

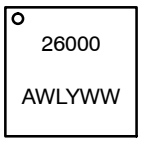
Features

- 10BASE−T1S − IEEE 802.3cg Compliant
- Data Rate of 10 Mb/s, Half−Duplex
- 3.3V supply
- 5 mm x 5 mm QFN32 Package
- Standard Media Independent Interface (MII). Connects to any CSMA/CD half−duplex capable MAC exposing the CRS and COL pins
- Physical Layer Collision Avoidance (PLCA) through Local Configuration for Collision−Free Operation on a Shared Medium (Multi−Drop)
- Configuration and Monitoring using a standard MII Management Interface (also known as MDIO)
- Partial configuration during boot sequence using pull resistors on dedicated pins when the device is booting
- Enhanced Noise Immunity Mode, Allowing Communication at Noise Levels Exceeding IEEE 802.3cg Specifications
- Supports > 8 Nodes over >25 m UTP Cable
- Fast Startup: less than 100 ms
- Support for Bootstrap in Isolated Mode

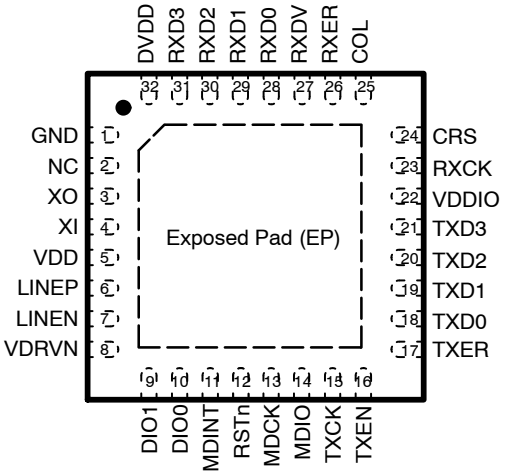
Typical Applications

- Industrial Automation
- Sensor interfacing
- Home / Building Control
- Security and Field Instrumentation

MARKING DIAGRAM



26000	= Specific Device Code
A	= Assembly Site
WL	= Wafer Lot Number
Y	= Year of Production
WW	= Work Week Number



ORDERING INFORMATION

See detailed ordering and shipping information on page 32 of this data sheet.

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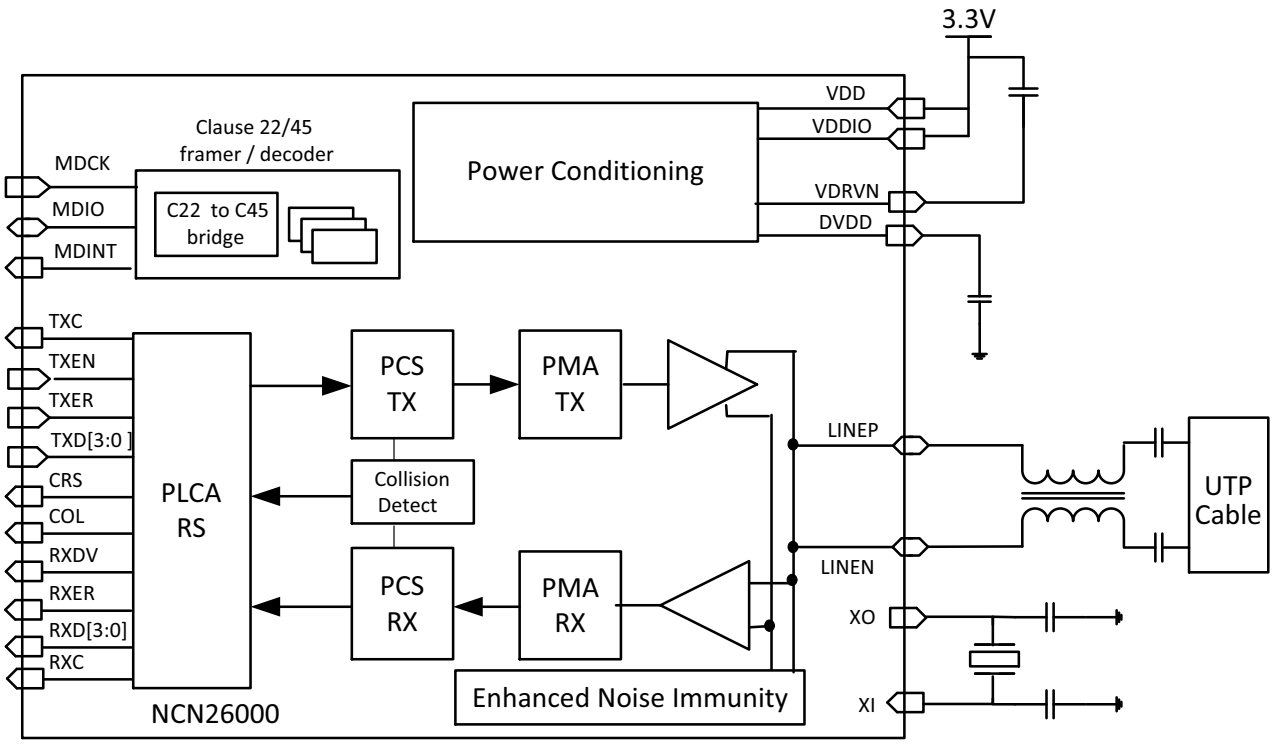

Note: Internal power distribution and GND lines from Power Supply block not shown.

Figure 1. NCN26000 Block Diagram

Table 1. PIN DESCRIPTION

Pin QFN32	Name	I/O	Type	Function
1	GND	Supply		Ground
2	NC	Reserved		Reserved, do not connect
3	XO	Output	XTAL	Clock Crystal Connection. If a crystal is used as a clock source, one pin of the crystal shall be connected to this pin. If an external clock source is used, XO shall be left floating (no connect)
4	XI	Input	XTAL LVCMOS	System Clock / Crystal Connection. Can be connected to an external 25 MHz crystal or a 3.3 V LVCMOS reference clock signal.
5	VDD	Supply		3.3 V Supply
6	LINEP	Bi−Directional	Analog	Data Line (Positive)
7	LINEN	Bi−Directional	Analog	Data Line (Negative)
8	VDRVN		Analog	TX Driver regulator output Connect to an off−chip 2.2 F decoupling capacitor
9	LED1/DIO1	Output	8X−LVCMOS	General Purpose IO with programmable pull−up/down. This pin can be configured to drive an external LED (through a proper bias resistor) or other circuitry.
10	LED0/DIO0	Output	8X−LVCMOS	General Purpose IO with programmable pull−up/down. This pin can be configured to drive an external LED (through a proper bias resistor) or other circuitry.
11	MDINT	Output	LVCMOS	Open−Drain, active−low MIIM interrupt signal. MDINT can be configured for providing various register status change notifications (see MIIM IRQ Control Register)

Table 1. PIN DESCRIPTION

Pin QFN32	Name	I/O	Type	Function
12	RSTn	Bi−Directional	8X−Open Drain / Schmitt−Trigger	Active−low asynchronous reset pin. This pin features an internal pull−up of 54 k typical. For noise sensitive applications **onsemi** recommends the use of an external 4.7 k to 10 k pull−up resistor to VDDIO. Since this pin can be driven by the NCN26000, to prevent permanent damage when driving this from a MCU or any other active driver, ensure that such driver is open drain.
13	MDCK	Input	LVCMOS	MIIM clock input. MDCK can either be a continuous clock or provided only during MDIO transactions. The MIIM interface works in both NORMAL and ISOLATED mode.
14	MDIO	Bi−Directional	LVCMOS	MIIM data input/output. Used to read or write PHY registers.
15	TXCK	Output	LVCMOS	MII 2.5 MHz PHY to MAC transmit clock
16	TXEN	Input	LVCMOS	MII MAC to PHY transmit enable
17	TXER	Input	LVCMOS	MII MAC to PHY transmit error
18	TXD0	Input	LVCMOS	MII MAC to PHY transmit data
19	TXD1			
20	TXD2			
21	TXD3			
22	VDDIO	Analog		3.3 V supply for Digital IO. Can also be set to 2.5 V to support 2.5 V LVCMOS
23	RXCK	Output	LVCMOS	MII PHY to MAC receive clock
24	CRS	Output	LVCMOS	MII PHY to MAC carrier sense (busy signal)
25	COL	Output	LVCMOS	MII PHY to MAC collision detection
26	RXER	Output	LVCMOS	MII PHY to MAC receive error
27	RXDV	Output	LVCMOS	MII PHY to MAC receive data valid
28	RXD0	Output	LVCMOS	MII PHY to MAC receive data
29	RXD1			
30	RXD2			
31	RXD3			
32	DVDD	Supply		Output of the LDO supplying the digital core. Connect to a 2.2 F decoupling capacitance.
Exposed PAD	GND	Supply		Ground

Table 2. ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Value	Unit
V_{DD}	Chip Supply	−0.3 to 3.63	V
GND	Ground	−0.3 to 0	V
T_{STG}	Storage Temperature Range	−65 to 150	°C
T_{SLD}	Lead Temperature, Soldering (10 Sec)	260	°C
LINEP	Line Voltage P	−30 to 30	V
LINEN	Line Voltage N	−30 to 30	V
ESD_{HBM}	ESD Capability, Human Body Model (Note 1)	2	kV
ESD_{HBM_LINE}	ESD Capability for LINEP and LINEN Pins, Human Body Model (Note 1)	8	kV
ESD_{CDM}	ESD Capability, Charged Device Model (Note 1)	0.5	kV
LU	Latch−up Current Immunity (Note 1)	100	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Tested by the following methods @ T_A = 25°C:
   ESD Human Body Model tested per JESD22−A114
   ESD Charged Device Model per ESD STM5.3.1
   Latch−up Current tested per JESD78

Table 3. RECOMMENDED OPERATING RANGES

Symbol	Rating	Min	Typ	Max	Unit
V_{DD}	Chip Supply	2.97	3.3	3.63	V
V_{DDIO}	I/O Supply for 3.3 V Operation	2.97	3.3	3.63	V
V_{DDIO}	I/O Supply for 2.5 V Operation	2.25	2.5	2.75	V
GND	Ground	−	0	−	V
T_{AMB}	Ambient Operating Temperature	−40	−	125	°C

Table 4. PACKAGE THERMAL CHARACTERISTICS

Symbol	Rating	Device	Value	Unit
θ_{JA}	Junction−to−Ambient, Still Air	NCN26000MNTXG	55	K/W

Table 5. ELECTRICAL CHARACTERISTICS

These specifications are over recommended supply voltage and operating free−air temperature unless otherwise noted.

Symbol	Rating	Condition	Min	Typ	Max	Unit
SUPPLY POWER						
PACTIVE	Power Consumption (Transmitting and Receiving Ethernet Packets)	VDDIO = VDD = 3.3 V ±10%	–	145	195	mW
PACTIVERX	Receive only Power Consumption (Powered On, but not Transmitting Ethernet Packets)	VDDIO = VDD = 3.3 V ±10%	–	60	–	mW
PIDLE	Idle Power Consumption (Clocked and Enabled, but not Transmitting or Actively Receiving, No Activity on SPI)	VDDIO = VDD = 3.3 V ±10%	–	40	–	mW
CLOCK						
FXTAL	XTAL Clock Frequency	VDD = VDDIO = 3.3 V ±10%	−100 ppm	25	+ 100 ppm	MHz
FEXT	External Clock Frequency	VDD = 3.3 V ±10%, VDDIO = 2.5 V ±10%	−100 ppm	25	+100 ppm	MHz
FSPI	SPI Clock Frequency	VDD = VDDIO = 3.3 V ±10%	–	–	25	MHz
		VDD = 3.3 V ±10%, VDDIO = 2.5 V ±10%	–	–	20	
LINE TRANSMITTER CHARACTERISTICS						
BIT_f	Data Rate (10BASE−T1S)		–	–	10	Mb/s
V_{OUTpp}	Peak Differential Output (Peak−to−peak) (Note 2)	VDD = 3.3 V ±10% TX_GAIN = default	800	1000	1200	mV
JTX	Cycle−to−Cycle Jitter		–	0.2	1	ns
trise	Rise Time	VDD = 3.3 V ±10%	–	10	–	ns
tfall	Fall Time	VDD = 3.3 V ±10%	–	10	–	ns
ROUT	Output Impedance	VDD = 3.3 V ±10%	40	50	60	Ω
LINE RECEIVER CHARACTERISTICS (at the MDI)						
VTHRX	Receiver Threshold		–	0	–	mV
VEDRX	Energy Detection Threshold (Note 2)	VDD = 3.3 V ±10% RX_ED = default	–	250	–	mV
Vacc	Threshold Accuracy		−30	–	30	mV
VCM	Common Mode Voltage Range		−20	–	20	V
RIN	Differential Input Resistance	Driver is High−Z (Not Transmitting)	25	40	60	k
CIN	Differential Input Capacitance (at 20 MHz)		–	5.5	7.5	pF

Table 5. ELECTRICAL CHARACTERISTICS

These specifications are over recommended supply voltage and operating free−air temperature unless otherwise noted.

Symbol	Rating	Condition	Min	Typ	Max	Unit
DIGITAL IOs						
VIL	LVCMOS Input Level Low	VDDIO = 2.5 V ±10%	−0.3	–	0.7	V
		VDDIO = 3.3 V ±10%	−0.3	–	0.8	V
VIH	LVCMOS Input Level High	VDDIO = 2.5 V ±10%	1.7	–	VDDIO +0.3	V
		VDDIO = 3.3 V ±10%	2.0	–	VDDIO +0.3	V
Vt−(VIL)	Schmitt Trigger Input Level Low	VDDIO = 2.5 V ±10%	0.7	–	1.5	V
		VDDIO = 3.3 V ±10%	0.7	–	1.9	V
Vt+(VIH)	Schmitt Trigger Input Level High	VDDIO = 2.5 V ±10%	0.9	–	1.7	V
		VDDIO = 3.3 V ±10%	0.9	–	2.1	V
Vhyst ($\|V_{t+}-V_{t-}\|$)	Schmitt Trigger Input Hysteresis	VDDIO = 2.5 V ±10%	0.2	–	1.0	V
		VDDIO = 3.3 V ±10%	0.2	–	1.4	V
VOL	Output Level Low	VDDIO = 2.5 V − 10% 4X−Type (Note 3) IOL = 2.48 mA	0	–	0.45	V
		VDDIO = 2.5 V − 10% 8X−Type IOL = 4.83 mA				
		VDDIO = 3.3 V − 10% 4X−Type IOL = 2.93 mA	0	–	0.4	V
		VDDIO = 3.3 V − 10% 8X−Type IOL = 5.65 mA				
VOH	Output Level High	VDDIO = 2.5 V −10% 4X−Type IOH = −2.63 mA	VDDIO − 0.45	–	VDDIO	V
		VDDIO = 2.5 V −10% 8X−Type IOH = −5.11 mA				
		VDDIO = 3.3 V − 10% 4X−Type IOH = 3.19 mA	VDDIO − 0.4	–	VDDIO	V
		VDDIO = 3.3 V − 10% 8X−Type IOH = −6.12 mA				
IIL	Input Current Low	0.0 V ≤ Vin ≤ VDDIO, max supply = 3.63 V	−11	–	11	A
IIH	Input Current High	0.0 V ≤ Vin ≤ VDDIO, max supply = 3.63 V	−11	–	11	A
RPU	Pull−Up Resistance		33	54	103	kΩ
RPD	Pull−Down Resistance		30	44	73	kΩ

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Default Value, can be altered by device configuration.
3. 4X and 8X denote the number of std LVCMOS input loads the buffer is designed to drive.

DETAILED DESCRIPTION

The NCN26000 is a 10BASE−T1S Physical Layer Transceiver as specified in IEEE 802.3cg integrating a PLCA Reconciliation Sublayer.

It supports operation over a shared media (multi−drop) network segment with up to at least 25 m of a single twisted pair (UTP / STP) connection.

The NCN26000 provides a Media Independent Interface (MII) to connect to a standard IEEE CSMA/CD Ethernet MAC. The NCN26000 provides a shared bus speed of 10 Mb/s in Half−Duplex mode.

NCN26000 can be locally configured to run Physical Layer Collision Avoidance (PLCA), which supports at least eight nodes on the shared medium, depending on environmental conditions.

PLCA improves data throughput under high network load and provides additional benefits:

- Nodes are granted transmit opportunities using a round robin arbitration scheme, enabling fair access to the medium.
- By avoiding multiple back−off and retry events in the host's MAC, maximum latencies are significantly reduced.
- Protects against the "babbling idiot" problem, as a single station can only transmit when granted an opportunity.

The integration of the PLCA reconciliation sublayer (PLCA RS) in the device enables existing MACs to take full advantage of collision free Ethernet communication on a single twisted pair, shared medium.

Additional non−standard features are implemented into the NCN26000:

- Enhanced Noise Immunity PMA operation (ENI)
- PCS reflection mode
- Collision Detection masking
- PLCA Precedence Mode
- PLCA coordinator selection

The NCN26000 runs off a single 3.3 V supply.

The integrated Crystal Oscillator circuitry allows the use of an external CMOS oscillator, a quartz crystal (25 MHz only), or any other external clock source, if its accuracy is in line with the specifications.

Boot Options

The NCN26000 offers two boot modes that can be selected using strap−pins during boot (hard reset or power up).

NORMAL mode: the NCN26000 works as a standard 10BASE−T1S PHY connecting to a CSMA/CD compatible MAC through its MII interface.

ISOLATED mode: same as NORMAL mode, except that all interface pins (except for MDC/MDIO) are kept in high impedance state until the ISOLATED mode is disabled via MDIO (Control Register, address 0, bit 10).

After power−on reset, or when the nRST pin is released (low−to−high transition), the NCN26000 enters BOOT mode.

During BOOT mode, all interface pins are either inputs or tri−stated outputs.

After sampling the strap−pins, the device enters NORMAL or ISOLATED mode, and all interface pins are re−configured accordingly. The MDINT pin is asserted low to indicate the end of the boot process. Thereafter, the NCN26000 grants some additional time before re−configuring the strap−pins as outputs to avoid contentions when the configuration is supplied by an external device. Please, see Figure 5 and Table 11 for detailed timing information about the boot process.

Table 6. BOOTSTRAP PINS

Pin Name	Bootstrap Function	Description
DIO0	ISOLATE	Selects the operating mode: 0 = NORMAL 1 = ISOLATE
RXER	PHYAD[4]	MDIO Address This setting configures the management address of the NCN26000, allowing up to 32 devices to be connected to the same MDIO bus
RXD[3]	PHYAD[3]	
RXD[2]	PHYAD[2]	
RXD[1]	PHYAD[1]	
RXD[0]	PHYAD[0]	

Each strap−pin can be driven High or Low during boot, using an external device or a pull resistor between 1 kΩ and 10 kΩ.

When the configuration is supplied by an external device (e.g., MCU or FPGA), extra care has to be taken to avoid contentions when the NCN26000 leaves the boot state (see Figure 5 and Table 11).

Normal Mode

In NORMAL mode, the NCN26000 exposes a standard MII running at 2.5 MHz, allowing connection to a standard CSMA/CD Media Access Controller (MAC).

The NCN26000 can be managed using Clause 22 MDIO transactions for reading and writing both Clause 22 and Clause 45 MIIM registers.

The internal PLCA RS can be configured using Clause 45 registers compatible with the OPEN Alliance PLCA registers specification·

Isolated Mode

In ISOLATED mode, all the MII pins and LINEx pins are held in high impedance. To leave ISOLATED mode, the user shall clear the ISOM bit in register 0.10 (Clause 22) using an MDIO write access. The DIOx pins are not isolated, as well as the management interface pins consisting of MDC, MDIO and MDINT. The ISOLATED mode could be helpful, for example, when the attached MAC device requires additional configuration before operating, or to solve complex power−up sequences at the system level.

MIIM Interface (MDIO)

NCN26000 supports an MII Management interface, also referred to as MDIO, allowing access to 16 standard and 16 vendor−defined registers using the Clause 22 access method.

The 10BASE−T1S specific registers, as defined by IEEE802.3cg−2019, reside in the register space specified under Clause 45.

Clause 22 Registers

The following Clause 22 registers are implemented:

Table 7. CLAUSE 22 REGISTERS

Register Address	Register Name
0	Control register
1	Status register
2,3	PHY Identifier registers
13	MMD Access Control Register
14	MMD Access Address Data Register
16	MIIM IRQ Control Register
17	MIIM IRQ Status Register
18	DIO Configuration Register

1. OPEN Alliance “TC6 − 10BASE−T1x MACPHY Serial interface Version 1.1”, available from http://www.opensig.org.

CONTROL REGISTER (Address 0)

Bit(s)	Name	Description	Default Value	Register Type (Note 4)
15	Reset	This bit triggers a soft reset of the PHY. 1 = PHY reset 0 = Normal Operation When a soft reset is triggered, all registers revert to their default values and any communication is interrupted. After the soft reset procedure is completed, this bit is automatically reset to 0 (default). The soft reset does not cause the device to enter BOOT state. Therefore, the last strap−pin configuration is preserved, and the device internal initialization will be much faster compared to a hard reset (i.e., driving the nRST pin low).	0	R/W SC
14	Loopback	This bit controls the data loop−back mode of the PHY. 1 = loopback mode enabled 0 = loopback mode disabled When set to 1, all data sent via MII TX is looped backed to MII RX rather than being sent over the line. While loop−back is enabled, the LINEx pins are tri−stated.	0	R/W
13	Speed (LSB)	See Bit 0.6	0	R
12	Link Control	This bit controls the operational status of the PHY. 1 = PHY transmit/receive enabled 0 = PHY transmit/receive disabled NOTE: the implementation of this bit differs from IEEE 802.3 Clause 22.2.4.1.4 (Auto Negotiation Enable). However, it allows the device to be managed by standard software drivers	0	R/W
11	Low−Power	Not implemented. The NCN26000 does not support Low−Power mode.	0	R
10	Isolate	This bit allows entering or leaving the ISOLATED state of the device. 1 = Isolation Enabled 0 = Normal Operation When enabled, all interface pins are set to high−impedance, except for MDC, MDIO, MDINT, DIO0 and DIO1. The default (initial) value of this bit depends on the bootstrap configuration.	−	R/W
9	Link Reset	This bit can be used to reset the TX and RX functions of the PHY. When set to 1, the link is reset, then normal operation resumes. 1 = Reset Link Status 0 = Normal Operation NOTE: the implementation of this bit differs from IEEE 802.3 Clause 22.2.4.1.7. However, it allows the device to be managed by standard software drivers.	0	R/W SC
8	Duplex Mode	This bit controls the duplex mode of operation of the PHY. 0 = Half−Duplex 1 = Full−Duplex Since the NCN26000 supports only the Half−Duplex mode of operation, this bit always reads as 0. Additionally, writing to this bit has no effect.	0	R
7	Collision Test	This bit enables the collision test mode. 1 = Collision Test enabled 0 = Normal Operation For a description of collision test mode, see IEEE 802.3 Clause 22.2.4.1.9.	0	R/W
6	Speed (MSB)	Link speed capability Together with bit 0.13 this bit indicates that the PHY only supports 10 Mb/s operation. Both bit 0.6 and bit 0.13 always read as 0. Additionally, writes to bits 0.6 and 0.13 have no effect.	0	R

CONTROL REGISTER (Address 0)

Bit(s)	Name	Description	Default Value	Register Type (Note 4)
5	Unidirectional Enable	This function is not available on 10BASE−T1S PHY devices. Therefore, this bit always reads as 0. Additionally, writing to this bit has no effect.	0	R
4:0	−	Not used	0	R

4. Register Type: R = Read, W = Write, SC = Self−Clearing, LH = Latching High

STATUS REGISTER (Address 1)

Bit(s)	Name	Description	Default Value	Type
15:12	−	Always reads as 0	0	RO
11	10 Mb/s Half Duplex	Always reads as 1 Indicates that the PHY supports 10 Mb/s Half-Duplex operation.	1	RO
10:8	−	Always reads 0	000	RO
7	Unidirectional Ability	Always reads 0 10BASE−T1S PHY devices do not support unidirectional links	0	RO
6	MF Preamble Suppression	Always reads as 0 The PHY does not accept MDIO frames with suppressed preamble.	0	RO
5	Link Negotiation Complete	1 = link negotiation complete 0 = link negotiation in progress The PHY sets this bit when the PHY Control register bit 12 is set to 1 and bit 9 is set to 0. This bit is further masked by the PLCA status bit when PLCA is enabled. This prevents standard drivers from sending data while PLCA is starting. NOTE: The implementation of this bit is different from IEEE 802.3 Clause 22.2.4.2.10 (Auto negotiation Enable). However, it allows the NCN26000 to be managed by standard software drivers.	−	RO
4	Remote Fault	This bit indicates whether a remote jabber condition was detected since the last read. 1 = remote jabber detected 0 = no remote jabber detected The jabber condition is latched until this field is read or the PHY is reset.	−	R−LH SC
3	Auto−Negotiation Ability	Always reads 1 While auto−negotiation is not supported, this bit is set to 1 to allow the NCN26000 to be managed by standard software drivers.	1	RO
2	Link Status	Although there is not concept of link status for 10BASE−T1S PHY devices, this bit is set after the link control setting. This bit is further masked by the PLCA status bit when PLCA is enabled. This prevents standard drivers from sending data while PLCA is starting. 1 = link is up 0 = link is down NOTE: the implementation of this bit differs from IEEE 802.3 Clause 22.2.4.2.13 (Link Status), because the status is affected by the PLCA−RS status.	−	RO

STATUS REGISTER (Address 1)

Bit(s)	Name	Description	Default Value	Type
1	Jabber Detect	This bit is set when a local jabber fault is detected. 1 = local jabber detected 0 = no local jabber detected The fault condition is latched until this field is read, or the integrated PHY is reset. See also 802.3cg Clause 147.3.2.9	–	R–LH SC
0	Extended Capability	Always reads 1 Indicates that the integrated PHY contains registers that are normally found in Clause 45 of the IEEE802.3 specification.	1	RO

PHY IDENTIFIER REGISTER (Address 2)

Bit(s)	Name	Description	Default Value	Register Type
15:0	PHY identifier MSB	OUI [3:18] Note that the bit order is reversed. Bit 15 corresponds to bit 3 of the OUI; bit 0 corresponds to bit 18 of the OUI.	0x180F	R

PHY IDENTIFIER REGISTER (Address 3)

Bit(s)	Name	Description	Default Value	Register Type
15:10	PHY Identifier LSB	OUI[19:24] Note that the bit order is reversed. Bit 15 corresponds to bit 19 of the OUI, bit 10 corresponds to bit 24 of the OUI.	0x3D	R
9:4	PHY Identifier LSB	IC Model Number	0x1A	R
3:0	PHY Identifier LSB	Chip Revision Number	0x1	R

MMD ACCESS CONTROL REGISTER (Address 13)

Bit(s)	Name	Description	Default Value	Register Type
15:14	Function	0 0 = Select Clause 45 register address 0 1 = Select Clause 45 register content, no address increment 1 0 = Select Clause 45 register content, increment address on both read and write 1 1 = Select Clause 45 register content, increment address on write Refer to IEEE 802.3 Clause 22.2.4.3.11 for details		R/W
13:5	Reserved	Always reads as 0	0	R
4:0	DEVADD	Device address This is also known as MMD (MDIO Manageable Device) in IEEE 802.3 documentation. Refer to IEEE 802.3 Clause 22.2.4.3.11 for details	0	R/W

MMD ACCESS ADDRESS DATA REGISTER (Address 14)

Bit(s)	Name	Description	Default Value	Register Type
15:0	Address Data	Refer to IEEE 802.3 Clause 22.2.4.3.12 for details		R/W

MIIM IRQ CONTROL REGISTER (Address 16)

Bit(s)	Name	Description	Default Value	Type
15:6	Not Used	Not used	0x000	R
5	Physical Collision IRQ Control	1 = MDINT on Physical Collision enabled 0 = MDINT on Physical Collision disabled If enabled, MDINT event is issued every time a physical collision is detected.	0	R/W
4	PLCA Recovery IRQ Control	1 = MDINT on PLCA Recovery enabled 0 = MDINT on PLCA Recovery disabled When enabled, a MDINT event is issued on every PLCA Recovery event. PLCA recovery is flagged when a false carrier event (e.g., impulse noise) occurs on the line. When a CRS event is not followed by the reception of a packet within a certain amount of time the PHY goes into a state depending on its PLCA configuration: When configured as coordinator node, the PHY waits for the line to be quiet for a certain amount of time and then sends a new BEACON. When not configured as a coordinator node, the PHY waits for a BEACON before getting a new transmit opportunity.	0	R/W
3	Remote Jabber IRQ Control	1 = MDINT on Remote Jabber enabled 0 = MDINT on Remote Jabber disabled When enabled, a MDINT event is issued every time the embedded PHY detects a remote jabber condition. A remote jabber condition occurs if a station transmits for longer than maxEnvelopeFrameSize (2000 bytes, including FCS).	0	R/W
2	Local Jabber IRQ Control	1 = MDINT on Local Jabber enabled 0 = MDINT on Local Jabber disabled When enabled, a MDINT event is asserted each time the PHY detects a local jabber condition. A local jabber condition occurs if the TXEN pin is asserted for longer than maxEnvelopeFrameSize (2000 bytes, including FCS).	0	R/W
1	PLCA Status Change IRQ Control	1 = MDINT on change of PLCA Status 0 = no MDINT on change of PLCA Status When enabled, the device issues a MDINT every time the PLCA Status changes. The actual value of PLCA status can be read from the PLCA STATUS REGISTER (MMD 31, Address 51715)	0	R/W
0	Link Status IRQ Control	1 = MDINT on change of Link Status enabled 0 = MDINT on change of Link Status disabled When enabled, a MDINT event is issued every time the link status changes. The actual value of link status can be read from the Link Status bit (1.2) in the PHY Status register (Clause 22, Address 1).	0	R/W

MIIM IRQ STATUS REGISTER (Address 17)

Bit(s)	Name	Description	Default Value	Type
15	Reset IRQ Status	This bit is set at POR or when nRST is asserted. Write 1 to clear. This bit does not generate an interrupt on MDINT and cannot be set once cleared. Its only purpose is to notify the host of a potentially unsolicited reset.	1	R
14:6	Not Used	Not used	0x000	R
5	Physical Collision IRQ Status	When high, this bit indicates that at least one physical collision has been detected since the last read of this register	0	R−LH SC
4	PLCA Recovery IRQ Status	When high, this bit indicates that at least one PLCA recovery event occurred since the last read of this register	0	R−LH SC
3	Remote Jabber IRQ Status	When high, this bit indicates that at least one remote jabber event occurred since the last read of this register	0	R−LH SC
2	Local Jabber IRQ Status	When high, this bit indicates that at least one local jabber event occurred since the last read of this register	0	R−LH SC
1	PLCA Status Change IRQ Status	When high, this bit indicates that the PLCA status bit changed since the last read of this register. The actual value of PLCA status can be read from the PLCA Status Register, PLCASTATUS (MMD 31, Address 51715).	0	R−LH SC
0	Link Status Change IRQ Status	When high, this bit indicates that the link status bit changed since the last read of this register. The actual value of link status can be read from the Link Status bit (1.2) in the PHY Status register (Clause 22, Address 1).	0	R−LH SC

DIO CONFIGURATION REGISTER (Address 18)

The DIO configuration register controls the function of the General Purpose I/O pins DIO1 and DIO0.

Bit(s)	Name	Description	Default Value	Type
15	Slew Rate 1	Sets the slew rate of the DIO1 output. 1 = slow 0 = fast	0	R/W
14	Pull Enable 1	When enabled, DIO1 is programed to provide an internal pull−up or pull−down resistor, depending on bit 13 of this register. 1= enabled 0 = disabled	1	R/W
13	Pull Resistor Type 1	Sets the type of the internal pull when bit 14 is set. 1 = Pull Down 0 = Pull Up	1	R/W
12:9	FN1[3:0]	Selects the function of the DIO1 pin. See table for FNx below.	0	R/W
8	VAL1	Sets the output value of DIO1 when FN1[3:0] is set to GPIO function. For all other functions, sets the polarity of the DIO1 pin 1 = active high 0 = active low	0	R/W
7	Slew Rate 0	Sets the slew rate of the DIO0 output. 1 = slow 0 = fast	0	R/W
6	Pull Enable 0	When enabled, DIO0 is programed to provide an internal pull−up or pull−down resistor, depending on bit 5. 1 = enabled 0 = disabled	1	R/W
5	Pull Resistor Type 0	Sets the type of the internal pull when bit 6 is enabled. 1 = Pull Down 0 = Pull Up	1	R/W

DIO CONFIGURATION REGISTER (Address 18)

The DIO configuration register controls the function of the General Purpose I/O pins DIO1 and DIO0.

Bit(s)	Name	Description			Default Value	Type
4:1	FN0[3:0]	Selects the function of the DIO0 pin according to the below table:			0x0	R/W
		FNx[3:0]	**Function**	**Description**		
		0x0	Disable	DIOx is set to high−impedance (default)		
		0x1	GPIO (output)	Output value is set after VALx		
		0x2	SFD−TX	Generates a pulse at SFD transmission. VALx sets the pulse polarity.		
		0x3	SFD−RX	Generates a pulse when SFD is detected during RX. VALx sets the pulse polarity. (Note 5)		
		0x4	LED Link Control	Pin drives a LED when port is enabled and link status is up		
		0x5	LED PLCA Status	Pin drives a LED when PLCA status is up		
		0x6	LED TX	LED indicating TX activity		
		0x7	LED RX	LED indicating RX activity. (Note 5)		
		0x8	CLK25M	Output 25 MHz clock		
		0x9 – 0xA	Reserved	Don't use		
		0xB	SFD− RX&TX	Pulse on DIOx at SFD (RX or TX), VALx sets the polarity of the pulse		
		0xC – 0xE	Reserved	Don't use		
		0xF	LED TX&RX	LED indicating TX and RX activity		
0	VAL0	Sets the output value of DIO0 when FN0[3:0] is set to GPIO function. It sets the polarity (1 = active high, 0 = active low) for all other modes.			0	R/W

5. Also triggers on TX

CLAUSE 45 REGISTERS

The following Clause 45 registers are implemented (reserved registers not shown)

MMD	Register Address		Standard = S Vendor Specific = V	Register Name
	Decimal	Hex		
1	5	0005	S	Devices in Package 1
	6	0006		Devices in Package 2
	18	0012		BASE−T1 Extended Ability
	2297	08F9		10BASE−T1S PMA Control
	2298	08FA		10BASE−T1S PMA Status
	2299	08FB		10BASE−T1S Test Mode
3	5	0005		Devices in Package 1
	6	0006		Devices in Package 2
	2291	08F3		10BASE−T1S PCS Control
	2292	08F4		10BASE−T1S PCS Status
	2293	08F5		10BASE−T1S PCS Diagnostic 1
	2294	08F6		10BASE−T1S PCS Diagnostic 2

CLAUSE 45 REGISTERS

The following Clause 45 registers are implemented (reserved registers not shown)

MMD	Register Address		Standard = S Vendor Specific = V	Register Name
	Decimal	Hex		
30	4096	1000	V	**onsemi** Chip Revision
	4097	1001		PHY Tweaks
	4100	1004		Chip Info
	4101	1005		NVM Health
31	32768	8000	V	PHY Revision
	32769	8001		PHY Configuration 1
	32770	8002		PLCA Extensions
	32771	8003		PMA Tune 0
	32772	8004		PMA Tune1
	51712	CA00	S	PLCA Register Map and Identification, PLCIDVER
	51713	CA01		PLCA Control 0
	51714	CA02		PLCA Control 1
	51715	CA03		PLCA Status
	51716	CA04		PLCA Transmit Opportunity Timer
	51717	CA05		PLCA Burst Mode

DEVICES IN PACKAGE 1 REGISTER (MMD 1 / 3, Address 5)

Bit(s)	Name	Description	Default Value	Register Type
15:4	–	Always reads as 0	0x000	R
3	PCS Present	Always reads as 1 Indicating that the device contains the PCS	1	R
2	–	Always reads as 0	0	R
1	PMA Present	Always reads as 1 Indicating that the device contains the PMA	1	R
0	Clause 22 Registers present	Always reads as 1 Indicating that the device contains Clause 22 standard registers	1	R

DEVICES IN PACKAGE 2 REGISTER (MMD 1 / 3, Address 6)

Bit(s)	Name	Description	Default Value	Register Type
15:0	–	Always reads as 0	0x0000	R

BASE−T1 EXTENDED ABILITY REGISTER (MMD 1, Address 18)

Bit(s)	Name	Description	Default Value	Register Type
15:4	–	Always read as 0	0	R
3	10BASE−T1S	Always read as 1 This is a 10BASE−T1S only PHY	1	R
2:0	–	Always reads as 0	0	R

10BASE−T1S PMA CONTROL REGISTER (MMD 1, Address 2297)

Bit(s)	Name	Description	Default Value	Register Type
15	PMA Reset	Alias of Clause 22 bit 0.15	0	R/W SC
14	Transmit Disable	When enabled, the PHY's transmitter is disabled and TX requests from the MII are ignored as well as any configuration that requires the PHY to drive the LINEx pins, which stay in a high−impedance state. 1 = disable Transmit 0 = enable Transmit	0	R/W
13:12	−	Always reads as 0	0	R
11	Low power Mode	Alias of Clause 22 bit 0.11	0	R
10	Multi−Drop enable	This bit controls the multi−drop mode of the PHY. Since the NCN26000 is a multi−drop only device, this bit always reads as 1. Additionally, writing to this bit has no effect.	1	R
9:1	−	Always reads as 0	0	R
0	Loopback Mode	Alias of Clause 22 bit 0.14	0	R/W

10BASE−T1S PMA STATUS REGISTER (MMD 1, Address 2298)

Bit(s)	Name	Description	Default Value	Register Type
15:14	−	Always reads as 0	0	R
13	Loopback ability	Always reads as 1, indicating the PHY supports loopback	1	R
12	−	Always reads as 0	0	R
11	Low power ability	Always reads as 0 because the PHY does not support Low Power Mode	0	R
10	Multi−Drop ability	Always reads as 1, indicating that the NCN26000 supports Half−Duplex multi−drop operation	1	R
9	Receive Fault ability	Always reads as 1, indicating that the NCN26000 supports receive fault (jabber) detection.	1	R
8:2	−	Always reads as 0	0	R
1	Remote Jabber	Alias of Clause 22 Register 1.4.	0	R
0	−	Always reads as 0	0	R

10BASE−T1S TEST MODE CONTROL REGISTER (MMD 1, Address 2299)

Bit(s)	Name	Description		Default Value	Type
15:13	Test Mode	Test mode in accordance with IEEE802.3cg. The default is “normal operation”		000	R/W
		Pattern	**Test Mode**		
		000	Normal Operation		
		001	Transmitter Output Voltage test		
		010	Transmitter Output Droop test		
		011	Transmitter PSD mask test		
		100	Transmitter high Impedance test		
		101	Reserved		
		110	Reserved		
		111	Reserved		
12:0	reserved	Always reads as 0		0	R

10BASE−T1S PCS CONTROL REGISTER (MMD 3, Address 2291)

Bit(s)	Name	Description	Default Value	Type
15	PCS Reset	1 = PCS reset 0 = normal operation Setting this bit to 1 sets all registers to their default state. Resetting the PCS also causes the PMA and PLCA layers to reset, as if a soft reset was issued.	0	R/W SC
14	Loopback	This bit controls the PCS loopback mode of the PHY. 1 = Loopback enabled 0 = Loopback disabled When enabled, data sent by the MAC through the MII TX is looped back to the MII RX traversing the PCS. This allows testing the MII interface, the 4B/5B encoder/decoder, the TX/RX state machines, and the scrambler/descrambler.	0	R/W
13:0	reserved	Always reads as 0	0	R

10BASE−T1S PCS STATUS Register (MMD 3, Address 2292)

Bit(s)	Name	Description	Default Value	Type
15:8	−	Always read 0	0	R
7	Fault	1 = Fault condition detected 0 = No fault condition detected If this bit reads as 1, the PCS has latched a jabber fault condition since the last read of this register. This can either be a local or a remote jabber condition.	−	RO−LH
6:0	−	Always read 0	0	R

10BASE−T1S PCS DIAGNOSTICS REGISTER 1 (MMD 3, Address 2293)

Bit(s)	Name	Description	Default Value	Type
15:0	PCS Remote Jabber Count	Counts the number of detected remote jabber events since this register was last read. For details, see IEEE802.3cg Clause 45.2.3.68e.1. If the count reaches 0xFFFF, no more errors are counted to prevent the counter from overflowing.	0	RO−SC

10BASE−T1S PCS DIAGNOSTICS REGISTER 2 (MMD 3, Address 2294)

Bit(s)	Name	Description	Default Value	Type
15:0	PCS Physical Collisions Count	Counts the number of physical collision events detected by the PHY since this register was last read. If the count reaches 0xFFFF, no more errors are counted to prevent the counter from overflowing. NOTE: Physical collisions are caused by the superposition of signals transmitted simultaneously by more than one station on the same medium. In contrast to physical collisions, logical collisions in PLCA mode are triggered by the PLCA RS arbitration algorithm.	0	RO−SC

CHIP REVISION REGISTER (MMD 30, Address 4096)

Bit(s)	Name	Description	Default Value	Type
15:12	Major Revision	Major release number	−	R
11 8	Minor Revision	Minor release number	−	R
7:6	Stage	Maturity level − Stable	−	R
5:0	Patch	Patch level build number	−	R

PHY TWEAKS REGISTER (MMD 30, Address 4097)

The PHY TWEAKS register allows experienced users to customize the parameters of the analog line driver among other custom parameters. The default values have been carefully selected for optimum performance and do not need modification under typical conditions.

Bit(s)	Name	Description		Default Value	Type
15:14	TX Gain	Specifies the Transmitter Amplitude gain.		0b00	R/W
		TX Gain	**TX Amplitude (mV_{pp})**		
		0b00	1000		
		0b01	1100		
		0b10	900		
		0b11	800		
		NOTE: This is an advanced configuration register. It is recommended to consult with **onsemi** before changing the value from its default settings			

PHY TWEAKS REGISTER (MMD 30, Address 4097)

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<table>
<tr><th>Bit(s)</th><th>Name</th><th colspan="2">Description</th><th>Default Value</th><th>Type</th></tr>
<tr><td rowspan="19">13:10</td><td rowspan="19">CD Threshold</td><td colspan="2">Specifies the Collision Detection threshold level.
$CD_{Threshold}$ = 150 mV + 50 mV_{pp} * CDL</td><td rowspan="19">0xB</td><td rowspan="19">R/W</td></tr>
<tr><td>CDL</td><td>Threshold Level (mV_{pp})</td></tr>
<tr><td>0</td><td>150</td></tr>
<tr><td>1</td><td>200</td></tr>
<tr><td>2</td><td>250</td></tr>
<tr><td>3</td><td>300</td></tr>
<tr><td>4</td><td>350</td></tr>
<tr><td>5</td><td>400</td></tr>
<tr><td>6</td><td>450</td></tr>
<tr><td>7</td><td>500</td></tr>
<tr><td>8</td><td>550</td></tr>
<tr><td>9</td><td>600</td></tr>
<tr><td>10</td><td>650</td></tr>
<tr><td>11</td><td>700 (default)</td></tr>
<tr><td>12</td><td>750</td></tr>
<tr><td>13</td><td>800</td></tr>
<tr><td>14</td><td>850</td></tr>
<tr><td>15</td><td>900</td></tr>
<tr><td colspan="2">NOTE: This is an advanced configuration register. It is recommended to consult with onsemi before changing the value from its default settings.</td></tr>
</table>

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The PHY TWEAKS register allows experienced users to customize the parameters of the analog line driver among other custom parameters. The default values have been carefully selected for optimum performance and do not need modification under typical conditions.

<table>
<tr><th>Bit(s)</th><th>Name</th><th>Description</th><th>Default Value</th><th>Type</th></tr>
<tr><td>9:6</td><td>RX_ED Threshold</td><td>Specifies the RX energy detection threshold level following this equation $RX_{ED\ Threshold}$ = 150 mV + 50 mV_{pp} * RX_ED
<table>
<tr><th>RX_ED</th><th>ED Threshold Level (mV_{pp})</th></tr>
<tr><td>0</td><td>150</td></tr>
<tr><td>1</td><td>200</td></tr>
<tr><td>2</td><td>250 (default)</td></tr>
<tr><td>3</td><td>300</td></tr>
<tr><td>4</td><td>350</td></tr>
<tr><td>5</td><td>400</td></tr>
<tr><td>6</td><td>450</td></tr>
<tr><td>7</td><td>500</td></tr>
<tr><td>8</td><td>550</td></tr>
<tr><td>9</td><td>600</td></tr>
<tr><td>10</td><td>650</td></tr>
<tr><td>11</td><td>700</td></tr>
<tr><td>12</td><td>750</td></tr>
<tr><td>13</td><td>800</td></tr>
<tr><td>14</td><td>850</td></tr>
<tr><td>15</td><td>900</td></tr>
</table>
NOTE: This is an advanced configuration register. It is recommended to consult with onsemi before changing the value from its default settings.</td><td>2</td><td>R/W</td></tr>
<tr><td>5</td><td>Digital Slew Rate</td><td>1 = fast (default)
0 = slow
Sets the output slew rate of all digital I/O pins, excluding DIO0 and DIO1. Setting the slew rate to “fast” improves signal integrity when
driving high capacitive loads but this could lead to an increased power consumption and may adversely affect emissions on the PCB.</td><td>1</td><td>R/W</td></tr>
<tr><td>4:3</td><td>CMC compensation</td><td>In case a common mode choke is used on the line, these bits can be set to compensate for the added common−mode choke resistance and improve EMI performance in high noise environments:
<table>
<tr><th>CMC</th><th>CMC Typical Series Resistance (Ω)</th></tr>
<tr><td>0b00</td><td>0 – 0.5</td></tr>
<tr><td>0b01</td><td>0.5 – 2−25</td></tr>
<tr><td>0b10</td><td>2.25 – 3.75</td></tr>
<tr><td>0b11</td><td>3.75 – 5</td></tr>
</table>
Please, check the CMC supplier datasheet for selecting the optimal value of this parameter.</td><td>0</td><td>R/W</td></tr>
<tr><td>2</td><td>TX Slew</td><td>This bit sets the slew rate of the TX line driver output.

1 = fast
0 = slow

The “slow” setting can help improving the EME performance but may adversely affect the return loss, which may decrease the collision detection mechanism performance.</td><td>0</td><td>RW</td></tr>
</table>

PHY TWEAKS REGISTER (MMD 30, Address 4097)

The PHY TWEAKS register allows experienced users to customize the parameters of the analog line driver among other custom parameters. The default values have been carefully selected for optimum performance and do not need modification under typical conditions.

Bit(s)	Name	Description	Default Value	Type
1	Not used	–	0	R
0	Reserved	Reserved	1	R/W

CHIP INFO REGISTER (MMD 30, Address 4100)

Bit(s)	Name	Description	Default Value	Register Type
15	Not used		0	R
14:8	Wafer_Y	Y position on the Wafer where the part was picked from	–	R
7	Not used		0	R
6:0	Wafer_X	X position on the Wafer where the part was picked from	–	R

NVM HEALTH REGISTER (MMD 30, Address 4101)

This register reports if there are errors in the factory configuration data set by **onsemi** during manufacturing of the NCN26000. There are three different zones for the configuration data stored inside the device non−volatile memory:

Zone	Description
Green	Manufacturing related data Errors in this zone do not cause any device failure or misbehavior in the application.
Yellow	Functional Data: MAC and OUI Corrupted data in this area does not cause the part to malfunction, but a host relying on this information may not initialize correctly. However, countermeasures taken in the host software could be used to fall back to a state where operation is still possible.
Red	Configuration data Data corruption in this area may render the part unusable, prevent the part from operating within the specified electrical characteristic, or impair performance.

Note that the configuration memory cannot be written by the user, so corrupted data cannot be recovered.

The configuration memory is protected by an ECC scheme that allows the automatic correction of a single bit error and the detection of multiple bit errors. With this feature, a single bit error (SBERR) can be considered a warning, while a reported multiple bit error shall be interpreted as an error impairing the function of the part (partially or entirely), depending on the zone in which it appears.

Bit(s)	Name	Description	Default Value	Type
15	Red Zone NVM Warning	When this bit reads as 1, the ECC controller has corrected a single bit error in the red zone. As single bit errors are corrected by the ECC controller, this is just a warning. The NCN26000 remains fully functional.	0	R
14	Red Zone NVM Error	When this bit reads as 1, the ECC controller has detected at least two unrecoverable bit errors in the red zone. This shall be treated as a permanent error, as correct functionality cannot be guaranteed. The part may still be able to operate with degraded performance.	0	R
13	Yellow Zone NVM Warning	When this bit reads as 1, the ECC controller has corrected a single bit error in the yellow zone. The NCN26000 remains fully functional, and a host relying on the information stored in the NVM is not affected.	0	R
12	Yellow Zone NVM Error	When this bit reads as 1, the ECC controller has detected at least two unrecoverable bit errors in the yellow zone. While this is a permanent error invalidating the content of the OUI and the MAC ID, the NCN26000 remains fully functional. However, a host relying on such information may not initialize correctly.	0	R
11	Green Zone NVM warning	When this bit reads as 1, the ECC controller has corrected a single bit error in the green zone of the trim and configuration memory. The NCN26000 remains fully functional.	0	R
10	Green Zone NVM error	When this bit reads as 1, the ECC controller has detected at least two unrecoverable bit errors in the green zone. As the green zone contains only manufacturing and tracing information, the NCN26000 remains fully functional. However, a part affected by this error loses its manufacturing traceability.	0	R
9:0	Reserved	Reserved	–	R

PHY REVISION REGISTER (MMD 31, Address 32768)

Bit(s)	Name	Description	Default Value	Type
15 : 12	Major Revision	Major release number	–	R
11 : 8	Minor Revision	Minor release number	–	R
7 : 6	Stage	Maturity level – Stable	–	R
5 : 0	Patch	Patch level build number	–	R

PHY CONFIGURATION 1 REGISTER (MMD31, Address 32769)

The PHY configuration 1 register allows using non−IEEE802.3 compliant operation modes that can help with debugging and increased performance in noisy environments. Note that these setting should be used with care as they might result in a network configuration that prohibits successful communication.

Bit(s)	Name	Description	Default Value	Type
15	Packet Loop	This bit controls whether the PHY loops back transmitted packets to the MII. 1 = Packet Loop enabled 0 = Packet Loop disabled When enabled, the PHY receives loop back any packet transmitted on the line. While this behavior is generally unwanted and not defined in IEEE 802.3cg specifications, it may be useful if the PHY is connected to an obsolete / non−IEEE compliant MAC or Ethernet bridge that requires the PHY to loop back transmitted frames. **onsemi** strongly recommends leaving this bit to 0 (default) unless the user is experiencing problems with the connected host device. Note that this configuration differs from the PCS/PMA loop back mode (clause 22 register 0 bit 14), as in that case the transmitted frames are not sent over the line.	0	R/W
14:8	Not used	−	0x00	R
7	Enhanced Noise Immunity	This bit controls the Enhanced Noise Immunity (ENI) mode of the PHY. 1 = Enhanced noise immunity enabled 0 = Enhanced noise immunity disabled Enhanced Noise Immunity (ENI) mode allows extending the PHY noise immunity to values above the IEEE 802.3cg defined noise levels, allowing the device to withstand and exceed industry standard immunity tests. ENI mode changes the way the PHY detects a carrier to overcome false carrier detection when noise on the line roughly exceeds 220 mVPP. Instead of relying solely on energy detection, the PMA further qualifies carrier detection by detecting a valid Manchester coding, thus rejecting in−band noise. While ENI is a non−standard feature, it is fully interoperable with pure PLCA−enabled networks. On this kind of networks, immunity can be further improved by disabling physical collision detection.	0	R/W
6	Unjab Timer Enable	This bit controls whether the device shall automatically try to resume transmissions after a local jabber event occurred. 1 = Unjab Timer enabled 0 = Unjab Timer disabled When the Unjab Timer is enabled, the PHY restores the transmit functions after some time since the last detected local jabber error. When Unjab Timer is disabled, only a device (soft or hard) reset can restore transmissions. See Clause 147.3.2 of the IEEE 802.3cg specification for more details. Note that a local jabber error is typically created by a permanent failure of the host device. Therefore, the Unjab Timer is disabled by default to prevent unwanted transmissions to flood the shared bus.	0	R/W
5:3	Not used	−	0x0	R
2	Scrambler Disable	This bit controls the scrambling function of the PHY. 1 = PCS scrambling disabled 0 = PCS scrambling enabled When set, the PCS scrambling function is disabled and the 4B data is sent unaltered to the 4B/5B and DME encoders. In addition, data received from the line is not de−scrambled after the 5B/4B conversion. This is a debug feature not intended for normal operation.	0	R/W

PHY CONFIGURATION 1 REGISTER (MMD31, Address 32769)

The PHY configuration 1 register allows using non−IEEE802.3 compliant operation modes that can help with debugging and increased performance in noisy environments. Note that these setting should be used with care as they might result in a network configuration that prohibits successful communication.

Bit(s)	Name	Description	Default Value	Type
1	No Collision Masking	This bit controls whether the PHY shall ignore physical collision events on the line when PLCA and ENI modes are both enabled. 1 = ENI collision detection masking disabled 0 = ENI collision detection masking enabled If set, this bit prevents masking of collision detection when Enhanced Noise Immunity (ENI) mode and PLCA are enabled. Note that even if collisions are masked, the PCS Diagnostic Register 2 still counts detected corruptions of the transmitted signal for diagnostic/debug purposes.	1	R/W
0	RX Delayed	This bit configures the internal path delay length when receiving frames. 1 = delayed reception enabled 0 = delayed reception disabled Setting this bit enables an additional RX data path delay of 14 MII clock cycles. This may be required when connecting the NCN26000 to non−IEEE compliant MAC controllers that do not support receiving frames across collisions when operating in Half−Duplex mode. Note that although this setting is enabled by default for maximum compatibility, most MAC controllers are not affected by this problem. This bit can therefore be set to 0 to decrease the RX latency by approximately 5.6 μs.	1	R/W

PLCA EXTENSIONS REGISTER (MMD31, Address 32770)

Bit(s)	Name	Description	Default Value	Type
15	PLCA Precedence	This bit controls the proprietary PLCA precedence mode feature. 1 = Precedence Mode enabled 0 = Precedence Mode disabled While in Precedence Mode, the PLCA RS implicitly terminates a cycle at each transmitted or received packet, causing the network to emulate a CAN network where nodes with lower local node IDs get strict precedence over nodes with higher PLCA IDs. With strict precedence, a node could transmit for indefinite time without being interrupted. Depending on how the network is engineered, nodes with higher PLCA IDs are subject to starvation (as they might never get permission to transmit). Note that all nodes shall support precedence mode for this feature to work, and that precedence mode is not interoperable with standard PLCA.	0	R/W
14:12	Not used	–	0x0	R
11	MII extensions disable	This bit controls whether the MII shall expose the encoding/decoding of PLCA commands when the internal PLCA RS is disabled. 1 = MII extensions disabled 0 = MII extensions enabled When this bit is set, and PLCA is not enabled, the PHY does not forward PLCA BEACON and COMMIT indications to/from the MII. Unless the PHY is connected to an ***external*** PLCA RS, this bit should be set to 1 (default) to maximize the compatibility with existing Media Access Controller implementations.	1	R/W
10:2	Not used	–	0x00	R

PLCA EXTENSIONS REGISTER (MMD31, Address 32770)

Bit(s)	Name	Description	Default Value	Type
1	Coordinator Mode	This bit controls whether the PLCA coordinator node is allowed to take non−zero IDs. 1 = Coordinator Mode enabled 0 = Coordinator Mode disabled When enabled, the NCN26000 coordinator role is determined by the 'Coordinator Role' bit setting in this register. When disabled, the NCN26000 is assigned the coordinator role if its PLCA ID is set to 0 in the PLCA CONTROL 1 Register (as per IEEE 802.3cg specifications)	0	R/W
0	Coordinator Role	1 = node is the PLCA coordinator 0 = node is a PLCA follower When the 'Coordinator Mode' bit in this register is set to 1, the PLCA RS takes the coordinator role based only on the setting of this bit.	0	R/W

PMA TUNE 0 REGISTER (MMD31, Address 32771)

This register allows fine tuning of the NCN26000 line receiver when ENI mode is enabled.
WARNING: changing the setting from their default should only be considered by experienced users at their own risk. Invalid setting may lead to unexpected link down and dropped or corrupted Ethernet frames.

Bit(s)	Name	Description		Default Value	Type
15:14	Not used	–		0x0	R
13:8	PLCA Beacon Detection Threshold	This field selects the threshold level for the PLCA Beacon (NN*) detection in the PMA when ENI mode is enabled. Higher values reduce the chance of false detection (false positive) but reduces the noise tolerance. Lower values achieve the opposite effect.		0x20	R/W
7:3	Not used	–		0x0	R
2:1	Drift Compensation Window Selection	Selects the size of the integration window for the clock drift compensator inside the PMA when ENI is enabled. A lower value allows for compensation of more drift at the expense of jitter rejection. Higher values achieve the opposite effect.		0x5	R/W
		Window Selection value	**Integration Window Size**		
		0	reserved		
		1	reserved		
		2	31 bit times		
		3	63 bit times		
		4	127 bit times		
		5	optimized default		
		6	reserved		
		7	reserved		

PMA TUNE 1 REGISTER (MMD31, Address 32772)

This register allows fine tuning of the NCN26000 line receiver when ENI is enabled.
Warning: changing the setting from their default should only be considered by experienced users at their own risk. Invalid setting may lead to unexpected link down and dropped or corrupted Ethernet frames.

Bit(s)	Name	Description	Default Value	Type
15:14	Not used	–	0x0	R
13:8	Packet Preamble Detection Threshold	Sets the threshold level for the packet preamble (JJHH) detection in the PMA RX when ENI mode is enabled. Higher values reduce the chance of false detection (false positive) but reduce the noise tolerance. Lower values achieve the opposite effect.	0x35	R/W
7:6	Not used	–	0x0	R
5:0	Commit Detection Threshold	Sets the threshold for the Commit (JJ*) detection of the PMA RX when ENI mode is enabled. Higher values reduce the chance of false detection (false positive) but reduce the noise tolerance. Lower values achieve the opposite effect.	0x20	R/W

PLCA REGISTER MAP AND IDENTIFICATION REGISTER, PLCIDVER (MMD 31, Address 51712)

This register provides the PLCA register map identification and version, as defined in the Open Alliance Specification

Bit(s)	Name	Description	Default Value	Type
15:8	PLCA memory map identifier MAPID	Indicates compatibility with the OA PLCA memory map definition	0x0A	R
7:0	PLCA memory map version MAPVER	Indicates the version of the OA memory map definition the NCN26000 device adheres to	0x10	R

PLCA CONTROL 0 REGISTER (MMD 31, Address 51713)

Bit(s)	Name	Description	Default Value	Type
15	PLCA Enable	1 = PLCA enabled 0 = PLCA disabled When enabled, the PLCA RS functions are switched on. Otherwise, the PHY behaves in plain CSMA/CD half duplex mode.	0	R/W
14	PLCA Reset	1 = PLCA reset 0 = normal operation When set, the PLCA RS is reset to its initial state. This will also reset the PCS and PMA layers. The NCN26000 registers are not altered by this reset. Upon PLCA reset, this bit is cleared.	0	R/W SC
13:0	–	Always reads 0	0	R

PLCA CONTROL 1 REGISTER (MMD 31, Address 51714)

Bit(s)	Name	Description	Default Value	Type
15:8	PLCA Node Count NCNT	Configures the number of transmit opportunities generated in a PLCA cycle. This parameter is only meaningful when the NCN26000 is operating as the coordinator node in a PLCA enabled network.	0x08	R/W
7:0	PLCA Local Node ID ID	Sets the PHY's local node ID in a PLCA enabled network. This number shall be less than or equal to the PLCA node count (see bits 15:8) of the PLCA coordinator node. When set to 0x0, the PHY acts as PLCA coordinator unless coordinator mode is enabled. Note that the default value of 0xFF disables the PLCA function.	0xFF	R/W

PLCA STATUS REGISTER (MMD 31, Address 51715)

Bit(s)	Name	Description	Default Value	Register Type
15	Beacon TX / RX Status PST	When this bit reads as 1, the PLCA RS is receiving / transmitting the BEACON. Note that only the coordinator node transmits the BEACON. When this bit reads as 0, the PHY is not ready to send or receive data in PLCA mode. This could also be interpreted as an indicator of PLCA activity on the line.	–	R
14:0	–	Always reads as 0	0x0000	R

PLCA TRANSMIT OPPORTUNITY TIMER REGISTER (MMD 31, Address 51716)

Bit(s)	Name	Description	Default Value	Type
15:8	–	Always read 0	0x00	R/W
7:0	Transmit Opportunity Timer TOTMR	Defines the minimum duration, in bit times, of the PLCA transmit opportunity timer as described in the OPEN Alliance PLCA registers specification version 1.0. The default value is 24BT (2.4 μs). Larger values allow for extending the maximum reach of the mixing segment, while lower values improve performance by reducing the overall unused TO time. See IEEE802.3cg Clause 30 and Clause 147 for a detailed description. This parameter shall be set to the same value across all nodes sharing the same medium. WARNING: the NCN26000 default is 24 BT (0x18) while the default value defined in the IEEE802.3cg and the newer version of the OPEN Alliance documentation is 32 BT (0x20).	0x18	R/W

PLCA BURST MODE REGISTER (MMD 31, Address 51717)

Bit(s)	Name	Description	Default Value	Type
15:8	Maximum Burst Count	Sets the number of additional Ethernet frames that may be transmitted during a single transmit opportunity. The default allows only one frame to be sent per transmit opportunity. See IEEE802.3cg Clause 148.4.4.2 for more details.	0x00	R/W
7:0	Inter Frame Gap Compensation Timer	Sets the number of bit times that the PLCA RS waits for the MAC to send a frame, after CRS is de−asserted. The default of 128 comprises the minimum inter−frame gap of 96 bits, as defined in IEEE802.3 Clause 4.4.2, plus additional margin. This setting can be used to fine tune the PLCA burst performance.	0x80	R/W

Timings

MII TX

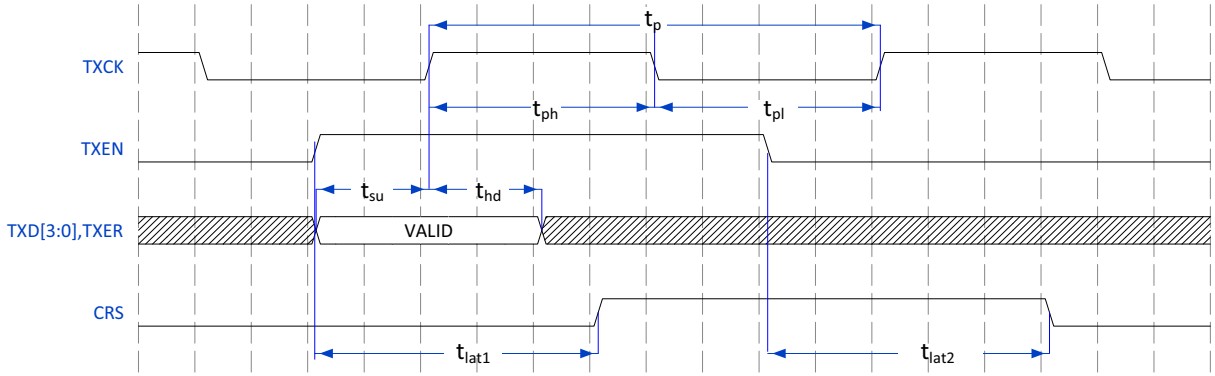


Figure 2. MII Transmit Timing

Table 8. MII TX TIMING PARAMETERS

Item	Parameter	Min	Typ	Max	Unit
t_p	TXCK period	399.96	400	400.04	ns
t_{ph}	TXCK high pulse width	–	200	–	ns
t_{pl}	TXCK low pulse width	–	200	–	ns
t_{su}	TXD, TXER, TXEN setup time with respect to rising edge of TXCK	10	–	–	ns
t_{hd}	TXD, TXER, TXEN hold time with respect to rising edge of TXCK	10	–	–	ns
t_{lat1}	TXEN high to CRS latency	–	800	–	ns
t_{lat2}	TXEN low to CRS deassert	–	800	–	ns

MII RX

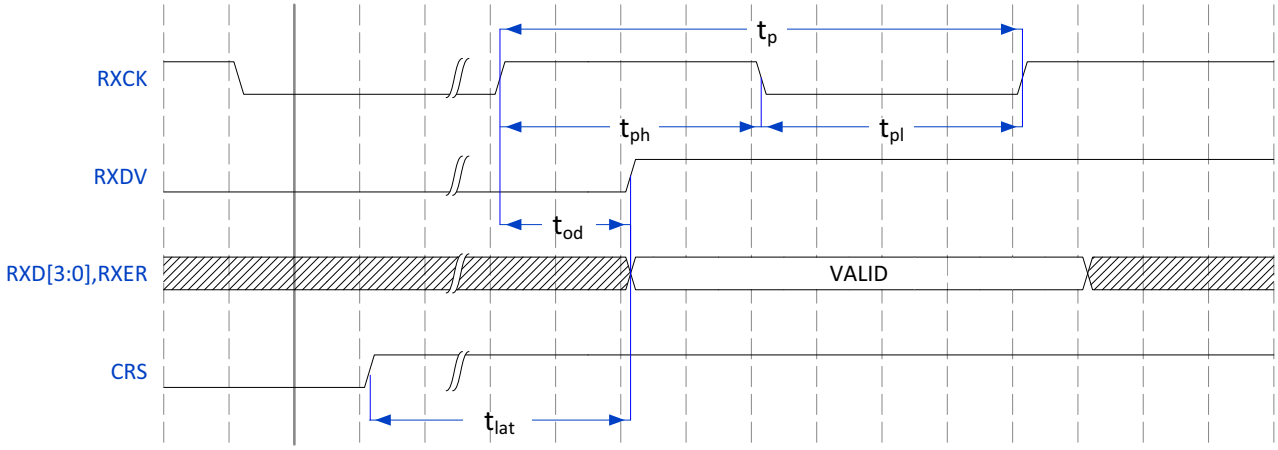


Figure 3. MII Receive Timing

Table 9. MII RX TIMING PARAMETERS

Item	Parameter	Min	Typ	Max	Unit
t_p	RXCK period	399.96	400	400.04	ns
t_{ph}	RXCK high pulse width	–	200	–	ns
t_{pl}	RXCK low pulse width	–	200	–	ns
t_{od}	RXD, RXER, RXDV output delay from rising edge of RXCK	182	–	250	ns
t_{lat}	CRS to RXD, RXER, RXDV latency	–	6.4	–	μs

MIIM

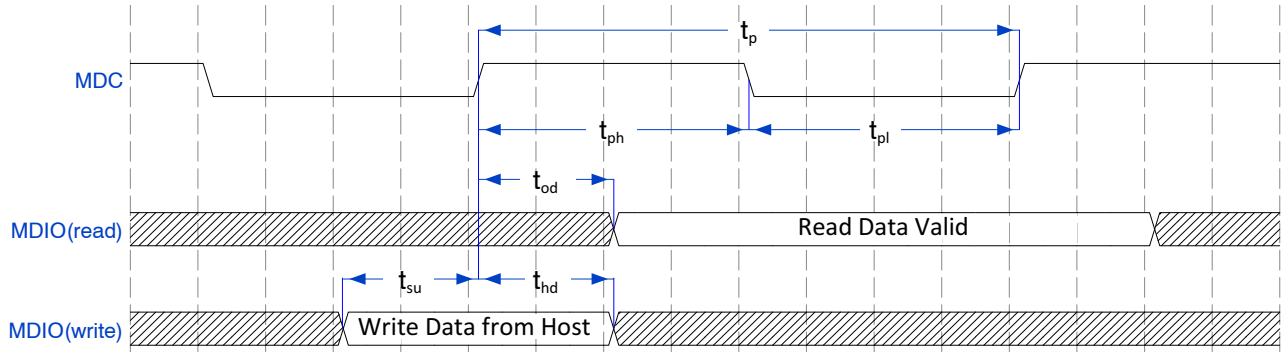


Figure 4. Management Interface Timing

Table 10. MIIM TIMING PARAMETERS

Item	Parameter	Min	Typ	Max	Unit
t_p	MDC clock period			400	ns
t_{ph}	MDC high pulse width	–	200	–	ns
t_{pl}	MDC low pulse width	–	200	–	ns
t_{od}	MDIO (PHY output) delay from rising edge of MCD	–	222	–	ns
t_{su}	MDIO (PHY input) setup time to rising edge of MDC	10	–	–	ns
t_{hd}	MDIO (PHY input) hold time from rising edge of MDC	4	–	–	ns

Bootstrap

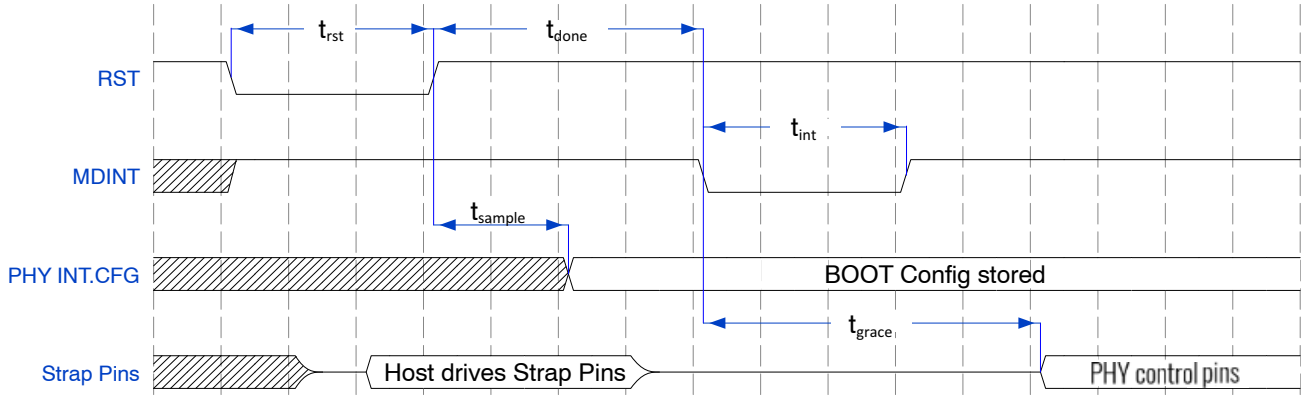


Figure 5. Boot Timing

Table 11. BOOT TIMING PARAMETERS

Item	Parameter	Min	Typ	Max	Unit
t_{rst}	Reset pulse width	160	–	–	ns
t_{samp}	RST released to strap pins sampled	2	–	16	μs
t_{done}	RST released to MDINT low (boot done)	0.5	1.5	2	ms
t_{int}	MDINT pulse width	160	–	320	ns
t_{su}	MDIO (PHY input) setup time to rising edge of MDC	10	–	–	ns
t_{grace}	MDINT asserted to pins controlled by PHY	640	–	–	ns

Applications Information

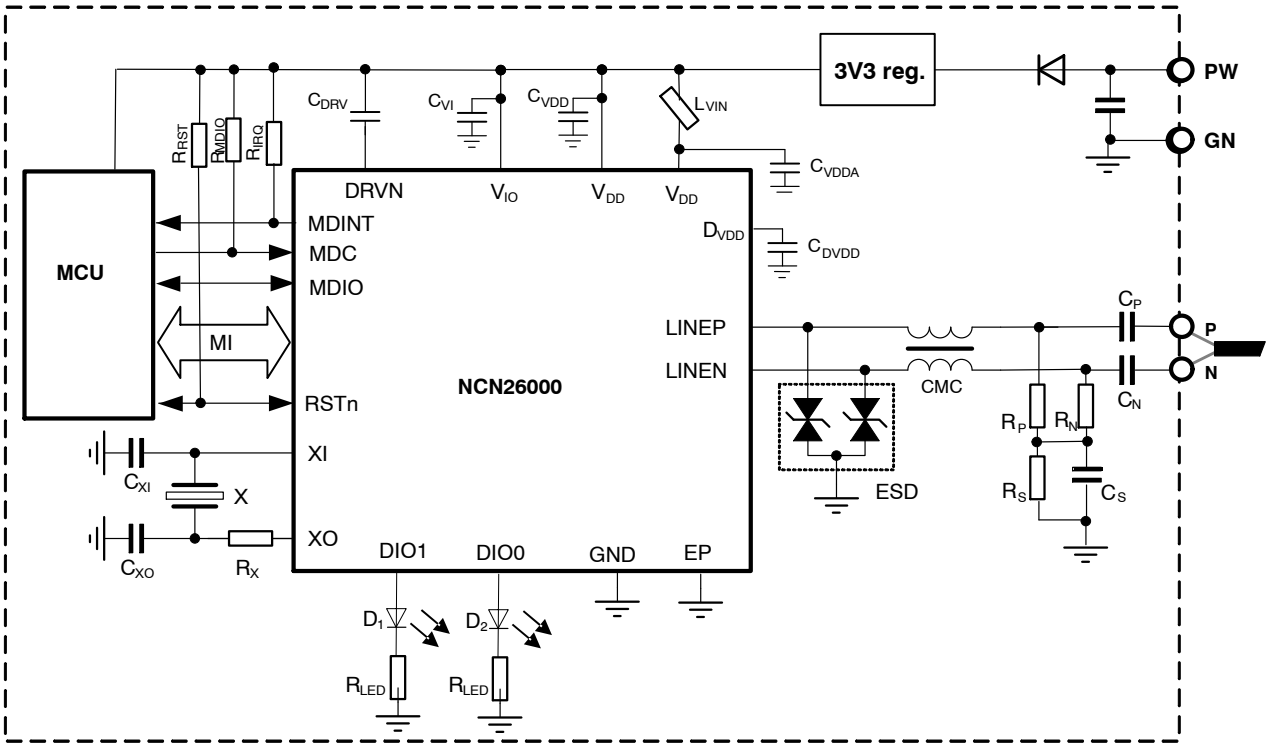


Figure 6. Application Diagram

Table 12. EXTERNAL COMPONENT VALUES

Component	Function	Value	Unit	Note
C_{VDD}, C_{VDDa}	Filtering capacitor, ceramic	2.2	μF	
C_{VIO}	Filtering capacitor, ceramic	100	nF	
C_{DRVN}	Filtering capacitor, ceramic	2.2	μF	
C_{DVDD}	Filtering capacitor, ceramic	2.2	μF	
L_{VIN}	Noise Suppression Chip Ferrite Bead	1	kΩ	At 100 MHz (Murata BLM18HG102SH1D)
R_{IRQ}, R_{RST} R_{MDIO}	Pull up resistor	10	kΩ	
X	Crystal (Murata XRCGB25M000F3A00R0)	25	MHz	100 ppm or better
R_{XS}	Series resistor	0	Ω	Depending on drive Level of the Crystal
C_{XI},C_{XO}	Load capacitors	12	pF	<10%

Table 12. EXTERNAL COMPONENT VALUES

Component	Function	Value	Unit	Note
CMC	Common mode choke (e.g. Murata DLW43MH201XK2L or TDK ACT1210E−241−2P−TL−000)	200	μH	
C_P,C_N	DC−blocking coupling capacitors	100	nF	<10%, 50 V
R_P, R_N	Terminating Resistors	49.9	Ω	<1%
C_S	Capacitor	4.7	nF	<10%, 50 V, optional
R_S	Resistor	100	kΩ	<10%, ≥0.1 W, optional
ESD	ESD protection	SZESD7205		optional
D1, D2	Low current LED 2 mA	If = 2 mA Vf = 1.9V Typ		Kingbright APT1608LCGCK
R_{LED}	Current limiting resistor for LED	680	Ω	

Clock Source

The NCN26000 requires a precise and robust 25 MHz clock source for correct operation.

The clock can either be fed from an external 25 MHz clock source or be generated using a quartz crystal connected to the XTAL Oscillator circuit of the NCN26000.

Crystal Oscillator

The oscillator circuit is designed to drive a 25 MHz parallel resonance AT cut quartz crystal. The external crystal is connected between the XI pin and the XO pins. XI is the input pin and XO is the output pin of the internal crystal oscillator circuit.

A typical crystal connection circuit is shown in Figure 7.

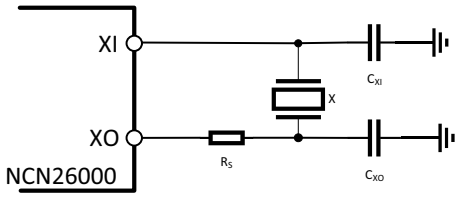


Figure 7. Crystal Connection Diagram

External Clock Source

In situations where a 25 MHz (±100 ppm) clock signal is already available in the system, the NCN26000 can be clocked using such a signal, removing the need of adding a crystal and load capacitors. In this case, the external clock signal shall be connected to the XI pin of the NCN26000, while the XO pin shall be left floating.

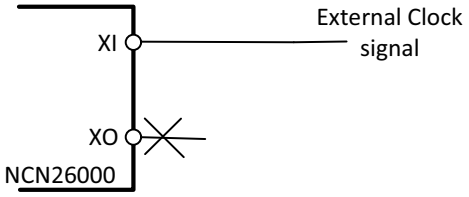


Figure 8. Connecting an External Clock Source

Clock Output

The NCN26000 also offers to provide a stable 25 MHz clock to other components (like MCUs) on the same PCB. Both, the DIO0 and DIO1 ping can be configured to output the 25 MHz clock signal. See DIO Configuration Register (Address 18) for details on how the configure the DIOx pins for clock output.

Device Configuration Examples

To configure the NCN26000, dedicated registers (see memory map) can be accessed using the Media Independent Management Interface (MIIM, also known as MDIO). Note that after any reset event, normal communication is inhibited. The following two examples briefly describe how to setup the NCN26000 for plain CSMA/CD or PLCA mode of operation.

Basic Configuration for Plain CSMA/CD Operation

To connect the NCN26000 device to a 10BASE−T1S multi−drop network in plain CSMA/CD mode of operation, a few MDIO accesses are needed.

1. Issue a device reset by setting bit 15 in the Control register (Address 0)
2. If NCN26000 was booted in ISOLATE mode, set bit 10 to 0 to have the device enter NORMAL mode.
3. Enable the link by setting bit 13 of the same register

Basic Configuration for PLCA Operation

To connect the NCN26000 device to a 10BASE−T1S multi−drop network in PLCA mode of operation, the following configuration is required:

1. Assign the node a unique PLCA ID in the range of 0 to 254, with 0 being the coordinator. This can be achieved by writing register PLCA Control 1 Register (MMD 31, Address 51714)
2. If the node is the coordinator, set the maximum number of allowed transmit opportunities. i.e., the maximum number of nodes allowed to share the media (Note 2). This can be achieved by writing register PLCA Control 1 Register (MMD 31, Address 51714)
3. Configure the TO_TIMER to the value chosen for the network (typically, 24 or 32) (Note 3). This can be achieved by writing register PLCA Transmit Opportunity Timer Register (MMD 31, Address 51716)
4. Configure any additional PLCA feature, if required (e.g., PLCA burst mode)
5. Enable PLCA by writing a one to bit 15 of the PLCA CONTROL 0 REGISTER (MMD 31, Address 51713).
6. If NCN26000 was booted in ISOLATE mode, set bit 10 to 0 in the PHY Control register (Address 0) to have the device enter NORMAL mode.
7. Enable the link by setting bit 13 of the same register

Table 13. DEVICE ORDERING INFORMATION

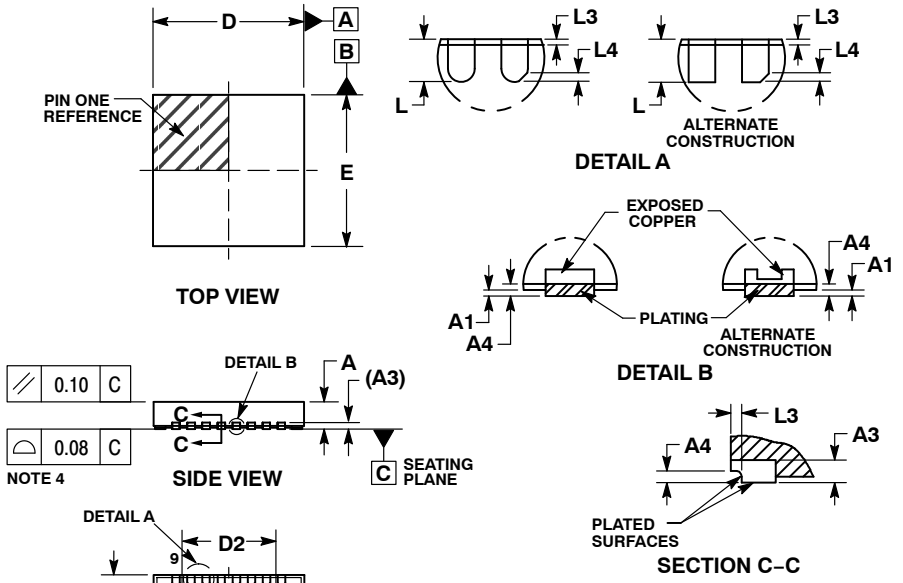
Device	Package Type	Shipping†
NCN26000XMNTXG	QFN 32, 5x5	4000 / Tape & Reel
NCN26000XMNTBG	QFN 32, 5x5	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

2. Typically, this should be set after the maximum assigned node ID plus one.
3. It is strongly recommended to always set the TO_TIMER value because different PHYs may have different default values depending on the version of the OPEN Alliance specifications they comply to.

PACKAGE DIMENSIONS

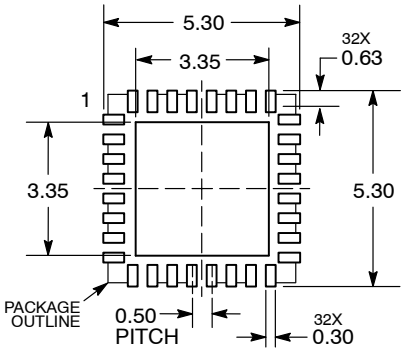
QFNW32 5x5, 0.5P
CASE 484AB
ISSUE D



NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	---	---	0.05
A3		0.20 REF	
A4	0.10	---	---
b	0.20	0.25	0.30
D	4.90	5.00	5.10
D2	3.00	3.10	3.20
E	4.90	5.00	5.10
E2	3.00	3.10	3.20
e		0.50 BSC	
K	0.35	---	---
L	0.30	0.40	0.50
L3	---	---	0.10
L4		0.08 REF	

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSION: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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