# NCP1217, NCP1217A

# PWM Controller, Fixed Frequency, Current Mode

Housed in an SO−8 or PDIP−7 package, the NCP1217 represents the enhanced version of the NCP1203−based controllers. Due to its high drive capability, NCP1217 drives large gate−charge MOSFETs, which together with internal ramp compensation and built−in overvoltage protection, ease the design of modern AC/DC adapters. NCP1217 offers a true alternative to UC384X−based designs.

With an internal structure operating at different fixed frequencies (65–100–133 kHz), the controller features a high−voltage startup FET, which ensures a clean and loss less startup sequence. Its current−mode control topology provides an excellent input audio−susceptibility and inherent pulse−by−pulse control. Internal ramp compensation easily prevents subharmonic oscillations from taking place in continuous conduction mode designs.

When the current setpoint falls below a given value, e.g. the output power demand diminishes, the IC automatically enters the so−called skip cycle mode and provides excellent efficiency at light loads. Because this occurs at a user adjustable low peak current, no acoustic noise takes place.

The NCP1217 features two efficient protective circuitries: 1) In presence of an overcurrent condition, the output pulses are disabled and the device enters a safe burst mode, trying to restart. Once the default has gone, the device auto−recovers. 2) If an external signal (e.g. a temperature sensor) pulls Pin 1 above 3.2 V, output pulses are immediately stopped and the NCP1217 stays latched in this position. Reset occurs when the $V_{CC}$ collapses to ground, e.g. the user unplugs the power supply.

### Features

- Current−Mode with Adjustable Skip−Cycle Capability
- Built−in Internal Ramp Compensation
- Auto−Recovery Internal Output Short−Circuit Protection
- Internal 1.0 ms Soft−Start (NCP1217A Only)
- Limited Duty−Cycle to 50% (NCP1217A Only)
- Full Latchoff if Adjustment Pin is Brought High
- Extremely Low No−Load Standby Power
- Internal Temperature Shutdown
- 500 mA Peak Current Capability
- Fixed Frequency Versions at 65 kHz, 100 kHz and 133 kHz
- Direct Optocoupler Connection
- Internal Leading Edge Blanking
- SPICE Models Available for TRANsient and AC Analysis
- These are Pb−Free Devices

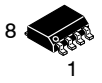
### Typical Applications

- High Power AC/DC Converters for TVs, Set−Top Boxes, etc.
- Offline Adapters for Notebooks
- Telecom DC−DC Converters
- All Power Supplies

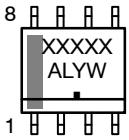
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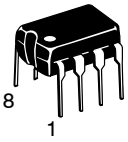
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### MARKING DIAGRAMS

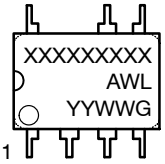



**SOIC−8**
**D SUFFIX**
**CASE 751**




**PDIP−7**
**P SUFFIX**
**CASE 626B**

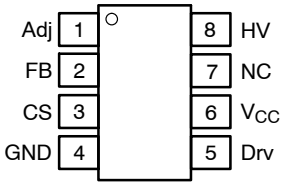



| | | |
|---|---|---|
| XXXXXX | = | Specific Device Code |
| A | = | Assembly Location |
| L, WL | = | Wafer Lot |
| Y, YY | = | Year |
| W, WW | = | Work Week |
| ▪ or G | = | Pb−Free Package |

### DEVICE MARKING INFORMATION

See detailed device marking information in the ordering information section on page 17 of this data sheet.

### PIN CONNECTIONS




(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 17 of this data sheet.

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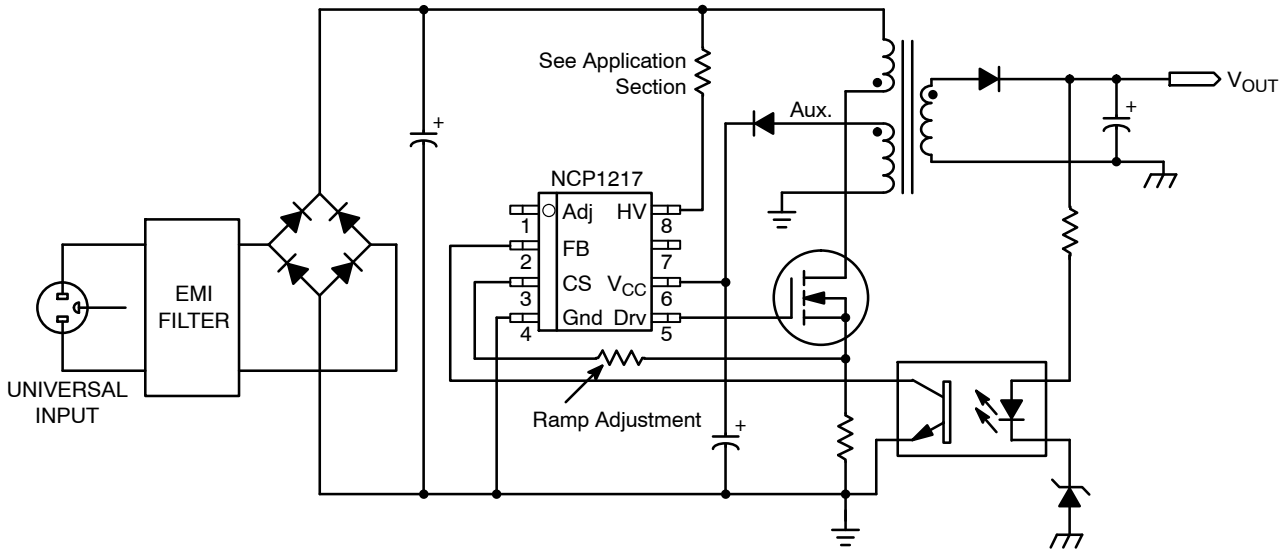
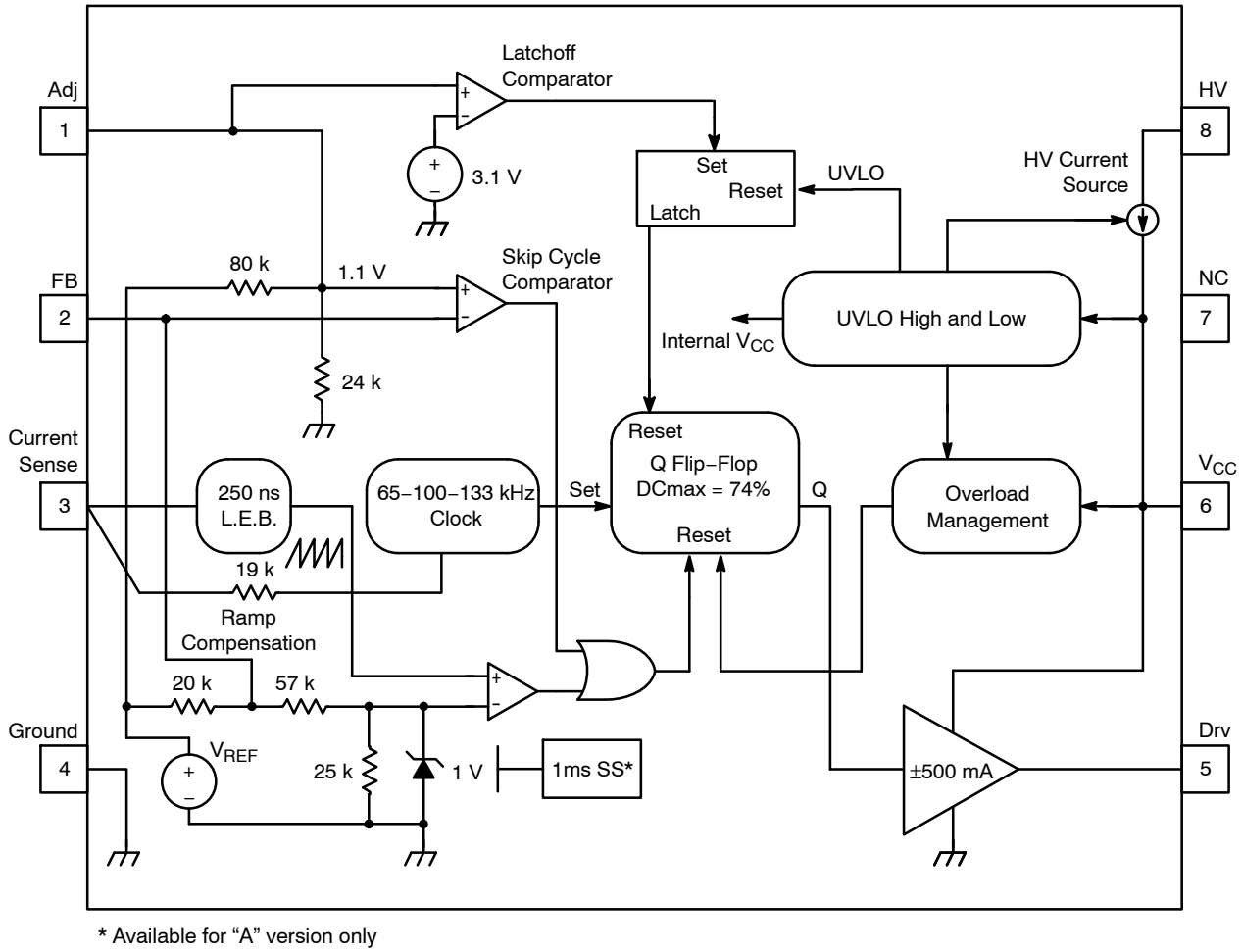



**Figure 1. Typical Application Example**

## PIN FUNCTION DESCRIPTION

| Pin No. | Pin Name | Function | Description |
|---|---|---|---|
| 1 | Adj | Adjust the skipping peak current | This pin lets you adjust the level at which the cycle skipping process takes place. Shorting this pin to ground permanently disables the skip cycle feature.<br>By bringing this pin above 3.1 V, you permanently shut off the device. |
| 2 | FB | Sets the peak current setpoint | By connecting an optocoupler to this pin, the peak current setpoint is adjusted accordingly to the output power demand. |
| 3 | CS | Current sense input | This pin senses the primary current and routes it to the internal comparator via an L.E.B. By inserting a resistor in series with the pin, you control the amount of ramp compensation you need. |
| 4 | GND | The IC ground | – |
| 5 | Drv | Driving pulses | The driver's output to an external MOSFET. |
| 6 | $V_{CC}$ | Supplies the IC | This pin is connected to an external bulk capacitor of typically 22 μF. |
| 7 | NC | – | This unconnected pin ensures adequate creepage distance. |
| 8 | HV | Ensures a clean and lossless startup sequence | Connected to the high−voltage rail, this pin injects a constant current into the $V_{CC}$ capacitor during the startup sequence. |




* Available for “A” version only

**Figure 2. Internal Circuit Architecture**

## MAXIMUM RATINGS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Power Supply Voltage | $V_{CC}$ | 16 | V |
| Power Supply Voltage on All Other Pins Except Pin 8 (HV), Pin 6 ($V_{CC}$) and Pin 5 (Drv) | – | −0.3 to 10 | V |
| Maximum Voltage on Pin 8 (HV), Pin 6 ($V_{CC}$) Decoupled to Ground with 10 μF | $V_{HV}$ | 500 | V |
| Maximum Voltage on Pin 8 (HV), Pin 6 ($V_{CC}$) Grounded | $V_{HV}$ | 450 | V |
| Minimum Operating Voltage on Pin 8 (HV) | | 28 | V |
| Maximum Current into All Pins Except $V_{CC}$ (6) and HV (8) when 10 V ESD Diodes are Activated | – | 5.0 | mA |
| Thermal Resistance, Junction−to−Case | $R_{\theta JC}$ | 57 | °C/W |
| Thermal Resistance, Junction−to−Air, PDIP−7 Version<br>Thermal Resistance, Junction−to−Air, SO−8 Version | $R_{\theta JA}$<br>$R_{\theta JA}$ | 100<br>178 | °C/W |
| Maximum Junction Temperature | $T_{JMAX}$ | 150 | °C |
| Temperature Shutdown | – | 155 | °C |
| Hysteresis in Shutdown | – | 30 | °C |
| Storage Temperature Range | – | −60 to +150 | °C |
| ESD Capability, HBM Model (All Pins Except $V_{CC}$ and HV) | – | 2.0 | kV |
| ESD Capability, Machine Model | – | 200 | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection rated using the following tests:
   Human Body Model (HBM) 2000 V per JEDEC Standard JESD22, Method A114E.
   Machine Model (MM) 200 V per JEDEC Standard JESD22, Method A115A.

**ELECTRICAL CHARACTERISTICS** (For typical values $T_J$ = 25°C, for min/max values $T_J$ = 0°C to +125°C, Max $T_J$ = 150°C, $V_{CC}$ = 11 V unless otherwise noted.)

| Characteristic | Pin | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY SECTION** (All frequency versions, unless otherwise noted) | | | | | | |
| Turn−On Threshold Level, $V_{CC}$ Going Up | 6 | $VCC_{ON}$ | 11.8 | 12.8 | 13.8 | V |
| Minimum Operating Voltage After Turn−On | 6 | $VCC_{min}$ | 6.9 | 7.6 | 8.3 | V |
| $V_{CC}$ Decreasing Level at which the Latchoff Phase Ends | 6 | $VCC_{latch}$ | – | 5.6 | – | V |
| Internal IC Consumption, No Output Load on Pin 5, $F_{SW}$ = 65 kHz | 6 | ICC1 | – | 960 | 1110 (Note 1) | μA |
| Internal IC Consumption, No Output Load on Pin 5, $F_{SW}$ = 100 kHz | 6 | ICC1 | – | 1020 | 1180 (Note 1) | μA |
| Internal IC Consumption, No Output Load on Pin 5, $F_{SW}$ = 133 kHz | 6 | ICC1 | – | 1060 | 1200 (Note 1) | μA |
| Internal IC Consumption, 1.0 nF Output Load on Pin 5, $F_{SW}$ = 65 kHz | 6 | ICC2 | – | 1.7 | 2.0 (Note 1) | mA |
| Internal IC Consumption, 1.0 nF Output Load on Pin 5, $F_{SW}$ = 100 kHz | 6 | ICC2 | – | 2.1 | 2.4 (Note 1) | mA |
| Internal IC Consumption, 1.0 nF Output Load on Pin 5, $F_{SW}$ = 133 kHz | 6 | ICC2 | – | 2.4 | 2.9 (Note 1) | mA |
| Internal IC Consumption, Latchoff Phase, $V_{CC}$ = 6.0 V | 6 | ICC3 | – | 230 | – | μA |
| **INTERNAL STARTUP CURRENT SOURCE** ($T_J$ > 0°C) | | | | | | |
| High−Voltage Current Source, $V_{CC}$ = 10 V | 8 | IC1 | 3.5 (Note 2) | 6.0 | 7.8 | mA |
| High−Voltage Current Source, $V_{CC}$ = 0 | 8 | IC2 | – | 7.0 | – | mA |
| **DRIVE OUTPUT** | | | | | | |
| Output Voltage Rise−Time @ CL = 1.0 nF, 10−90% of a 12 V Output Signal | 5 | $T_r$ | – | 60 | – | ns |
| Output Voltage Fall−Time @ CL = 1.0 nF, 10−90% of a 12 V Output Signal | 5 | $T_f$ | – | 20 | – | ns |
| Source Resistance | 5 | $R_{OH}$ | 15 | 20 | 35 | Ω |
| Sink Resistance | 5 | $R_{OL}$ | 5.0 | 10 | 18 | Ω |
| **CURRENT COMPARATOR** (Pin 5 Unloaded) | | | | | | |
| Input Bias Current @ 1.0 V Input Level on Pin 3 | 3 | $I_{IB}$ | – | 0.02 | – | μA |
| Maximum Internal Current Setpoint | 3 | $I_{Limit}$ | 0.9 | 1.0 | 1.1 | V |
| Default Internal Current Setpoint for Skip Cycle Operation | 3 | $I_{Lskip}$ | – | 330 | – | mV |
| Propagation Delay from Current Detection to Gate OFF State | 3 | $T_{DEL}$ | – | 90 | 150 | ns |
| Leading Edge Blanking Duration | 3 | $T_{LEB}$ | – | 250 | – | ns |
| **INTERNAL OSCILLATOR** ($V_{CC}$ = 11 V, Pin 5 Loaded by 1.0 kΩ) | | | | | | |
| Oscillation Frequency, 65 kHz Version | – | $f_{OSC}$ | 58.5 | 65 | 71.5 | kHz |
| Oscillation Frequency, 100 kHz Version | – | $f_{OSC}$ | 90 | 100 | 110 | kHz |
| Oscillation Frequency, 133 kHz Version | – | $f_{OSC}$ | 120 | 133 | 146 | kHz |
| Maximum Duty−Cycle, NCP1217 | – | Dmax | 69 | 74 | 80 | % |
| Maximum Duty−Cycle, NCP1217A | – | Dmax | 42 | 46.5 | 50 | % |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Maximum Value @ $T_J$ = 0°C.
2. Minimum Value @ $T_J$ = 125°C.

**ELECTRICAL CHARACTERISTICS** (continued) (For typical values $T_J$ = 25°C, for min/max values $T_J$ = 0°C to +125°C, Max $T_J$ = 150°C, $V_{CC}$ = 11 V unless otherwise noted.)

| Characteristic | Pin | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **FEEDBACK SECTION** ($V_{CC}$ = 11 V, Pin 5 Loaded by 1.0 kΩ) | | | | | | |
| Internal Pull−Up Resistor | 2 | Rup | – | 19 | – | kΩ |
| Pin 2 (FB) to Internal Current Setpoint Division Ratio | – | Iratio | – | 3.3 | – | – |
| **SKIP CYCLE GENERATION** | | | | | | |
| Default Skip Mode Level | 1 | Vskip | 0.93 | 1.1 | 1.26 | V |
| Pin 1 Internal Output Impedance | 1 | Zout | – | 27 | – | kΩ |
| **INTERNAL RAMP COMPENSATION** | | | | | | |
| Internal Ramp Level @ 25°C (Note 3) | 3 | Vramp | 2.6 | 2.9 | 3.2 | V |
| Internal Ramp Resistance to CS Pin | 3 | Rramp | – | 19 | – | kΩ |
| **ADJUSTMENT LATCHOFF LEVEL** | | | | | | |
| Latching Level | 1 | Vlatch | 2.69 | 3.10 | 3.42 | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. A 1.0 MΩ resistor is connected to the ground for the measurement.

## TYPICAL CHARACTERISTICS

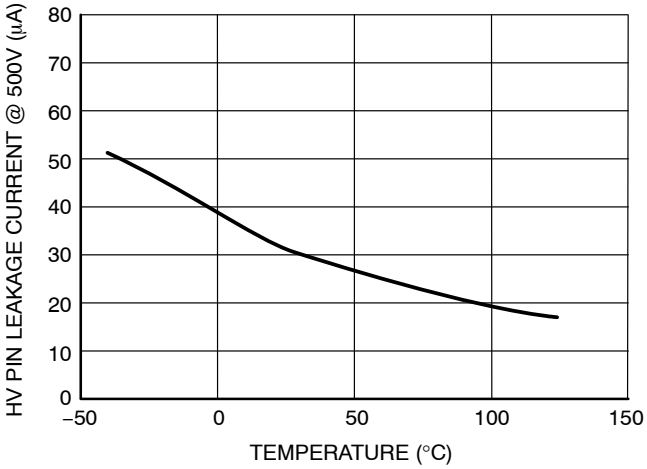



**Figure 3. High Voltage Pin Leakage Current vs. Temperature**

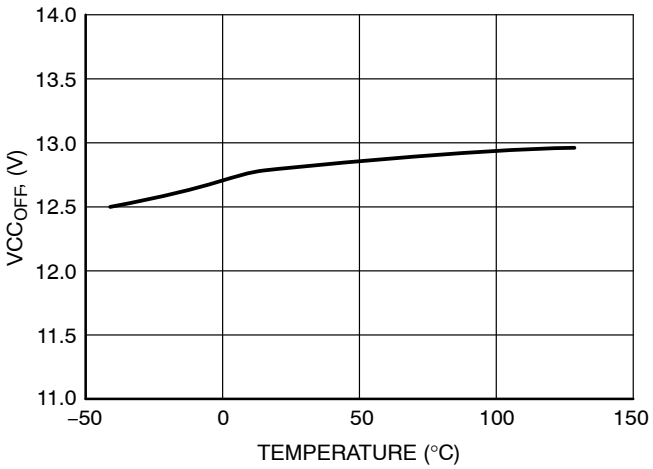



**Figure 4. $VCC_{OFF}$ vs. Temperature**

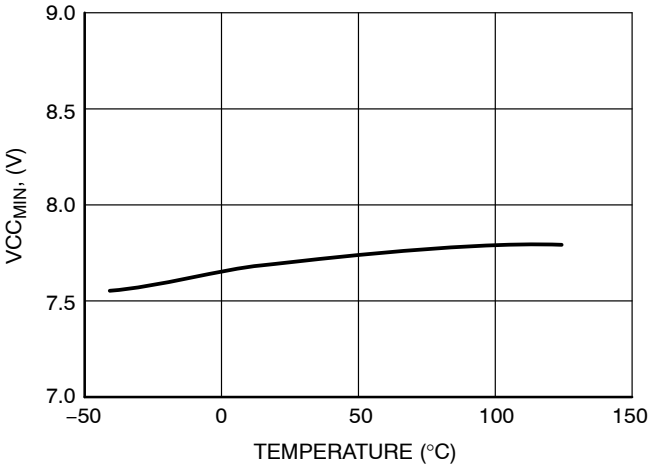



**Figure 5. $VCC_{MIN}$ vs. Temperature**

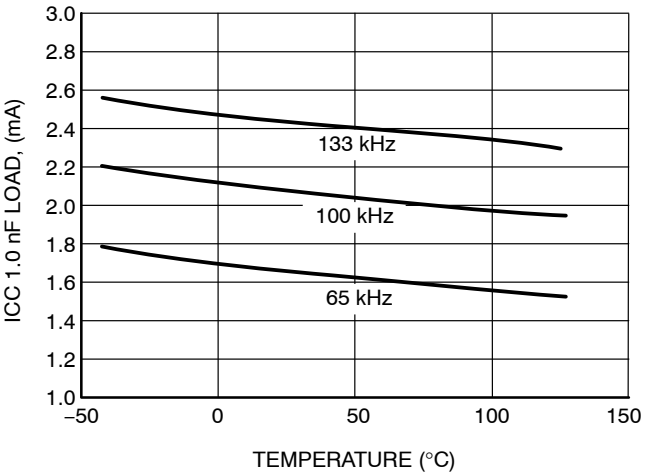



**Figure 6. ICC 1.0 nF Load vs. Temperature**

## TYPICAL CHARACTERISTICS (continued)

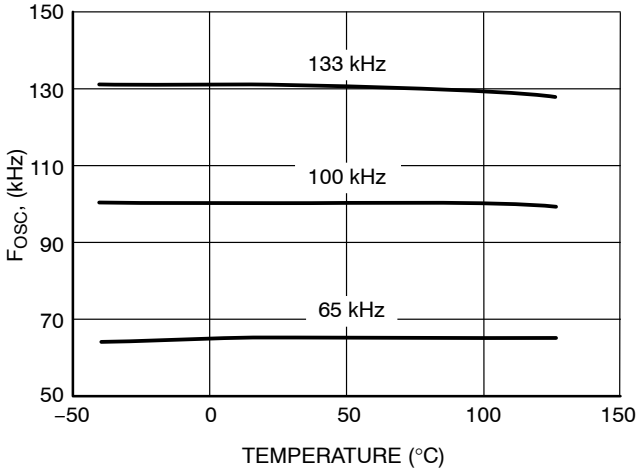



**Figure 7. Switching Frequency vs. Temperature**

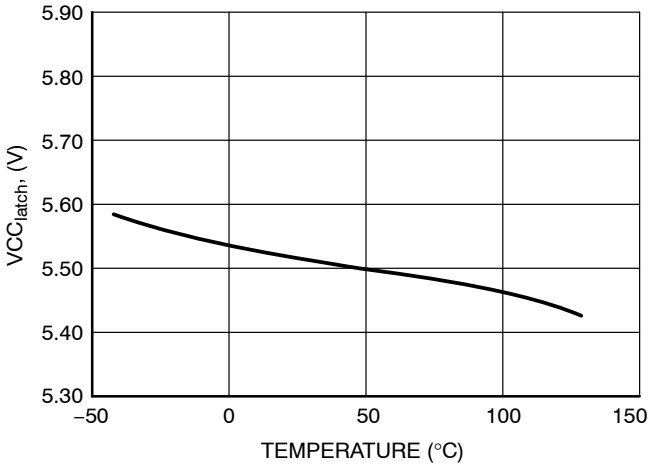



**Figure 8. $VCC_{latch}$ vs. Temperature**

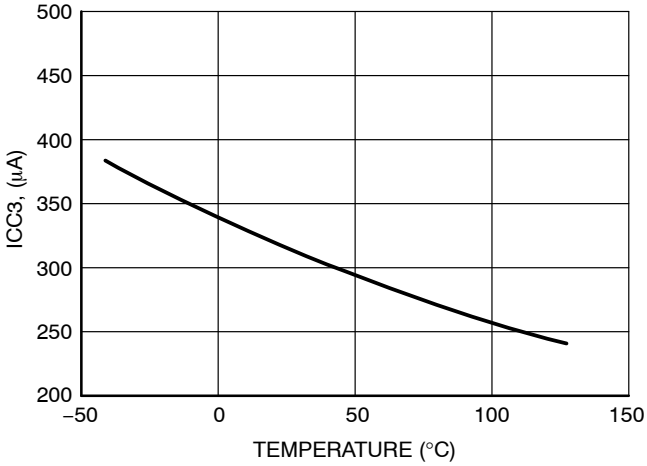



**Figure 9. ICC3 vs. Temperature**

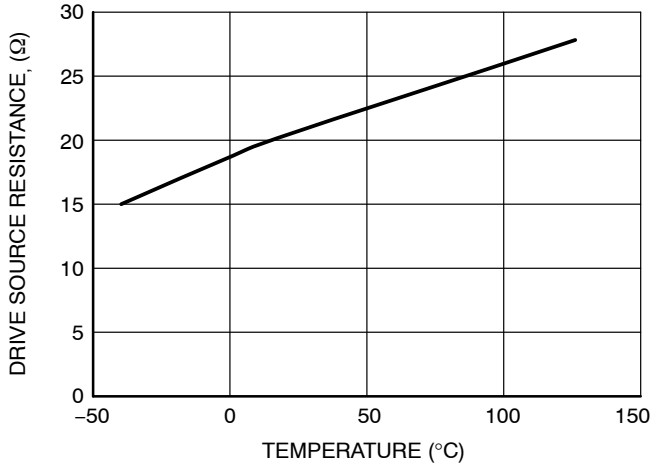



**Figure 10. Drive Source Resistance vs. Temperature**

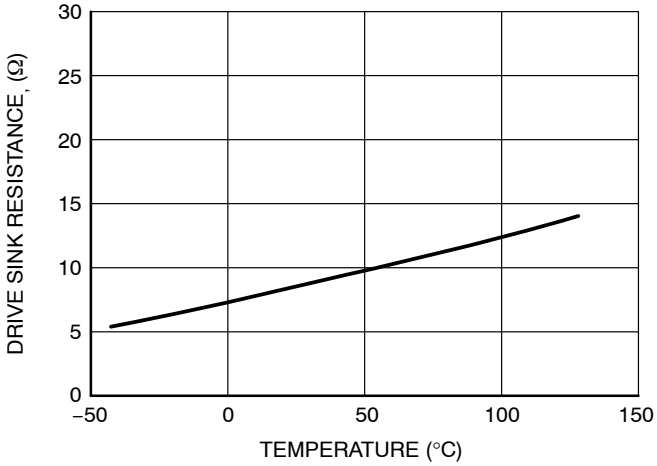



**Figure 11. Drive Sink Resistance vs. Temperature**

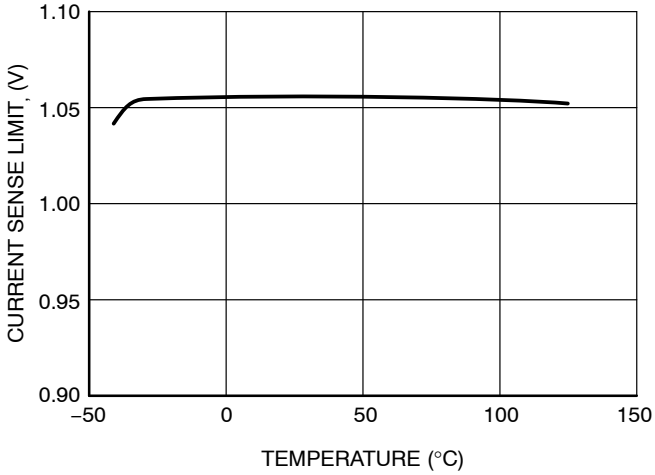



**Figure 12. Current Sense Limit vs. Temperature**

## TYPICAL CHARACTERISTICS (continued)

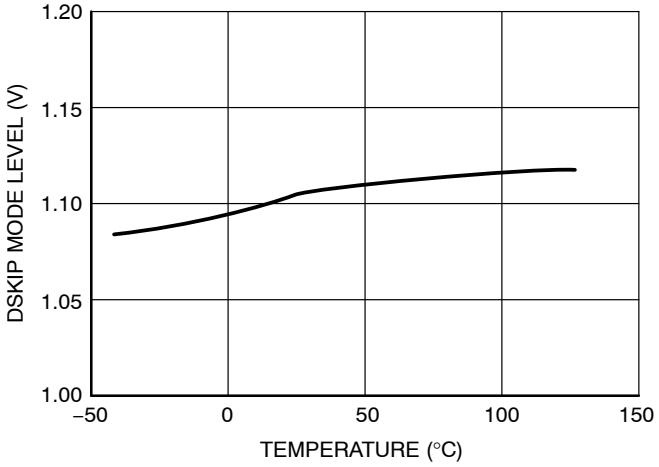



**Figure 13. Skip Mode Level vs. Temperature**

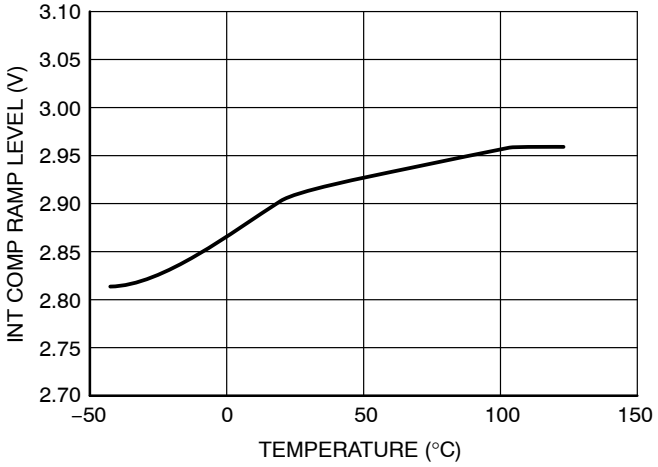



**Figure 14. Int Comp Ramp Max Level vs. Temperature**

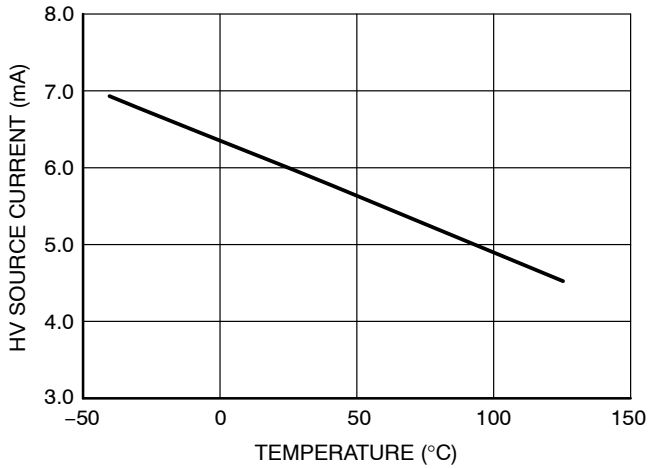



**Figure 15. High Voltage Current Source (@ $V_{CC}$ = 10V) vs. Temperature**

## APPLICATION INFORMATION

### Introduction

The NCP1217 implements a standard current mode architecture where the switch−off event is dictated by the peak current setpoint. This component represents the ideal candidate where low part−count is the key parameter, particularly in low−cost AC/DC adapters, TV power supplies, etc. Due to its high−performance High−Voltage technology, the NCP1217 incorporates all the necessary components normally needed in UC384X based supplies: timing components, feedback devices, low−pass filter and startup device but also enhances the original component by offering: 1) an externally triggerable latchoff 2) ramp compensation and finally, 3) short−circuit protection. Due to its high−voltage current source, ON Semiconductor's NCP1217 does not need an external startup resistance but supplies the startup current directly from the high−voltage rail. On the other hand, more and more applications are requiring low no−load standby power, e.g. for AC/DC adapters, VCRs, etc. UC384X series have a lot of difficulty to reduce the switching losses at low power levels. NCP1217 elegantly solves this problem by skipping unwanted switching cycles at a user−adjustable power level. By ensuring that skip cycles take place at low peak current, the device ensures quiet, noise−free operation:

**Current−Mode Operation:** As the UC384X series, the NCP1217 features a well−known current mode control architecture which provides superior input audio−susceptibility compared to traditional voltage−mode controllers. Primary current pulse−by−pulse checking together with a fast over current comparator offers greater security in the event of a difficult fault condition, e.g. a saturating transformer.

**Ramp Compensation:** By inserting a resistor between the current−sense (CS) pin and the actual sense resistor, it becomes possible to inject a given amount of ramp compensation since the internal saw tooth clock is routed to the CS pin. Subharmonic oscillations in Continuous Conduction Mode (CCM) can thus be compensated via a single resistor.

**Adjustable Skip Cycle Level:** By offering the ability to tailor the level at which the skip cycle takes place, the designer can make sure that the skip operation only occurs at low peak current. This point guarantees a noise−free operation with cheap transformers. Skip cycle offers a proven mean to reduce the standby power in no or light loads situations.

**Wide Switching−Frequency Offer:** Three different options are available: 65 kHz – 100 kHz–133 kHz. Depending on the application, the designer can pick up the right device to help reducing magnetics or improve the EMI signature before reaching the 150 kHz starting point.

**Overcurrent Protection (OCP):** By continuously monitoring the $V_{CC}$ auxiliary winding voltage, NCP1217 enters burst mode as soon as the power supply undergoes an overload: when the $V_{CC}$ voltage goes down until it crosses the undervoltage lockout level ($VCC_{min}$). When the NCP1217 reaches this level (typically 7.6 V), it stops the switching pulses until the $V_{CC}$ pin voltage reaches $VCC_{latch}$ (5.6 V). At $VCC_{latch}$, the NCP1217 attempts to restart. As soon as the default disappears, the power supply resumes operation.

**Overvoltage Protection (OVP):** If pin1 is brought to a level higher than the internal 3.2 V reference voltage, the controller is permanently shut down until the user cycles the VCC OFF and ON again. This allows the building of efficient and low−cost over voltage protection circuits.

**Wide Duty−Cycle Operation:** Wide mains operation requires a large duty−cycle excursion. The NCP1217 can go up to 74% typically.

**Low Standby−Power:** If SMPS naturally exhibit a good efficiency at nominal load, they begin to be less efficient when the output power demand diminishes. By skipping unneeded switching cycles, the NCP1217 drastically reduces the power wasted during light load conditions. In no−load conditions, the NPC1217 allows the total standby power to easily reach next International Energy Agency (IEA) recommendations.

**No Acoustic Noise While Operating:** Instead of skipping cycles at high peak currents, the NCP1217 waits until the peak current demand falls below a user−adjustable 1/3 of the maximum limit. As a result, cycle skipping can take place without having a singing transformer … You can thus select cheap magnetic components free of noise problems.

**External MOSFET Connection:** By leaving the external MOSFET external to the IC, you can select avalanche proof devices, which in certain cases (e.g. low output powers), let you work without an active clamping network. Also, by controlling the MOSFET gate signal flow, you have an option to slow down the device commutation, therefore reducing the amount of ElectroMagnetic Interference (EMI).

**SPICE Model:** A dedicated model to run transient cycle−by−cycle simulations is available but also an averaged version to help you closing the loop. Ready−to−use templates can be downloaded in OrCAD's Pspice and INTUSOFT's IsSpice from ON Semiconductor web site, NCP1217 related section.

### Startup Sequence

When the power supply is first powered from the mains outlet, the internal current source (typically 7.0 mA) is biased and charges up the $V_{CC}$ capacitor. When the voltage on this $V_{CC}$ capacitor reaches the $VCC_{ON}$ level (typically 12.8 V), the current source turns off and no longer wastes any power. At this time, the $V_{CC}$ capacitor only supplies the controller and the auxiliary supply is supposed to take over before $V_{CC}$ collapses below $VCC_{min}$. Figure 16 shows the internal arrangement of this structure.

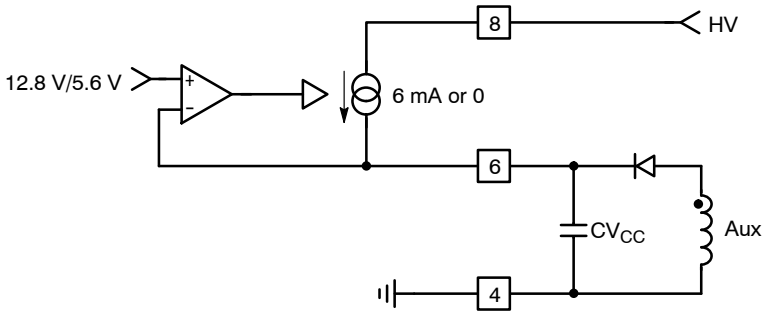



**Figure 16. The Current Source Brings $V_{CC}$ Above 12.8 V and then Turns Off**

Once the power supply has started, the $V_{CC}$ shall be constrained below 16 V, which is the maximum rating on Pin 6. Figure 17 portrays a typical startup sequence with a $V_{CC}$ regulated at 12.5 V.

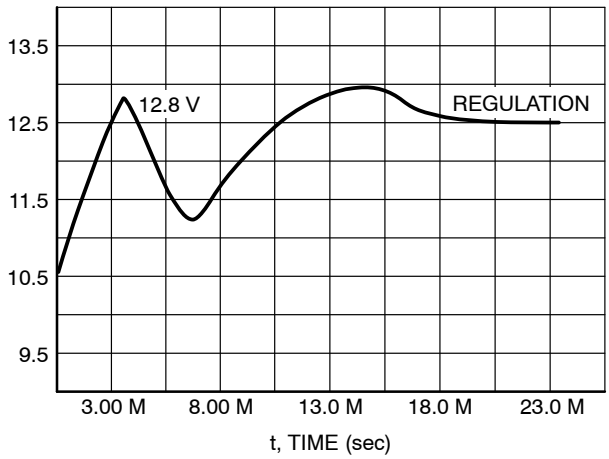



**Figure 17. A Typical Startup Sequence for the NCP1217**

### Overload Operation

In applications where the output current is purposely not controlled (e.g. wall adapters delivering raw DC level), it is interesting to implement a true short−circuit protection. A short−circuit actually forces the output voltage to be at a low level, preventing a bias current to circulate in the optocoupler LED. As a result, the auxiliary voltage also decreases because it also operates in Flyback and thus duplicates the output voltage, providing the leakage inductance between windings is kept low. To account for this situation and properly protect the power supply, NCP1217 hosts a dedicated overload detection circuitry. Once activated, this circuitry imposes to deliver pulses in a burst manner with a low duty−cycle. The system auto−recovers when the fault condition disappears.

During the startup phase, the peak current is pushed to the maximum until the output voltage reaches its target and the feedback loop takes over. The auxiliary voltage takes place after a few switching cycles and self−supplies the IC. In presence of a short circuit on the output, the auxiliary voltage will go down until it crosses the undervoltage lockout level of typically 7.6 V. When this happens, NCP1217 immediately stops the switching pulses and unbiases all unnecessary logical blocks. The overall consumption drops, while keeping the gate grounded, and the $V_{CC}$ slowly falls down. As soon as $V_{CC}$ reaches typically 5.6 V, the startup source turns−on again and a new startup sequence occurs, bringing $V_{CC}$ toward 12.8 V as an attempt to restart. If the default has gone, then the power supply normally restarts. If not, a new protective burst is initiated, shielding the SMPS from any runaway. Figure 18 portrays the typical operating signals in short circuit.

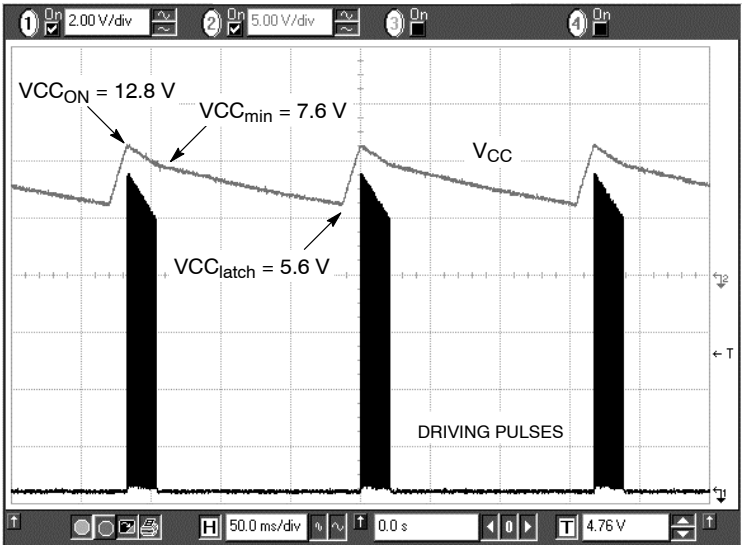



**Figure 18. Typical Waveforms in Short Circuit Conditions**

### Calculating the $V_{CC}$ Capacitor

The $V_{CC}$ capacitor can be calculated knowing the IC consumption as soon as $V_{CC}$ reaches 12.8 V. Suppose that a NCP1217P065 is used and drives a MOSFET with a 30 nC total gate charge (Qg). The total average current is thus made of ICC1 (750 μA) plus the driver current, $Fsw * Qg = 1.95$ mA. The total current is therefore 2.7 mA. The ΔV available to fully startup the circuit (e.g. never reach the 8.2 V $VCC_{min}$ during power on) is $13.7–8.2 = 5.5$ V best case or 4.9 V worse case (11.9–7.0). We have a capacitor that then needs to supply the NCP1217 with 2.7 mA during a given time until the auxiliary supply takes over. Suppose that this time was measured at around 15 ms. $CV_{CC}$ is calculated using the equation $C = \frac{\Delta t \cdot i}{\Delta V}$ or $C \geq 8.3$ μF. Select a 22 μF/25 V and this will fit.

### Skipping Cycle Mode

The NCP1217 automatically skips switching cycles when the output power demand drops below a given level. This is accomplished by monitoring the FB pin. In normal operation, pin 2 imposes a peak current accordingly to the load value. If the load demand decreases, the internal loop asks for less peak current. When this setpoint reaches a determined level (Vpin 1), the IC prevents the current from decreasing further down and starts to blank the output pulses: the IC enters the so−called skip cycle mode, also named controlled burst operation. The power transfer now depends upon the width of the pulse bunches (Figure 20). Suppose we have the following component values:

Lp, primary inductance = 350 μH
Fsw, switching frequency = 65 kHz
Ip skip = 600 mA (or 333 mV/Rsense)

The theoretical power transfer is therefore: $\frac{1}{2} \cdot Lp \cdot Ip^2 \cdot Fsw = 4.1$ W. If this IC enters skip cycle mode with a bunch length of 10 ms over a recurrent period of 100 ms, then the total power transfer is: $4.1 * 0.1 = 410$ mW.

To better understand how this skip cycle mode takes place, a look at the operation mode versus the FB level immediately gives the necessary insight.

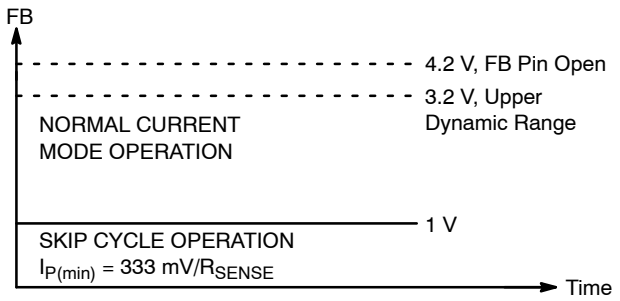



**Figure 19.**

When FB is above the skip cycle threshold (1.0 V by default), the peak current cannot exceed 1.0 V/Rsense. When the IC enters the skip cycle mode, the peak current cannot go below Vpin1/3.3. The user still has the flexibility to alter this 1.0 V by either shunting pin 1 to ground through a resistor or raising it through a resistor up to the desired level. In this later case, care must be taken to keep sufficient margin between this pin 1 adjustment level and the latchoff level. Grounding pin 1 permanently invalidates the skip cycle operation.

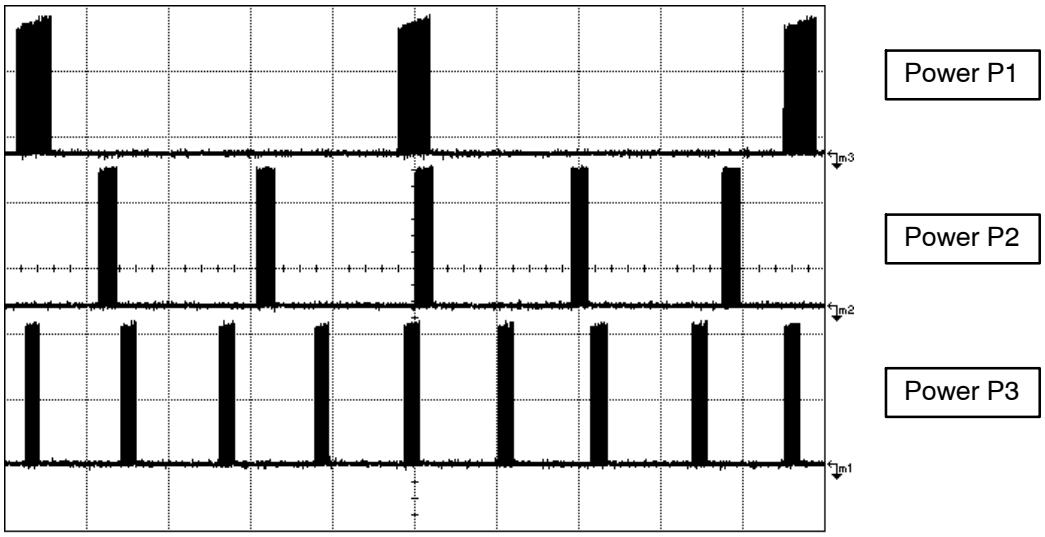



**Figure 20. Output Pulses at Various Power Levels (X = 5.0 μs/div) P1 < P2 < P3**

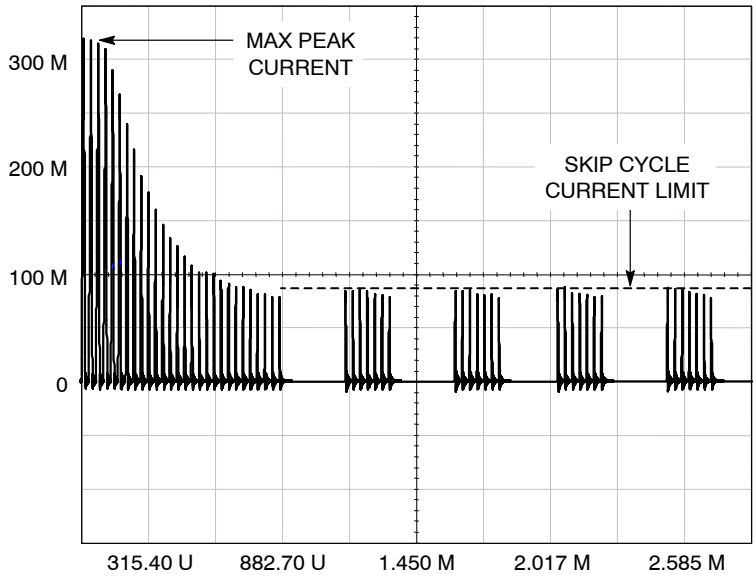



**Figure 21. The Skip Cycle Takes Place at Low Peak Currents which Guarantees Noise−Free Operation**

Sufficient margin shall be kept between normal Pin1 level and the latchoff point in order to avoid false triggering.

### Ramp Compensation

Ramp compensation is a known mean to cure subharmonic oscillations. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty−cycle greater than 50%. To lower the current loop gain, one usually injects between 50 and 100% of the inductor down−slope. Figure 22 depicts how internally the ramp is generated.

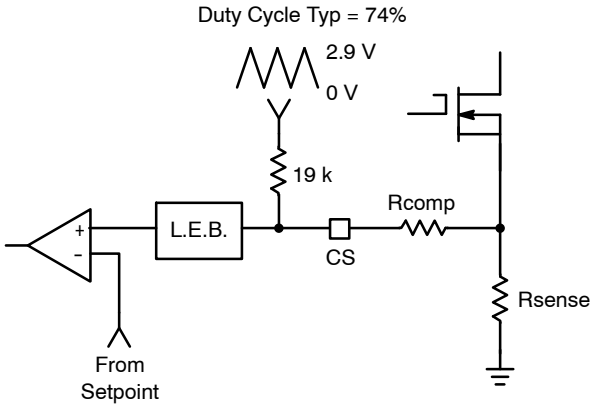



**Figure 22. Inserting a Resistor in Series with the Current Sense Information Brings Ramp Compensation**

In the NCP1217, the ramp features a swing of 2.9 V with a duty cycle max at 74%. Over a 65 kHz frequency, for instance, it corresponds to a 254 mV/µs ramp. In our FLYBACK design, let's suppose that our primary inductance Lp is 350 µH, delivering 12 V with a Np:Ns ratio of 1:0.1. The OFF time primary current slope is thus given by: $\frac{(Vout + Vf) \cdot \frac{Np}{Ns}}{Lp} = 371\ mA/\mu s$ or $37\ mV/\mu s$ when projected over an Rsense of 0.1 Ω, for instance. If we select 75% of the downslope as the required amount of ramp compensation, then we shall inject 27 mV/µs. Our internal compensation being of 254 mV/µs, the divider ratio (*divratio*) between Rcomp and the 19 kΩ is 0.106. A few lines of algebra to determine Rcomp: $\frac{19\ k \cdot divratio}{(1-divratio)} = 2.26\ k\Omega$.

**Latching Off the NCP1217**

Total latched shutdown can easily be implemented through a simple PNP bipolar transistor as depicted by Figure 23. When OFF, Q1 is transparent to the operation. When forward biased, the transistor pulls the Adj pin toward $V_{CC}$ and permanently latches−off the IC as soon Vadj goes above the latching level (typical 3.1 V). Figure 23 shows how to wire the bipolar transistor to activate the latchoff. A typical candidate for Q1 could be an MMBT3906 from ON Semiconductor.

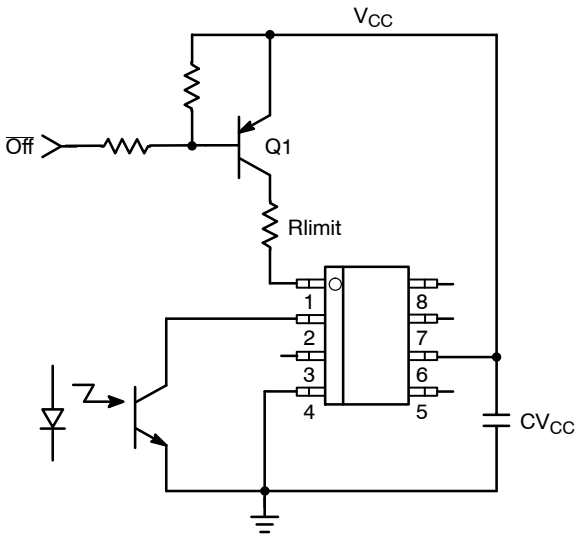



**Figure 23. A Simple Bipolar Transistor Totally Disables the IC**

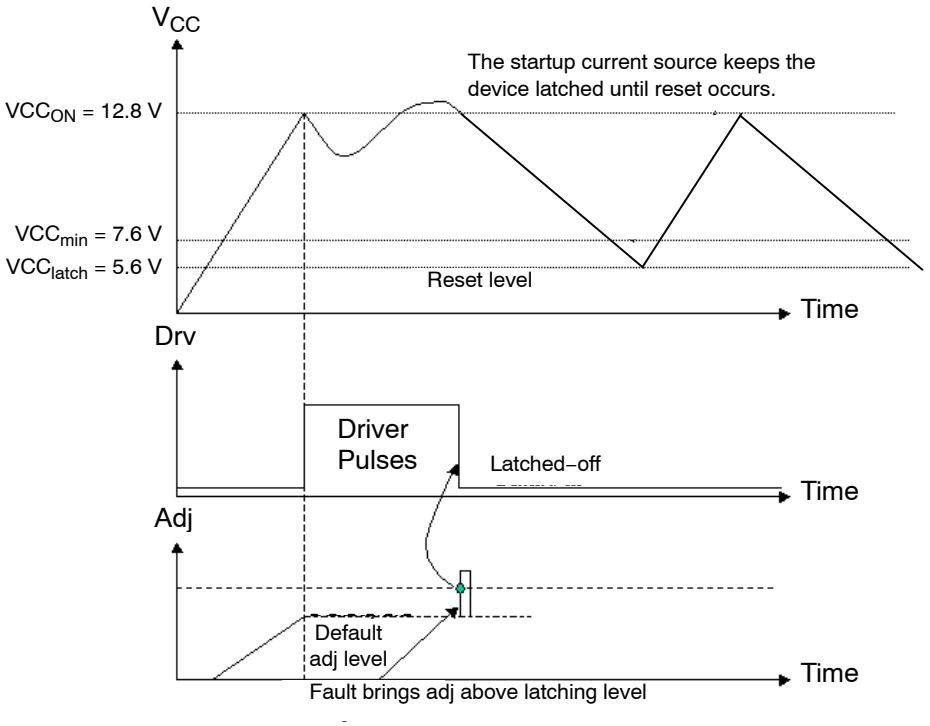



**Figure 24. When Vadj is Pulled Above 3.1 V, NCP1217 Permanently Latches−Off the Output Pulses**

In normal operation, the Adj pin level is kept at a fixed level, the default one or lower. As soon as some external signal pulls this Adj pin level above 3.1 V typical, the output pulses are permanently disabled. Care must be taken to limit the injected current into pin 1 to less than 2.0 mA, e.g. through a series resistor of 5.6 k with a 10 V $V_{CC}$. The startup switch is activated every time $V_{CC}$ reaches 5.6 V and maintains a $V_{CC}$ voltage ramping up and down between 5.6 V and 12.8 V. Reset occurs when $V_{CC}$ falls below 5.6 V, e.g. when the user cycle the SMPS down. Figure 25 illustrates the operation. Adding a zener diode from Q1 base to ground makes a cheap OVP, protecting the supply from any lethal open−loop operation. If a thermistor (NTC) is added in parallel with the Zener−diode, overtemperature protection is also ensured.

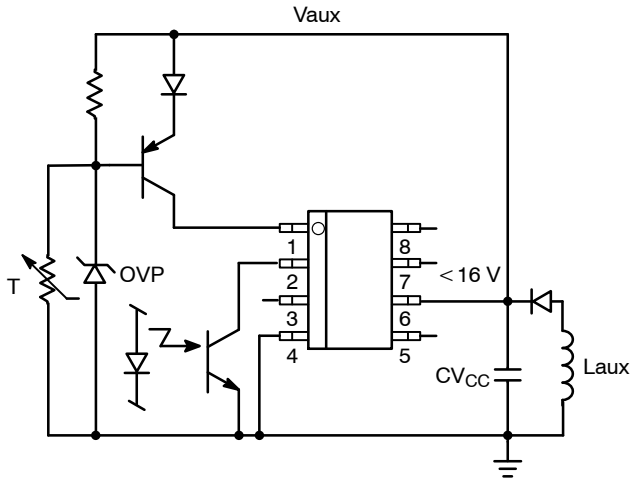



**Figure 25. A Thermistor and a Zener Diode Offer Both OVP and Overtemperature Latched−Off Protection**

### Nonlatching Shutdown

In some cases, it might be desirable to shut off the part temporarily and authorize its restart once the default has disappeared. This option can easily be accomplished through a single NPN bipolar transistor wired between FB and ground. By pulling FB below the Adj Pin 1 level, the output pulses are disabled as long as FB is pulled below Pin 1. As soon as FB is relaxed, the IC resumes its operation. Figure 26 depicts the application example.

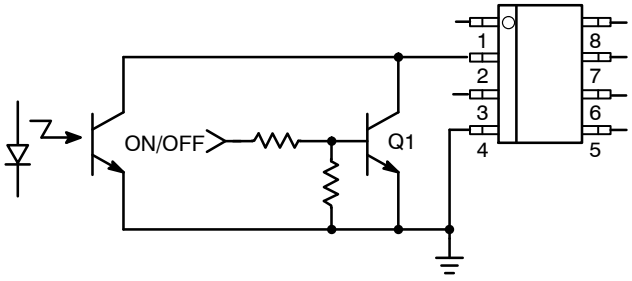



**Figure 26. Another Way of Shutting Down the IC Without a Definitive Latchoff State**

### Protecting the Controller Against Negative Spikes

As with any controller built upon a CMOS technology, it is the designer's duty to avoid the presence of negative spikes on sensitive pins. Negative signals have the bad habit to forward bias the controller substrate and induce erratic behaviors. Sometimes, the injection can be so strong that internal parasitic SCRs are triggered, engendering irremediable damages to the IC if a low impedance path is offered between $V_{CC}$ and GND. If the current sense pin is often the seat of such spurious signals, the high−voltage pin can also be the source of problems in certain circumstances. During the turn−off sequence, e.g. when the user unplugs the power supply, the controller is still fed by its $V_{CC}$ capacitor and keeps activating the MOSFET ON and OFF with a peak current limited by Rsense. Unfortunately, if the quality coefficient Q of the resonating network formed by Lp and Cbulk is low (e.g. the MOSFET Rdson + Rsense are small), conditions are met to make the circuit resonate and thus negatively bias the controller. Since we are talking about ms pulses, the amount of injected charge (Q = I * t) immediately latches the controller that brutally discharges its $V_{CC}$ capacitor. If this $V_{CC}$ capacitor is of sufficient value, its stored energy damages the controller. Figure 27 depicts a typical negative shot occurring on the HV pin where the brutal $V_{CC}$ discharge testifies for latchup.

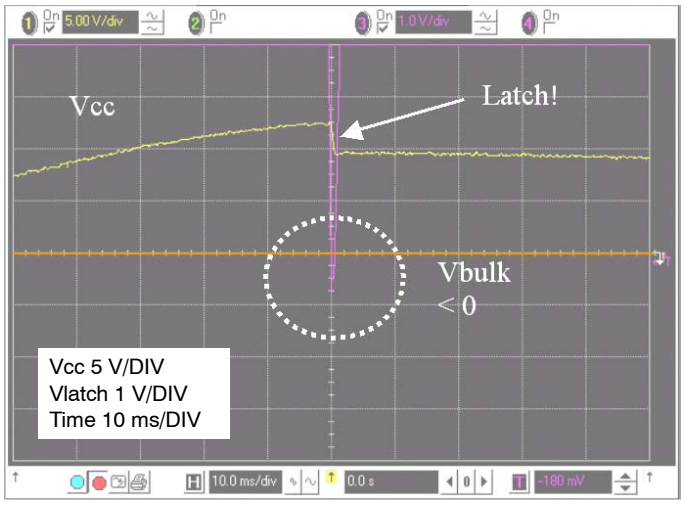



**Figure 27. A Negative Spike Takes Place on the Bulk Capacitor at the Switch−Off Sequence**

Simple and inexpensive cures exist to prevent from internal parasitic SCR activation. One of them consists in inserting a resistor in series with the high−voltage pin to keep the negative current to the lowest when the bulk becomes negative (Figure 28). Please note that the negative spike is clamped to (−2*Vf) thanks to the diode bridge. Also, the power dissipation of this resistor is extremely small since it only heats up during the startup sequence.

Another option (Figure 29) consists in wiring a diode from $V_{CC}$ to the bulk capacitor to force $V_{CC}$ to reach $VCC_{ON}$ sooner and thus stops the switching activity before the bulk capacitor gets deeply discharged. For security reasons, two diodes can be connected in series.

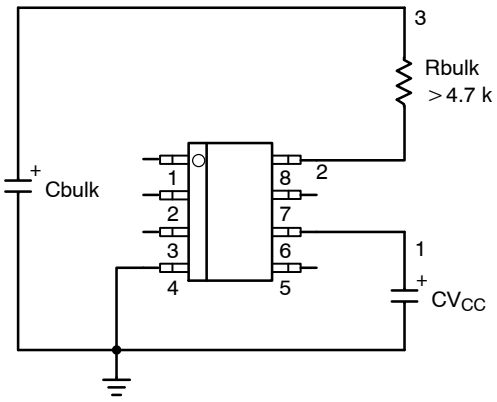



**Figure 28. A simple resistor in series avoids any latch−up in the controller . . .**

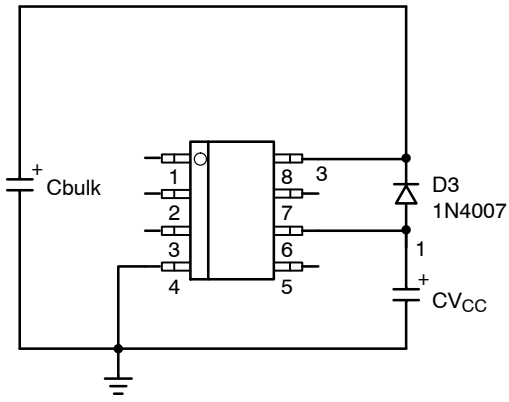



**Figure 29. . . . or one diode forces $V_{CC}$ to reach $VCC_{ON}$ sooner.**

**Soft−Start (NCP1217A only)**

The NCP1217A features an internal 1.0 ms soft−start activated during the power on sequence (PON). As soon as $V_{CC}$ reaches $VCC_{OFF}$, the peak current is gradually increased from nearly zero up to the maximum clamping level (e.g. 1.0 V). This situation lasts during 1.0 ms and further to that time period, the peak current limit is blocked to 1.0 V until the supply enters regulation. The soft−start is also activated during the Over Current Burst (OCP) sequence. Every restart attempt is followed by a soft−start activation. Generally speaking, the soft−start will be activated when $V_{CC}$ ramps up either from zero (fresh power−on sequence) or 5.6 V, the latchoff voltage occurring during OCP. Figure 30 portrays the soft−start behavior. The time scales are purposely shifted to offer a better zoom portion.

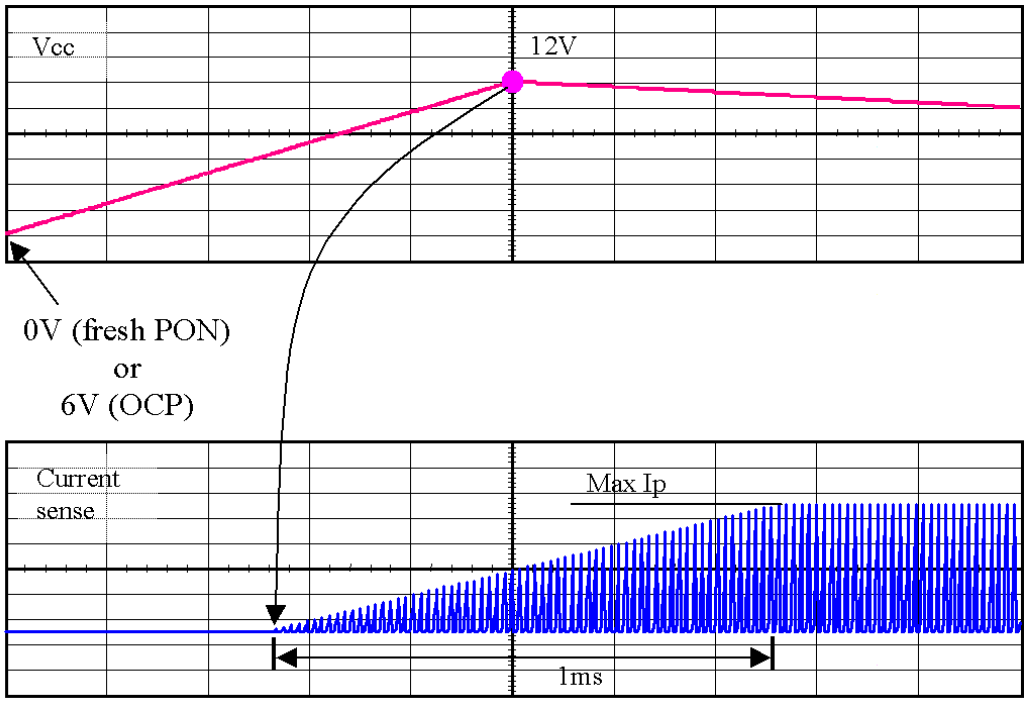



**Figure 30. Soft−start is activated during a startup sequence or an OCP condition**

## ORDERING INFORMATION

| Device | Version | Marking | Package | Shipping† |
|---|---|---|---|---|
| NCP1217D65R2G | 65 kHz | 17D06 | SO−8 (Pb−Free) | 2500 / Tape & Reel |
| NCP1217D100R2G | 100 kHz | 17D10 | SO−8 (Pb−Free) | 2500 / Tape & Reel |
| NCP1217D133R2G | 133 kHz | 17D13 | SO−8 (Pb−Free) | 2500 / Tape & Reel |
| NCP1217P65G | 65 kHz | P1217P065 | PDIP−7 (Pb−Free) | 50 Units / Rail |
| NCP1217P100G | 100 kHz | P1217P100 | PDIP−7 (Pb−Free) | 50 Units / Rail |
| NCP1217P133G | 133 kHz | N1217P133 | PDIP−7 (Pb−Free) | 50 Units / Rail |
| NCP1217AD65R2G | 65 kHz | 17A06 | SO−8 (Pb−Free) | 2500 / Tape & Reel |
| NCP1217AD100R2G | 100 kHz | 17A10 | SO−8 (Pb−Free) | 2500 / Tape & Reel |
| NCP1217AD133R2G | 133 kHz | 17A13 | SO−8 (Pb−Free) | 2500 / Tape & Reel |
| NCP1217AP65G | 65 kHz | 1217AP06 | PDIP−7 (Pb−Free) | 50 Units / Rail |
| NCP1217AP100G | 100 kHz | P1217AP10 | PDIP−7 (Pb−Free) | 50 Units / Rail |
| NCP1217AP133G | 133 kHz | 1217AP13 | PDIP−7 (Pb−Free) | 50 Units / Rail |

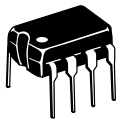
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

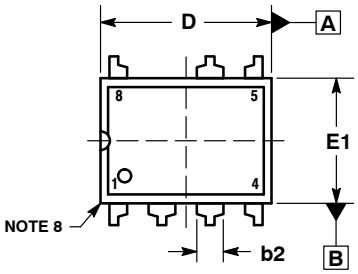
ON Semiconductor®

**PDIP−7 (PDIP−8 LESS PIN 7)**
CASE 626B
ISSUE D

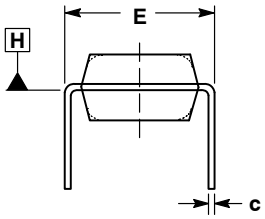
DATE 22 APR 2015



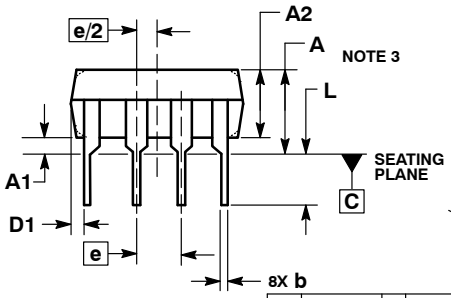
SCALE 1:1



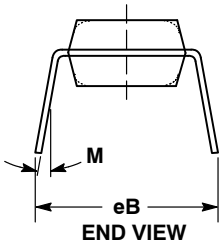

TOP VIEW




END VIEW
WITH LEADS CONSTRAINED
NOTE 5




SIDE VIEW



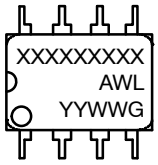

END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | ---- | 0.210 | --- | 5.33 |
| A1 | 0.015 | ---- | 0.38 | --- |
| A2 | 0.115 | 0.195 | 2.92 | 4.95 |
| b | 0.014 | 0.022 | 0.35 | 0.56 |
| b2 | 0.060 TYP | | 1.52 TYP | |
| C | 0.008 | 0.014 | 0.20 | 0.36 |
| D | 0.355 | 0.400 | 9.02 | 10.16 |
| D1 | 0.005 | ---- | 0.13 | --- |
| E | 0.300 | 0.325 | 7.62 | 8.26 |
| E1 | 0.240 | 0.280 | 6.10 | 7.11 |
| e | 0.100 BSC | | 2.54 BSC | |
| eB | ---- | 0.430 | --- | 10.92 |
| L | 0.115 | 0.150 | 2.92 | 3.81 |
| M | ---- | 10° | --- | 10° |

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. NOT USED
8. $V_{CC}$

### GENERIC MARKING DIAGRAM*




XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

| DOCUMENT NUMBER: | 98AON12198D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
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| DESCRIPTION: | PDIP−7 (PDIP−8 LESS PIN 7) | PAGE 1 OF 1 |

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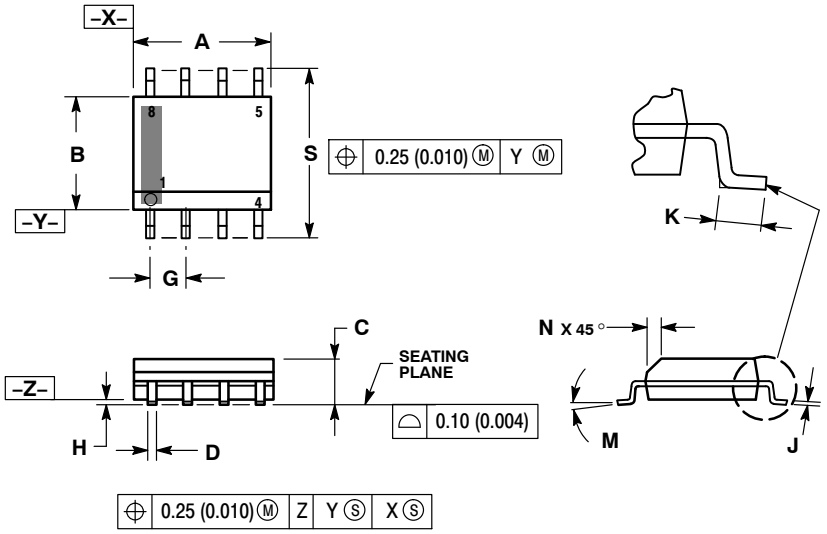
# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS



**SCALE 1:1**

**SOIC−8 NB**
CASE 751−07
ISSUE AK

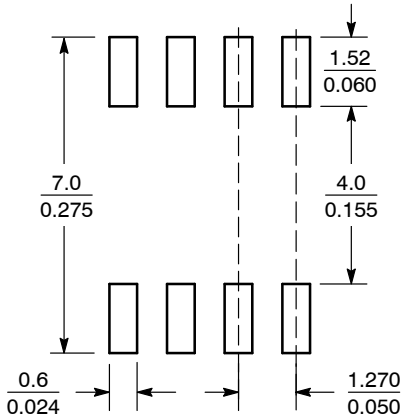
DATE 16 FEB 2011




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

| | MILLIMETERS | | INCHES | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 4.80 | 5.00 | 0.189 | 0.197 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.053 | 0.069 |
| D | 0.33 | 0.51 | 0.013 | 0.020 |
| G | 1.27 BSC | | 0.050 BSC | |
| H | 0.10 | 0.25 | 0.004 | 0.010 |
| J | 0.19 | 0.25 | 0.007 | 0.010 |
| K | 0.40 | 1.27 | 0.016 | 0.050 |
| M | 0 ° | 8 ° | 0 ° | 8 ° |
| N | 0.25 | 0.50 | 0.010 | 0.020 |
| S | 5.80 | 6.20 | 0.228 | 0.244 |

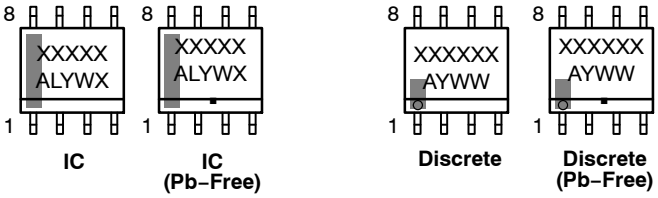
### SOLDERING FOOTPRINT*




SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

### GENERIC MARKING DIAGRAM*




IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

**STYLES ON PAGE 2**

| | | |
|---|---|---|
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| **DESCRIPTION:** | **SOIC−8 NB** | **PAGE 1 OF 2** |

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**SOIC−8 NB**
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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