NCP1230

PWM Controller, Fixed Frequency, Current Mode

The NCP1230 represents a major leap towards achieving standby power in medium−to−high power Switched−Mode Power Supplies such as notebook adapters, offline battery chargers and consumer electronics equipment. Housed in a compact 8−pin package (SOIC−8, SOIC−7, or PDIP−7), the NCP1230 contains all needed control functionality to build a rugged and efficient power supply. The NCP1230 is a current mode controller with internal ramp compensation. Among the unique features offered by the NCP1230 is an event management scheme that can disable the front−end PFC circuit during standby, thus reducing the no load power consumption.

The NCP1230 itself goes into cycle skipping at light loads while limiting peak current (to 25% of nominal peak) so that no acoustic noise is generated. The NCP1230 has a high−voltage startup circuit that eliminates external components and reduces power consumption.

The NCP1230 also features an internal latching function that can be used for OVP protection. This latch is triggered by pulling the CS pin above 3.0 V and can only be reset by pulling V_{CC} to ground. True overload protection, internal 2.5 ms soft−start, internal leading edge blanking, internal frequency dithering for low EMI are some of the other important features offered by the NCP1230.

Features

- Current−Mode Operation with Internal Ramp Compensation
- Internal High−Voltage Startup Current Source for Loss−Less Startup
- Extremely Low No−Load Standby Power
- Skip−Cycle Capability at Low Peak Currents
- Direct Connection to PFC Controller for Improved No−Load Standby Power
- Internal 2.5 ms Soft−Start
- Internal Leading Edge Blanking
- Latched Primary Overcurrent and Overvoltage Protection
- Short−Circuit Protection Independent of Auxiliary Level
- Internal Frequency Jittering for Improved EMI Signature
- +500 mA/−800 mA Peak Current Drive Capability
- Available in Three Frequency Options: 65 kHz, 100 kHz, and 133 kHz
- Direct Optocoupler Connection
- SPICE Models Available for TRANsient and AC Analysis
- This is a Pb−Free Device

Typical Applications

- High Power AC−DC Adapters for Notebooks, etc.
- Offline Battery Chargers
- Set−Top Boxes Power Supplies, TV, Monitors, etc.

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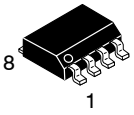
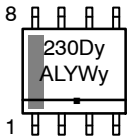
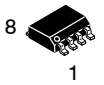
MARKING DIAGRAM

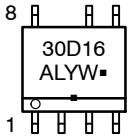


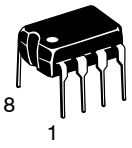
SOIC−8 VHVIC
D SUFFIX
CASE 751



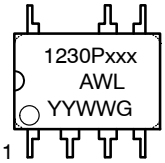


SOIC−7
D1 SUFFIX
CASE 751U





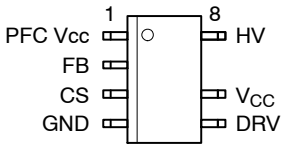
PDIP−7 VHVIC
P SUFFIX
CASE 626B



xxx	= Device Code: 65, 100, 133
y	= Device Code: 6, 1, 1
y	5 0 3
A	= Assembly Location
L	= Wafer Lot
Y, YY	= Year
W, WW	= Work Week
G	= Pb−Free Package
▪	= Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 4 of this data sheet.

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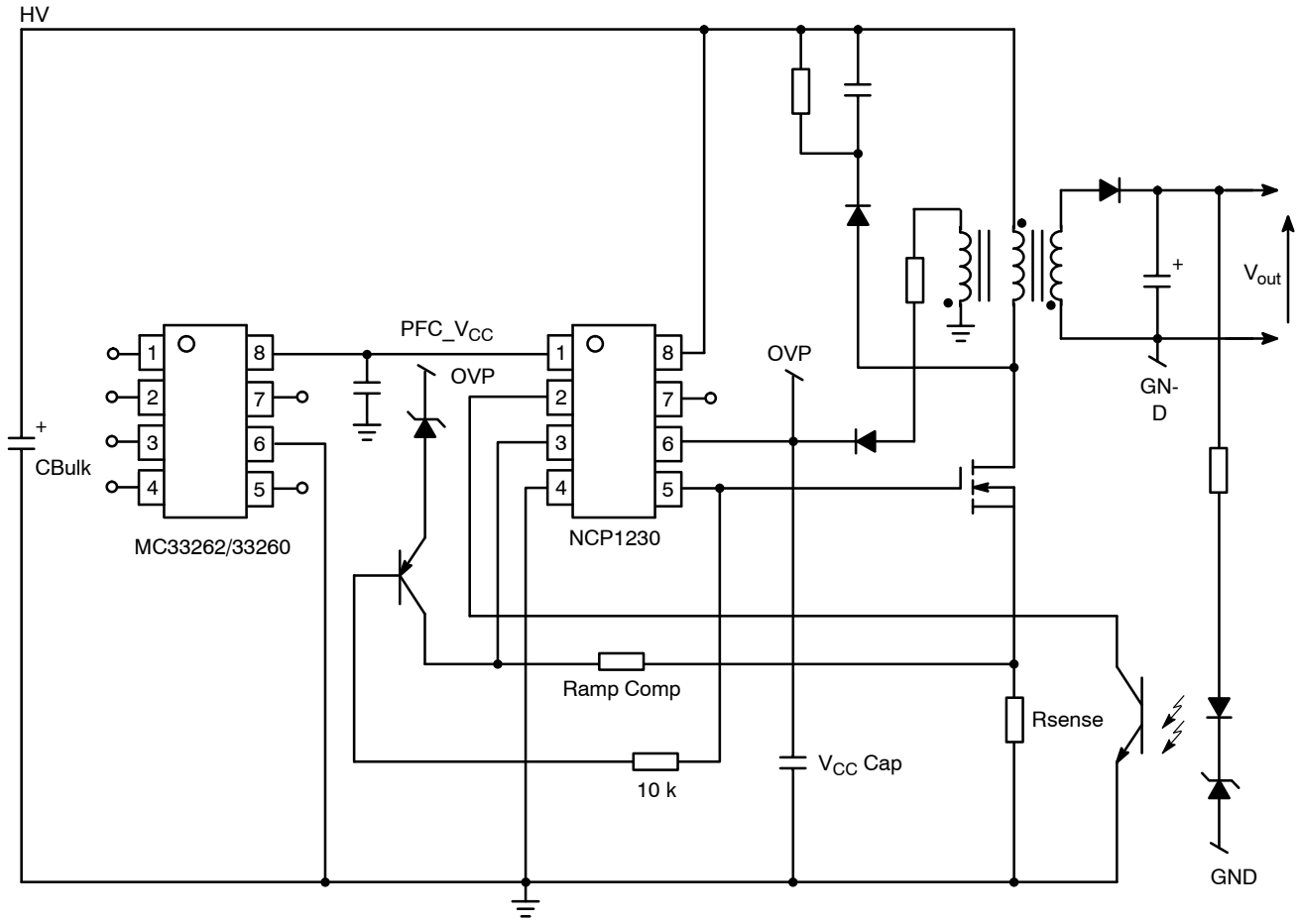


Figure 1. Typical Application Example

PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1	PFC V_{CC}	This pin provides the bias voltage to the PFC controller.	This pin is a direct connection to the V_{CC} pin (Pin 6) via a low impedance switch. In standby and during the startup sequence, the switch is open and the PFC V_{CC} is shut down. As soon as the aux. winding is stabilized, Pin 1 connects to the V_{CC} pin and provides bias to the PFC controller. It goes down in standby and fault conditions.
2	FB	Feedback Signal	An optocoupler collector pulls this pin low to regulate. When the current setpoint reaches 25% of the maximum peak, the controller skips cycles.
3	CS/OVP	Current Sense	This pin incorporates three different functions: the current sense function, an internal ramp compensation signal and a 3.0 V latch−off level which latches the output off until V_{CC} is recycled.
4	GND	IC Ground	−
5	DRV	Driver Output	With a drive capability of +500 mA / −800 mA, the NCP1230 can drive large Qg MOSFETs.
6	V_{CC}	V_{CC} Input	The controller accepts voltages up to 18 V and features a UVLO turn−off threshold of 7.7 V typical.
7	NC	−	−
8	HV	High−Voltage	This pin connects to the bulk voltage and offers a lossless startup sequence. The charging current is high enough to support the bias needs of a PWM controller through Pin 1.

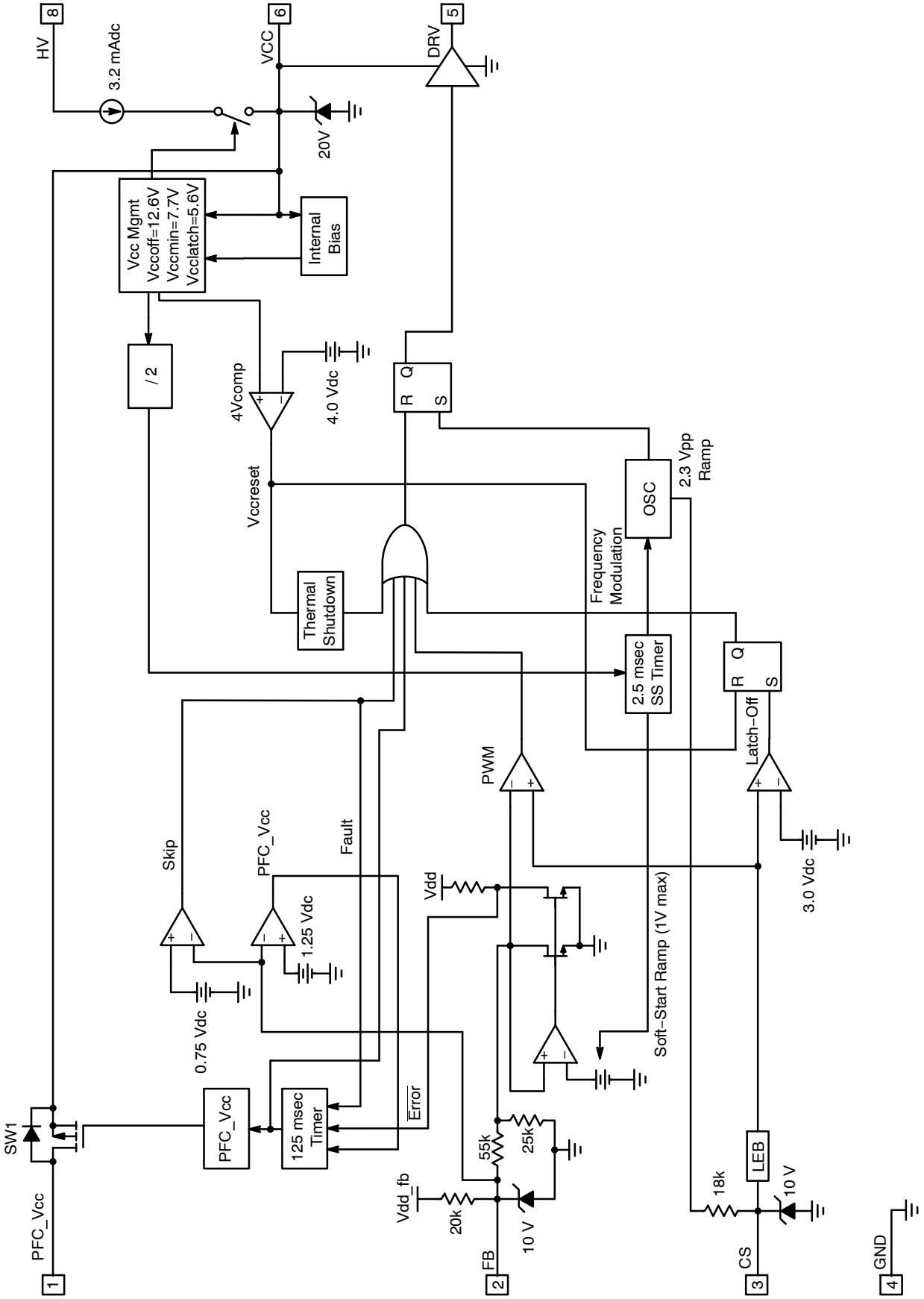


Figure 2. Internal Circuit Architecture

MAXIMUM RATINGS (Notes 1 and 2)

Rating		Symbol	Value	Unit
Maximum Voltage on Pin 8 Maximum Current		V_{DS} I_{C2}	−0.3 to 500 100	V mA
Power Supply Voltage, Pin 6 Current		V_{CC} I_{CC2}	−0.3 to 18 100	V mA
Drive Output Voltage, Pin 5 Drive Current		V_{DV} I_o	18 1.0	V A
Voltage Current Sense Pin, Pin 3 Current		V_{cs} I_{cs}	10 100	V mA
Voltage Feedback, Pin 2 Current		V_{fb} I_{fb}	10 100	V mA
Voltage, Pin 1 Maximum Continuous Current Flowing from Pin 1		V_{PFC} I_{PFC}	18 35	V mA
Thermal Resistance, Junction−to−Air, PDIP Version		$R_{\theta JA}$	100	°C/W
Thermal Resistance, Junction−to−Air, SOIC Version		$R_{\theta JA}$	178	°C/W
Maximum Power Dissipation @ T_A = 25°C	PDIP SOIC	P_{max}	1.25 0.702	W
Maximum Junction Temperature		T_J	150	°C
Storage Temperature Range		T_{stg}	−60 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device series contains ESD protection and exceeds the following tests:
   Pin 1−6: Human Body Model 2000 V per JEDEC Standard JES22, Method A114E.
   Machine Model Method 200 V per JEDEC Standard JESD22, Method A115A.
   Pin 8 is the HV startup of the device and is rated to the maximum rating of the part, or 500 V.
2. This device contains latchup protection and exceeds 100 mA per JEDEC Standard JESD78.

ORDERING INFORMATION

Device	Package	Shipping†
NCP1230D165R2G	SOIC−7 (Pb−Free)	2500 / Tape & Reel
NCP1230D65R2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1230D100R2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1230D133R2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1230P65G	PDIP−7 (Pb−Free)	50 Units/ Rail
NCP1230P100G	PDIP−7 (Pb−Free)	50 Units/ Rail
NCP1230P133G	PDIP−7 (Pb−Free)	50 Units/ Rail

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 13 V, V_{PIN8} = 30 V unless otherwise noted.)

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
Supply Section (All frequency versions, otherwise noted)						
Turn−On Threshold Level, V_{CC} Going Up (V_{fb} = 2.0 V)	V_{CCOFF}	6	11.6	12.6	13.6	V
Minimum Operating Voltage after Turn−On	$V_{CC(min)}$	6	7.0	7.7	8.4	V
V_{CC} Decreasing Level at which the Latch−Off Phase Ends (V_{fb} = 3.5 V)	$V_{CClatch}$	6	5.0	5.6	6.2	V
V_{CC} Level at which the Internal Logic gets Reset	$V_{CCreset}$	6	–	4.0	–	V
Internal IC Consumption, No Output Load on Pin 6 (V_{fb} = 2.5 V)	I_{CC1}	6	0.6	1.1	1.8	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 6, F_{SW} = 65 kHz (V_{fb} = 2.5 V)	I_{CC2}	6	1.3	1.8	2.5	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 6, F_{SW} = 100 kHz	I_{CC2}	6	1.3	2.2	3.0	mA
Internal IC Consumption, 1.0 nF Output Load on Pin 6, F_{SW} = 133 kHz	I_{CC2}	6	1.3	2.8	3.3	mA
Internal IC Consumption, Latch−Off Phase	I_{CC3}	6	400	680	1000	μA
Internal Startup Current Source						
High−Voltage Current Source, 1.0 nF Load (V_{CCOFF} −0.2 V, V_{fb} = 2.5 V, V_{PIN8} = 30 V)	I_{C1}	8	1.8	3.2	4.2	mA
High−Voltage Current Source (V_{CC} = 0 V)	I_{C2}	8	1.8	4.4	5.6	mA
Minimum Startup Voltage (I_c = 0.5 mA, V_{CCOFF} −0.2 V, V_{fb} = 2.5 V)	V_{HVmin}	8	–	20	23	V
Startup Leakage (V_{PIN8} = 500 V)	I_{HVLeak}	8	10	30	80	μA
Drive Output						
Output Voltage Rise−Time @ C_L = 1.0 nF, 10−90% of Output Signal	T_r	5	–	40	–	ns
Output Voltage Fall−Time @ C_L = 1.0 nF, 10−90% of Output Signal	T_f	5	–	15	–	ns
Source Resistance, R_{Load} 300 Ω (V_{fb} = 2.5 V)	R_{OH}	5	6.0	12.3	25	Ω
Sink Resistance, at 1.0 V on Pin 5 (V_{fb} = 3.5 V)	R_{OL}	5	3.0	7.5	18	Ω
Pin 1 Output Impedance (or R_{dson} between Pin 1 and Pin 6 when SW1 is closed) R_{load} on Pin 1 = 680 Ω	RPFC	1	6.0	11.7	23	Ω
Current Comparator and Thermal Shutdown						
Input Bias Current @ 1.0 V Input Level on Pin 3	I_{IB}	3	–	0.02	–	μA
Maximum Internal Current Setpoint Tj = 25°C Tj = −40°C to +125°C	I_{Limit}	3	1.010 0.979	1.063 –	1.116 1.127	V
Default Internal Setpoint for Skip Cycle Operation and Standby Detection	V_{skip}	3	600	750	900	mV
Default Internal Setpoint to Leave Standby	$V_{stby−out}$	–	1.0	1.25	1.5	V
Propagation Delay from CS Detected to Gate Turned Off (V_{Gate} = 10 V) (Pin 5 Loaded by 1.0 nF)	$T_{DEL\ CS}$	3	–	90	180	ns
Leading Edge Blanking Duration	T_{LEB}	3	100	200	350	ns
Soft−Start Period (Note 3)	SS	–	–	2.5	–	ms
Temperature Shutdown, Maximum Value (Note 3)	T_{SD}	–	150	165	–	°C
Hysteresis while in Temperature Shutdown (Note 3)	T_{SD} hyste	–	–	25	–	°C

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Verified by Design.

ELECTRICAL CHARACTERISTICS (For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{CC} = 13 V, V_{PIN8} = 30 V unless otherwise noted.)

Characteristic	Symbol	Pin	Min	Typ	Max	Unit
Internal Oscillator						
Oscillation Frequency, 65 kHz Version (V_{fb} = 2.5 V) Tj = 25°C Tj = 0°C to +125°C Tj = −40°C to +125°C	f_{OSC}	–	60 58 55	65 – –	70 72 72	kHz
Oscillation Frequency, 100 kHz Version Tj = 25°C Tj = 0°C to +125°C Tj = −40°C to +125°C	f_{OSC}	–	93 90 85	100 – –	107 110 110	kHz
Oscillation Frequency, 133 kHz Version Tj = 25°C Tj = 0°C to +125°C Tj = −40°C to +125°C	f_{OSC}	–	123 120 113	133 – –	143 146 146	kHz
Internal Modulation Swing, in Percentage of F_{sw} (V_{fb} = 2.5 V) (Note 4)	–	–	–	±6.4	–	%
Internal Swing Period (Note 4)	–	–	–	5.0	–	ms
Maximum Duty−Cycle (CS = 0, V_{fb} = 2.5 V)	D_{max}	–	75	80	85	%
Internal Ramp Compensation						
Internal Resistor (Note 4)	R_{up}	3	9.0	18	36	kΩ
Ramp Compensation Sawtooth Amplitude	–	3	–	2.3	–	Vpp
Feedback Section						
Opto Current Source (V_{fb} = 0.75 V)	–	2	200	235	270	μA
Pin 3 to Current Setpoint Division Ratio (Note 4)	I_{ratio}	–	–	2.8	–	–
Protection						
Timeout before Validating Short−Circuit or PFC V_{CC} (Note 4)	T_{DEL}	–	–	125	–	ms
Latch−Off Level	V_{latch}	3	2.7	3.0	3.3	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Verified by Design.

TYPICAL PERFORMANCE CHARACTERISTICS

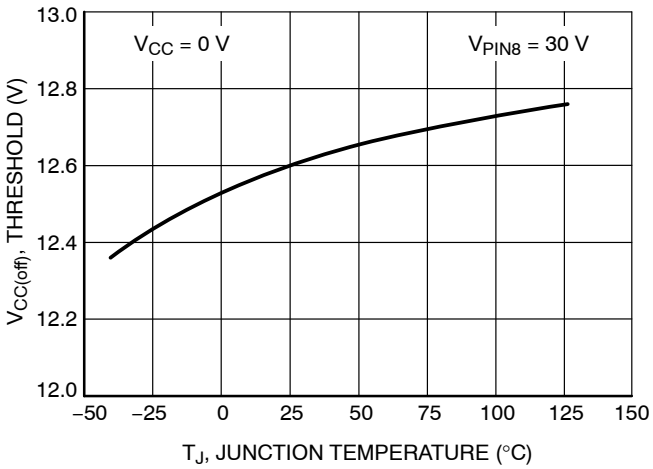


Figure 3. $V_{CC(OFF)}$ Threshold vs. Temperature

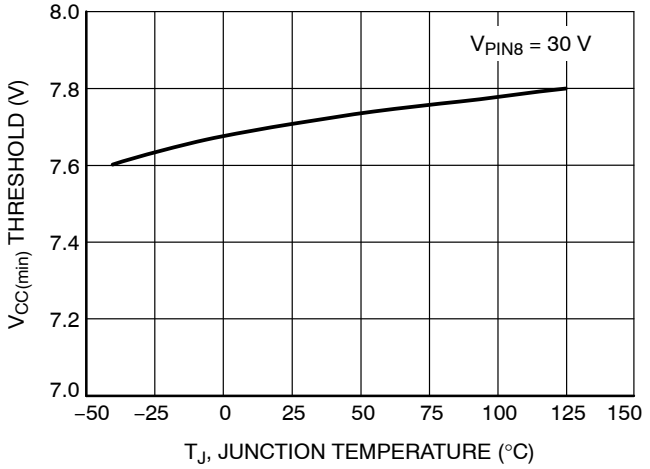


Figure 4. $V_{CC(min)}$ Threshold vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

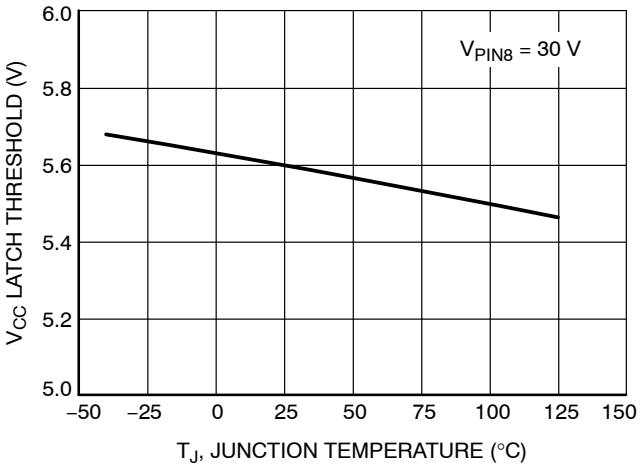


Figure 5. V_{CC} Latch Threshold vs. Temperature

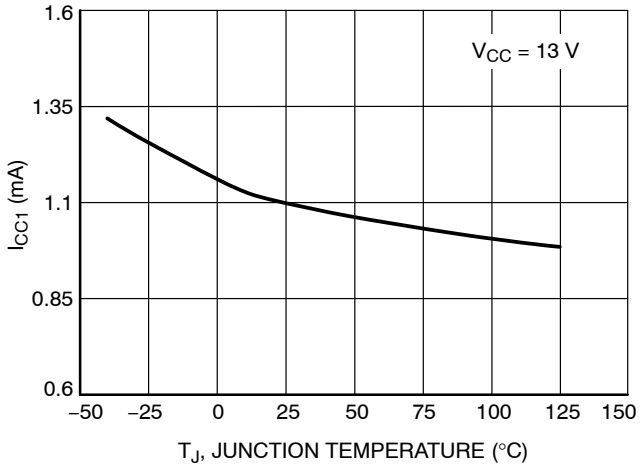


Figure 6. I_{CC1} Internal Current Consumption, No Load vs. Temperature

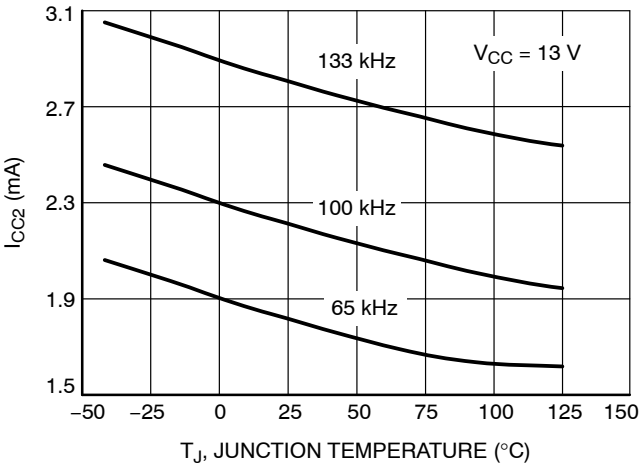


Figure 7. I_{CC2} Internal Current Consumption, 1.0 nF Load vs. Temperature

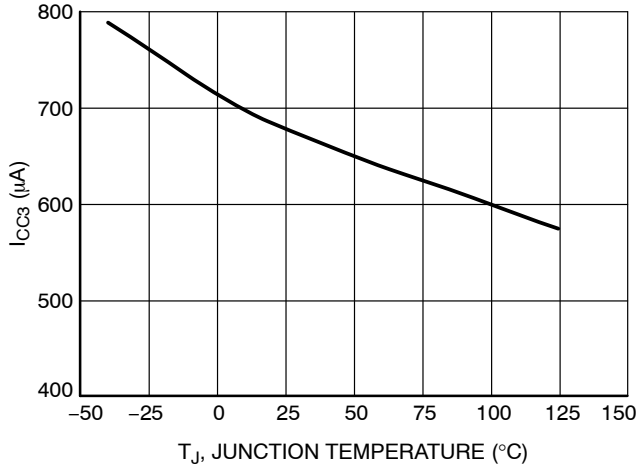


Figure 8. I_{CC3} Internal Consumption, Latch−Off Phase vs. Temperature

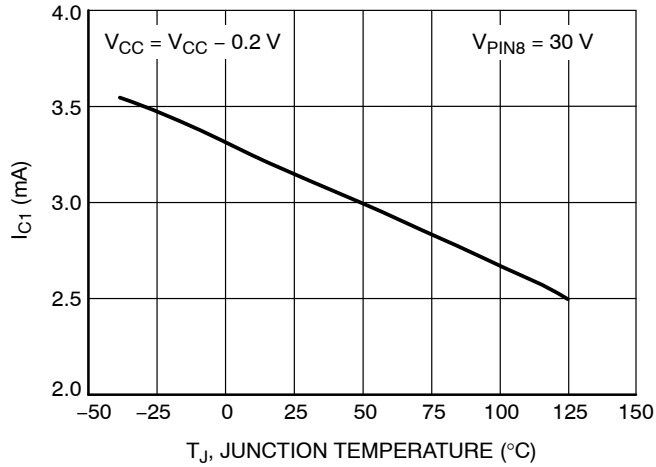


Figure 9. I_{C1} Startup Current vs. Temperature

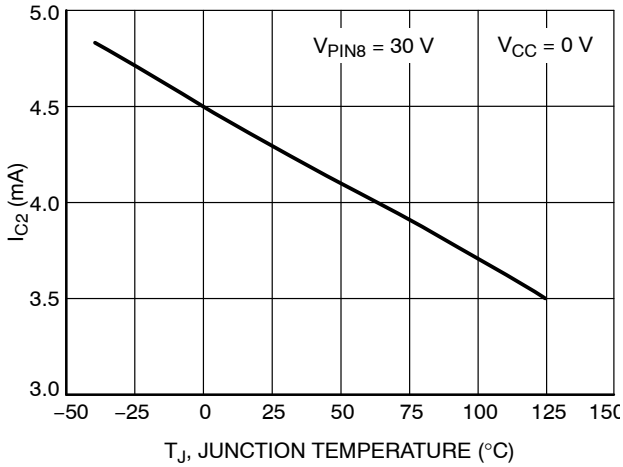


Figure 10. I_{C2} Startup Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

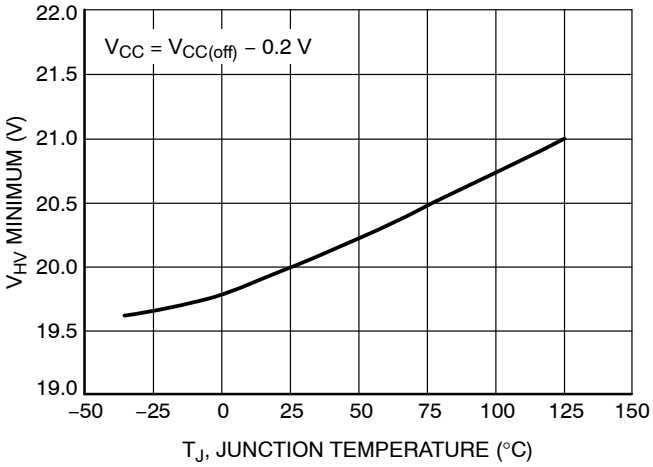


Figure 11. Minimum Startup Voltage vs. Temperature

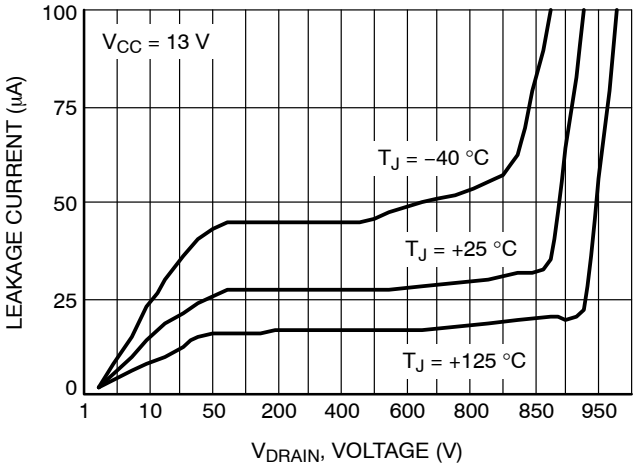


Figure 12. Leakage Current vs. Temperature

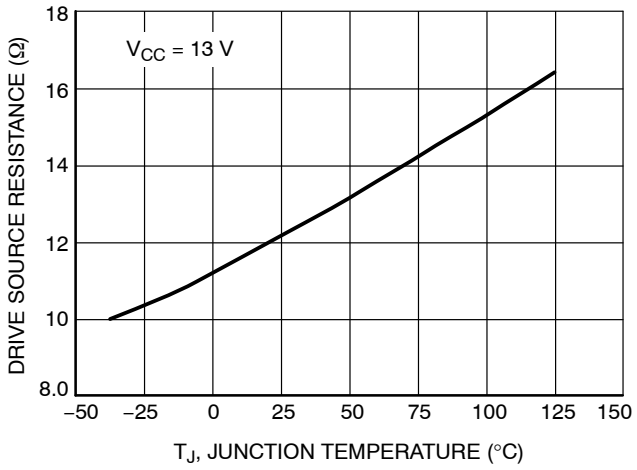


Figure 13. Drive Source Resistance vs. Temperature

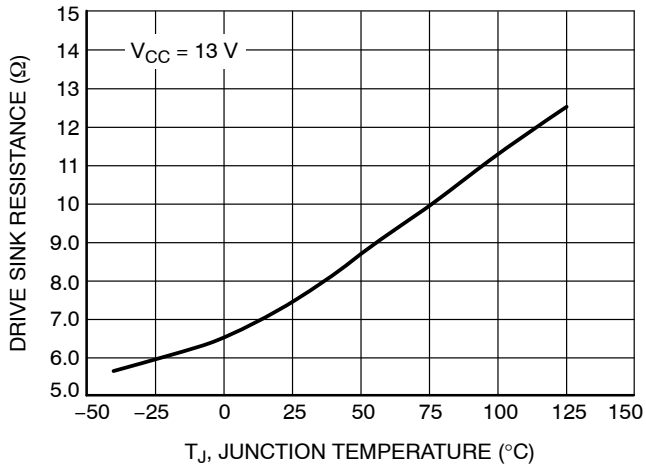


Figure 14. Drive Sink Resistance vs. Temperature

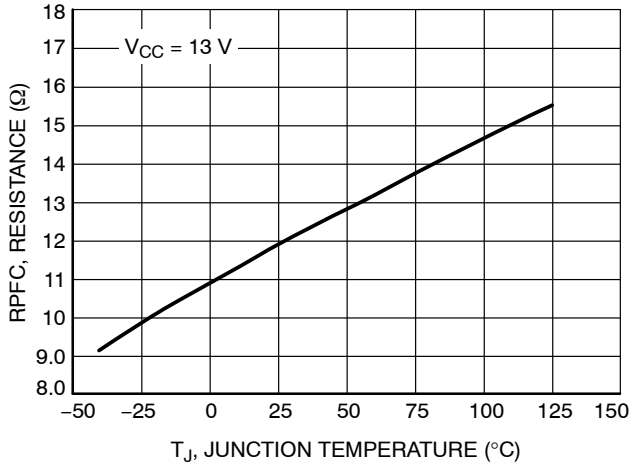


Figure 15. RPFC vs. Temperature

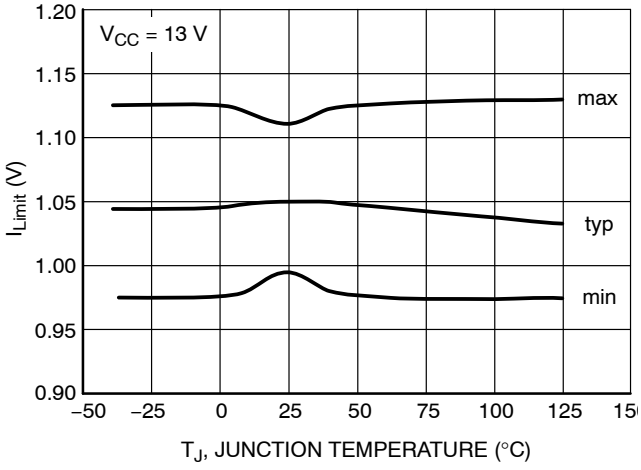


Figure 16. I_{Limit} vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

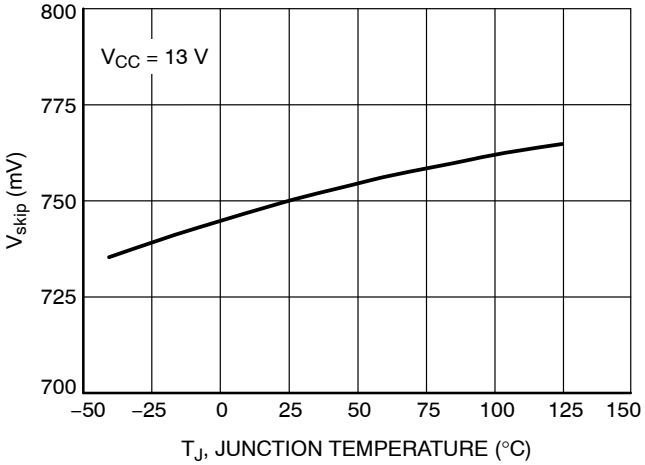


Figure 17. V_{skip} vs. Temperature

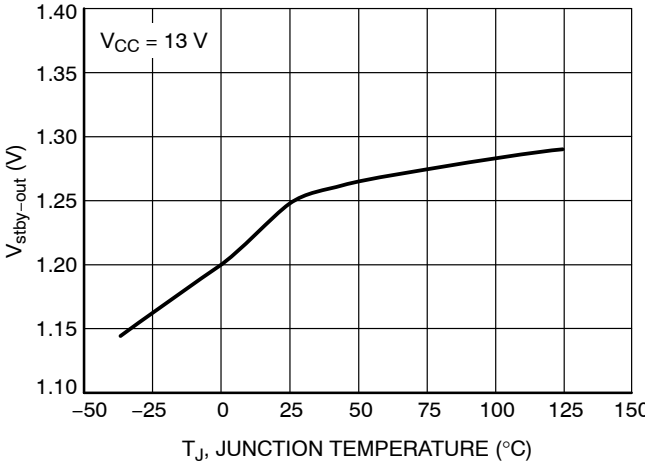


Figure 18. $V_{stby-out}$ vs. Temperature

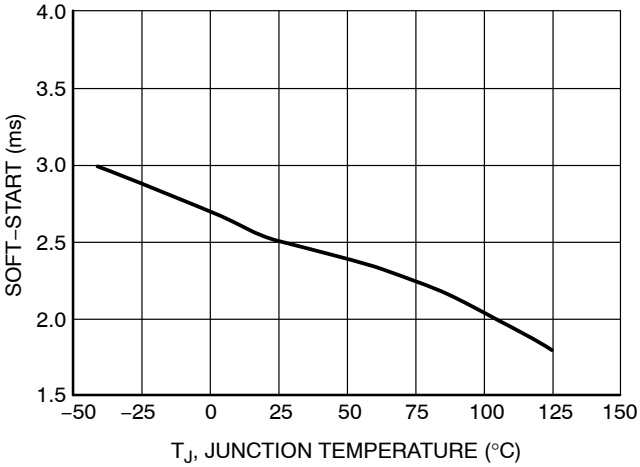


Figure 19. Soft−Start vs. Temperature

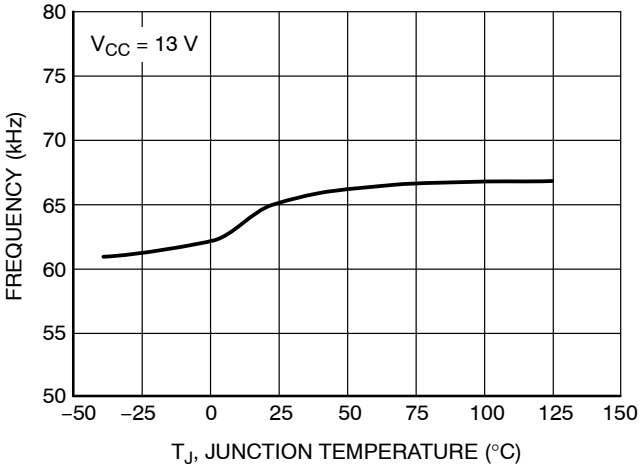


Figure 20. Frequency (65 kHz) vs. Temperature

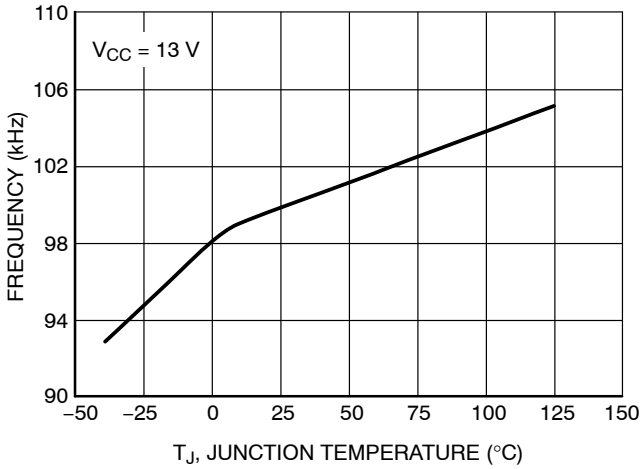


Figure 21. Frequency (100 kHz) vs. Temperature

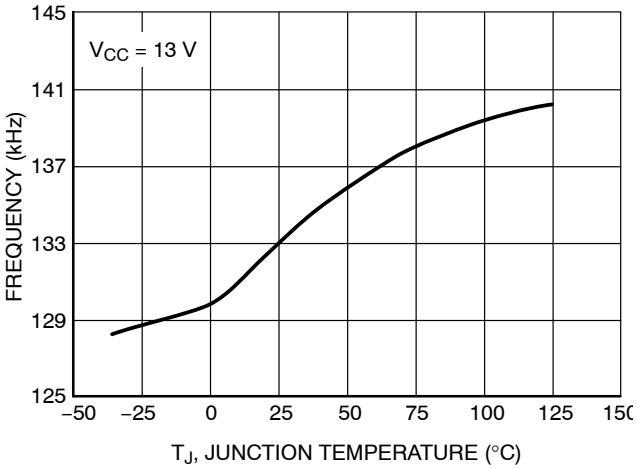


Figure 22. Frequency (133 kHz) vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

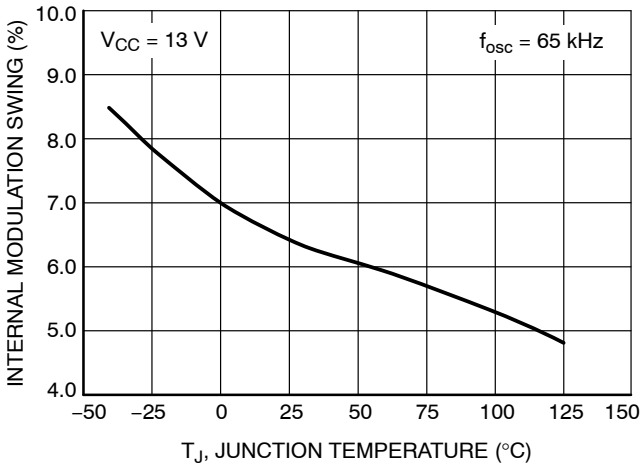


Figure 23. Internal Modulation Swing vs. Temperature

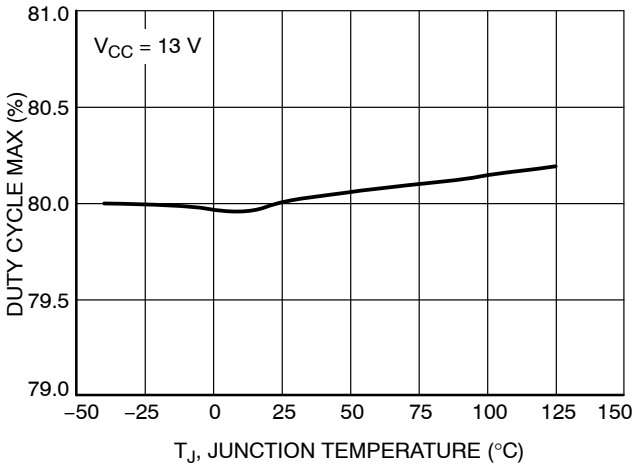


Figure 24. Maximum Duty Cycle vs. Temperature

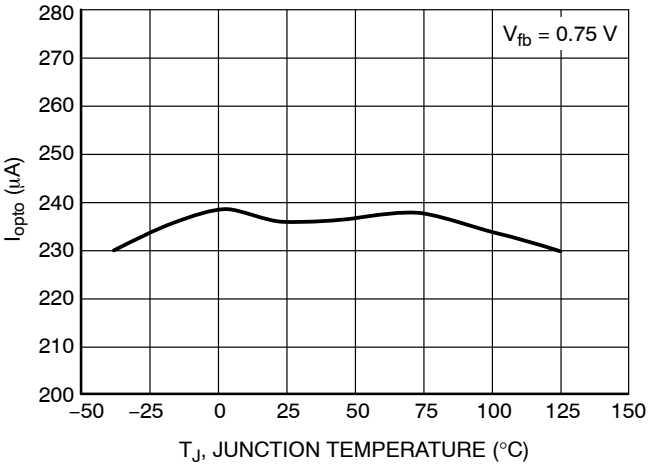


Figure 25. I_{opto} vs. Temperature

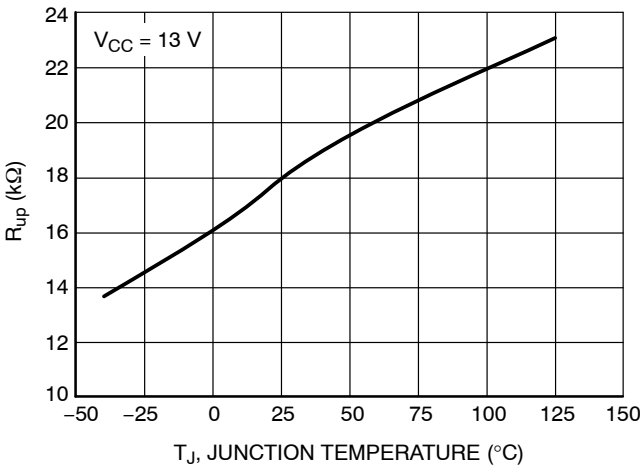


Figure 26. Internal Ramp Compensation Resistor vs. Temperature

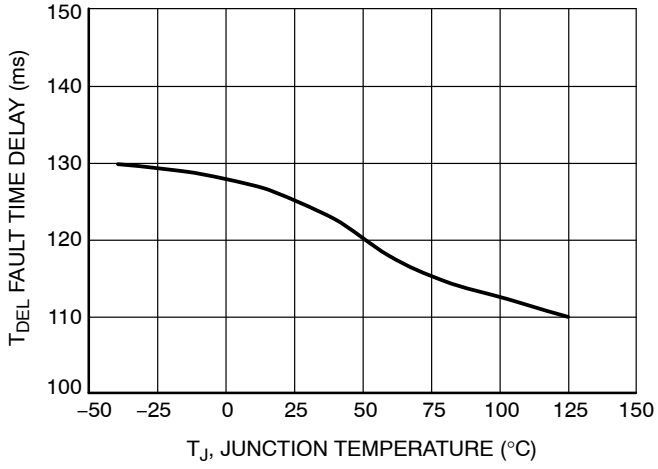


Figure 27. Fault Time Delay vs. Temperature

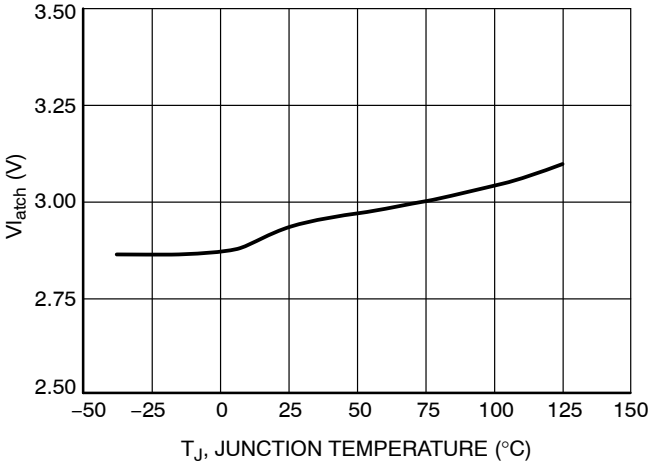


Figure 28. VI_{atch} vs. Temperature

OPERATING DESCRIPTION

Introduction

The NCP1230 is a current mode controller which provides a high level of integration by providing all the required control logic, protection, and a PWM Drive Output into a single chip which is ideal for low cost, medium to high power off−line application, such as notebook adapters, battery chargers, set−boxes, TV, and computer monitors.

The NCP1230 can be connected directly to a high voltage source providing lossless startup, and eliminating external startup circuitry. In addition, the NCP1230 has a PFC_V_{CC} output pin which provides the bias supply power for a Power Factor Correction controller, or other logic. The NCP1230 has an event management scheme which disables the PFC_V_{CC} output during standby, and overload conditions.

PFC_V_{CC}

As shown on the internal NCP1230 diagram, an internal low impedance switch SW1 routes Pin 6 (V_{CC}) to Pin 1 when the power supply is operating under nominal load conditions. The PFC_V_{CC} signal is capable of delivering up to 35 mA of continuous current for a PFC Controller, or other logic.

Connecting the NCP1230 PFC_V_{CC} output to a PFC Controller chip is very straight forward, refer to the “Typical Application Example” all that is generally required is a small decoupling capacitor (0.1 μF).

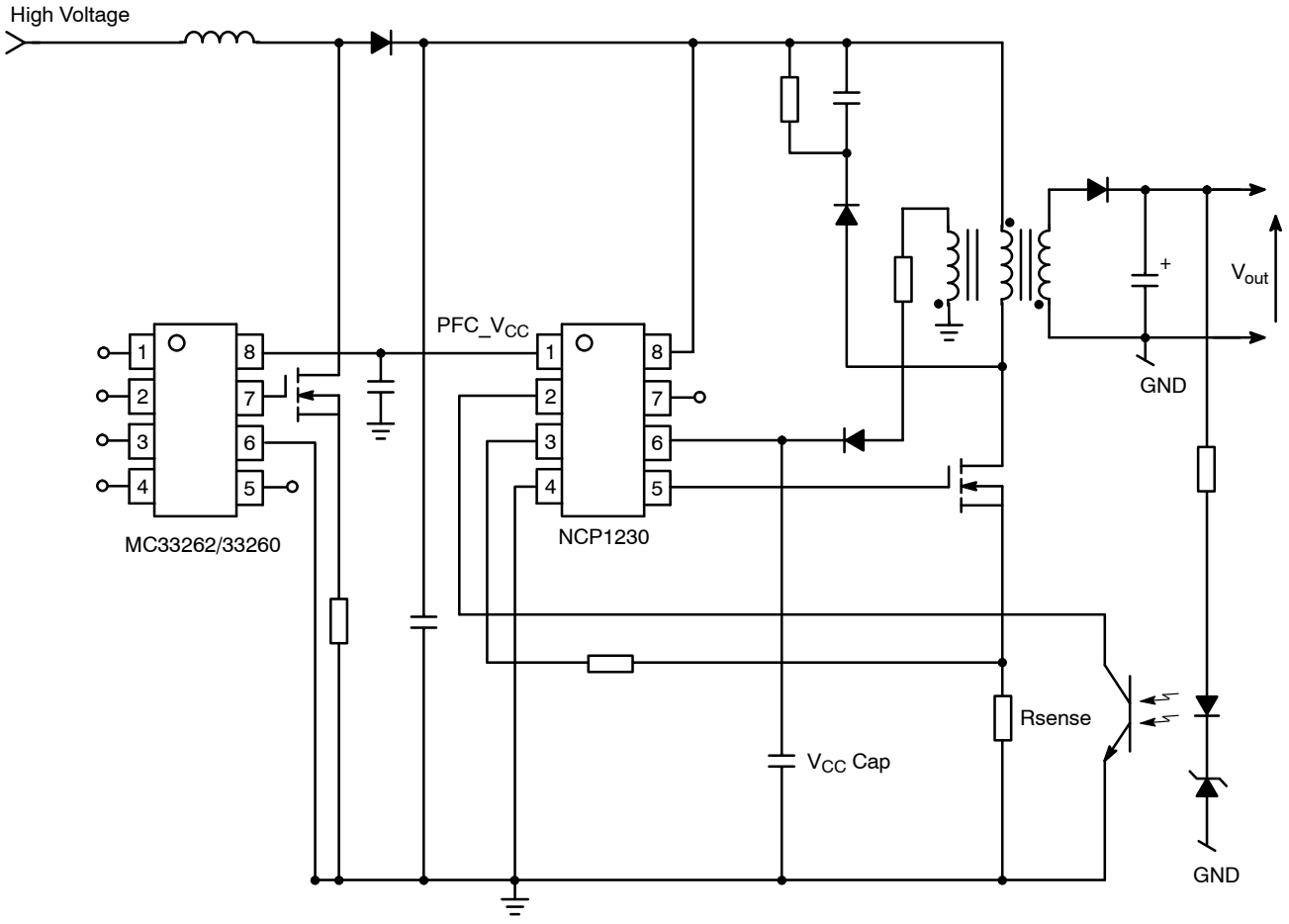


Figure 29. Typical Application Example

Feedback

The feedback pin has been designed to be connected directly to the open−collector output of an optocoupler. The pin is pulled−up through a 20 kΩ resistor to the internal Vdd_fb supply (5 volts nominal). The feedback input signal is divided down, by a factor of three, and connected to the negative (−) input of the PWM comparator. The positive (+) input to the PWM comparator is the current sense signal (Figure 30).

The NCP1230 is a peak current mode controller, where the feedback signal is proportional to the output power. At the beginning of the cycle, the power switch is turns−on and the current begins to increase in the primary of the transformer, when the peak current crosses the feedback voltage level, the PWM comparators switches from a logic level low, to a logic level high, resetting the PWM latching Flip−Flop, turning off the power switch until the next oscillator clock cycle begins.

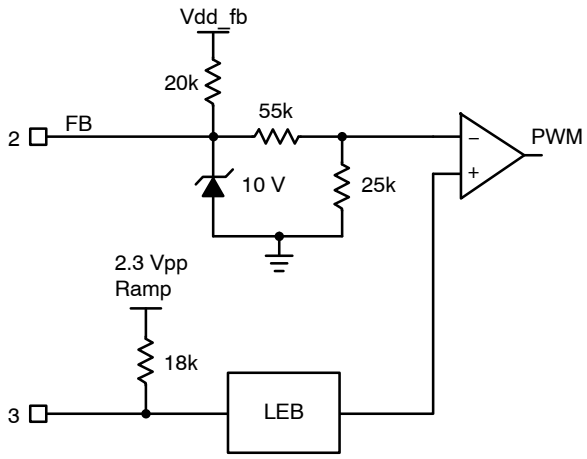


Figure 30.

The feedback pin input is clamped to a nominal 10 volt for ESD protection.

Skip Mode

The feedback input is connected in parallel with the skip cycle logic (Figure 31). When the feedback voltage drops below 25% of the maximum peak current (1.0 V/Rsense) the IC prevents the current from decreasing any further and starts to blank the output pulses. This is called the skip cycle mode. While the controller is in the burst mode the power transfer now depends upon the duty cycle of the pulse burst width which reduces the average input power demand.

$$V_c = I_{pk} \cdot R_s \cdot 3$$

where:

V_c = control voltage (Feedback pin input),
I_{pk} = Peak primary current,
R_s = Current sense resistor,
3 = Feedback divider ratio.

$$SkipLevel = 3V \cdot 25\% = 0.75V$$

$$I_{pk} = \frac{0.75}{R_s \cdot 3}$$

where:

$$I_{pk} \cdot R_s = 1V$$

$$I_{pk} = \sqrt{\frac{2 \cdot P_{in}}{L_p \cdot f}}$$

where:

P_{in} = is the power level where the NCP1230 will go into the skip mode

L_p = Primary inductance

f = NCP1230 controller frequency

$$P_{in} = \frac{L_p \cdot f \cdot I_{pk}^2}{2}$$

$$P_{in} = \frac{P_{out}}{Eff}$$

where:

Eff = the power supply efficiency

$$R_{out} = \frac{E_{out}^2}{P_{out}}$$

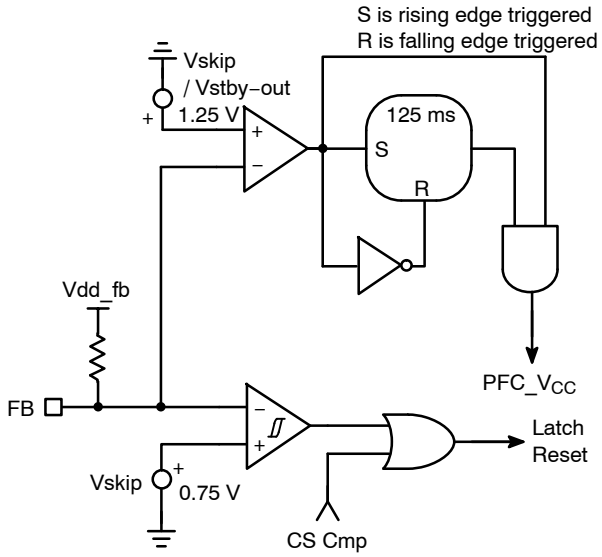


Figure 31.

During the skip mode the PFC_Vcc signal (pin 1) is asserted into a high impedance state when a light load condition is detected and confirmed, Figure 32 shows typical waveforms. The first section of the waveform shows a normal startup condition, where the output voltage is low, as a result the feedback signal will be high asking the controller to provide the maximum power to the output. The second phase is under normal loading, and the output is in regulation. The third phase is when the output power drops below the 25% threshold (the feedback voltage drops to 0.75 volts). When this occurs, the 125 msec timer starts, and if the conditions is still present after the time output period, the

NCP1230 confirms that the low output power condition is present, and the internal SW1 opens, and the PFC_Vcc signal output is shuts down. While the NCP1230 is in the skip mode the FB pin will move around the 750 mV threshold level, with approximately 100 mVp−p of hysteresis on the skip comparator, at a period which depends upon the (light) loading of the power supply and its various time constants. Since this ripple amplitude superimposed over the FB pin is lower than the second threshold (1.25 volt), the PFC_Vcc comparator output stays high (PFC_Vcc output Pin 1 is low).

In Phase four**,** the output power demands have increases and the feedback voltage rises above the 1.25 volts threshold, the NCP1230 exits the skip mode, and returns to normal operation.

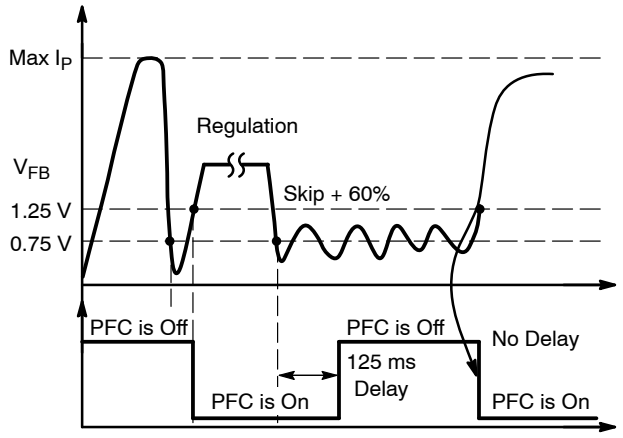


Figure 32.

Leaving Standby (Skip Mode)

When the feedback voltage rises above the 1.25 volts reference (leaving standby) the skip cycle activity stops and SW1 immediately closes and restarts the PFC, there is no delay in turning on SW1 under these conditions, refer to Figure 32.

Current Sense

The NCP1230 is a peak current mode controller, where the current sense input is internally clamped to 1.0 V, so the sense resister is determined by Rsense = 1.0 V /Ipk maximum.

There is a 18k resistor connected to the CS pin, the other end of the 18k resistor is connect to the output of the internal oscillator for ramp compensation (refer to Figure 33).

Ramp Compensation

In Switch Mode Power Supplies operating in Continuous Conduction Mode (CCM) with a duty−cycle greater than 50%, oscillation will take place at half the switching frequency. To eliminate this condition, Ramp Compensation can be added to the current sense signal to cure sub harmonic oscillations. To lower the current loop gain one typically injects between 50 and 100% of the inductor down slope.

The NCP1230 provides an internal 2.3 Vpp ramp which is summed internally through a 18 kΩ resistor to the current sense pin. To implement ramp compensation a resistor needs to be connected from the current sense resistor, to the current sense pin 3.

Example:

If we assume we are using the 65 kHz version of the NCP1230, at 65 kHz the dv/dt of the ramp is 130 mV/μs. Assuming we are designing a FLYBACK converter which has a primary inductance, Lp, of 350 μH, and the SMPS has a +12 V output with a Np:Ns ratio of 1:0.1. The OFF time primary current slope is given by:

$$\frac{(V_{out} + V_f) \cdot \frac{Ns}{Np}}{L_p} = 371 \text{ mA/μs or } 37 \text{ mV/μs}$$

when imposed on a current sense resistor (Rsense) of 0.1 Ω. If we select 75% of the inductor current downslope as our required amount of ramp compensation, then we shall inject 27 mV/μs.

With our internal compensation being of 130 mV, the divider ratio (*divratio*) between Rcomp and the 18 kΩ is 0.207. Therefore:

$$R_{comp} = \frac{18k \cdot divratio}{(1 - divratio)} = 4.69\ k\Omega$$

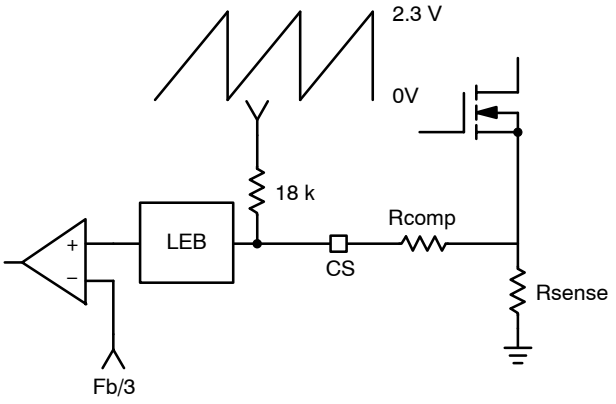


Figure 33.

Leading Edge Blanking

In Switch Mode Power Supplies (SMPS) there can be a large current spike at the beginning of the current ramp due to the Power Switch gate to source capacitance, transformer interwinding capacitance, and output rectifier recovery time. To prevent prematurely turning off the PWM drive output, a Leading Edges Blanking (LEB) (Figure 34) circuit is place is series with the current sense input, and PWM comparator. The LEB circuit masks the first 250 ns of the current sense signal.

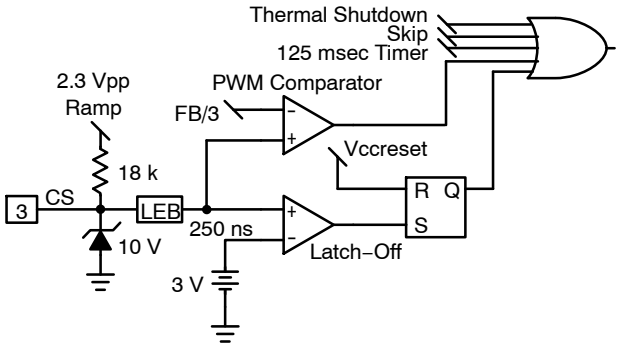


Figure 34.

Short−Circuit Condition

The NCP1230 is different from other controllers which use an auxiliary windings to detect events on the isolated secondary output. There maybe some conditions (for example when the leakage inductance is high) where it can be extremely difficult to implement short−circuit and overload protection. This occurs because when the power switch opens, the leakage inductance superimposes a large spike on the switch drain voltage. This spike is seen on the isolated secondary output and on the auxiliary winding. Because the auxiliary winding and diode form a peak rectifier, the auxiliary Vcc capacitor voltage can be charged up to the peak value rather than the true plateau which is proportional to the output level.

To resolve these issues the NCP1230 monitors the 1.0 V error flag. As soon as the internal 1.0 V error flag is asserted high, a 125 ms timer starts. If at the end of the 125 ms timeout period, the error flag is still asserted then the controller determines that there is a true fault condition and stops the PWM drive output, refer to Figure 35. When this occurs, Vcc starts to decrease because the power supply is locked out. When Vcc drops below UVLOlow (7.7 V typical), it enters a latch−off phase where the internal consumption is reduced down to 680 μA (typical). The voltage on the Vcc capacitor continues to drop, but at a lower rate. When Vcc reaches the latch−off level (5.6 V), the current source is turned on and pulls Vcc above UVLOhigh. To limit the fault output power, a divide−by−two circuit is connected to the Vcc pin that requires two startup sequences before attempting to restart the power supply. If the fault has gone and the error flag is low, the controller resumes normal operations.

Under transient load conditions, if the error flag is asserted, the error flag will normally drop prior to the 125 ms timeout period and the controller continues to operate normally.

If the 125 msec timer expires while the NCP1230 is in the Skip Mode, SW1 opens and the PFC_Vcc output will shut down and will not be activated until the fault goes away and the power supply resumes normal operations.

While in the Skip Mode, to avoid any thermal runaway it is desirable for the Burst duty cycle to be kept below 20%(the burst duty−cycle is defined as Tpulse / Tfault).

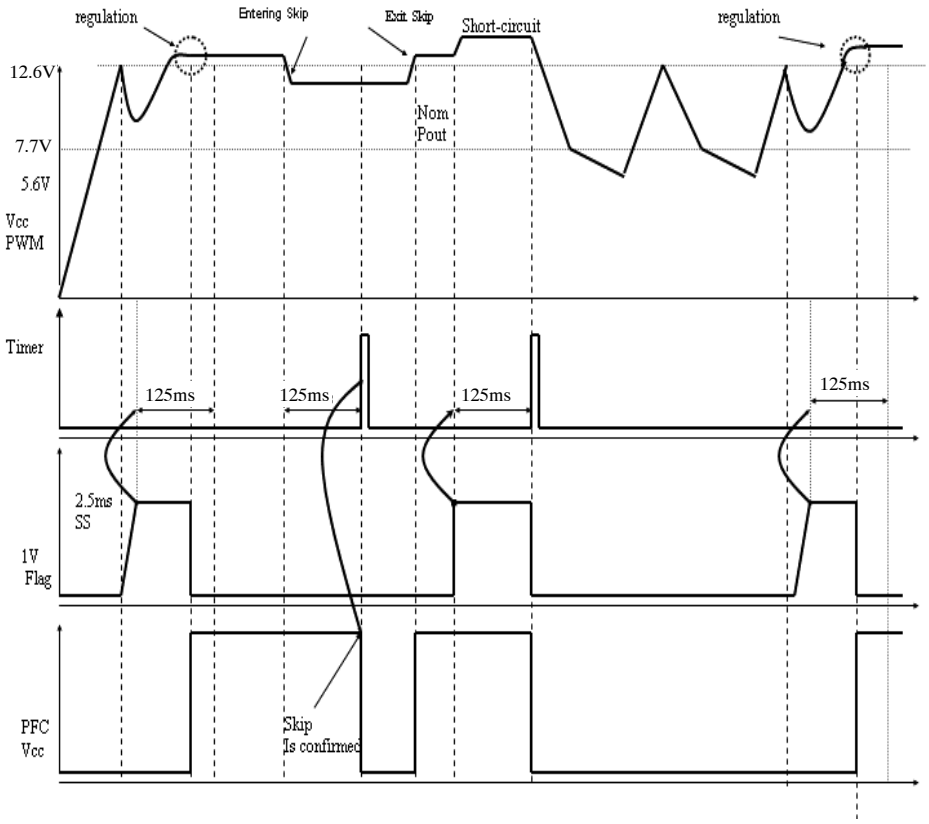


Figure 35.

The latch−off phase can also be initiated, more classically, when Vcc drops below UVLO (7.7 V typical). During this fault detection method, the controller will not wait for the 125 ms time−out, or the error flag before it goes into the latch−off phase, operating in the skip mode under these conditions, refer to Figure 36.

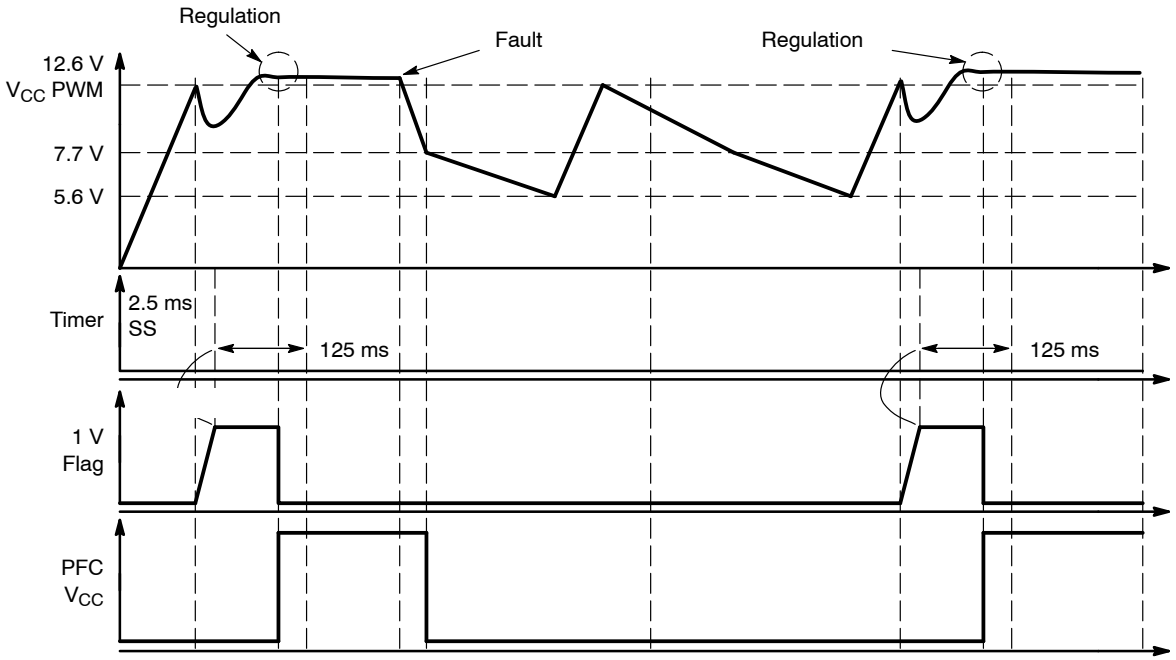


Figure 36.

Current Sense Input Pin Latch−Off

The NCP1230 features a fast comparator (Figure 34) that monitors the current sense pin during the controller off time. If for any reason the voltage on pin 3 increases above 3.0 V, the NCP1230 immediately stops the PWM drive pulses and permanently stays latched off until the bias supply to the NCP1230 is cycled down (Vcc must drop below 4.0 V, e.g. when the user unplugs the converter from the mains). This offers the designer the flexibility to implement an externally shutdown circuit (for example for overvoltage or overtemperature conditions). When the controller is latched off through pin 3 (current sense), SW1 opens and shuts off PFC_Vcc output.

Figure 37 shows how to implement the external latch via a Zener diode and a simple PNP transistor. The PNP actually samples the Zener voltage during the OFF time only, hence leaving the CS information un−altered during the ON time. Various component arrangements can be made, e.g. adding a NTC device for the Over Temperature Protection (OTP).

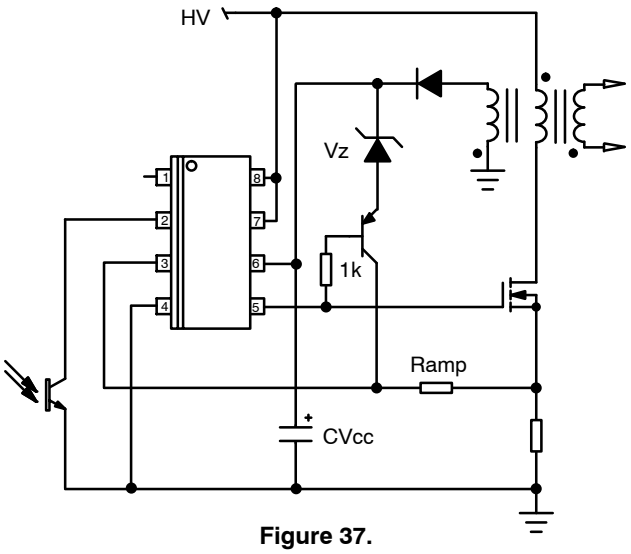


Figure 37.

Connecting the PNP to the drive only activates the offset generation during Toff. Here is a solution monitoring the auziliary Vcc rail.

Drive Output

The NCP1230 provides a Drive Output which can be connected through a current limiting resistor to the gate of a MOSFET. The Driver output is capable of delivering drive pulses with a rise time of 40 ns, and a fall time of 15 ns through its internal source and sink resistance of 12.3 ohms (typical), measured with a 1.0 nF capacitive load.

Startup Sequence

The NCP1230 has an internal High Voltage Startup Circuit (Pin 8) which is connected to the high voltage DC bus (Refer to Figure 36). When power is applied to the bus, the NCP1230 internal current source (typically 3.2 mA) is biased and charges up the external Vcc capacitor on pin 6, refer to Figure 38. When the voltage on pin 6 (Vcc) reaches Vccoff (12.6 V typically), the current source is turned off reducing the amount of power being dissipated in the chip. The NCP1230 then turns on the drive output to the external MOSFET in an attempt to increase the output voltage and charge up the Vcc capacitor through the Vaux winding in the transformer.

During the startup sequence, the controller pushes for the maximum peak current, which is reached after the 2.5 ms soft−start period. As soon as the maximum peak set point is reached, the internal 1.0 V Zener diode actively limits the current amplitude to 1.0 V/Rsense and asserts an error flag indicating that a maximum current condition is being observed. In this mode, the controller must determine if it is a normal startup period (or transient load) or is the controller is facing a fault condition. To determine the difference between a normal startup sequence, and a fault condition, the error flag is asserted, and the 125 ms timer starts to count down. If the error flag drops prior to the 125 ms time−out period, the controller resets the timer and determines that it was a normal startup sequence and enables the low impedance switch (SW1), enabling the PFC_Vcc output.

If at the end of the 125 ms period the error flag is still asserted, then the controller assumes that it is a fault condition and the PWM controller enters the skip mode and does not enable the PFC_Vcc output.

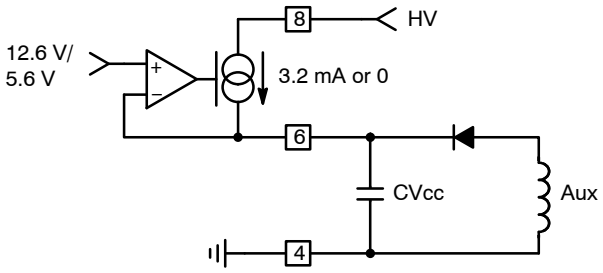


Figure 38.

ON Semiconductor recommends that the Vcc capacitor be at least 47 μF to be sure that the Vcc supply voltage does not drop below Vccmin (7.7 V typical) during standby power mode and unusual fault conditions.

Soft−Start

The NCP1230 features an internal 2.5 ms soft−start circuit. As soon as Vcc reaches a nominal 12.6 V, the soft−start circuit is activated. The soft−start circuit output controls a reference on the minus (−) input to an amplifier (refer to Figure 39), the positive (+) input to the amplifier is the feedback input (divided by 3). The output of the amplifier drives a FET which clamps the feedback signal. As the soft−start circuit output ramps up, it allow the feedback pin input to the PWM comparator to gradually increased from near zero up to the maximum clamping level of 1.0 V/Rsense. This occurs over the entire 2.5 ms soft−start period until the supply enters regulation. The soft−start is also activated every time a restart is attempted. Figure 40 shows a typical soft−start up sequence.

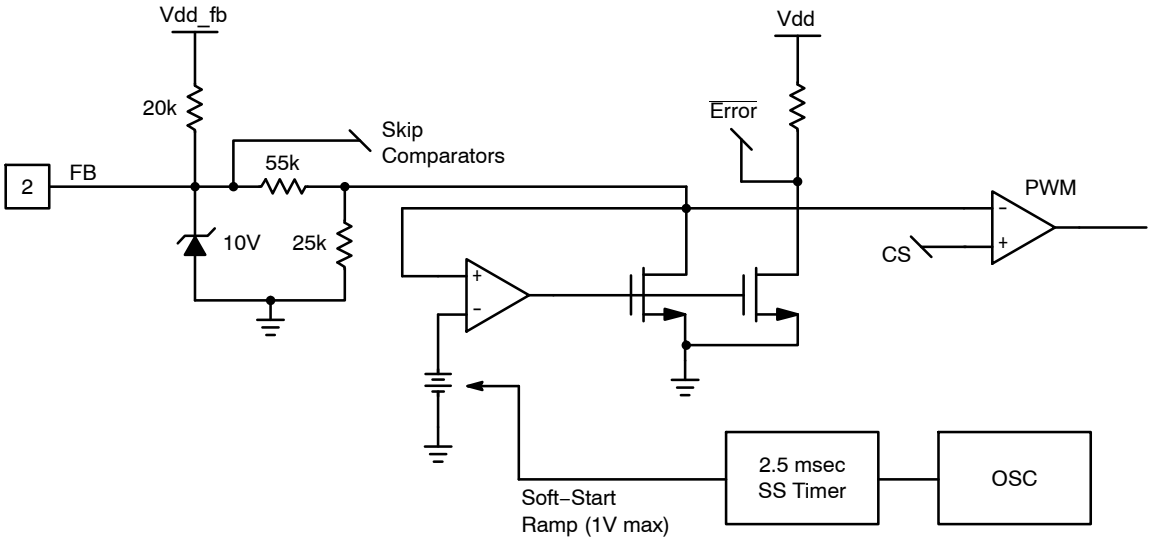


Figure 39.

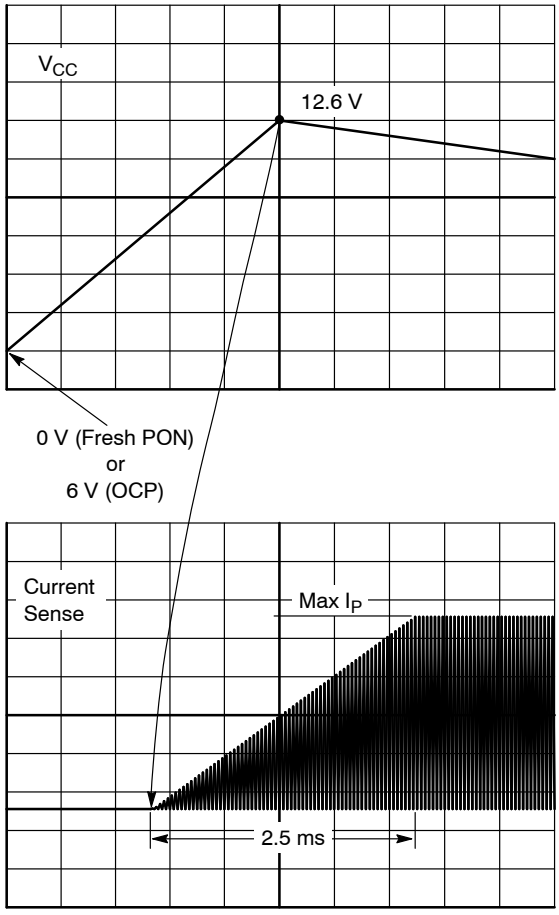


Figure 40. Soft−Start is Activated during a Startup Sequence or an OCP Condition

Frequency Jittering

Frequency jittering is a method used to soften the EMI signature by spreading out the average switching energy around the controller operating switching frequency. The NCP1230 offers a nominal ±6.4% deviation of the nominal switching frequency. The sweep sawtooth is internally generated and modulates the clock up and down with a 5 ms period. Figure 41 illustrates the NCP1230 behavior:

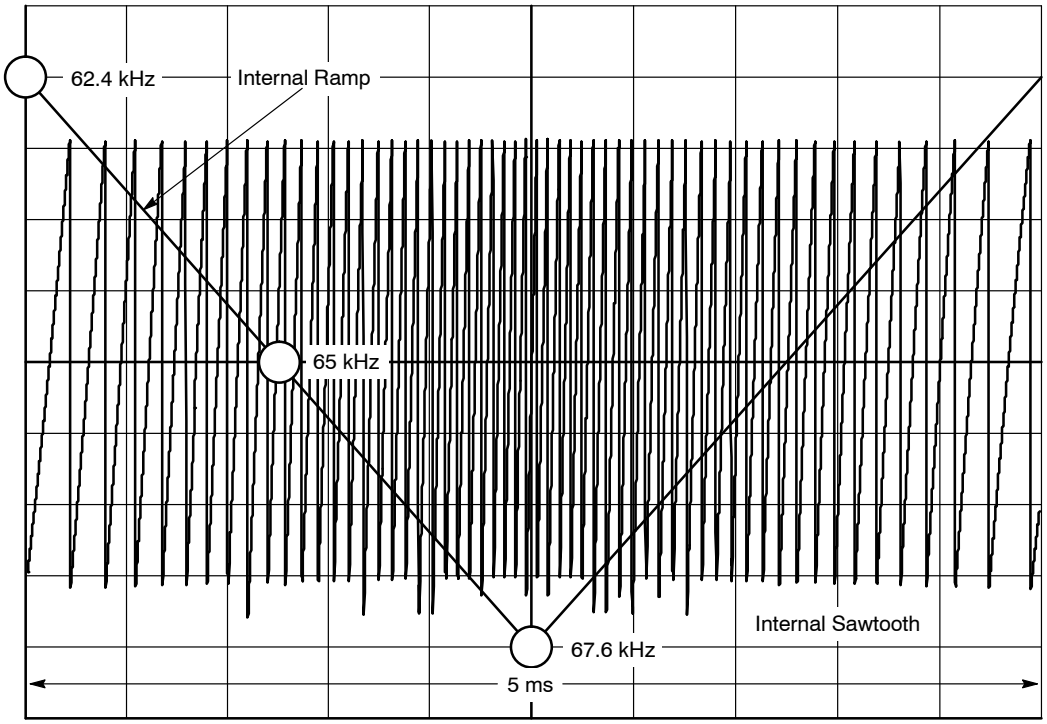


Figure 41. An Internal Ramp is used to Introduce Frequency Jittering on the Oscillator Saw Tooth

Thermal Protection

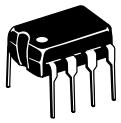
An internal Thermal Shutdown is provided to protect the integrated circuit in the event that the maximum junction temperature is exceeded. When activated (165°C typically) the controller turns off the PWM Drive Output. When this occurs, Vcc will drop (the rate is dependent on the NCP1230 loading and the size of the Vcc capacitor) because the controller is no longer delivering drive pulses to the auxiliary winding charging up the Vcc capacitor. When Vcc drops below 4.0 volts and the Vccreset circuit is activated, the controller will restart. If the user is using a fixed bias supply (the bias supply is provided from a source other than from an auxiliary winding, refer to the typical application) and Vcc is not allow to drop below 4.0 volts under a thermal shutdown condition, the NCP1230 will not restart. This feature is provided to prevent catastrophic failure from accidentally overheating the device.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

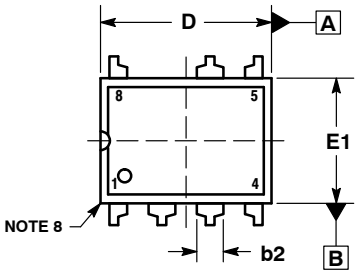
ON Semiconductor®

PDIP−7 (PDIP−8 LESS PIN 7)
CASE 626B
ISSUE D

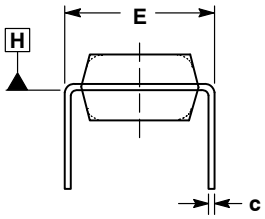
DATE 22 APR 2015



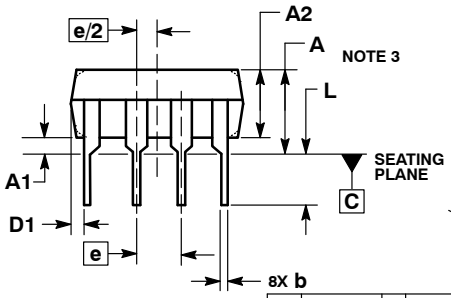
SCALE 1:1



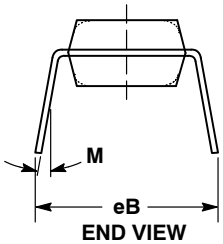
TOP VIEW



END VIEW
WITH LEADS CONSTRAINED
NOTE 5



SIDE VIEW



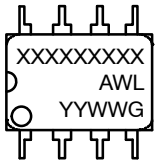
END VIEW
NOTE 6

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. NOT USED
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	PDIP−7 (PDIP−8 LESS PIN 7)	PAGE 1 OF 1

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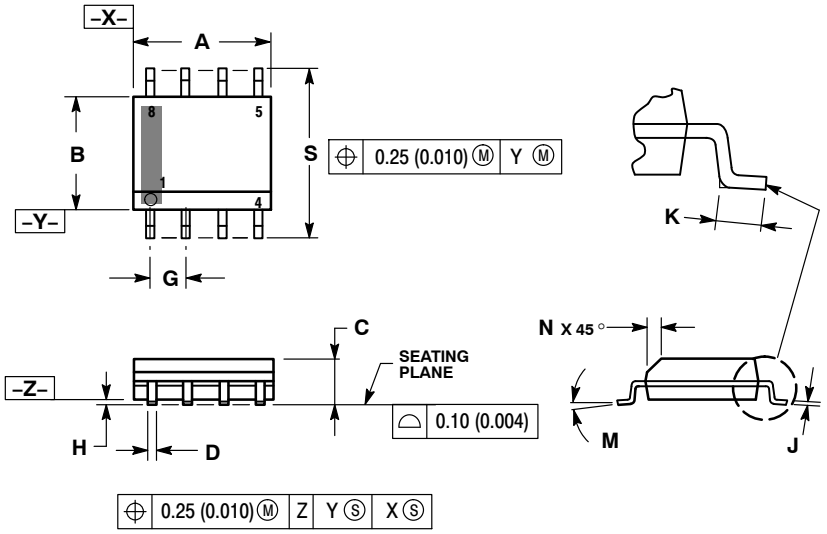
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

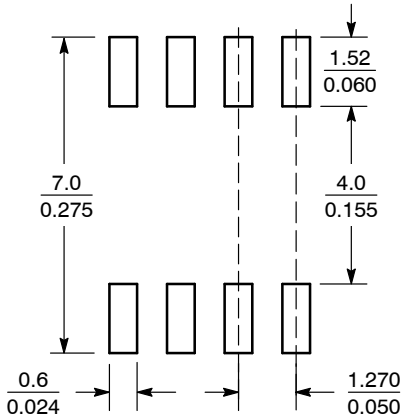
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

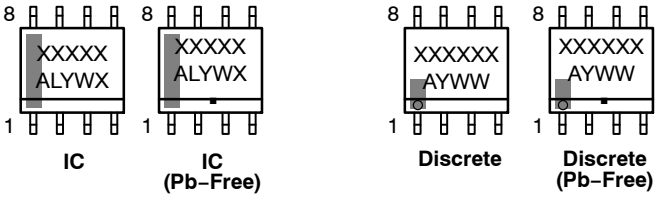
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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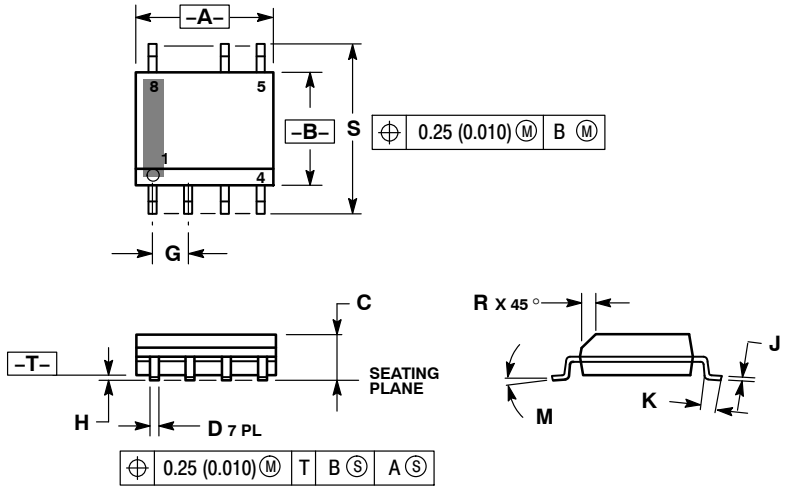
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

SOIC−7
CASE 751U
ISSUE E

DATE 20 OCT 2009



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B ARE DATUMS AND T IS A DATUM SURFACE.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
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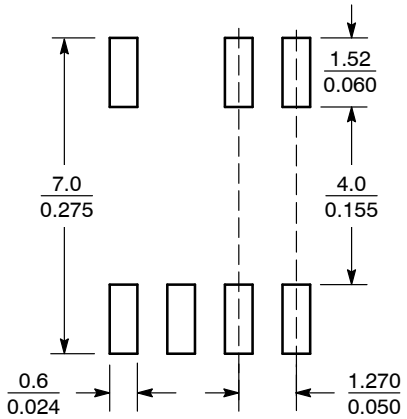
S	5.80	6.20	0.228	0.244

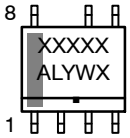
SOLDERING FOOTPRINT*



SCALE 6:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM



XXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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DESCRIPTION:	**SOIC−7**		**PAGE 1 OF 2**

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SOIC−7
CASE 751U
ISSUE E

DATE 20 OCT 2009

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6.
7. NOT USED
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. NOT USED
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. NOT USED
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. NOT USED
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5.
6.
7. NOT USED
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6.
7. NOT USED
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. NOT USED
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR (DIE 1)
2. BASE (DIE 1)
3. BASE (DIE 2)
4. COLLECTOR (DIE 2)
5. COLLECTOR (DIE 2)
6. EMITTER (DIE 2)
7. NOT USED
8. COLLECTOR (DIE 1)

STYLE 9:
PIN 1. EMITTER (COMMON)
2. COLLECTOR (DIE 1)
3. COLLECTOR (DIE 2)
4. EMITTER (COMMON)
5. EMITTER (COMMON)
6. BASE (DIE 2)
7. NOT USED
8. EMITTER (COMMON)

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. NOT USED
8. GROUND

STYLE 11:
PIN 1. SOURCE (DIE 1)
2. GATE (DIE 1)
3. SOURCE (DIE 2)
4. GATE (DIE 2)
5. DRAIN (DIE 2)
6. DRAIN (DIE 2)
7. NOT USED
8. DRAIN (DIE 1)

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