NCP1255

Current-Mode PWM Controller for Off-line Power Supplies featuring Peak Power Excursion

The NCP1255 is a highly integrated PWM controller capable of delivering a rugged and high performance offline power supply in a SOIC−8 package. With a supply range up to 35 V, the controller hosts a jittered 65−kHz switching circuitry operated in peak current mode control. When the power on the secondary side starts to decrease, the controller automatically folds back its switching frequency down to a minimum level of 26 kHz. As the power further goes down, the part enters skip cycle while freezing the peak current setpoint.

To help build rugged converters, the controller features several key protective features: a brown−out, a non−dissipative Over Power Protection for a constant maximum output current regardless of the input voltage, two latched over voltage protection inputs − either through a dedicated pin or via the V_{CC} input − and finally, the possibility to externally adjust an auto−recovery timer duration.

The controller architecture is arranged to authorize a transient peak power excursion when the peak current hits the limit. At this point, the switching frequency is increased from 65 kHz to 130 kHz until the peak requirement disappears. The timer duration is then modulated as the converter crosses a peak power excursion mode (long) or undergoes a short circuit (short).

Features

- 65−kHz Fixed−frequency Current−mode Control Operation with 130−kHz Excursion
- Internal and Adjustable Over Power Protection (OPP) Circuit
- Adjustable Brown−Out Protection Circuit
- Frequency Foldback down to 26 kHz and Skip−cycle in Light Load Conditions
- Adjustable Slope Compensation
- Internally Fixed 4−ms Soft−start
- Adjustable Timer−based Auto−recovery Overload/Short−circuit Protection
- 100% to 25% Timer Reduction from Overload to Short−circuit Fault
- Double V_{CC} Hiccup for a Reduced Average Power in Fault Mode
- Frequency Jittering in Normal and Frequency Foldback Modes
- Latched OVP Input for Improved Robustness and Latched OVP on V_{CC}
- Up to 35−V V_{CC} Maximum Rating
- Extremely Low No−load Standby Power
- This is a Pb−Free Device

Typical Applications

- Converters requiring peak−power capability such as printers power supplies, ac−dc adapters for game stations.

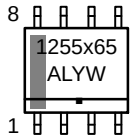
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SOIC−8
D1, D2 SUFFIX
CASE 751

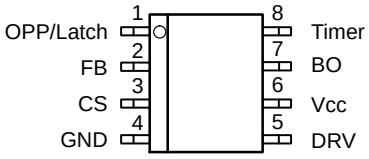
MARKING DIAGRAM



1255x65 = Specific Device Code
x = A, B, C or D
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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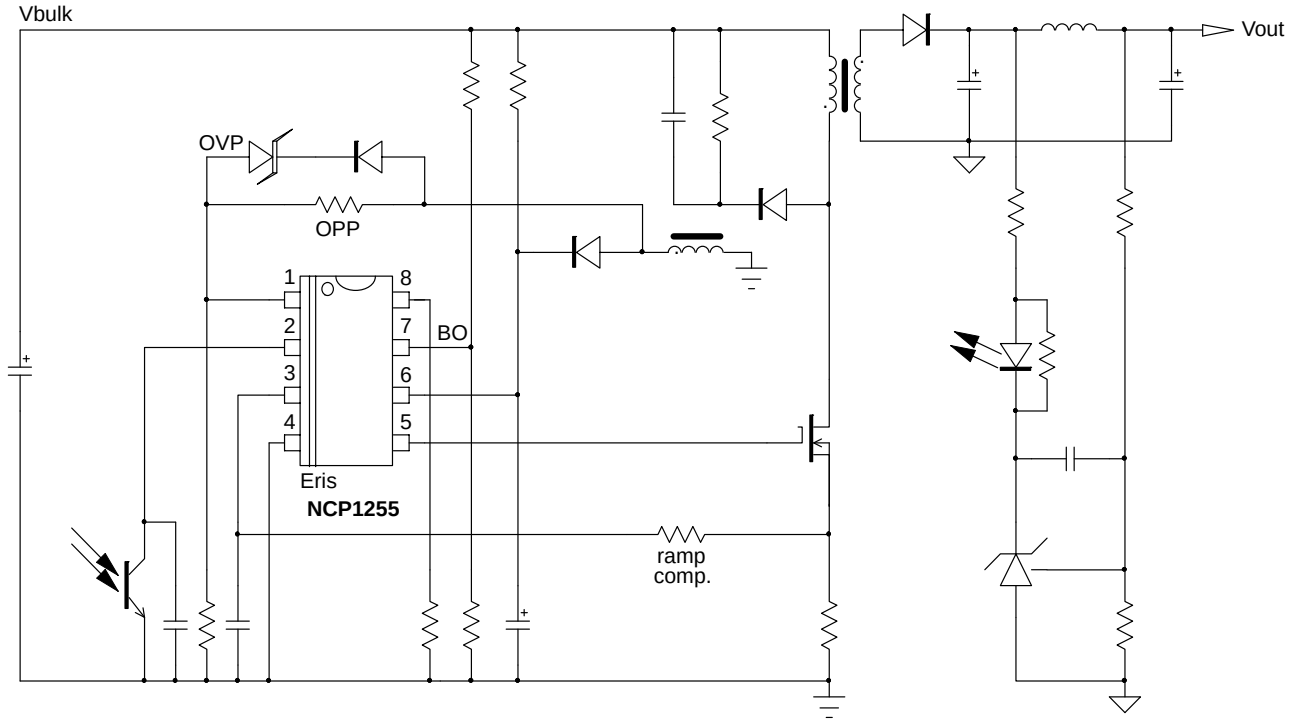


Figure 1. Typical Application Example

Table 1. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1	OPP/OVP	Adjust the Over Power Protection. Latches off the part	A resistive divider from the auxiliary winding to this pin sets the OPP compensation level. When brought above 3 V, the part is fully latched off.
2	FB	Feedback pin	Hooking an optocoupler collector to this pin will allow regulation.
3	CS	Current sense + ramp compensation	This pin monitors the primary peak current but also offers a means to introduce ramp compensation.
4	GND	−	The controller ground.
5	DRV	Driver output	The driver's output to an external MOSFET gate.
6	V_{cc}	Supplies the controller	This pin is connected to an external auxiliary voltage and supplies the controller. When above a certain level, the part fully latches off.
7	BO	Brown−Out input	A voltage below the programmed level stops the controller. When above, the controller can start.
8	Timer	Sets the timer duration	A 22−kΩ resistor sets the duration to 200 ms. When shorted to ground or made open, this pin limits the internal current and fixes the timer duration.

Table 2. ORDERING INFORMATION AND OPTIONS

Controller	Frequency	OCP Latched	OCP Auto−Recovery	V_{BOoff} (V)	Package	Shipping†
NCP1255AD65R2G	65 kHz	Yes	No	0.6	SOIC−8 (Pb−Free)	2500 / Tape & Reel
NCP1255BD65R2G	65 kHz	No	Yes	0.6		
NCP1255CD65R2G	65 kHz	Yes	No	0.7		
NCP1255DD65R2G	65 kHz	No	Yes	0.7		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

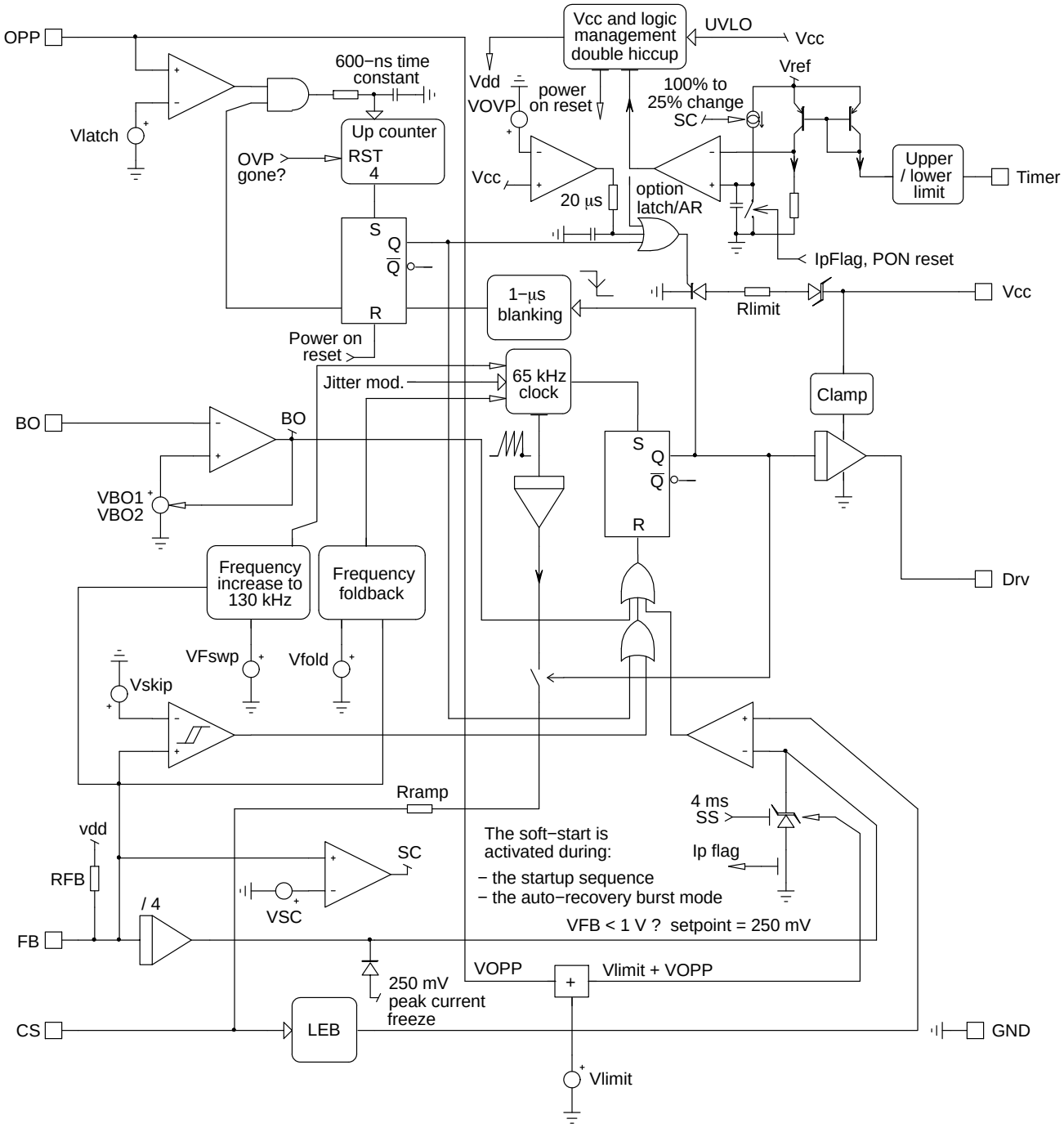


Figure 2. Internal Circuit Architecture

Table 3. MAXIMUM RATINGS TABLE

Symbol	Rating	Value	Unit
V_{cc}	Power Supply voltage, V_{cc} pin, continuous voltage	−0.3 to 35	V
	Maximum voltage on low power pins CS, FB, Timer, OPP and BO	−0.3 to 10	V
V_{DRV}	Maximum voltage on drive pin	−0.3 to V_{cc}+0.3	V
IOPP	Maximum injected current into the OPP pin	−2	mA
I_{SCR}	Maximum continuous current into the V_{cc} pin while in latched mode	3	mA
$R_{\theta J-A}$	Thermal Resistance Junction−to−Air	178	°C/W
$T_{J,max}$	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	−60 to +150	°C
HBM	Human Body Model ESD Capability (All pins except HV) per JEDEC JESD22−A114F	2	kV
MM	Machine Model ESD Capability (All pins except DRV) per JEDEC JESD22−A115C	200	V
CDM	Charged−Device Model ESD Capability per JEDEC JESD22−C101E	500	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. This device contains latch−up protection and exceeds 100 mA per JEDEC Standard JESD78.

Table 4. ELECTRICAL CHARACTERISTICS

(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{cc} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
SUPPLY SECTION						
VCC_{ON}	V_{CC} increasing level at which driving pulses are authorized	6	15.8	18	20	V
$VCC_{(min)}$	V_{CC} decreasing level at which driving pulses are stopped	6	8	8.8	9.4	V
VCC_{HYST}	Hysteresis Vcc_{ON}−$Vcc_{(min)}$	6	6	−	−	V
V_{ZENER}	Clamped V_{cc} when latched off @ ICC = 500 μA	6	−	7	−	V
ICC1	Start−up current	6	−	−	15	μA
ICC2	Internal IC consumption with V_{FB} = 3.2 V, F_{SW} = 65 kHz and C_L = 0	6	−	1.4	2.2	mA
ICC3	Internal IC consumption with V_{FB} = 3.2 V, F_{SW} = 65 kHz and C_L = 1 nF	6	−	2.1	3.0	mA
ICC4	Internal IC consumption with V_{FB} = 4.5 V, F_{SW} = 130 kHz and C_L = 0	6	−	1.7	2.5	mA
ICC5	Internal IC consumption with V_{FB} = 4.5 V, F_{SW} = 130 kHz and C_L = 1 nF	6	−	3.1	4.0	mA
ICCstby	Internal IC consumption while in skip mode (V_{cc} = 12 V, driving a typical 6−A/600−V MOSFET)	6		750		μA
ICC_{LATCH}	Current flowing into V_{CC} pin that keeps the controller latched: T_j = −40°C to 125°C	6	40			μA
R_{lim}	SCR current−limit series resistor	6		4		kΩ
DRIVE OUTPUT						
T_r	Output voltage rise−time @ CL = 1 nF, 10−90% of output signal	5	−	40	−	ns
T_f	Output voltage fall−time @ CL = 1 nF, 10−90% of output signal	5	−	30	−	ns
R_{OH}	Source resistance	5	−	13	−	Ω
R_{OL}	Sink resistance	5	−	6	−	Ω
I_{source}	Peak source current, V_{GS} = 0 V – (Note 2)	5		300		mA
I_{sink}	Peak sink current, V_{GS} = 12 V – (Note 2)	5		500		mA
V_{DRVlow}	DRV pin level at V_{CC} close to $VCC_{(min)}$ with a 33−kΩ resistor to GND	5	8	−	−	V

2. Guaranteed by design
3. See characterization table for linearity over negative bias voltage – we recommend keeping the level on pin 3 below −300 mV.
4. A 1−MΩ resistor is connected from pin 3 to the ground for the measurement.

Table 4. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{cc} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
DRIVE OUTPUT						
$V_{DRVhigh}$	DRV pin level at V_{CC}= V_{OVP}−0.2 V – DRV unloaded	5	10	12	14	V
CURRENT COMPARATOR						
I_{IB}	Input Bias Current @ 0.8 V input level on pin 3	3		0.02		μA
V_{Limit1}	Maximum internal current setpoint – Tj = 25°C – pin1 grounded	3	0.744	0.8	0.856	V
V_{Limit2}	Maximum internal current setpoint – Tj from −40° to 125°C – pin 1 grounded	3	0.72	0.8	0.88	V
V_{foldI}	Default internal voltage set point for frequency foldback trip point ≈ 59% of V_{limit}	3		475		mV
$V_{freezeI}$	Internal peak current setpoint freeze (≈31% of V_{limit})	3		250		mV
T_{DEL}	Propagation delay from current detection to gate off−state	3		100	150	ns
T_{LEB}	Leading Edge Blanking Duration	3		300		ns
TSS	Internal soft−start duration activated upon startup, auto−recovery	−		4		ms
IOPPo	Setpoint decrease for pin 3 biased to –250 mV – (Note 3)	3		31.3		%
IOOPv	Voltage setpoint for pin 1 biased to −250 mV – (Note 3), T_j = 25°C	3	0.51	0.55	0.6	V
IOOPv	Voltage setpoint for pin 1 biased to −250 mV – (Note 3), T_j from −40° to 125°C	3	0.5	0.55	0.62	V
IOPPs	Setpoint decrease for pin 1 grounded	3		0		%
INTERNAL OSCILLATOR						
$f_{OSC,nom}$	Oscillation frequency, V_{FB} < $V_{Fbtrans}$, pin 1 grounded	−	61	65	71	kHz
$V_{FBtrans}$	Feedback voltage above which F_{sw} increases	−		3.2		V
$f_{OSC,max}$	Maximum oscillation frequency for V_{FB} above V_{FBmax}	−	120	130	140	kHz
V_{FBmax}	Feedback voltage above which F_{sw} is constant	−	3.8	4.1	4.2	V
D_{max}	Maximum duty ratio	−	76	80	84	%
f_{jitter}	Frequency jittering in percentage of f_{OSC}	−		±5		%
f_{swing}	Swing frequency over the whole frequency range	−		240		Hz
FEEDBACK SECTION						
R_{up}	Internal pull−up resistor	2		15		kΩ
R_{eq}	Equivalent ac resistor from FB to gnd	2		13		kΩ
I_{ratio}	Pin 2 to current setpoint division ratio	−		4		
$V_{freezeF}$	Feedback voltage below which the peak current is frozen	2		1		V
FREQUENCY FOLDBACK						
V_{foldF}	Frequency foldback level on the feedback pin – ≈59% of maximum peak current	−		1.9		V
F_{trans}	Transition frequency below which skip−cycle occurs	−	22	26	30	kHz
$V_{fold,end}$	End of frequency foldback feedback level, F_{sw} = F_{min}			1.5		V
V_{skip}	Skip−cycle level voltage on the feedback pin	−		400		mV
Skip hysteresis	Hysteresis on the skip comparator – (Note 2)	−		30		mV
INTERNAL SLOPE COMPENSATION						
V_{ramp}	Internal ramp level @ 25°C – (Note 4)	3		2.5		V

2. Guaranteed by design
3. See characterization table for linearity over negative bias voltage – we recommend keeping the level on pin 3 below −300 mV.
4. A 1−MΩ resistor is connected from pin 3 to the ground for the measurement.

Table 4. ELECTRICAL CHARACTERISTICS
(For typical values T_J = 25°C, for min/max values T_J = −40°C to +125°C, Max T_J = 150°C, V_{cc} = 12 V unless otherwise noted)

Symbol	Rating	Pin	Min	Typ	Max	Unit
INTERNAL SLOPE COMPENSATION						
R_{ramp}	Internal ramp resistance to CS pin	3		20		kΩ
PROTECTIONS						
V_{latch}	Latching level input	1	2.7	3	3.3	V
$T_{latch-blank}$	Blanking time after drive turn off	1		1		μs
$T_{latch-count}$	Number of clock cycles before latch confirmation	–		4		
$T_{latch-del}$	OVP detection time constant	1		600		ns
V_{OVL}	Feedback voltage beyond which an overload is considered	2		3.2		V
V_{SC}	Feedback voltage beyond which a short−circuit – OPP pin is grounded	2	3.9	4.1	4.3	V
$Timer_1$	Fault timer duration for a 22−kΩ resistor from pin 8 to ground − overload	8	350	500	650	ms
$Timer_2$	Fault timer duration when V_{FB} > 4.1 V is $Timer_1/4$ – short−circuit condition	8	88	125	162	ms
$Timer_{fault1}$	Timer duration when pin 8 is shorted to ground – fault condition	8		50		ms
$Timer_{fault1}$	Timer duration when pin 8 is open – fault condition	8		1000		ms
I_{BO}	Brown−Out input bias current	7		0.02		μA
V_{BOon}	Turn−on voltage – T_J = 25°C	7	0.76	0.8	0.85	V
V_{BOoff}	Turn−off voltage – T_J = 25°C, NCP1255A/B	7	0.57	0.6	0.63	V
V_{BOoff}	Turn−off voltage – T_J = 25°C, NCP1255C/D	7	0.66	0.7	0.74	V
V_{OVP}	Latched Over voltage protection on the V_{cc} rail	6	30.7	32.3	34	V
T_{OVP}−del	Delay before OVP on V_{cc} confirmation	6		20		μs

2. Guaranteed by design
3. See characterization table for linearity over negative bias voltage – we recommend keeping the level on pin 3 below −300 mV.
4. A 1−MΩ resistor is connected from pin 3 to the ground for the measurement.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

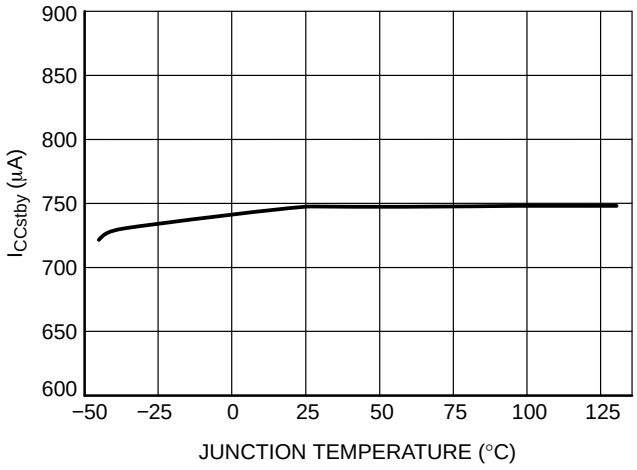


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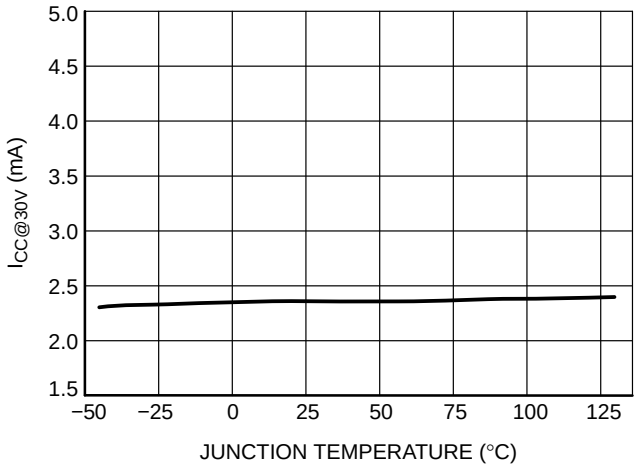


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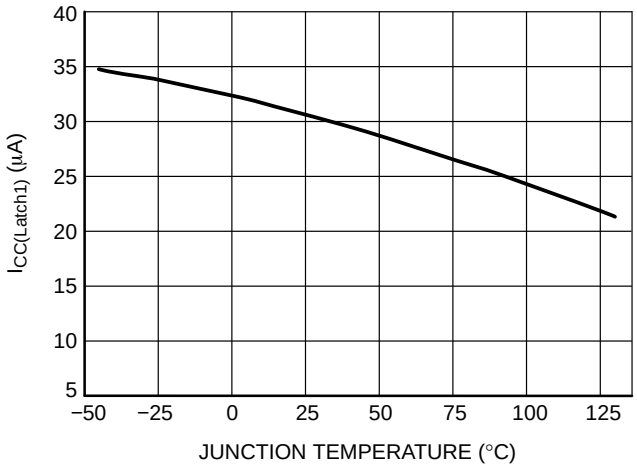


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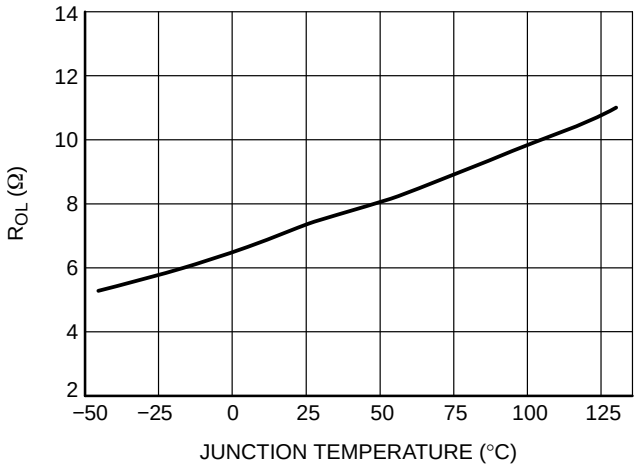


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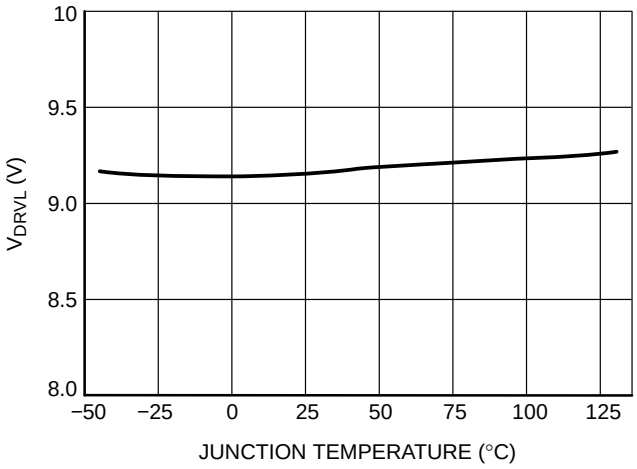


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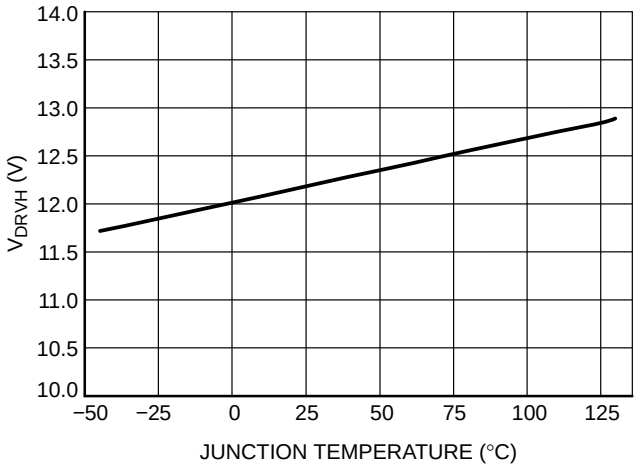


Figure 8.

TYPICAL CHARACTERISTICS

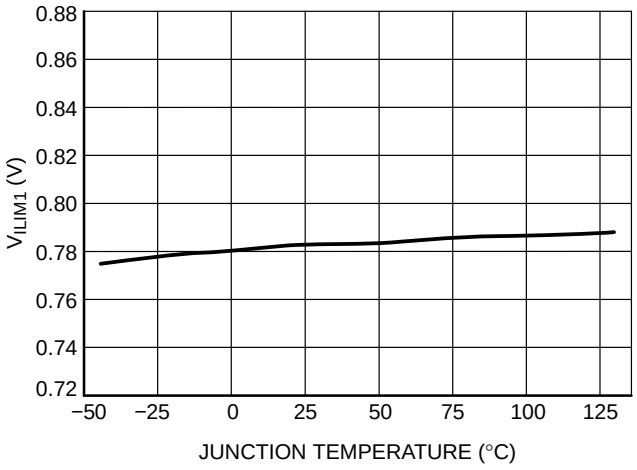


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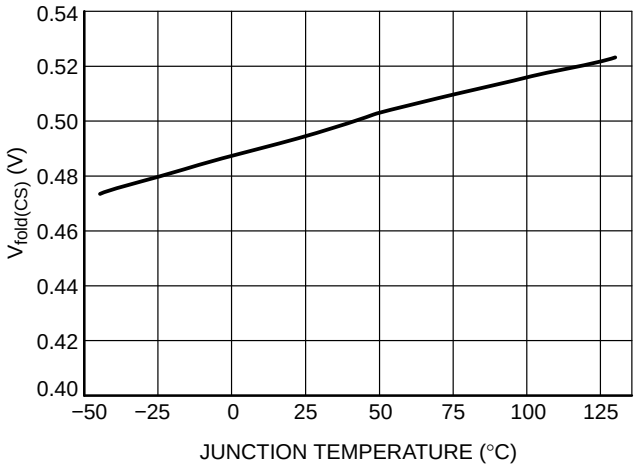


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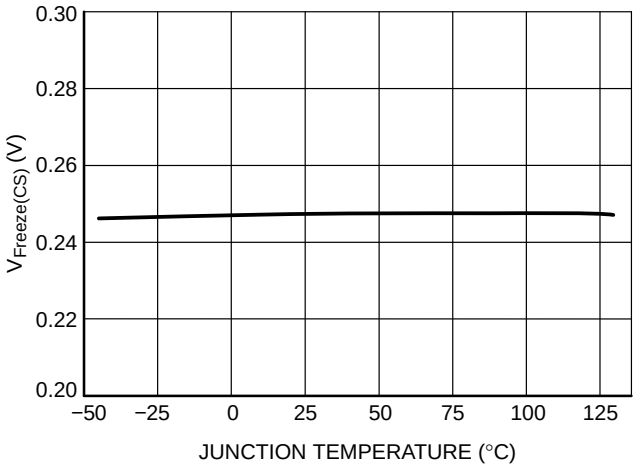


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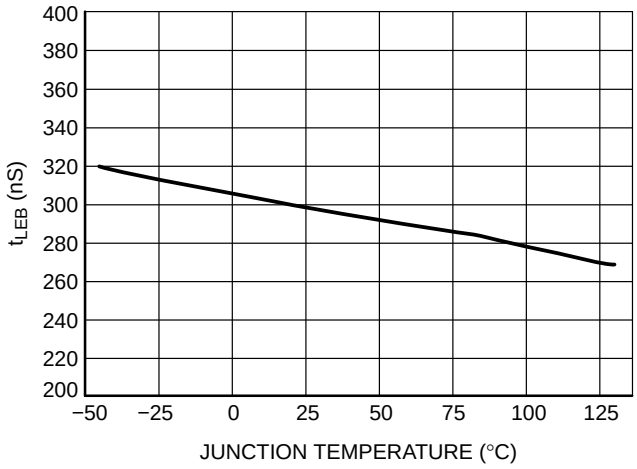


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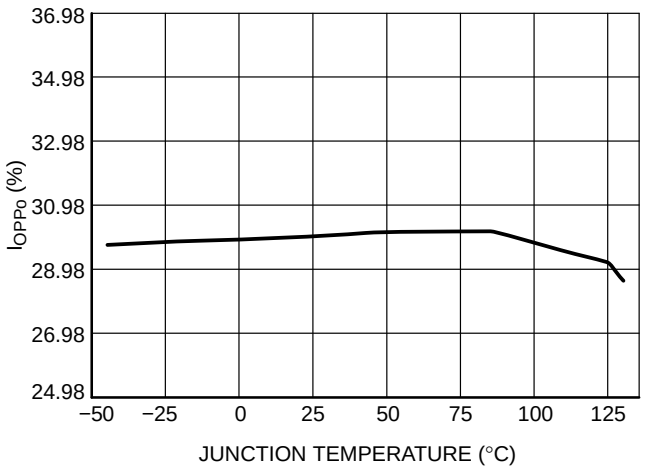


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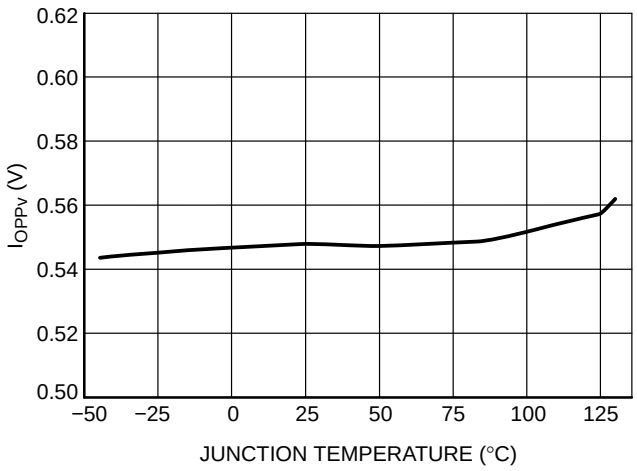


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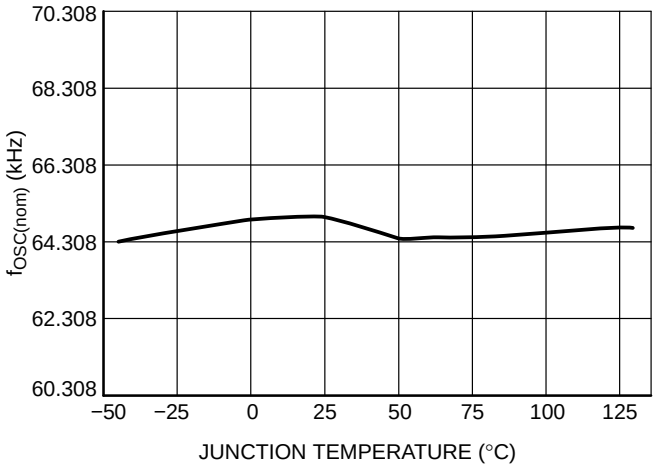


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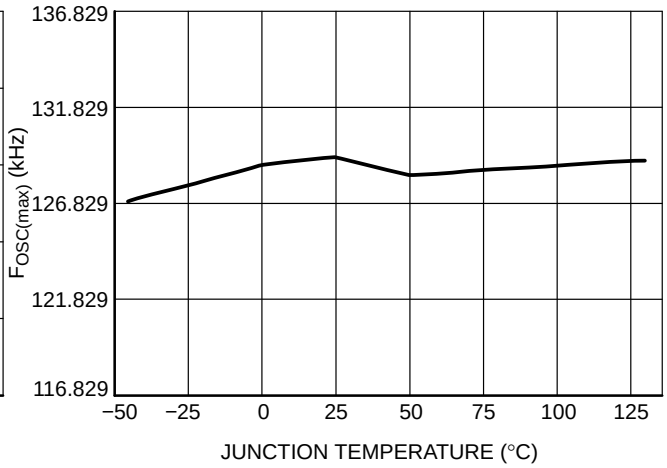


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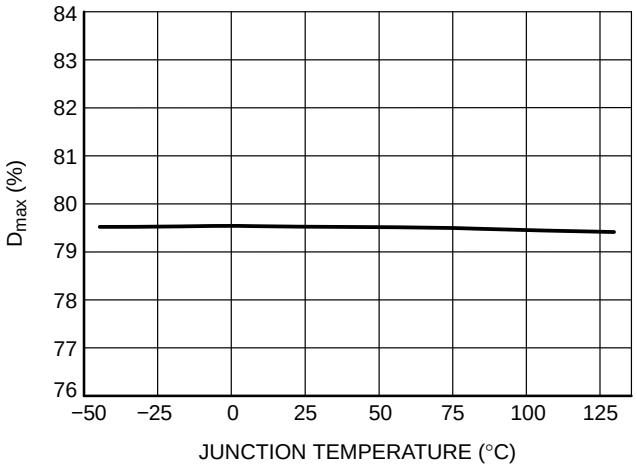


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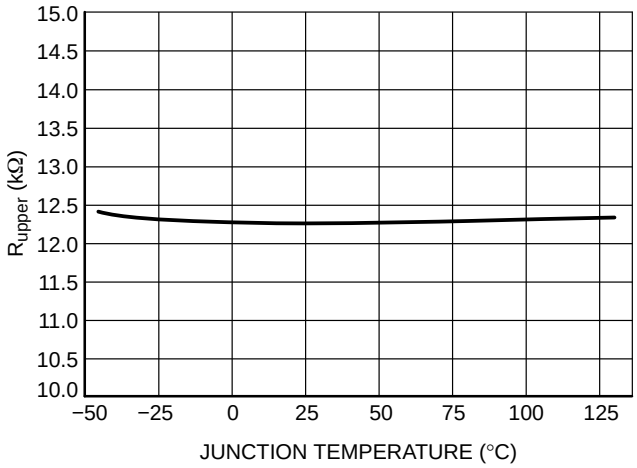


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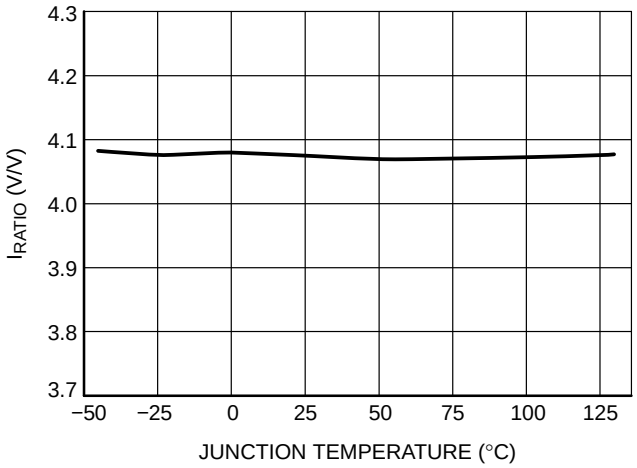


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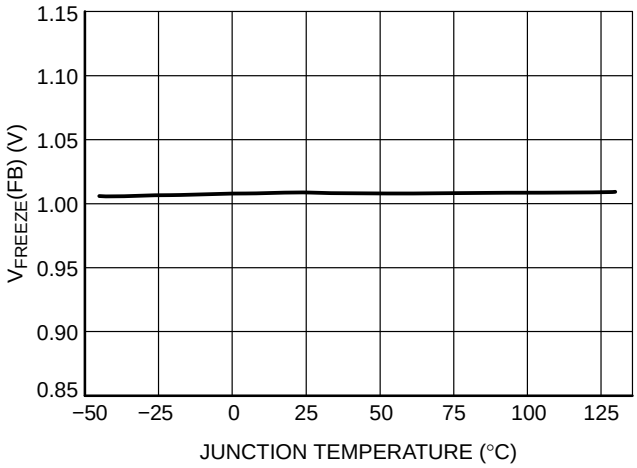


Figure 20.

TYPICAL CHARACTERISTICS

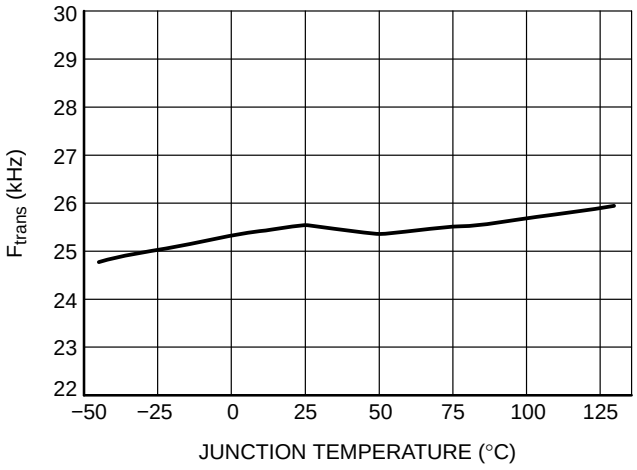


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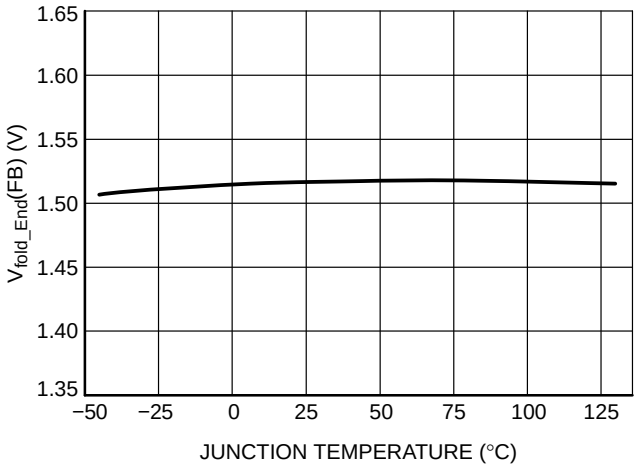


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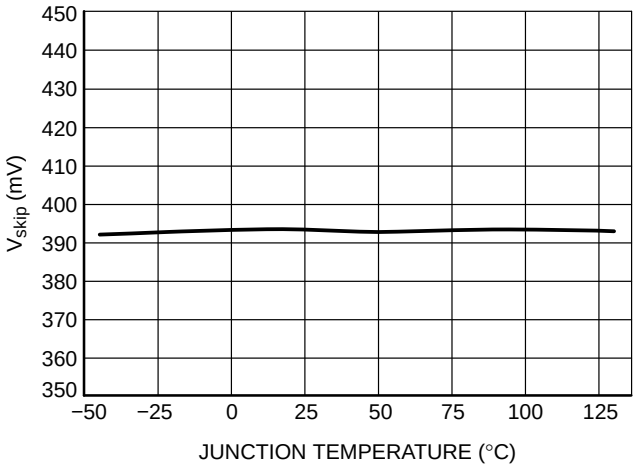


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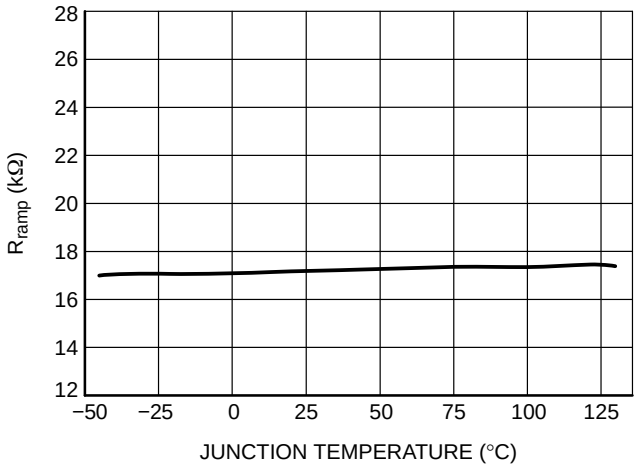


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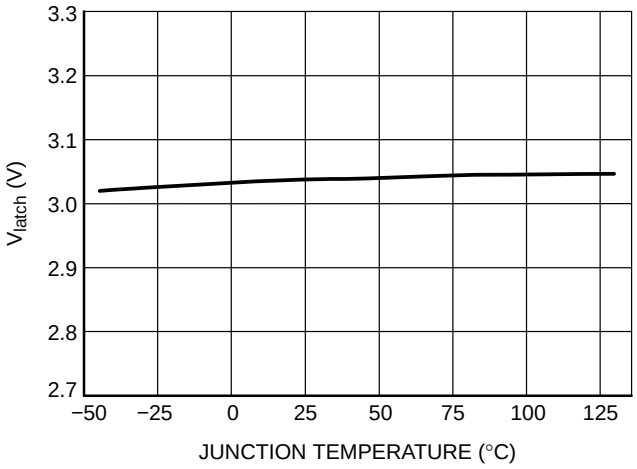


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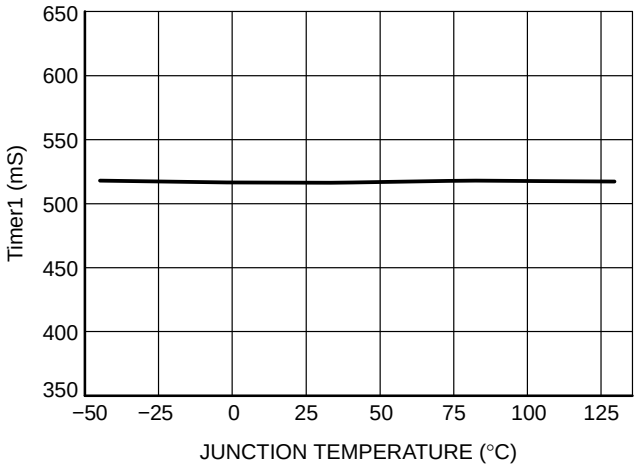


Figure 26.

TYPICAL CHARACTERISTICS

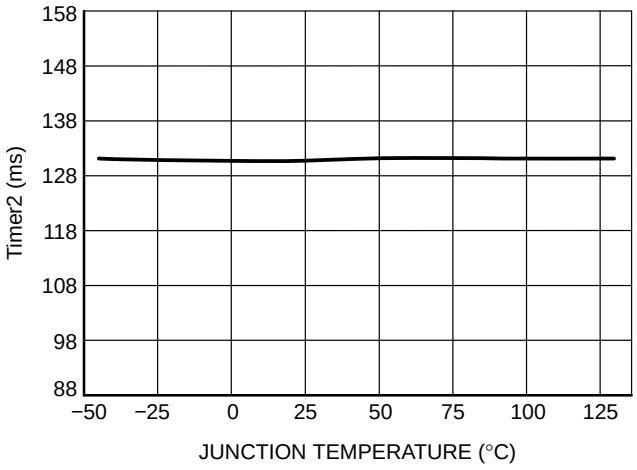


Figure 27.

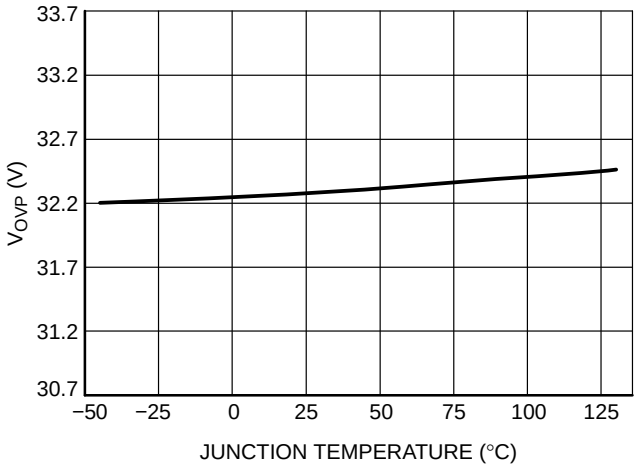


Figure 28.

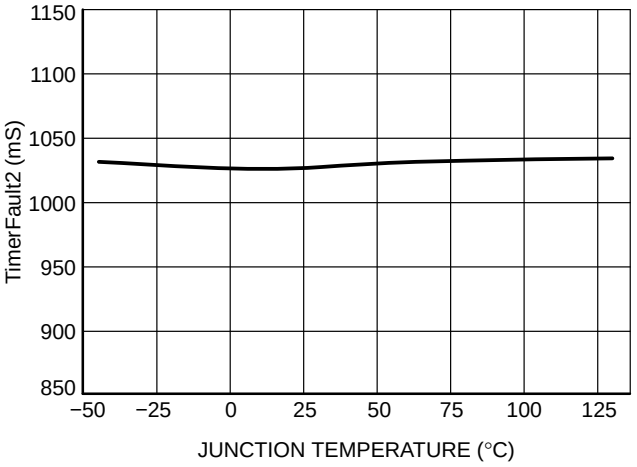


Figure 29.

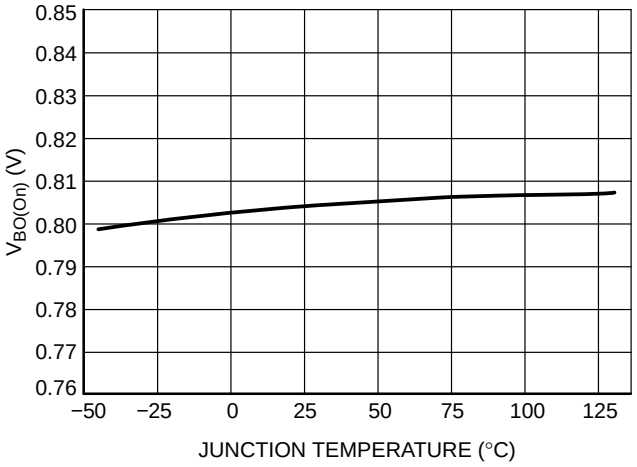


Figure 30.

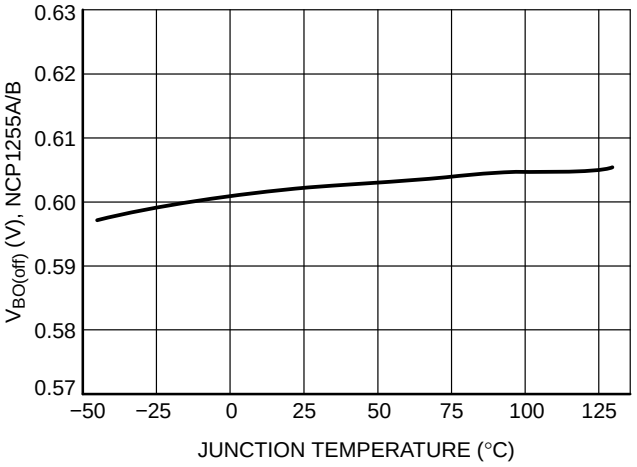


Figure 31.

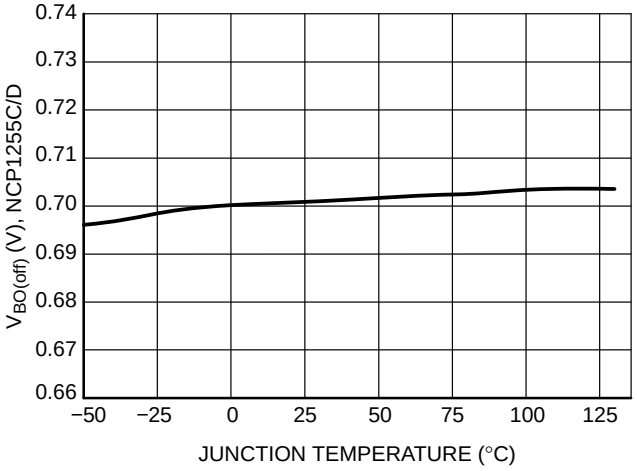


Figure 32.

TYPICAL CHARACTERISTICS

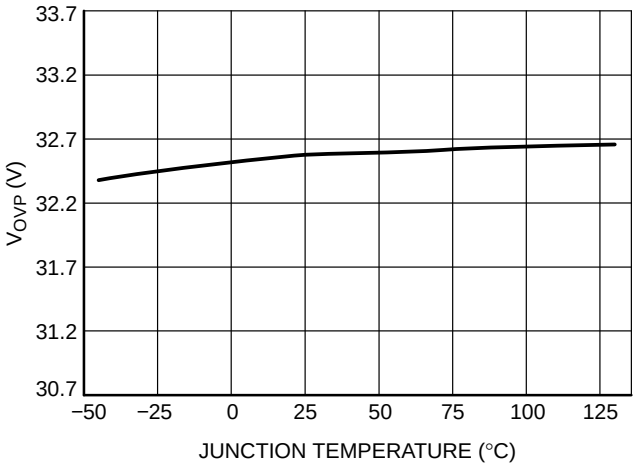


Figure 33.

APPLICATION INFORMATION

Introduction

The NCP1255 implements a standard current mode architecture where the switch−off event is dictated by the peak current setpoint. This component represents the ideal candidate where low part−count and cost effectiveness are the key parameters, particularly in low−cost ac−dc adapters, open−frame power supplies etc. The NCP1255 brings all the necessary components normally needed in today modern power supply designs, bringing several enhancements such as a non−dissipative OPP, a brown−out protection or peak power excursion for loads exhibiting variations over time.

- **Current−mode operation with internal slope compensation:** implementing peak current mode control at a fixed 65−kHz frequency, the NCP1255 offers an internal ramp compensation signal that can easily by summed up to the sensed current. Sub harmonic oscillations can thus be compensated via the inclusion of a simple resistor in series with the current−sense information.
- **Frequency excursion:** when the power demand forces the peak current setpoint to reach the internal limit (0.8 V/R_{sense} typically), the frequency is authorized to increase to let the converter deliver more power. The frequency excursion stops when 130 kHz are reached at a level of 4 V. This excursion can only be temporary and its duration is set by the overload timer.
- **Internal OPP:** by routing a portion of the negative voltage present during the on−time on the auxiliary winding to the dedicated OPP pin (pin 1), the user has a simple and non−dissipative means to alter the maximum peak current setpoint as the bulk voltage increases. If the pin is grounded, no OPP compensation occurs. If the pin receives a negative voltage down to –250 mV, then a peak current reduction down to 31.3% typical can be achieved. For an improved performance, the maximum voltage excursion on the sense resistor is limited to 0.8 V.
- **Low startup current:** reaching a low no−load standby power always represents a difficult exercise when the controller draws a significant amount of current during start−up. Thanks to its proprietary architecture, the NCP1255 is guaranteed to draw less than 15 μA maximum, easing the design of low standby power adapters.
- **EMI jittering:** an internal low−frequency modulation signal varies the pace at which the oscillator frequency is modulated. This helps spreading out energy in conducted noise analysis. To improve the EMI signature at low power levels, the jittering will not be disabled in frequency foldback mode (light load conditions).
- **Frequency foldback capability:** a continuous flow of pulses is not compatible with no−load/light−load standby power requirements. To excel in this domain, the controller observes the feedback pin and when it reaches a level of 1.9 V, the oscillator then starts to reduce its switching frequency as the feedback level continues to decrease. When the feedback level reaches 1.5−V, the frequency hits its lower stop at 26 kHz. When the feedback pin goes further down and reaches 1 V, the peak current setpoint is internally frozen. Below this point, if the power continues to drop, the controller enters classical skip−cycle mode.
- **Internal soft−start:** a soft−start precludes the main power switch from being stressed upon start−up. In this controller, the soft−start is internally fixed to 4 ms. Soft−start is activated when a new startup sequence occurs or during an auto−recovery hiccup.
- **OVP input:** the NCP1255 includes a latch input (pin 1) that can be used to sense an overvoltage condition on the adapter. If this pin is brought higher than the internal reference voltage V_{latch}, then the circuit permanently latches off. The V_{cc} pin is pulled down to a fixed level, keeping the controller latched. Reset occurs when the latch current goes below ICC_{latch} or when a brown−out transition is sensed by the controller.
- **V_{cc} OVP:** a latched OVP protects the circuit against V_{cc} runaways. The fault must be present at least 20 μs to be validated. Reset occurs when the latch current goes below ICC_{latch} or when a brown−out transition is sensed by the controller.
- **Short−circuit protection:** short−circuit and especially over−load protections are difficult to implement when a strong leakage inductance between auxiliary and power windings affects the transformer (the aux winding level does not properly collapse in presence of an output short). Here, every time the internal 0.8−V maximum peak current limit is activated (or less when OPP is used), an error flag is asserted and a time period starts, thanks to the programmable timer. The controller can distinguish between two faulty situations:
  - There is an extra demand of power, still within the power supply capabilities. In that case, the feedback level is in the vicinity of 3.2−4 V. It corresponds to 0.8 V as the maximum peak current setpoint without OPP. The timer duration is then 100% of its programmed value via the pull−down resistor on pin 8. If you put a 22−kΩ resistor, the typical duration is around 500 ms. If the fault disappears, e.g. the peak current setpoint no longer hits the maximum value (e.g. 0.8 V at no OPP), then the timer is reset.
  - The output is frankly shorted. The feedback level is thus pushed to its upper stop (4.5 V) and the timer is reduced to 25% of its normal value.
  - In either mode, when the fault is validated, all pulses are stopped and the controller enters an

auto−recovery burst mode, with a soft−start sequence at the beginning of each cycle. Please note the presence of a divider by two which ignores one hiccup cycle over two (double hiccup type of burst).

- As soon as the fault disappears, the SMPS resumes operation. Please note that some version offers an auto−recovery mode as we just described, some do not and latch off in case of a short circuit.

- **Brown−out protection:** a portion of the bulk voltage is brought to pin 7 via a resistive network. When the voltage on this pin is too low, the part stops pulsing. No re−start attempt is made until the controller senses that the voltage is back within its normal range. When the brown−out comparator senses the voltage is acceptable, it sends a general reset to the controller and authorizes to re−start. Please note that a re−start is always synchronized with a $V_{CC,ON}$ transition event. The brown−out recovery does not reset the internal latch.

Start−up Sequence

The NCP1255 start−up voltage is made purposely high to permit large energy storage in a small V_{cc} capacitor value. This helps to operate with a small start−up current which, together with a small V_{cc} capacitor, will not hamper the start−up time. To further reduce the standby power, the start−up current of the controller is extremely low, below 15 μA. The start−up resistor can therefore be connected to the bulk capacitor or directly to the mains input voltage if you wish to save a few more mW.

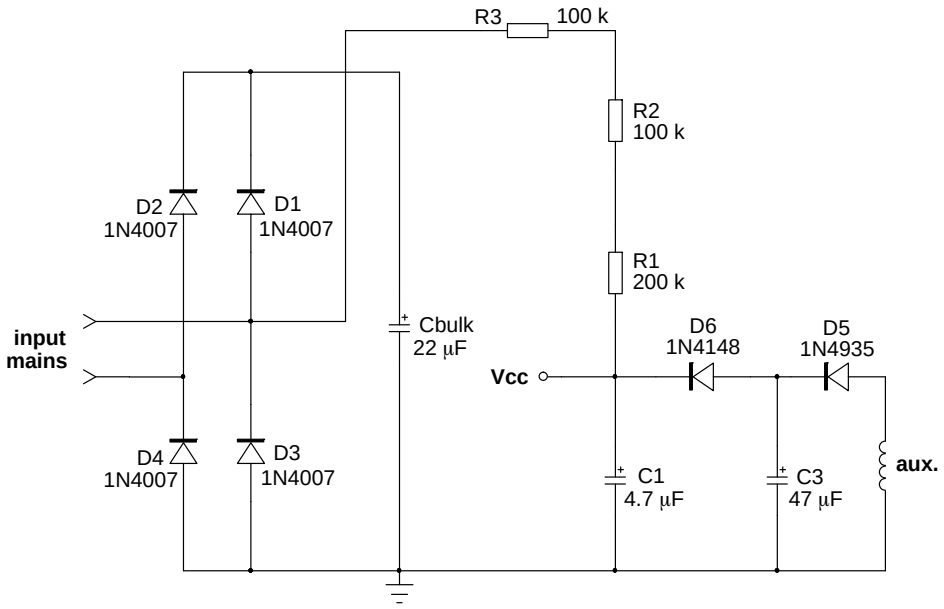


Figure 34. The startup resistor can be connected to the input mains for further power dissipation reduction.

The first step starts with the calculation of the needed V_{cc} capacitor which will supply the controller until the auxiliary winding takes over. Experience shows that this time t_1 can be between 5 and 20 ms. Considering that we need at least an energy reservoir for a t_1 time of 10 ms, the V_{cc} capacitor must be larger than:

$$CV_{cc} \geq \frac{I_{cc}t_1}{VCC_{on} - VCC_{min}} \geq \frac{3\text{ m} \times 10\text{ m}}{9} \geq 3.3\ \mu F \quad \text{(eq. 1)}$$

Let us select a 4.7−μF capacitor at first and experiments in the laboratory will let us know if we were too optimistic for t_1. The V_{cc} capacitor being known, we can now evaluate the charging current we need to bring the V_{cc} voltage from 0 to the VCC_{on} of the IC, 18 V typical. This current has to be selected to ensure a start−up at the lowest mains (85 V rms) to be less than 3 s (2.5 s for design margin):

$$I_{charge} \geq \frac{VCC_{on}C_{Vcc}}{2.5} \geq \frac{18 \times 4.7\ \mu}{2.5} \geq 34\ \mu A \quad \text{(eq. 2)}$$

If we account for the 15 μA that will flow inside the controller, then the total charging current delivered by the start−up resistor must be 49 μA. If we connect the start−up network to the mains (half−wave connection then), we know that the average current flowing into this start−up resistor will be the smallest when V_{cc} reaches the VCC_{on} of the controller:

$$I_{CVcc,min} = \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - VCC_{on}}{R_{start-up}} \quad \text{(eq. 3)}$$

To make sure this current is always greater than 49 μA, the minimum value for $R_{start-up}$ can be extracted:

$$R_{start-up} \leq \frac{\frac{V_{ac,rms}\sqrt{2}}{\pi} - VCC_{on}}{I_{CVcc,min}} \leq \frac{\frac{85 \times 1.414}{\pi} - 18}{49\ \mu} \leq 413\ k\Omega \quad \text{(eq. 4)}$$

This calculation is purely theoretical, considering a constant charging current. In reality, the take over time can be shorter (or longer!) and it can lead to a reduction of the V_{cc} capacitor. This brings a decrease in the charging current and an increase of the start−up resistor, for the benefit of standby power. Laboratory experiments on the prototype are thus mandatory to fine tune the converter. If we chose the 400−kΩ resistor as suggested by Equation 4, the dissipated power at high line amounts to:

$$P_{Rstartup,max} = \frac{V_{ac,peak}^2}{4R_{start-up}} = \frac{\left(230 \times \sqrt{2}\right)^2}{4 \times 400\ k} = \frac{105\ k}{1.6\ Meg} = 66\ mW \quad \text{(eq. 5)}$$

Now that the first V_{cc} capacitor has been selected, we must ensure that the self−supply does not disappear when in no−load conditions. In this mode, the skip−cycle can be so deep that refreshing pulses are likely to be widely spaced, inducing a large ripple on the V_{cc} capacitor. If this ripple is too large, chances exist to touch the VCC_{min} and reset the controller into a new start−up sequence. A solution is to grow this capacitor but it will obviously be detrimental to the start−up time. The option offered in Figure 34 elegantly solves this potential issue by adding an extra capacitor on the auxiliary winding. However, this component is separated from the V_{cc} pin via a simple diode. You therefore have the ability to grow this capacitor as you need to ensure the self−supply of the controller without affecting the start−up time and standby power.

Triggering the SCR

The latched−state of the NCP1255 is maintained via an internal thyristor (SCR). When the voltage on pin 1 exceeds the latch voltage for four consecutive clock cycles, the SCR is fired and immediately stops the output pulses. The same SCR is fired when an OVP is sensed on the V_{cc} pin. When this happens, all pulses are stopped and V_{cc} is discharged to a fix level of 7 V typically: the circuit is latched and the converter no longer delivers pulses. To maintain the latched−state, a permanent current must be injected in the part. If too low of a current, the part de−latches and the converter resumes operation. This current is characterized to 32 μA as a minimum but we recommend including a design margin and select a value around 60 μA. The test is to latch the part and reduce the input voltage until it de−latches. If you de−latch at V_{in} = 70 V rms for a minimum voltage of 85 V rms, you are fine. If it precociously recovers, you will have to increase the start−up current, unfortunately to the detriment of standby power.

The most sensitive configuration is actually that of the half−wave connection proposed in Figure 34. As the current disappears 5 ms for a 10−ms period (50−Hz input source), the latch can potentially open at low line. If you really reduce the start−up current for a low standby power design, you must ensure enough current in the SCR in case of a faulty event. An alternate connection to the above is shown below (Figure 35):

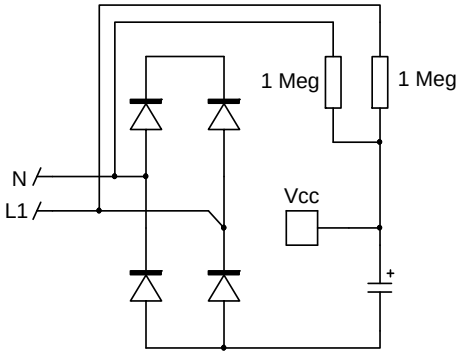


Figure 35. The full−wave connection ensures latch current continuity as well as a X2−discharge path.

In this case, the current is no longer made of 5−ms “holes” and the part can be maintained at a low input voltage. Experiments show that these 2−MΩ resistor help to maintain the latch down to less than 50 V rms, giving an excellent design margin. Standby power with this approach was also improved compared to Figure 34 solution. Please note that these resistors also ensure the discharge of the X2−capacitor up to a 0.47 μF type.

The de−latch of the SCR occurs when a) the injected current in the V_{cc} pin falls below the minimum stated in the data−sheet (32 μA at room temp). When the start−up resistors are connected as suggested by Figure 34 the reset time when unplugging the converter is extremely short, typically below the second.

Internal Over Power Protection

There are several known ways to implement Over Power Protection (OPP), all suffering from particular problems. These problems range from the added consumption burden on the converter or the skip−cycle disturbance brought by the current−sense offset. A way to reduce the power capability at high line is to capitalize on the negative voltage swing present on the auxiliary diode anode. During the turn−on time, this point dips to $-NV_{in}$, N being the turns ratio between the primary winding and the auxiliary winding. The negative plateau observed on Figure 36 will have an amplitude depending on the input voltage. The idea implemented in this chip is to sum a portion of this negative swing with the 0.8−V internal reference level. For instance, if the voltage swings down to −150 mV during the on time, then the internal peak current set point will be fixed to 0.8−0.150 = 650 mV. The adopted principle appears in Figure 37 and shows how the final peak current set point is constructed.

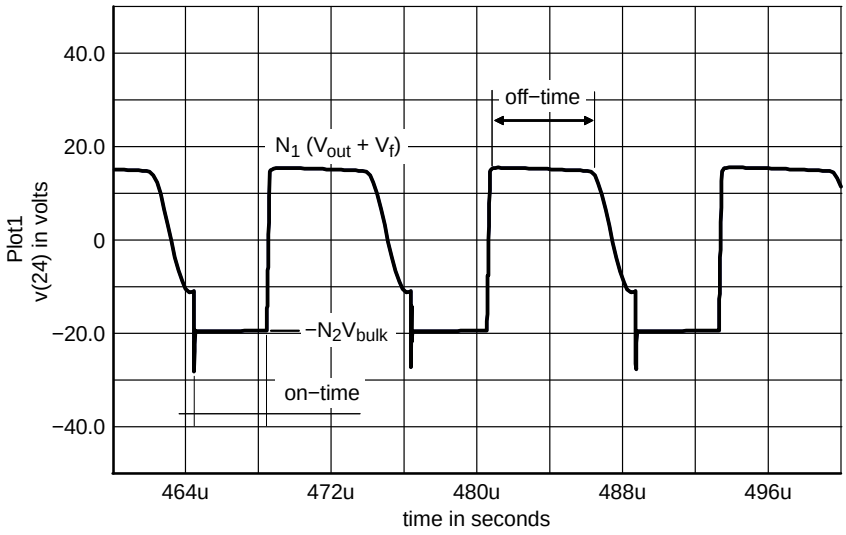


Figure 36. The signal obtained on the auxiliary winding swings negative during the on−time.

Let's assume we need to reduce the peak current from 2.5 A at low line, to 2 A at high line. This corresponds to a 20% reduction or a set point voltage of 640 mV. To reach this level, then the negative voltage developed on the OPP pin must reach:

$$V_{OPP} = 640\ m - 800\ m = -160\ mV \quad \text{(eq. 6)}$$

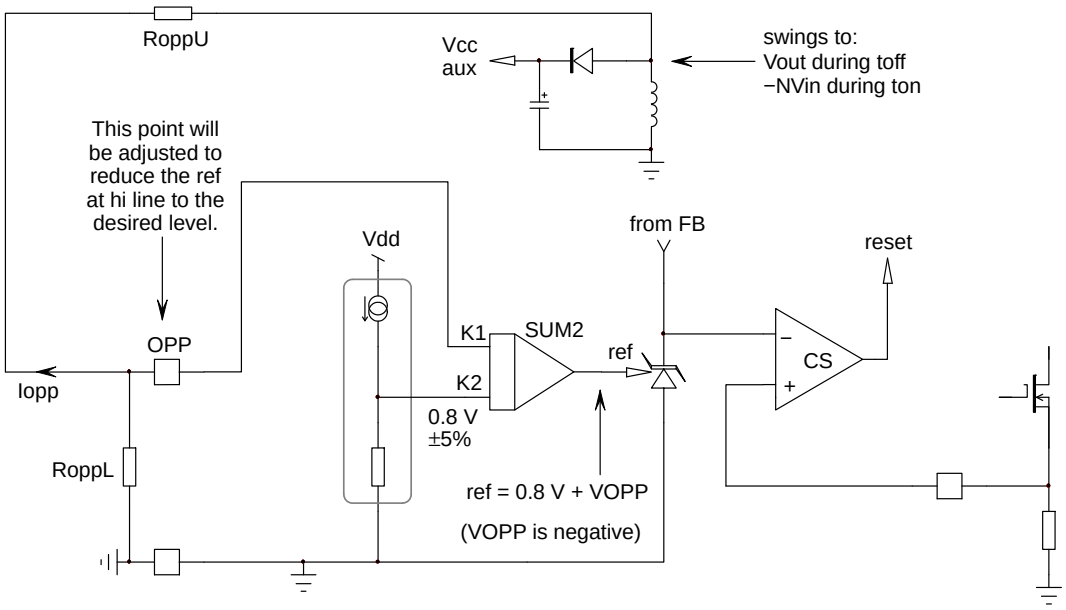


Figure 37. The OPP circuitry affects the maximum peak current set point by summing a negative voltage to the internal voltage reference.

Let us assume that we have the following converter characteristics:

V_{out} = 19 V

V_{in} = 85 to 265 V rms

$N_1 = N_p:N_s$ = 1:0.25

$N_2 = N_p:N_{aux}$ = 1:0.18

Given the turns ratio between the primary and the auxiliary windings, the on−time voltage at high line (265 Vac) on the auxiliary winding swings down to:

$$V_{aux} = -N_2 V_{in,max} = -0.18 \times 375 = -67.5\ V \quad \text{(eq. 7)}$$

To obtain a level as imposed by Equation 6, we need to install a divider featuring the following ratio:

$$Div = \frac{0.16}{67.5} \approx 2.4\ m \quad \text{(eq. 8)}$$

If we arbitrarily fix the pull−down resistor R_{OPPL} to 1 kΩ, then the upper resistor can be obtained by:

$$R_{OPPU} = \frac{67.5 - 0.16}{0.16/1\ k} \approx 421\ k\Omega \quad \text{(eq. 9)}$$

If we now plot the peak current set point obtained by implementing the recommended resistor values, we obtain the following curve (Figure 38):

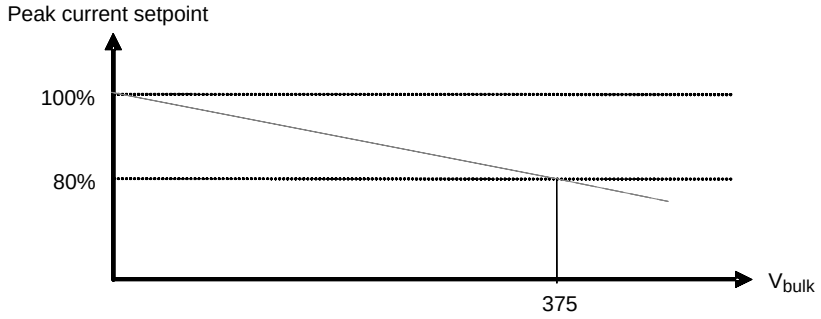


Figure 38. The peak current regularly reduces down to 20% at 375 V dc.

The OPP pin is surrounded by Zener diodes stacked to protect the pin against ESD pulses. These diodes accept some peak current in the avalanche mode and are designed to sustain a certain amount of energy. On the other side, negative injection into these diodes (or forward bias) can cause substrate injection which can lead to an erratic circuit behavior. To avoid this problem, the pin is internal clamped slightly below –300 mV which means that if more current is injected before reaching the ESD forward drop, then the maximum peak reduction is kept to 40%. If the voltage finally forward biases the internal Zener diode, then care must be taken to avoid injecting a current beyond –2 mA. Given the value of R_{OPPU}, there is no risk in the present example. Finally, please note that another comparator internally fixes the maximum peak current set point to 0.8 V even if the OPP pin is adversely biased above 0 V.

Frequency Foldback

The reduction of no−load standby power associated with the need for improving the efficiency, requires a change in the traditional fixed−frequency type of operation. This controller implements a switching frequency foldback when the feedback voltage passes below a certain level, V_{fold}, set around 1.9 V. At this point, the oscillator turns into a Voltage−Controlled Oscillator and reduces its switching frequency. Below this point, the frequency no longer changes and the feedback level still controls the peak current setpoint. When the feedback voltage reaches 1 V, the peak current freezes to (250 mV or »31% of the maximum 0.8−V setpoint). If the power continues to decrease, the part enters skip cycle at a moderate peak current for the best noise−free performance in no−load conditions. Figure 39 depicts the adopted scheme for the part.

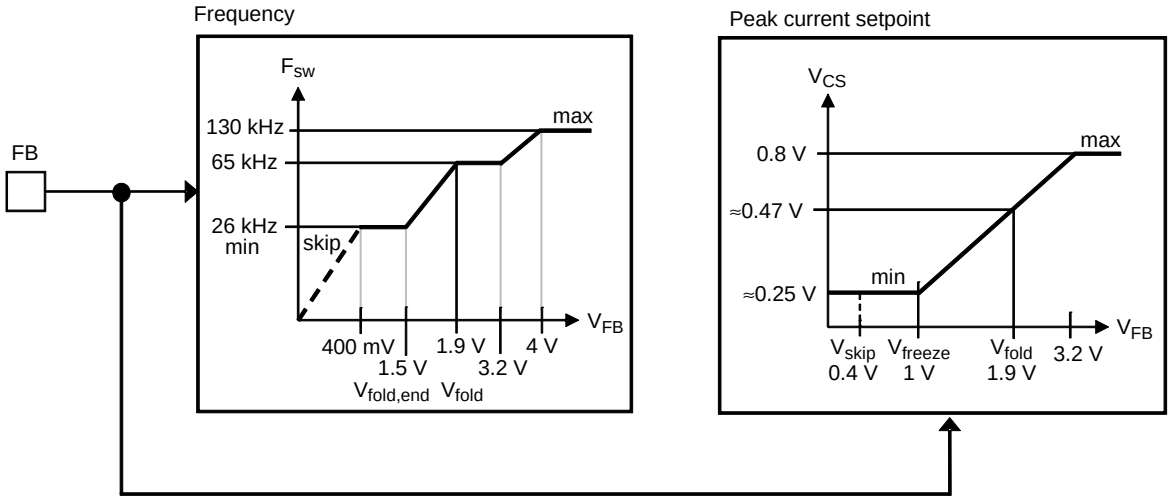


Figure 39. By observing the voltage on the feedback pin, the controller reduces its switching frequency for an improved performance at light load.

Auto−Recovery Short−Circuit Protection

In case of output short−circuit or if the power supply experiences a severe overloading situation, an internal error flag is raised and starts a countdown timer. If the flag is asserted longer than its programmed value (200 ms or 50 ms in the example), the driving pulses are stopped and V_{cc} falls down as the auxiliary pulses are missing. When it crosses $VCC_{(min)}$, the controller consumption is down to a few μA and the V_{cc} slowly builds up again thanks to the resistive starting network. When V_{cc} reaches VCC_{ON}, the controller purposely ignores the re−start and waits for another V_{cc} cycle: this is the so−called double hiccup. By lowering the duty ratio in fault condition, it naturally reduces the average input power and the rms current in the output cable. Illustration of such principle appears in Figure 40. Please note that soft−start is activated upon re−start attempt.

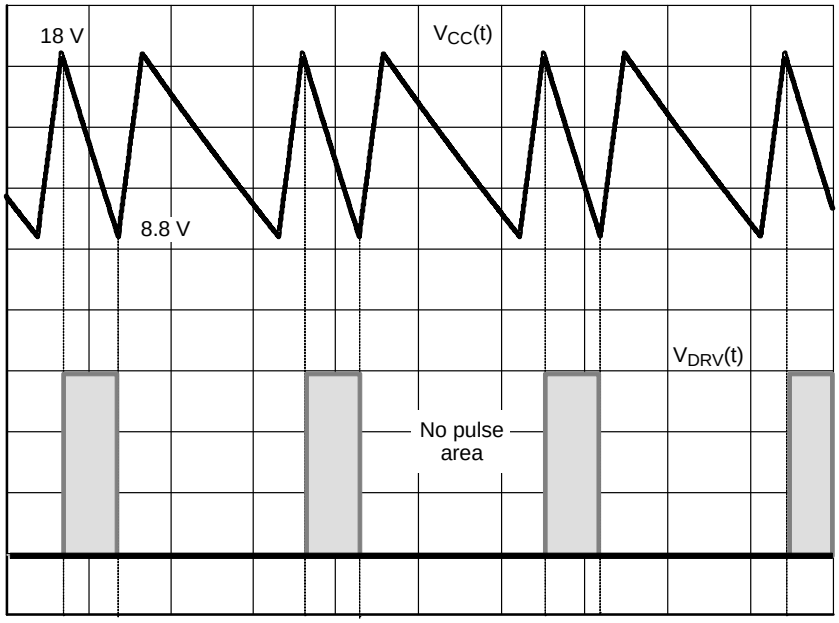


Figure 40. An auto−recovery hiccup mode is entered in case a faulty event longer than 100 ms is acknowledged by the controller.

The double hiccup is operating regardless of the brown−out level. However, when the internal comparator toggles indicating that the controller recovers from a brown−out situation (the input line was ok, then too low and back again to normal), the double hiccup is interrupted and the controller re−starts to the next available V_{cc} peak. Figure 41 displays the resulting waveform: the controller is protecting the converter against an overload. The mains suddenly went down, and then back again at a normal level. Right at this moment, the double hiccup logic receives a reset signal and ignores the next hiccup to immediately initiate a re−start signal.

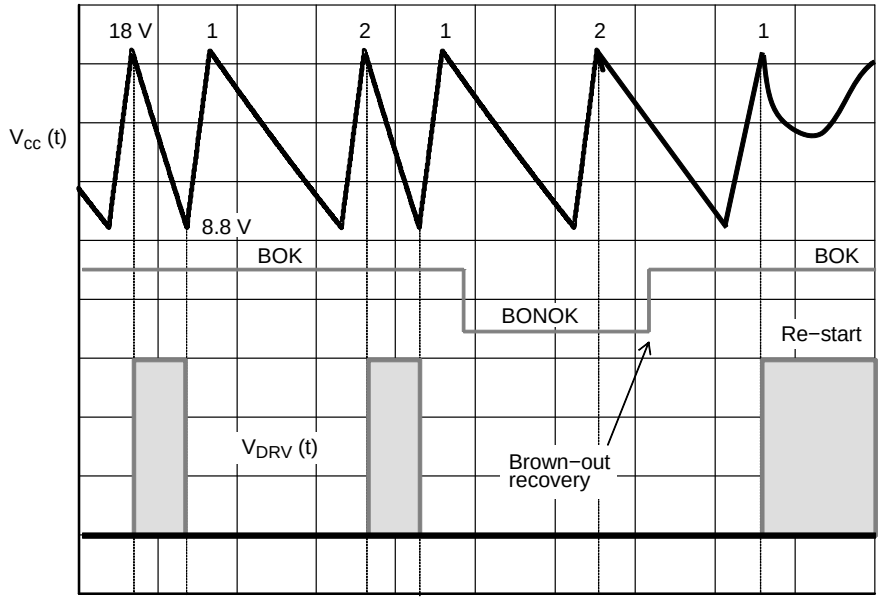


Figure 41. The hiccup latch is reset when a brown−out transition is detected to shorten the re−start time.

Slope compensation

The NCP1255 includes an internal ramp compensation signal. This is the buffered oscillator clock delivered during the on time only. Its amplitude is around 2.5 V at the maximum authorized duty ratio. Ramp compensation is a known means used to cure sub harmonic oscillations in CCM−operated current−mode converters. These oscillations take place at half the switching frequency and occur only during Continuous Conduction Mode (CCM) with a duty ratio greater than 50%. To lower the current loop gain, one usually mixes between 50 and 100% of the inductor downslope with the current−sense signal. Figure 42 depicts how internally the ramp is generated. Please note that the ramp signal will be disconnected from the CS pin, during the off−time.

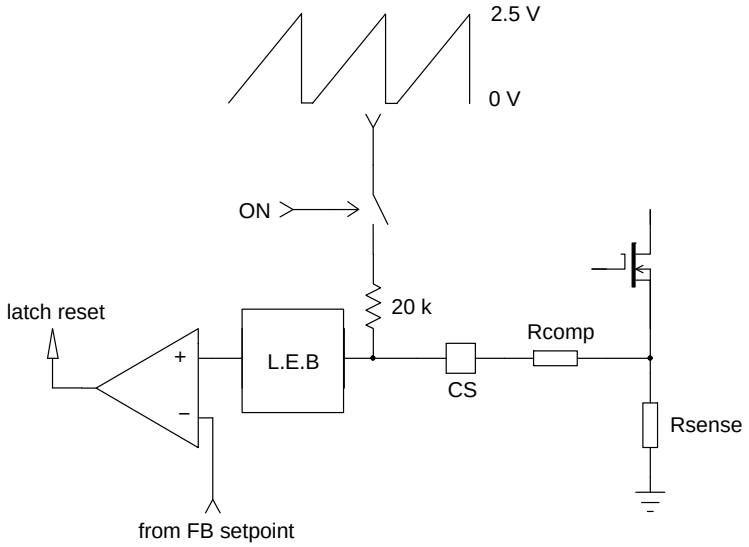


Figure 42. Inserting a resistor in series with the current sense information brings slope compensation and stabilizes the converter in CCM operation.

In the NCP1255 controller, the oscillator ramp exhibits a 2.5−V swing reached at a 80% duty ratio. If the clock operates at a 65−kHz frequency, then the available oscillator slope corresponds to:

$$S_{ramp} = \frac{V_{ramp,peak}}{D_{max}T_{sw}} = \frac{2.5}{0.8 \times 15\,\mu} = 208\ kV/s \text{ or } 208\ mV/\mu s \quad \text{(eq. 10)}$$

In our flyback design, let's assume that our primary inductance L_p is 770 μH, and the SMPS delivers 19 V with a N_p:N_s turns ratio of 1:0.25. The off−time primary current slope S_p is thus given by:

$$S_p = \frac{\left(V_{out} + V_f\right)\frac{N_p}{N_s}}{L_p} = \frac{(19 + 0.8) \times 4}{770\,\mu} = 103\ kA/s \quad \text{(eq. 11)}$$

Given a sense resistor of 330 mΩ, the above current ramp turns into a voltage ramp of the following amplitude:

$$S_{sense} = S_p R_{sense} = 208k \times 0.33 \approx 69kV/s \text{ or } 69mV/\mu s \quad \text{(eq. 12)}$$

If we select 50% of the downslope as the required amount of ramp compensation, then we shall inject a ramp whose slope is ≈34 mV/μs. Our internal compensation being of 208 mV/μs, the divider ratio (*divratio*) between R_{comp} and the internal 20 kΩ resistor is:

$$\text{divratio} = \frac{34\ m}{208\ m} = 0.163 \quad \text{(eq. 13)}$$

The series compensation resistor value is thus:

$$R_{comp} = R_{ramp}\text{divratio} = 20\ k \times 0.163 \approx 3.3\ k\Omega \quad \text{(eq. 14)}$$

A resistor of the above value will then be inserted from the sense resistor to the current sense pin. We recommend adding a small 100−pF capacitor, from the current sense pin to the controller ground for improved noise immunity. Please make sure both components are located very close to the controller.

Latching Off the Controller

The OPP pin not only allows a reduction of the peak current set point in relationship to the line voltage, it also offers a means to permanently latch−off the part. When the part is latched−off, the V_{cc} pin is internally pulled down to around 7 V and the part stays in this state until the user cycles the V_{cc} down and up again, e.g. by un−plugging the converter from the mains outlet. The latch detection is made by observing the OPP pin by a comparator featuring a 3−V reference voltage. However, for noise reasons and in particular to avoid the leakage inductance contribution at turn off, a 1−μs blanking delay is introduced before the output of the OVP comparator is checked. Then, the OVP comparator output is validated only if its high−state duration lasts a minimum of 600 ns. Below this value, the event is ignored. Then, a counter ensures that 4 successive OVP events have occurred before actually latching the part. There are several possible implementations, depending on the needed precision and the parameters you want to control.

The first and easiest solution is the additional resistive divider on top of the OPP one. This solution is simple and inexpensive but requires the insertion of a diode to prevent disturbing the OPP divider during the on−time.

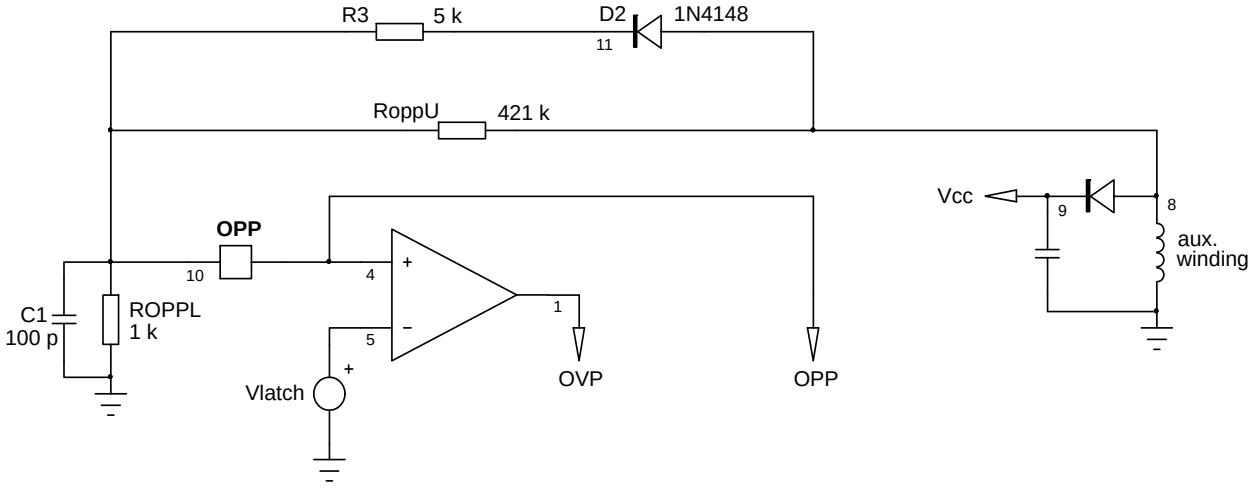


Figure 43. A simple resistive divider brings the OPP pin above 3 V in case of a V_{cc} voltage runaway above 18 V.

First, calculate the OPP network with the above equations. Then, suppose we want to latch off our controller when V_{out} exceeds 25 V. On the auxiliary winding, the plateau reflects the output voltage by the turns ratio between the power and the auxiliary windings. In case of voltage runaway for our 19−V adapter, the plateau will go up to:

$$V_{aux,OVP} = 25 \times \frac{0.18}{0.25} = 18\ V \qquad \text{(eq. 15)}$$

Since our OVP comparator trips at a 3−V level, across the 1−kΩ selected OPP pull−down resistor, it implies a 3−mA current. From 3 V to go up to 18 V, we need an additional 15 V. Under 3 mA and neglecting the series diode forward drop, it requires a series resistor of:

$$R_{OVP} = \frac{V_{latch} - V_{VOP}}{V_{OVP}/R_{OPPL}} = \frac{18 - 3}{3/1\ k} = \frac{15}{3\ m} = 5\ k\Omega \qquad \text{(eq. 16)}$$

In nominal conditions, the plateau establishes to around 14 V. Given the divide−by−6 ratio, the OPP pin will swing to 14/6 = 2.3 V during normal conditions, leaving 700 mV for the noise immunity. A 100−pF capacitor can be added to improve it and avoids erratic trips in presence of external surges. Do not increase this capacitor too much otherwise the OPP signal will be affected by the integrating time constant.

A second solution for the OVP detection alone, is to use a Zener diode wired as recommended by Figure 44.

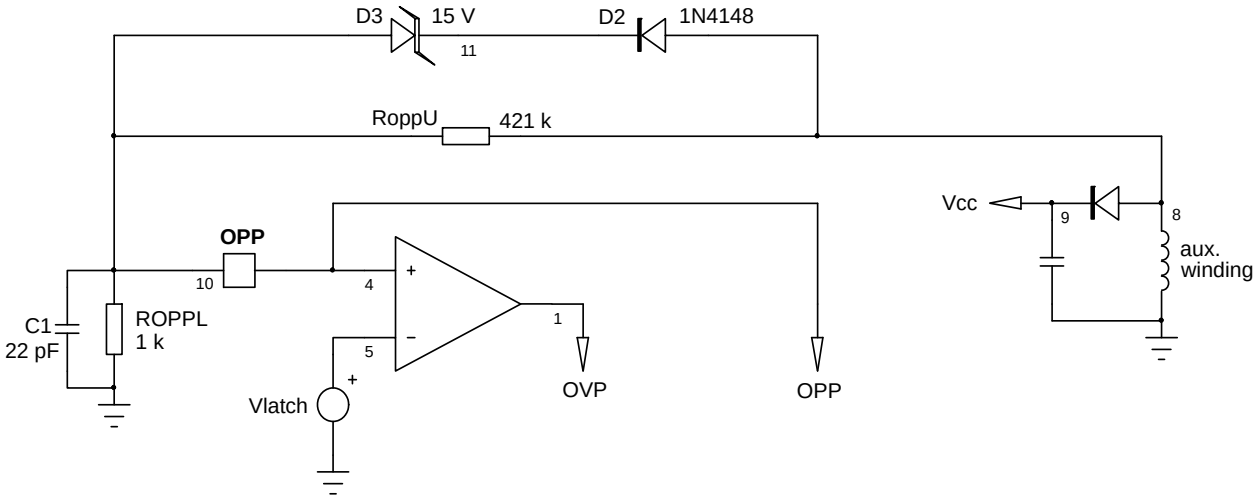


Figure 44. A Zener diode in series with a diode helps to improve the noise immunity of the system.

In this case, to still trip at a 18−V level, we have selected a 15−V Zener diode. In nominal conditions, the voltage on the OPP pin is almost 0 V during the off time as the Zener is fully blocked. This technique clearly improves the noise immunity of the system compared to that obtained from a resistive string as in Figure 43. Please note the reduction of the capacitor on the OPP pin to 10−22 pF. This is because of the potential spike going through the Zener parasitic capacitor and the possible auxiliary level shortly exceeding its breakdown voltage during the leakage inductance reset period (hence the internal 1−μs blanking delay at turn off). This spike despite its very short time is energetic enough to charge the added capacitor C_1 and given the time constant, could make it discharge slower, potentially disturbing the blanking circuit. When implementing the Zener option, it is important to carefully observe the OPP pin voltage (short probe connections!) and check that enough margin exists to that respect.

Over Temperature Protection

In a lot of designs, the adapter must be protected against thermal runaways, e.g. when the temperature inside the adapter box increases beyond a certain value. Figure 45 shows how to implement a simple OTP using an external NTC and a series diode. The principle remains the same: make sure the OPP network is not bothered by the additional NTC hence the presence of this diode. When the NTC resistor will diminish as the temperature increases, the voltage on the OPP pin during the off time will slowly increase and, once it crosses 3 V for 4 consecutive clock cycles, the controller will permanently latch off.

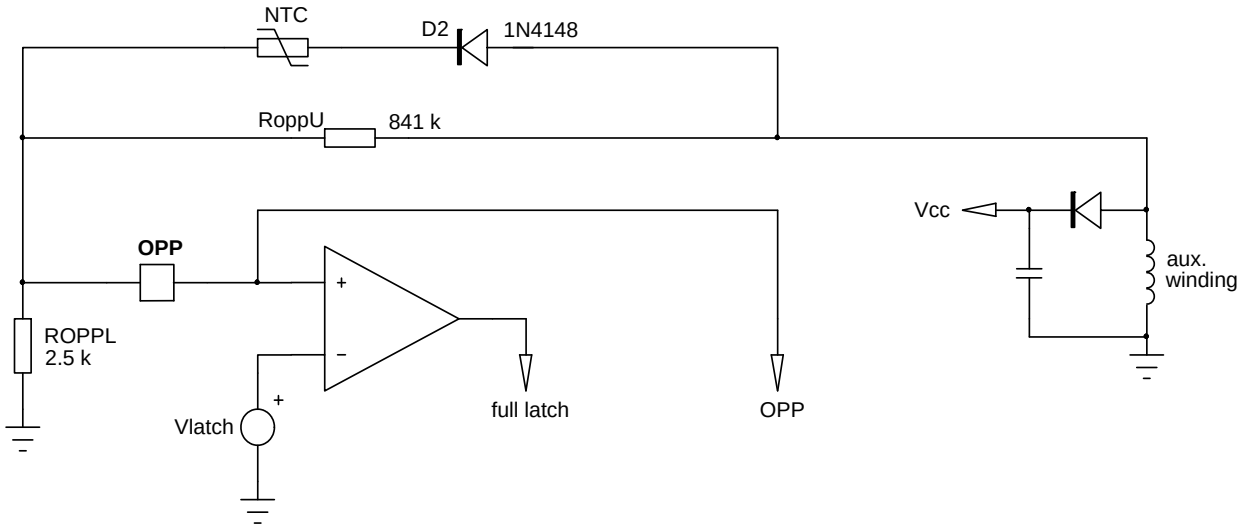


Figure 45. The internal circuitry hooked to pin 1 can be used to implement over temperature protection (OTP).

Back to our 19−V adapter, we have found that the plateau voltage on the auxiliary diode was 13 V in nominal conditions. We have selected an NTC which offers a 470−kΩ resistor at 25°C and drops to 8.8 kΩ at 110°C. If our auxiliary winding plateau is 14 V and we consider a 0.6−V forward drop for the diode, then the voltage across the NTC in fault mode must be:

$$V_{NTC} = 14 - 3 - 0.6 = 10.4\ V \qquad \text{(eq. 17)}$$

Based on the 8.8−kΩ NTC resistor at 110°C, the current inside the device must be:

$$I_{NTC} = \frac{10.4}{8.8\ k} \approx 1.2\ mA \qquad \text{(eq. 18)}$$

As such, the bottom resistor R_{OPPL}, can easily be calculated:

$$R_{OPPL} = \frac{3}{1.2\ m} = 2.5\ k\Omega \qquad \text{(eq. 19)}$$

Now that the pull−down OPP resistor is known, we can calculate the upper resistor value R_{OPPU} to adjust the power limit at the chosen output power level. Suppose we need a 200−mV decrease from the 0.8−V set point and the on−time swing on the auxiliary anode is −67.5 V, then we need to drop over R_{OPPU} a voltage of:

$$V_{R_{OPPU}} = 67.5 - 0.2 = 67.3\ V \qquad \text{(eq. 20)}$$

The current circulating in the pull down resistor R_{OPPL} in this condition will be:

$$I_{R_{OPPL}} = \frac{200\ m}{2.5\ k} = 80\ \mu A \qquad \text{(eq. 21)}$$

The R_{OPPU} value is therefore easily derived:

$$R_{OPPU} = \frac{67.3}{80\ \mu} = 841\ k\Omega \qquad \text{(eq. 22)}$$

Combining OVP and OTP

The OTP and Zener−based OVP can be combined together as illustrated by Figure 46.

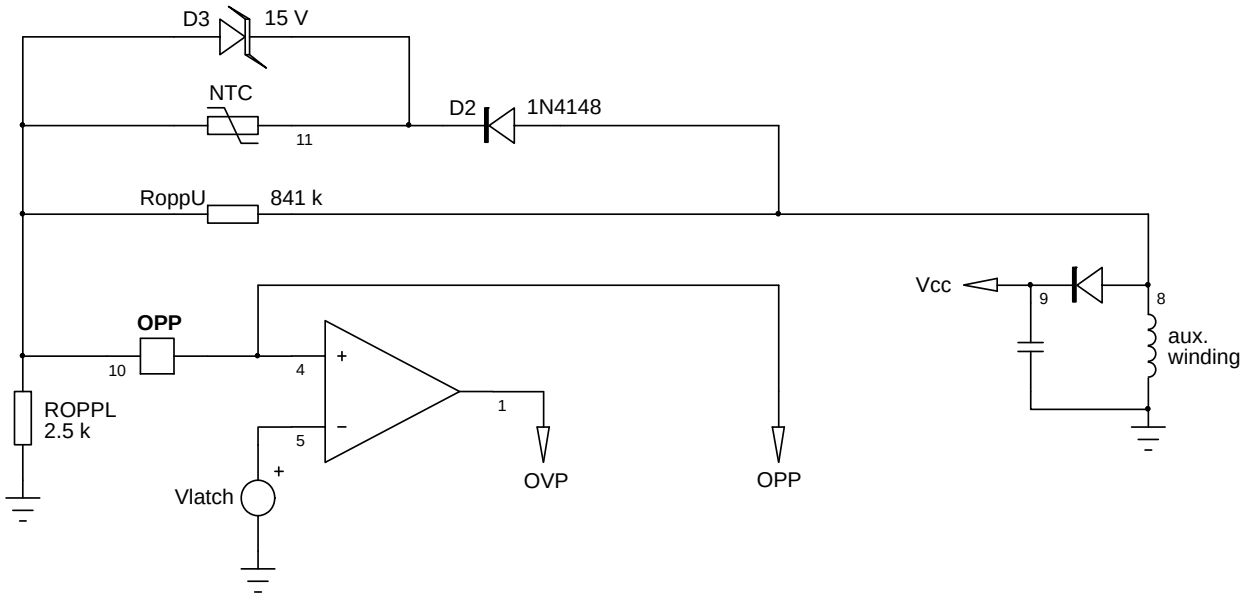


Figure 46. With the NTC back in place, the circuit nicely combines OVP, OTP and OPP on the same pin.

In nominal V_{cc}/output conditions, when the Zener is not activated, the NTC can drive the OPP pin and trigger the adapter in case of a fault. On the contrary, in nominal temperature conditions, if the loop is broken, the voltage runaway will be detected and acknowledged by the controller.

In case the OPP pin is not used for either OPP or OVP, it can simply be grounded.

Filtering the spikes

The auxiliary winding is the seat of spikes that can couple to the OPP pin via the parasitic capacitances exhibited by the Zener diode and the series diode. To prevent an adverse triggering of the Over Voltage Protection circuitry, it is possible to install a small *RC* filter before the detection network. Typical values are those given in Figure 47 and must be selected to provide the adequate filtering function without degrading the stand−by power by an excessive current circulation.

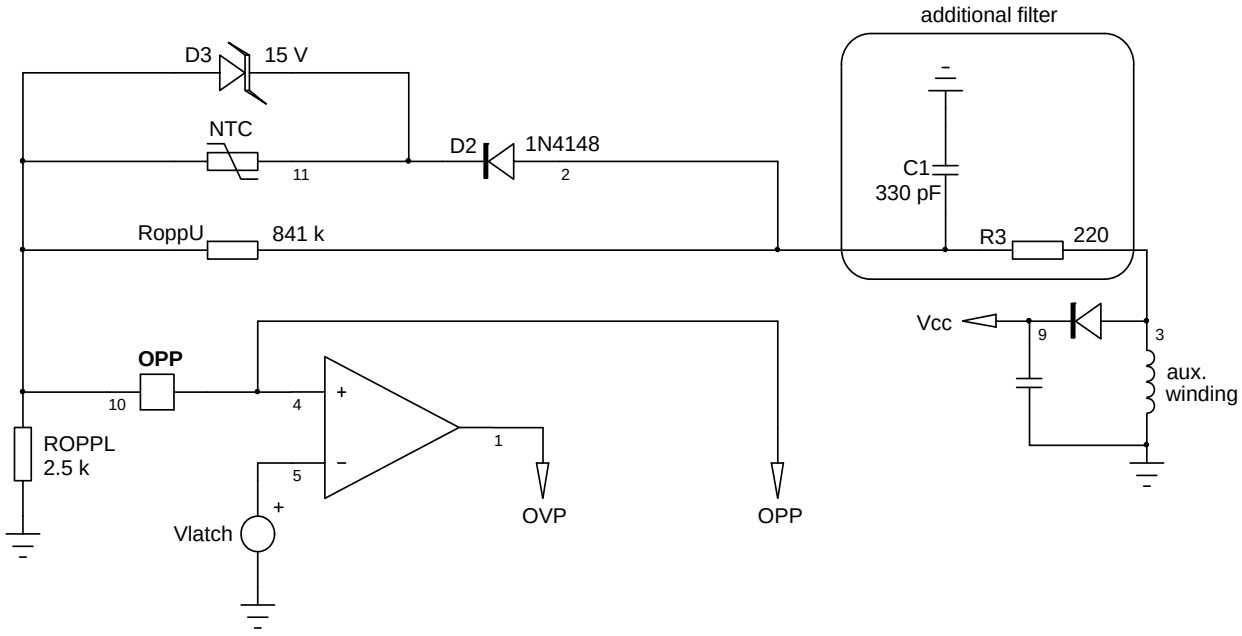


Figure 47. A small *RC* filter avoids the fast rising spikes from reaching the protection pin of the NCP125x in presence of energetic perturbations superimposed on the input line.

Latching Off with the V_{cc} Pin

The NCP1255 hosts a dedicated comparator on the V_{cc} pin. When the voltage on this pin exceeds 25.5 V typically for more than 20 μs, a signal is sent to the internal latch and the controller immediately stops the driving pulses while remaining in a lockout state. The part can be reset by cycling down its V_{cc}, for instance by pulling off the power plug but also if a brown−out recovery is sensed by the controller. This technique offers a simple and cheaper means to protect the converter against optocoupler failures without using the OPP pin and a Zener diode.

Peak Power Excursions

There are applications where the load profile heavily changes from a nominal to a peak value. For instance, it is possible that a 30−W ac−dc adapter accepts power excursions up to 60 W in certain conditions. Inkjet printers typically fall in that category of peak power adapters. However, to avoid growing the transformer size, an existing technique consists in freezing the peak current to a maximum value ($0.8/R_{sense}$ in our case) but authorizes frequency increase to a certain point. This point is internally fixed at 130 kHz.

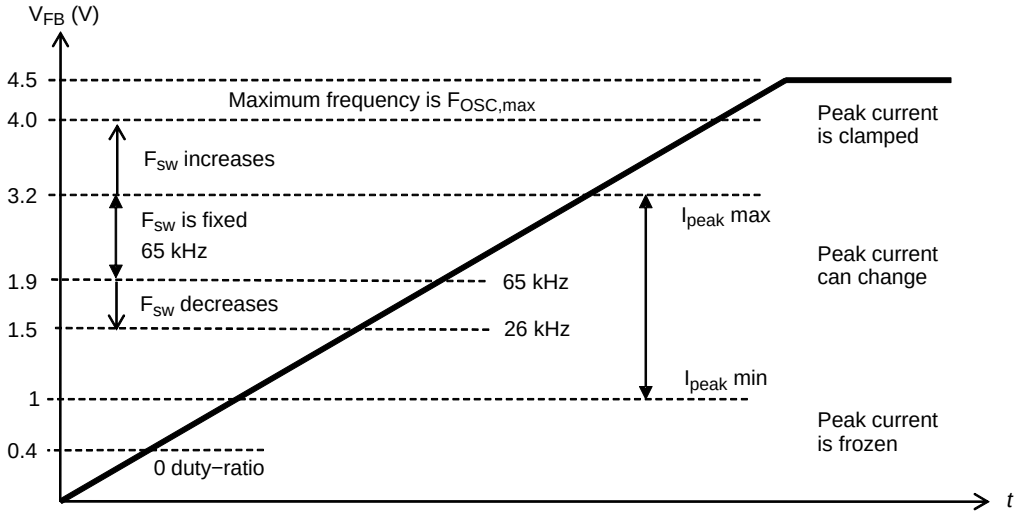


Figure 48. The feedback pin modulates the frequency up to 130 kHz (short−circuit, maximum power) or down to 26 kHz in frequency foldback.

Figure 48 shows the voltage evolution from almost 0 V to the open−loop level, around 4.5 V. At low power levels or in no−load operation, the feedback voltage stays in the vicinity of 400 mV and ensures skip−cycle operation. In this mode, the peak current is frozen to 31% of its maximum value. This freeze lasts as long as V_{FB} stays below 1 V. Beyond 1 V, the peak current is authorized to follow V_{FB} through a ratio of 4. When the power demand goes up, the switching frequency linearly increases from 26 kHz up to 65 kHz, a value reached when the feedback voltage exceeds 1.5 V. Beyond 1.9 V, the frequency no longer changes. As V_{FB} still increases, we are in a fixed−frequency variable peak current mode control type of operation until the feedback voltage hits 3.2 V. At this point, the maximum current is limited to $0.8\ V/R_{sense}$. If V_{FB} further increases, it means the converter undergoes an overload and requires more power from the source. As the peak current excursion is stopped, the only way to deliver more power is to increase the switching frequency. From 3.2 V up to 4 V, the frequency linearly increases from 65 kHz to 130 kHz. The maximum power delivered by the converter depends whether it operates in Discontinuous Conduction Mode (DCM) or in Continuous Conduction Mode (CCM):

$$P_{max,DCM} = \frac{1}{2} L_p F_{sw,max} I_{peak,max}^{\ 2} \eta \quad \text{(eq. 23)}$$

$$P_{max,CCM} = \frac{1}{2} L_p F_{sw,max} \left(I_{peak,max}^{\ 2} - I_{valley}^{\ 2} \right) \eta \quad \text{(eq. 24)}$$

Where $I_{peak,max}$ is the maximum peak current authorized by the controller and I_{valley} the valley current reached just before a new switching cycle begins. This current is expressed by the following formula:

$$I_{valley} = I_{peak} - \frac{V_{out} + V_f}{NL_p} t_{off} \quad \text{(eq. 25)}$$

In DCM, the valley current is equal to 0.

Two Levels of Protection

Once the feedback voltage asks for the maximum peak current, the controller knows that an overload condition has started. An internal timer is operated as soon as the maximum peak is reached. This timer duration is adjusted by a pull−down resistor to ground. Let's assume it is set to 200 ms. If the feedback voltage continues its rise, it means that the converter output voltage is going down further, close to a short−circuit situation. When the feedback voltage reaches the open−loop level (above 4.0 V typically), the original timer duration is divided by 4. For instance, at start−up, even if the overload timer is programmed to 200 ms, when the feedback voltage jumps above 4.0 V, the controller will wait 50 ms before fault detection occurs (the timer is reset upon start−up). Of course, if the feedback does not stay that long in the region of concern, the timer is reset when returning to a normal level. Figure 49 shows the timer values versus the feedback voltage.

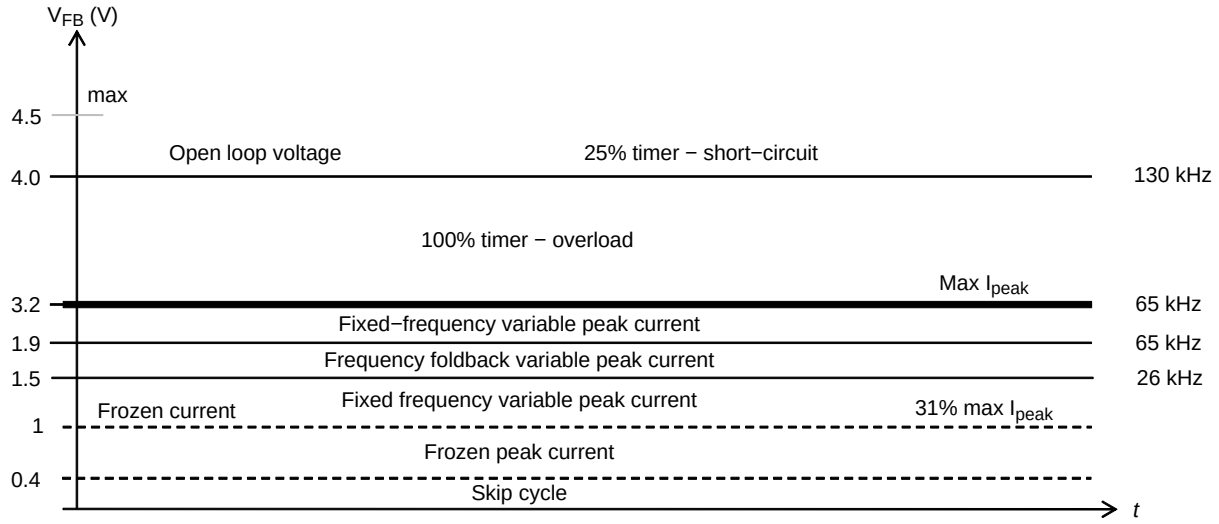


Figure 49. Depending on the feedback level, the timer will take two different values: it will authorize a transient overload, but will reduce a short−circuit duration.

Please note that the overload situation (OVL) is detected when the maximum peak current limit is hit. It can be 3.2 V as indicated in the graph in case of no Over Power Protection (OPP). If you have programmed an OPP level of −200 mV for instance, the OVL threshold becomes (0.8 − 0.2) x 4 = 2.4 V. When the maximum peak current situation is lifted, the converter returns to a normal situation, the timer is reset. The short circuit situation is detected by sensing a feedback voltage beyond 4 V. For the sake of the explanation, we have gathered two different events in Figure 50:

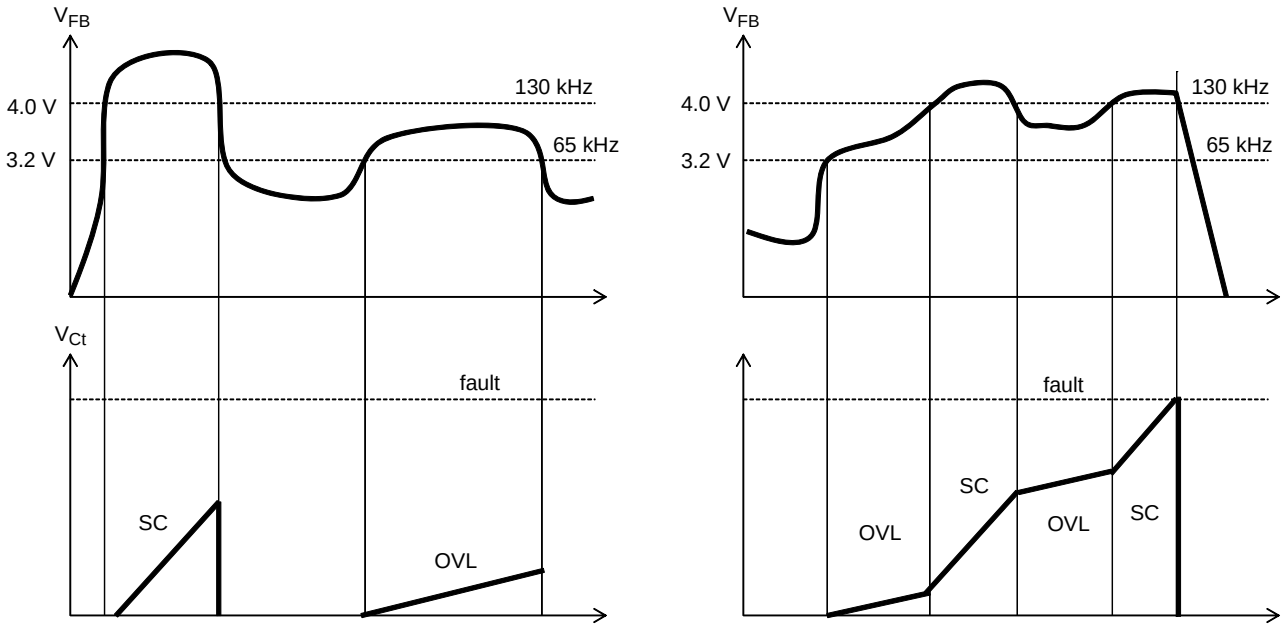


Figure 50.

When the feedback voltage exits a fault region before time completion, the timer is reset. On the contrary, if the timer elapses, the part enters an auto−recovery hiccup or latches off depending on the operated version.

In the first case, the feedback is pushed to the maximum upon start−up. The timer starts with a charging slope of the short−circuit condition (SC). If the timer would be externally set to 200 ms, the timer duration in this start−up sequence would be 50 ms. As soon as regulation occurs, the timer gets reset. An overload occurs shortly after (OVL). The internal timer immediately starts to count when the 3.2−V level is crossed (V_{FB} with no OPP). As the overload lasts less than 200 ms (in this example the timer is set to 200 ms), the feedback returns to its regulation level and resets the timer.

In the second case, the overload occurs after regulation but the feedback voltage quickly jumps into the short−circuit area. At this point, the countdown is accelerated as the

charging slope changed to a steeper one. The load goes back to an OVL mode and the counter slows down. Finally, back to short circuit again and the timer trips the fault circuitry after completion: all pulses are immediately stopped and an auto−recovery double hiccup takes places.

The OVL timer is adjusted by wiring a resistor from pin 8 to ground. The below chart shows what value to adopt to fit your timer duration needs. Typically, a 22−kΩ pull−down resistor will set the OVL duration to 500 ms. In case of short−circuit, the duration will be reduced to 500/4 or 125 ms.

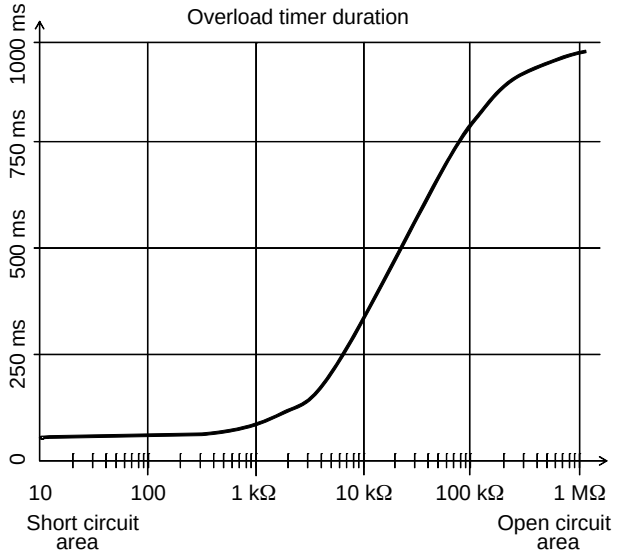


Figure 51. This curve shows how to program the OVL timer duration.

Please note that pin 8 includes a circuitry that manages the timer current in case of pin opening or shortening to ground. In both cases, the timer is set to known value as listed in the parameters sheet. The given duration is that of the OVL timer.

Brown Out Protection

Brown−out (BO) is a means to protect the converter against an erratic behavior that can occur at the lowest input voltage level. By safely stopping the output pulses when the mains is below a predetermined value, the converter prevents thermal runaway, greatly improving its robustness. Brown−out protection is another way to avoid an erratic hiccup mode when too low of an input voltage limits the power delivery. Some applications, such as printer power supplies, forbid this kind of operations and impose a clean stop. In that case, brown−out detection/protection is the way to go. Figure 52 shows a simplified implementation in the controller.

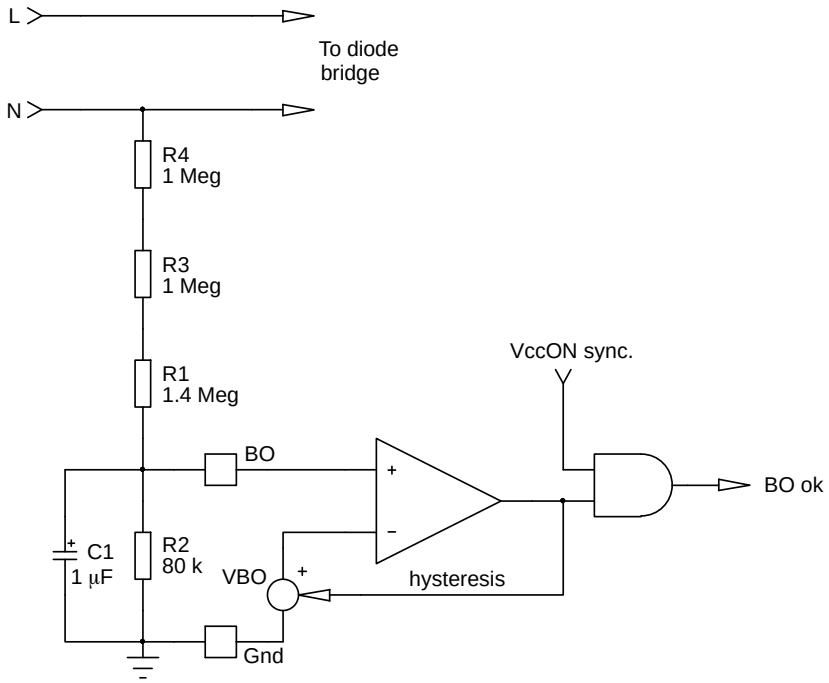


Figure 52. A simple comparator monitors the input voltage via a single pin. When this voltage is too low, the pulses are stopped and the V_{cc} hiccups.

To ensure a clean re−start, the BO information is only validated when V_{cc} reaches VCC_{ON}. This ensures a fully−charged V_{cc} capacitor when the controller pulses again. An asynchronous BO−related re−start could induce aborted start−up sequences if the V_{cc} capacitor would too close to the UVLO threshold.

From the above schematic, the calculation of the resistor is straightforward. We have connected the resistor to the input line and thus observe a single−wave signal peaking to $V_{in,peak}$. The average voltage seen on top of R_4 is thus:

$$V_{in,avg} = \frac{V_{in,peak}}{\pi} \quad \text{(eq. 26)}$$

Then, pick a bridge current compatible with the power consumption you can accept. If we chose 10 μA, the pull−down resistor R_2 calculation is straightforward:

$$R_2 = \frac{V_{BOon}}{I_{bridge}} = \frac{0.8}{10\ \mu} = 80\ k\Omega \quad \text{(eq. 27)}$$

Now suppose we want a typical turn−on voltage $V_{turn-on}$ of 78 V rms. From the two above equations, we can calculate the value of the upper resistive string:

$$R_{upper} = \frac{\left(\frac{V_{turn-on}\sqrt{2}}{\pi}\right) - V_{BOon}}{I_{bridge}} = \frac{\frac{78 \times 1.414}{3.14} - 0.8}{10\ \mu} = 3.4\ M\Omega \quad \text{(eq. 28)}$$

The hysteresis on the internal reference source is 200 mV typically. The ratio of the two voltages is 1.33. With the upper resistive network, the turn−off voltage can then easily be derived:

$$V_{turn-off} = \frac{V_{turn-on}}{1.33} = \frac{78}{1.33} \approx 59\ V\ rms \quad \text{(eq. 29)}$$

A 1−μF capacitor is necessary to filter out the input ripple. Reducing its value, hence allowing more ripple, can help to fine tune the hysteresis, if necessary.

When the controller senses a BO event, all pulses are immediately cut. An internal pull−down source (typically 1 mA) is activated and brings V_{cc} down towards UVLO. When this level is reached, the controller goes back into low−consumption mode and lifts V_{cc} up again. At VCC_{ON}, a check on the BO comparator is made: if the input level is correct, the part re−starts, if still too low, the 1−mA source brings V_{cc} down again. As a result, V_{cc} operates in hiccup mode during a BO event.

The below figure describes the typical waveforms obtained at start−up and in operation. Please note the synchronization of the BO validation with the VCC_{ON} point. This ensures a clean start−up sequence with a fully charged V_{cc} capacitor.

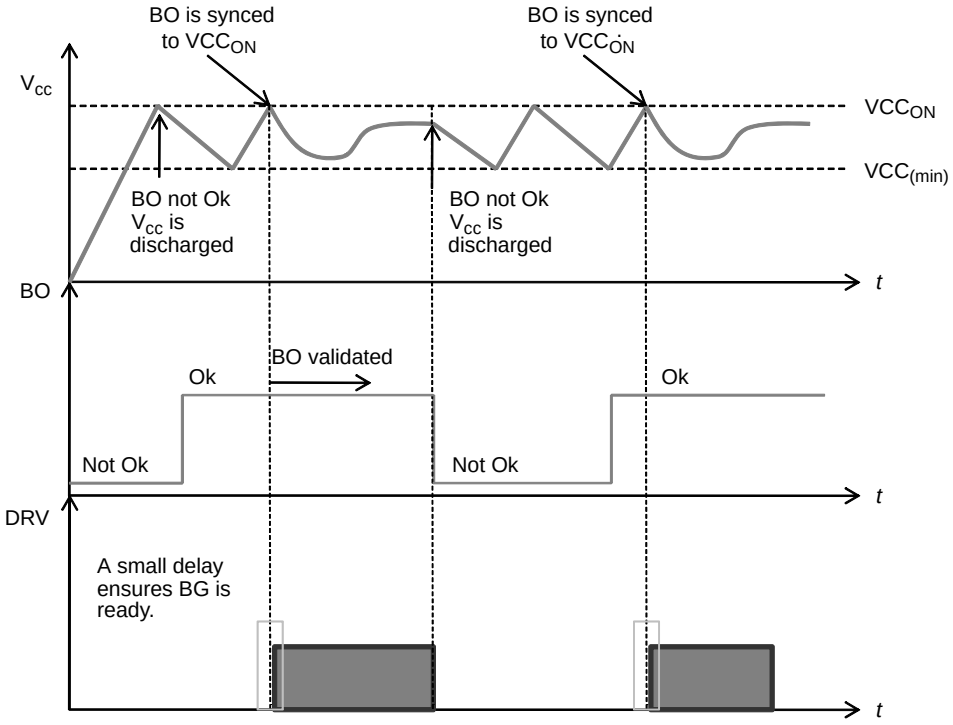


Figure 53. The brown−out recovery is always synchronized to the V_{cc} signal: when it reaches VCC_{ON}, the driver delivers the output pulses.

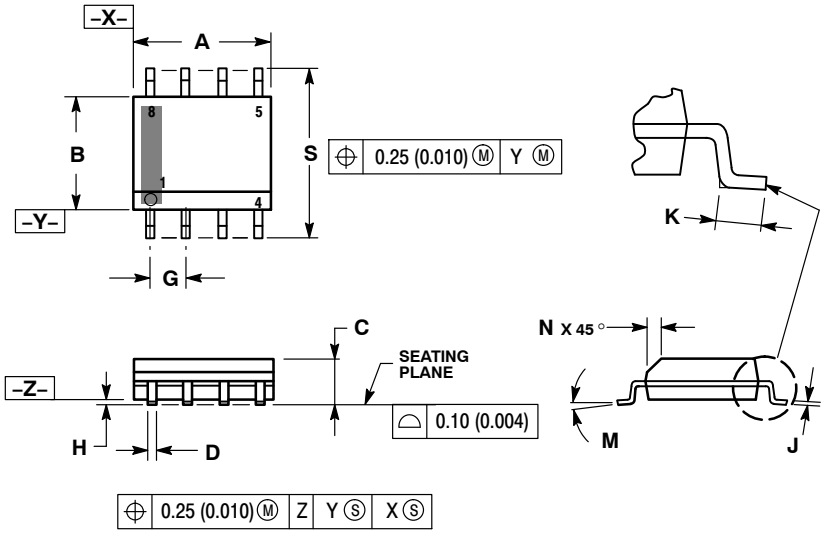
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS



SCALE 1:1

SOIC−8 NB
CASE 751−07
ISSUE AK

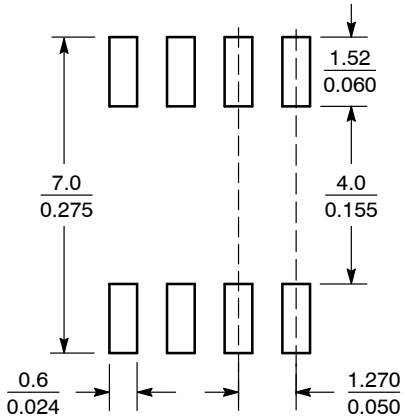
DATE 16 FEB 2011



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751−01 THRU 751−06 ARE OBSOLETE. NEW STANDARD IS 751−07.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0 °	8 °	0 °	8 °
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

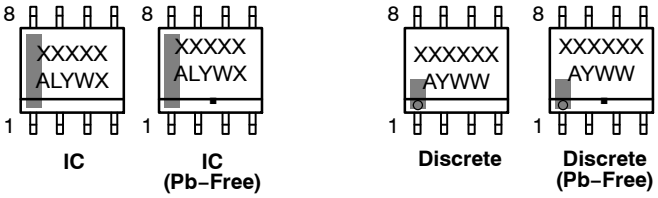
SOLDERING FOOTPRINT*



SCALE 6:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



IC | IC (Pb−Free) | Discrete | Discrete (Pb−Free)

XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

XXXXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

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SOIC−8 NB
CASE 751−07
ISSUE AK

DATE 16 FEB 2011

STYLE 1:
PIN 1. EMITTER
2. COLLECTOR
3. COLLECTOR
4. EMITTER
5. EMITTER
6. BASE
7. BASE
8. EMITTER

STYLE 2:
PIN 1. COLLECTOR, DIE, #1
2. COLLECTOR, #1
3. COLLECTOR, #2
4. COLLECTOR, #2
5. BASE, #2
6. EMITTER, #2
7. BASE, #1
8. EMITTER, #1

STYLE 3:
PIN 1. DRAIN, DIE #1
2. DRAIN, #1
3. DRAIN, #2
4. DRAIN, #2
5. GATE, #2
6. SOURCE, #2
7. GATE, #1
8. SOURCE, #1

STYLE 4:
PIN 1. ANODE
2. ANODE
3. ANODE
4. ANODE
5. ANODE
6. ANODE
7. ANODE
8. COMMON CATHODE

STYLE 5:
PIN 1. DRAIN
2. DRAIN
3. DRAIN
4. DRAIN
5. GATE
6. GATE
7. SOURCE
8. SOURCE

STYLE 6:
PIN 1. SOURCE
2. DRAIN
3. DRAIN
4. SOURCE
5. SOURCE
6. GATE
7. GATE
8. SOURCE

STYLE 7:
PIN 1. INPUT
2. EXTERNAL BYPASS
3. THIRD STAGE SOURCE
4. GROUND
5. DRAIN
6. GATE 3
7. SECOND STAGE Vd
8. FIRST STAGE Vd

STYLE 8:
PIN 1. COLLECTOR, DIE #1
2. BASE, #1
3. BASE, #2
4. COLLECTOR, #2
5. COLLECTOR, #2
6. EMITTER, #2
7. EMITTER, #1
8. COLLECTOR, #1

STYLE 9:
PIN 1. EMITTER, COMMON
2. COLLECTOR, DIE #1
3. COLLECTOR, DIE #2
4. EMITTER, COMMON
5. EMITTER, COMMON
6. BASE, DIE #2
7. BASE, DIE #1
8. EMITTER, COMMON

STYLE 10:
PIN 1. GROUND
2. BIAS 1
3. OUTPUT
4. GROUND
5. GROUND
6. BIAS 2
7. INPUT
8. GROUND

STYLE 11:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

STYLE 12:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 13:
PIN 1. N.C.
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 14:
PIN 1. N−SOURCE
2. N−GATE
3. P−SOURCE
4. P−GATE
5. P−DRAIN
6. P−DRAIN
7. N−DRAIN
8. N−DRAIN

STYLE 15:
PIN 1. ANODE 1
2. ANODE 1
3. ANODE 1
4. ANODE 1
5. CATHODE, COMMON
6. CATHODE, COMMON
7. CATHODE, COMMON
8. CATHODE, COMMON

STYLE 16:
PIN 1. EMITTER, DIE #1
2. BASE, DIE #1
3. EMITTER, DIE #2
4. BASE, DIE #2
5. COLLECTOR, DIE #2
6. COLLECTOR, DIE #2
7. COLLECTOR, DIE #1
8. COLLECTOR, DIE #1

STYLE 17:
PIN 1. VCC
2. V2OUT
3. V1OUT
4. TXE
5. RXE
6. VEE
7. GND
8. ACC

STYLE 18:
PIN 1. ANODE
2. ANODE
3. SOURCE
4. GATE
5. DRAIN
6. DRAIN
7. CATHODE
8. CATHODE

STYLE 19:
PIN 1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. MIRROR 2
7. DRAIN 1
8. MIRROR 1

STYLE 20:
PIN 1. SOURCE (N)
2. GATE (N)
3. SOURCE (P)
4. GATE (P)
5. DRAIN
6. DRAIN
7. DRAIN
8. DRAIN

STYLE 21:
PIN 1. CATHODE 1
2. CATHODE 2
3. CATHODE 3
4. CATHODE 4
5. CATHODE 5
6. COMMON ANODE
7. COMMON ANODE
8. CATHODE 6

STYLE 22:
PIN 1. I/O LINE 1
2. COMMON CATHODE/VCC
3. COMMON CATHODE/VCC
4. I/O LINE 3
5. COMMON ANODE/GND
6. I/O LINE 4
7. I/O LINE 5
8. COMMON ANODE/GND

STYLE 23:
PIN 1. LINE 1 IN
2. COMMON ANODE/GND
3. COMMON ANODE/GND
4. LINE 2 IN
5. LINE 2 OUT
6. COMMON ANODE/GND
7. COMMON ANODE/GND
8. LINE 1 OUT

STYLE 24:
PIN 1. BASE
2. EMITTER
3. COLLECTOR/ANODE
4. COLLECTOR/ANODE
5. CATHODE
6. CATHODE
7. COLLECTOR/ANODE
8. COLLECTOR/ANODE

STYLE 25:
PIN 1. VIN
2. N/C
3. REXT
4. GND
5. IOUT
6. IOUT
7. IOUT
8. IOUT

STYLE 26:
PIN 1. GND
2. dv/dt
3. ENABLE
4. ILIMIT
5. SOURCE
6. SOURCE
7. SOURCE
8. VCC

STYLE 27:
PIN 1. ILIMIT
2. OVLO
3. UVLO
4. INPUT+
5. SOURCE
6. SOURCE
7. SOURCE
8. DRAIN

STYLE 28:
PIN 1. SW_TO_GND
2. DASIC_OFF
3. DASIC_SW_DET
4. GND
5. V_MON
6. VBULK
7. VBULK
8. VIN

STYLE 29:
PIN 1. BASE, DIE #1
2. EMITTER, #1
3. BASE, #2
4. EMITTER, #2
5. COLLECTOR, #2
6. COLLECTOR, #2
7. COLLECTOR, #1
8. COLLECTOR, #1

STYLE 30:
PIN 1. DRAIN 1
2. DRAIN 1
3. GATE 2
4. SOURCE 2
5. SOURCE 1/DRAIN 2
6. SOURCE 1/DRAIN 2
7. SOURCE 1/DRAIN 2
8. GATE 1

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