NCP1596A

1.5 A, 1.5 MHz Current Mode PWM Buck Down Converter

The NCP1596A is a current mode PWM buck converter with integrated power switch. It can provide up to 1.5 A output current with high conversion efficiency. High frequency PWM control scheme can provide a low output ripple noise. Thus, it allows the usage of small size passive components to reduce the board space. In a low load condition, the controller will automatically change to PFM mode which provides a higher efficiency at low load. Additionally, the device includes soft−start, thermal shutdown with hysteresis, cycle−by−cycle current limit, and short circuit protection. This device is available in a compact 3x3 DFN package.

Features

- High Efficiency up to 90%, 1 A @ 3.3 V, 75% @ 1.2 V
- Fully Internal Compensation
- Low Output Voltage Ripple, 20 mV Typical
- ±1.5% Reference Voltage
- High PWM Switching Frequency, 1.5 MHz
- Automatic PWM / PFM Switchover at Light Load
- Built−in 1 ms Digital Soft Start
- Cycle−by−cycle Current Limit
- Thermal Shutdown with Hysteresis
- Internal UVLO Protection
- Ext. Adjustable Output Voltage
- Low Profile and Minimum External Components
- Designed for use with Ceramic Capacitor
- Compact 3x3 DFN Package
- These are Pb−Free Devices

Typical Applications

- Hard Disk Drives
- USB Power Device
- Wireless and DSL Modems

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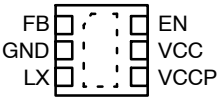
6 PIN DFN 3x3
MN SUFFIX
CASE 506AH

MARKING DIAGRAM



1596A = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1596AMNTWG	DFN6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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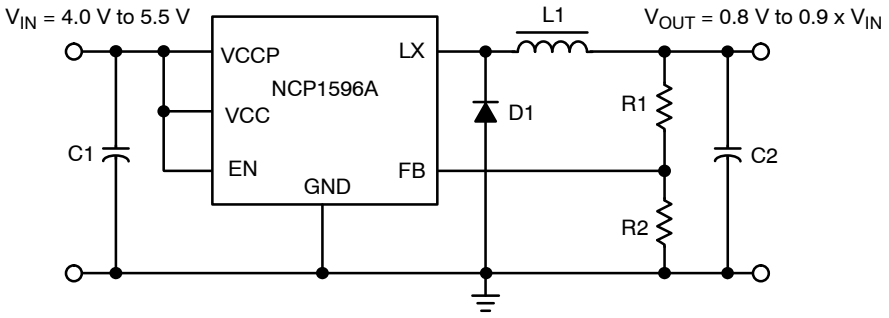


Figure 1. Typical Operating Circuit

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply (Pins 4, 5)	V_{IN}	6.0 −0.3 (DC) −1.0 (100 ns)	V
Input / Output Pins Pins 1, 3, 6	V_{IO}	6.0 −0.3 (DC) −1.0 (100 ns)	V
Thermal Characteristics 3x3 DFN Plastic Package Maximum Power Dissipation @ T_A = 25°C Thermal Resistance Junction−to−Ambient 0 lfpm	 P_D $R_{\theta JA}$	 1450 68.5	 mW °C/W
Operating Junction Temperature Range (Note 4)	T_J	−40 to +150	°C
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Temperature Soldering (10 sec)		230	°C
Moisture Sensitivity Level (Note 3)	MSL	1	−

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

NOTE: ESD data available upon request.

1. This device series contains ESD protection and exceeds the following tests:
   Human Body Model (HBM) 2.0 kV per JEDEC standard: JESD22−A114.
   Machine Model (MM) 200 V per JEDEC standard: JESD22−A115.
2. Latch−up Current Maximum Rating: 150 mA per JEDEC standard: JESD78.
3. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
4. The maximum package power dissipation limit must not be exceeded.

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

ELECTRICAL CHARACTERISTICS

(V_{IN} = 5.0 V, V_{OUT} = 1.2 V, T_A = 25°C for typical value, −40°C ≤ T_A ≤ 85°C for min/max values unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Operating Voltage	V_{IN}	4.0	–	5.5	V
Under Voltage Lockout Threshold	V_{UVLO}	3.2	3.5	3.8	V
Under Voltage Lockout hysteresis	V_{UVLO_HYS}	–	180	–	mV
PFET Leakage Current (Pins 5, 4) T_A = 25°C T_A = −40°C to 85°C	I_{LEAK-P}	 – –	 1.0 –	 10 15	µA
FEEDBACK VOLTAGE					
FB Input Threshold (T_A = −40°C to 85°C)	V_{FB}	0.788	0.800	0.812	V
FB Input Current	I_{FB}	–	10	100	nA
THERMAL SHUTDOWN					
Thermal Shutdown Threshold (Note 5)	T_{SHDN}	–	160	–	°C
Hysteresis (Note 5)	T_{SDHYS}	–	30	–	°C
PWM SMPS MODE					
Switching Frequency (T_A = −40°C to 85°C)	F_{OSC}	1.27	1.5	1.725	MHz
Internal PFET ON−Resitance (I_{LX} = 100 mA, V_{IN} = 5.0 V, T_A = 25°C) (Note 5)	$R_{DS(on)_P}$	–	0.2	0.3	Ohm
Minimum Duty Cycle	D_{MIN}	–	0	–	%
Maximum Duty Cycle	D_{MAX}	–	100	–	%
Soft−Start Time (V_{IN} = 5.0 V, V_o = 1.2 V, I_{LOAD} = 0 mA, T_A = 25°C)	T_{SS}	0.8	1.0	1.2	ms
Main PFET Switch Current Limit (Note 5)	I_{LIM}	2.0	2.5	–	A
ENABLE					
Enable Threshold High	V_{EN_H}	1.8	–	–	V
Enable Threshold Low	V_{EN_L}	–	–	0.4	V
Enable bias current (EN = 0 V)	I_{EN}	–	500	–	nA
EFFICIENCY					
Output Load Current 10 mA @ 1.2 V (Note 5)	η	–	50	–	%
Output Load Current 100 mA to 1.2 A @ 1.2 V (Note 5)	η	–	70	–	%
TOTAL DEVICE					
Quiescent Current Into V_{CCP} (V_{IN} = 5 V, V_{FB} = 1.0 V, T_A = 25°C)	I_{CCP}	–	10	–	µA
Quiescent Current Into V_{CC} (V_{IN} = 5 V, V_{FB} = 1.0 V, T_A = 25°C)	I_{CC}	–	500	–	µA
Shutdown Quiescent Current into V_{CC} and V_{CCP} (EN = 0, V_{IN} = 5 V, V_{FB} = 1.0 V, T_A = 25°C)	I_{CC_SD}	–	1.0	3.0	µA

5. Values are design guaranteed.

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	FB	Feedback pin. Part is internally compensated. Only necessary to place a voltage divider or connect the output directly to this pin.
2	GND	Ground
3	LX	Pin connected internally to power switch. Connect externally to inductor.
4	VCCP	Power connection to the power switch.
5	VCC	IC power connection.
6	EN	Device Enable pin. This pin has an internal current source pull up. No connect is enable the device. With this pin pulled down below 0.8 V, the device is disabled and enters the shutdown mode.

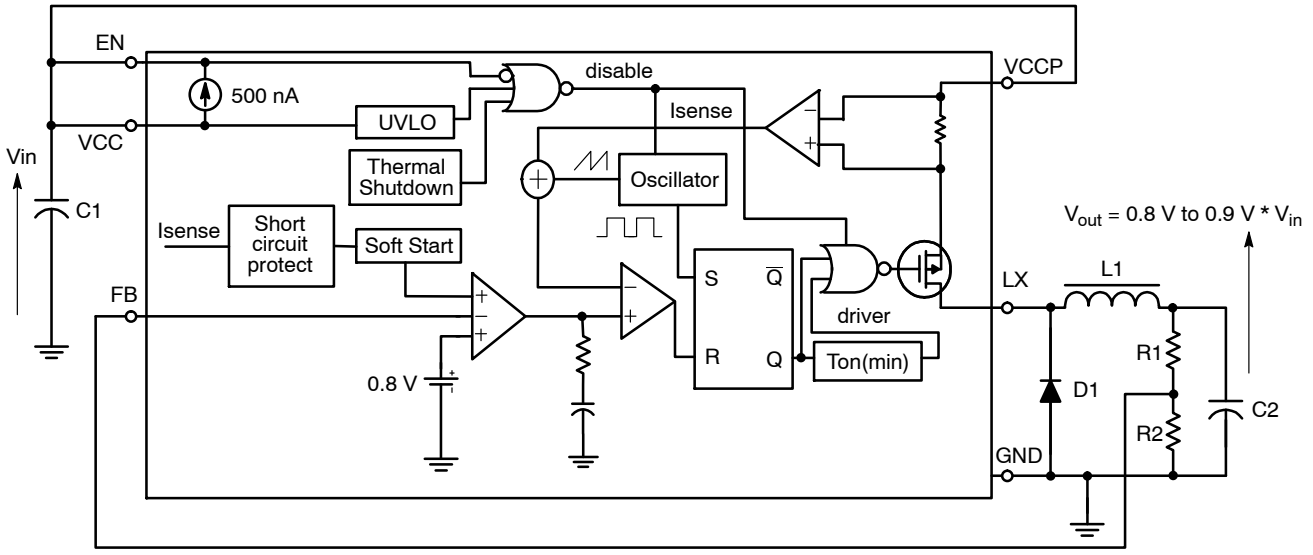


Figure 2. Detail Block Diagram

EXTERNAL COMPONENT REFERENCE DATA

V_{OUT}	Inductor Model	Inductor (L1)	Diode (D1)	C_{IN} (C1)	C_{OUT} (C2)	R1	R2
3.3 V	CDC5D23 3R3 (1 A) CDRH6D38 3R3 (1.5 A)	3.3 μH	MBRA210LT3G	22 μF 22 μF x 2	22 μF 22 μF x 2	31 k	10 k
2.5 V	CDC5D23 3R3 (1 A) CDRH6D38 3R3 (1.5 A)	3.3 μH	MBRA210LT3G	22 μF 22 μF x 2	22 μF 22 μF x 2	21 k	10 k
1.5 V	CDC5D23 3R3 (1 A) CDRH6D38 3R3 (1.5 A)	3.3 μH	MBRA210LT3G	22 μF 22 μF x 2	22 μF 22 μF x 2	8 k	10 k
1.2 V	CDC5D23 3R3 (1 A) CDRH6D38 3R3 (1.5 A)	3.3 μH	MBRA210LT3G	22 μF 22 μF x 2	22 μF 22 μF x 2	5 k	10 k

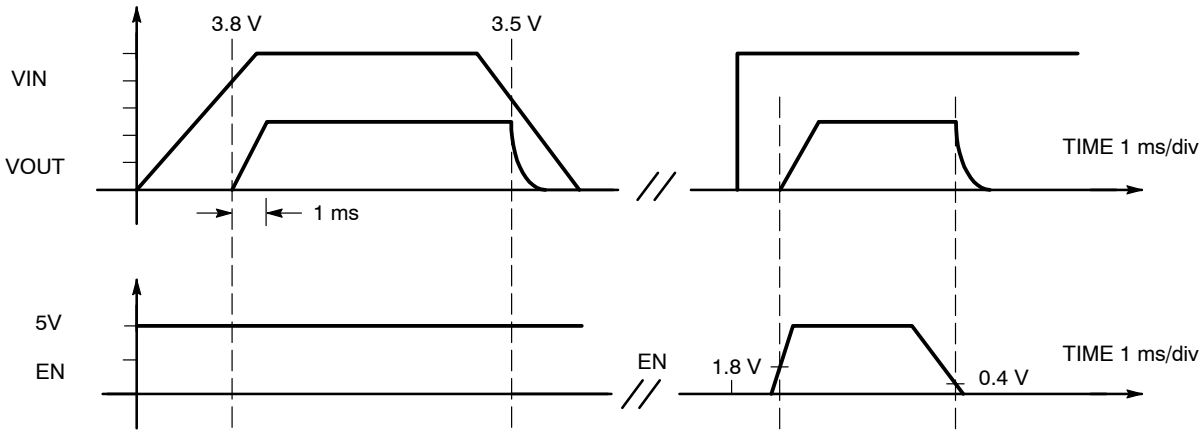


Figure 3. Timing Diagram

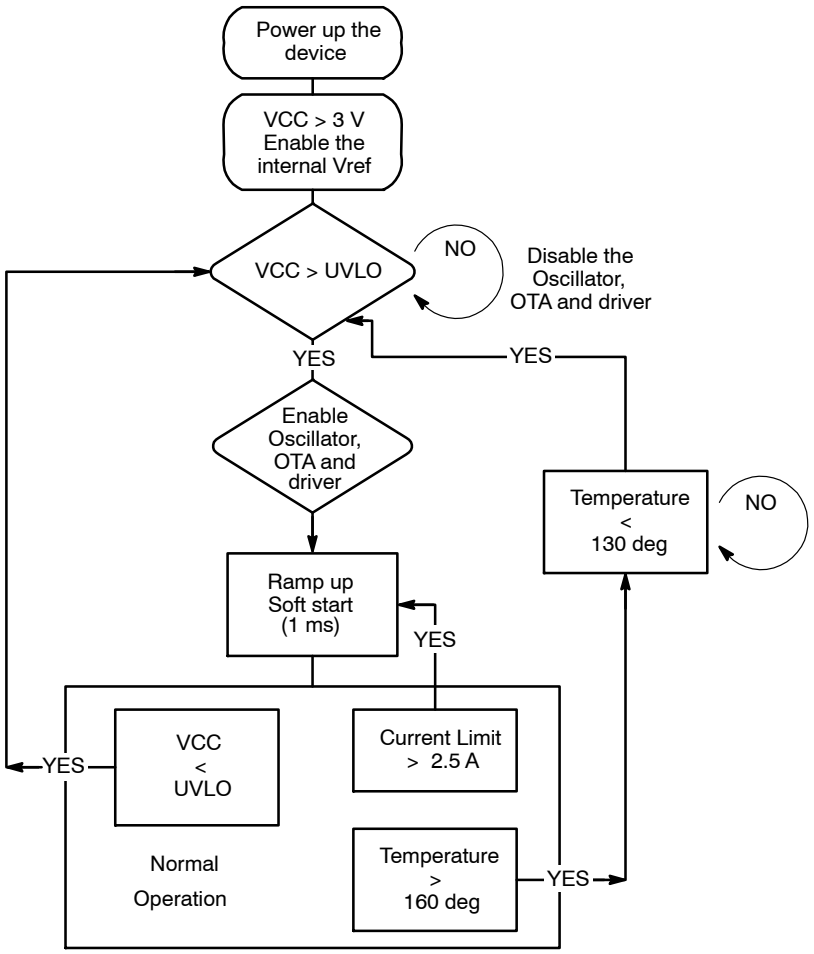


Figure 4. State Diagram

TYPICAL OPERATING CHARACTERISTICS

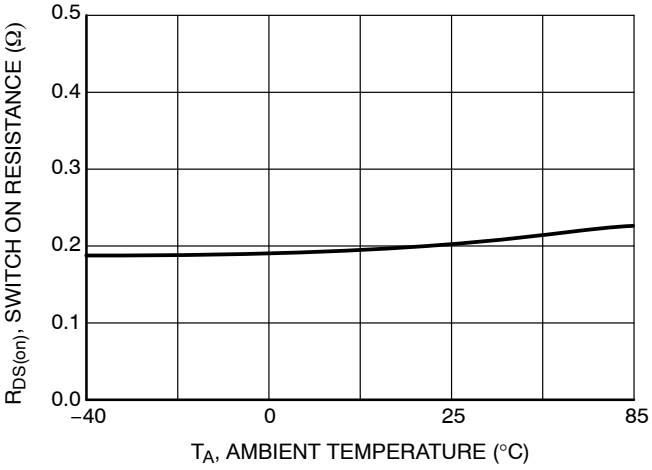


Figure 5. Switch ON Resistance vs. Temperature

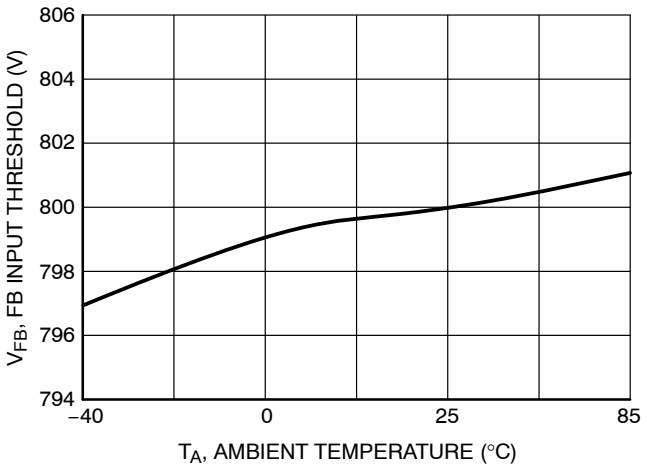


Figure 6. Feedback Input Threshold vs. Temperature

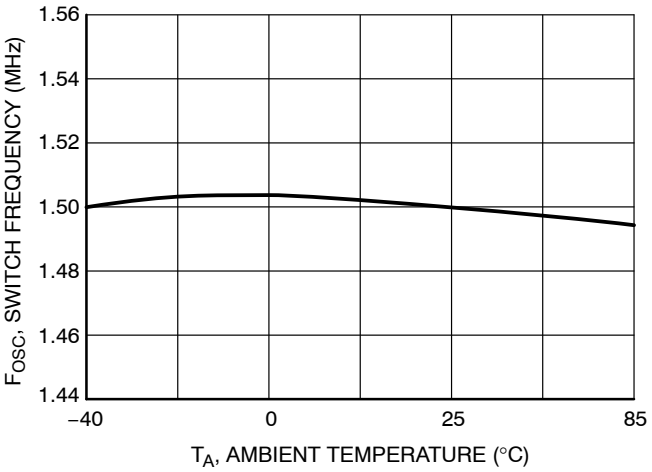


Figure 7. Switching Frequency vs. Temperature

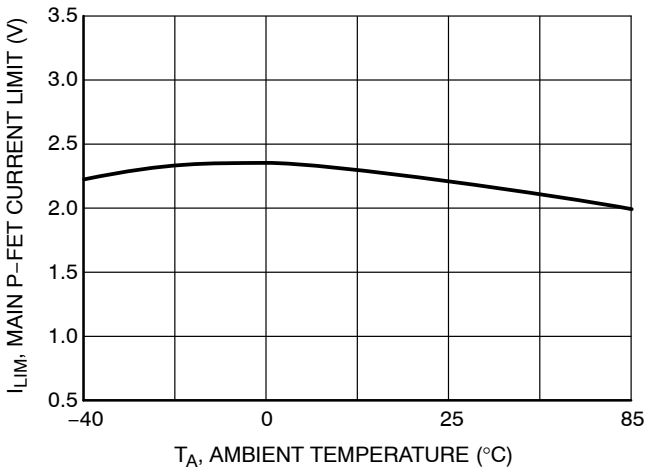


Figure 8. Main P−FET Current Limit vs. Temperature

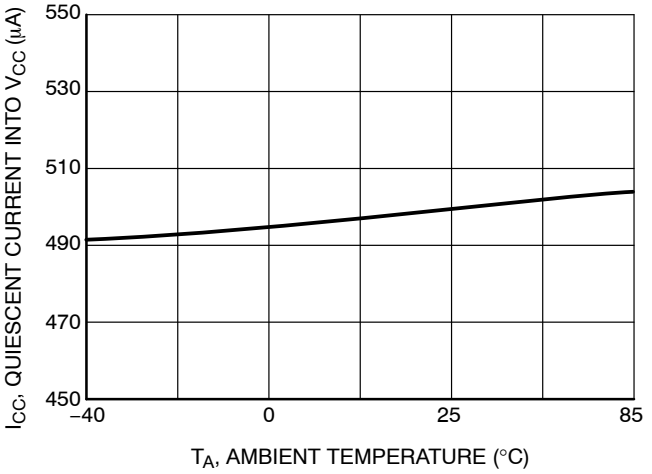


Figure 9. Quiescent Current Into V_{CC} vs. Temperature

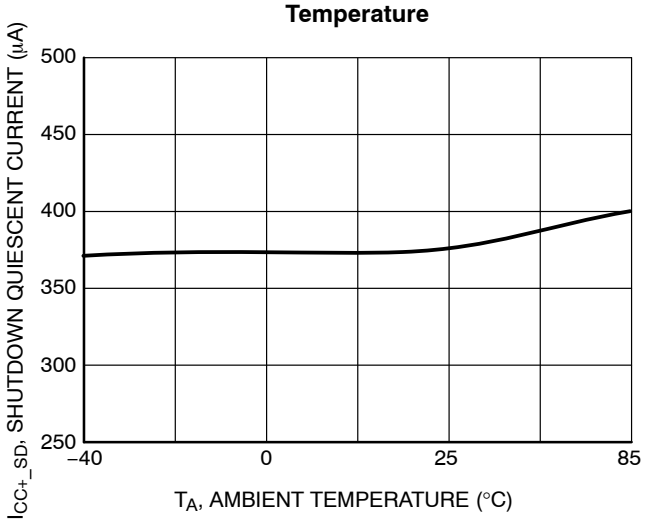


Figure 10. Shutdown Quiescent Current vs. Temperature

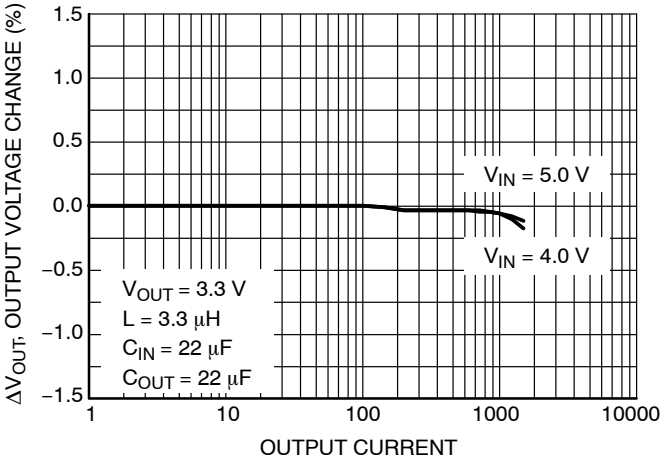


Figure 11. Output Voltage Change vs. Output Current

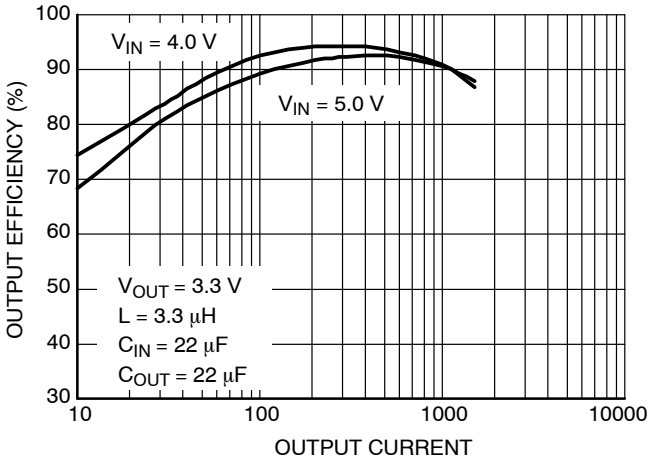


Figure 12. Efficiency vs. Output Current

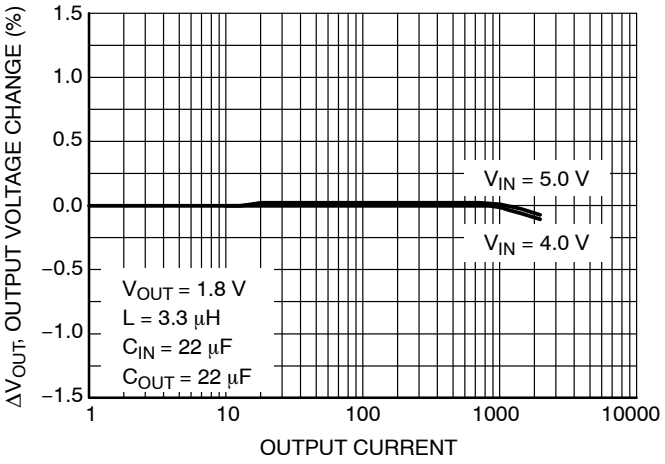


Figure 13. Output Voltage Change vs. Output Current

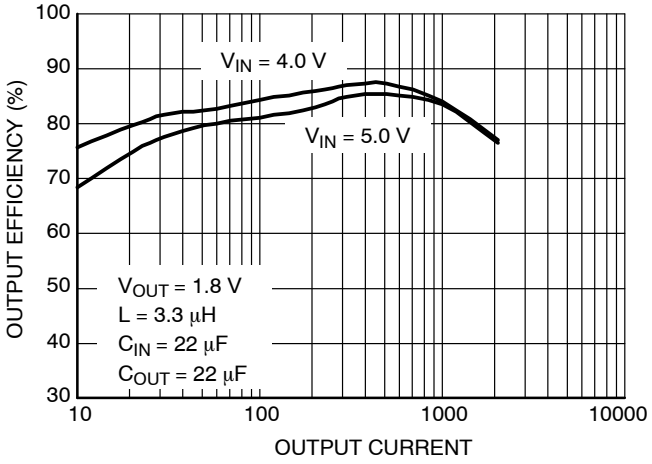


Figure 14. Efficiency vs. Output Current

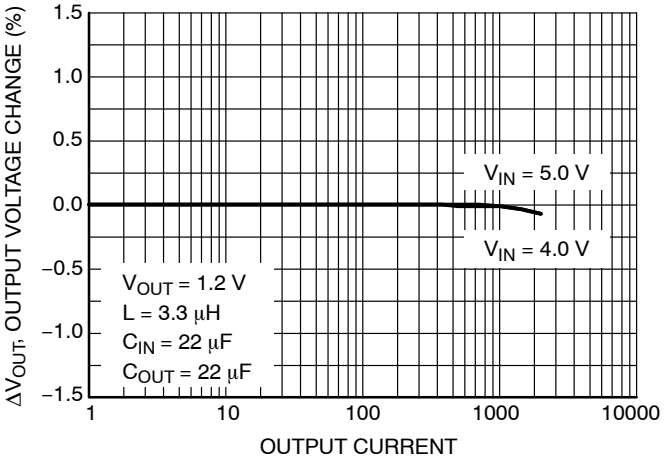


Figure 16. Output Voltage Change vs. Output Current

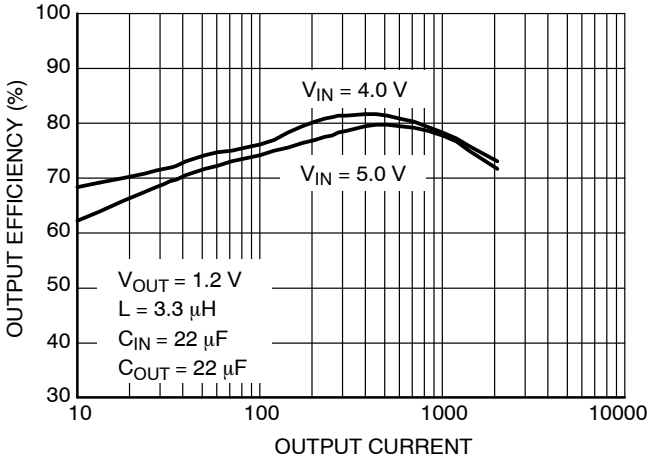
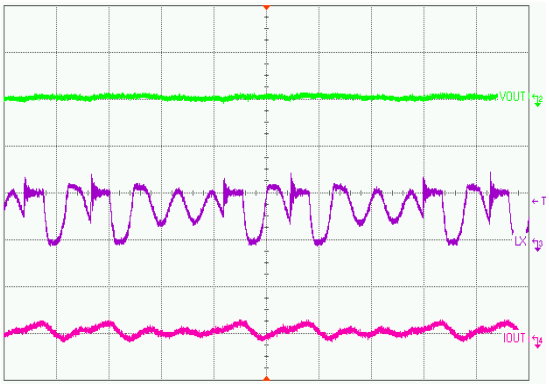
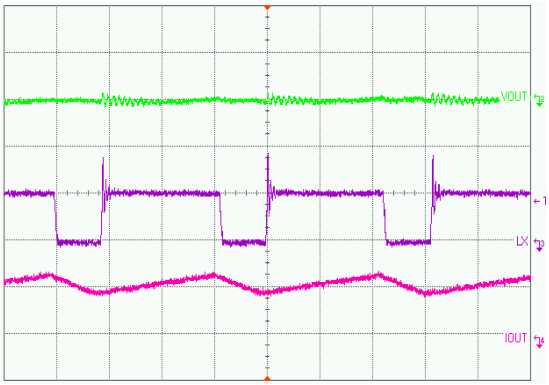


Figure 15. Efficiency vs. Output Current



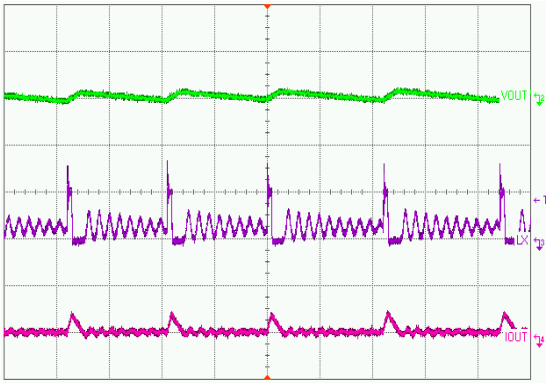
(V_{IN} = 5 V, I_{LOAD} = 10 mA, L = 3.3 μH, C_{OUT} = 20 μF)
Upper Trace: Output Ripple Voltage, 20 mV/div
Middle Trace: L_X Pin Switching Waveform, 5 V/div
Lower Trace: Inductor Current Waveform, 500 mA/div
Time Base: 500 ns/div

Figure 17. DCM Switching Waveform for V_{OUT} = 3.3 V



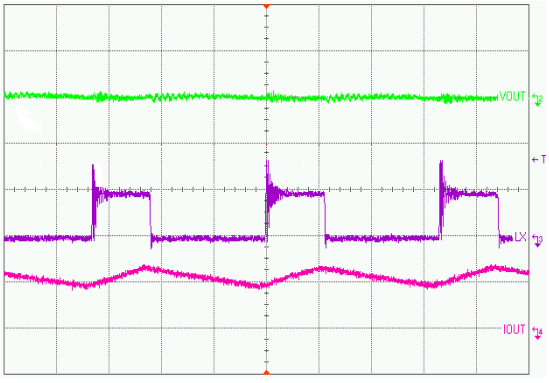
(V_{IN} = 5 V, I_{LOAD} = 500 mA, L = 3.3 μH, C_{OUT} = 20 μF)
Upper Trace: Output Ripple Voltage, 20 mV/div
Middle Trace: L_X Pin Switching Waveform, 5 V/div
Lower Trace: Inductor Current Waveform, 500 mA/div
Time Base: 200 ns/div

Figure 18. CCM Switching Waveform for V_{OUT} = 3.3 V



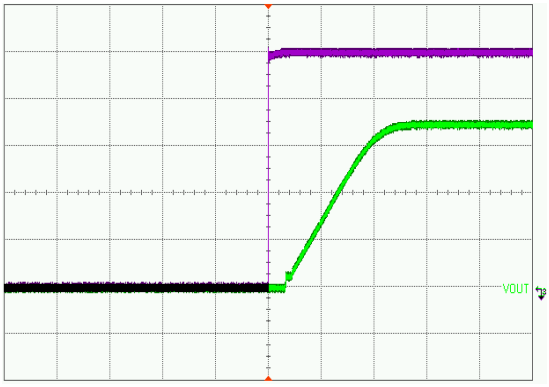
(V_{IN} = 5 V, I_{LOAD} = 10 mA, L = 3.3 μH, C_{OUT} = 20 μF)
Upper Trace: Output Ripple Voltage, 20 mV/div
Middle Trace: L_X Pin Switching Waveform, 5 V/div
Lower Trace: Inductor Current Waveform, 500 mA/div
Time Base: 2 μs/div

Figure 19. DCM Switching Waveform for V_{OUT} = 1.2 V



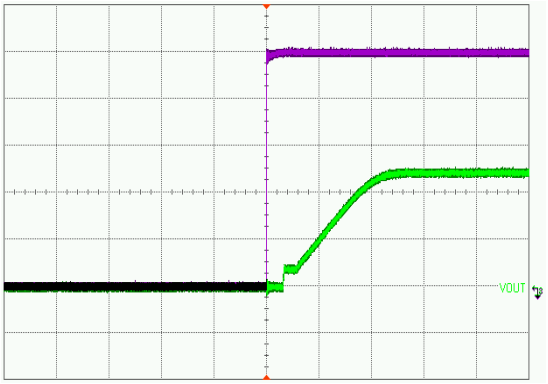
(V_{IN} = 5 V, I_{LOAD} = 500 mA, L = 3.3 μH, C_{OUT} = 20 μF)
Upper Trace: Output Ripple Voltage, 20 mV/div
Middle Trace: L_X Pin Switching Waveform, 5 V/div
Lower Trace: Inductor Current Waveform, 500 mA/div
Time Base: 200 ns/div

Figure 20. CCM Switching Waveform for V_{OUT} = 1.2 V



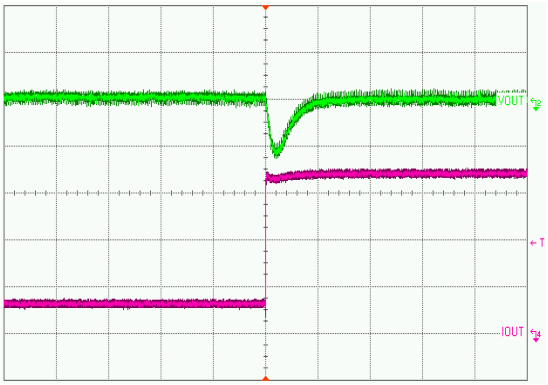
(V_{IN} = 5 V, I_{LOAD} = 10 mA, L = 3.3 μH, C_{OUT} = 20 μFx2)
Upper Trace: Input Voltage, 1 V/div
Lower Trace: Output Voltage, 1 V/div
Time Base: 500 μs/div

Figure 21. Soft−Start Waveforms for V_{OUT} = 3.3 V



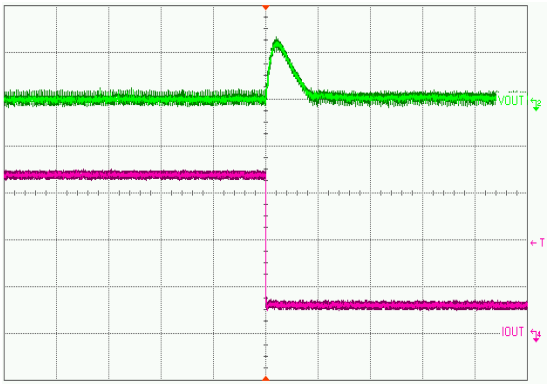
(V_{IN} = 5 V, I_{LOAD} = 10 mA, L = 3.3 μH, C_{OUT} = 20 μFx2)
Upper Trace: Input Voltage, 1 V/div
Lower Trace: Output Voltage, 500 mV/div
Time Base: 500 μs/div

Figure 22. Soft−Start Waveforms for V_{OUT} = 1.2 V



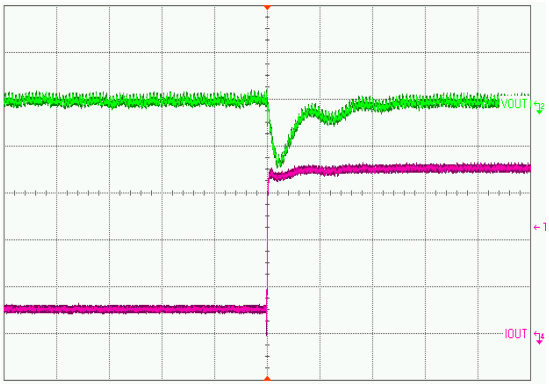
(V_{IN} = 5 V, L = 3.3 μH, C_{OUT} = 10 μFx2)
Upper Trace: Output Dynamic Voltage, 100 mV/div
Lower Trace: Output Current, 200 mA/div
Time Base: 20 ns/div

Figure 23. Load Regulation for V_{OUT} = 3.3 V



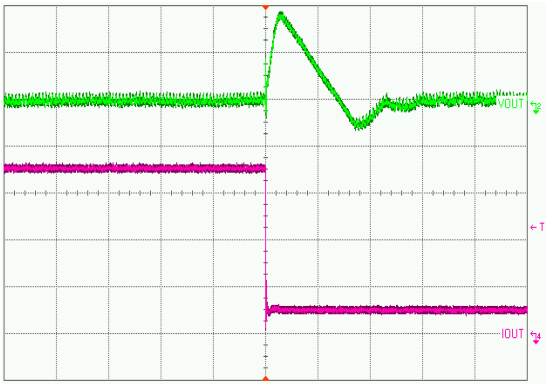
(V_{IN} = 5 V, L = 3.3 μH, C_{OUT} = 10 μFx2)
Upper Trace: Output Dynamic Voltage, 100 mV/div
Lower Trace: Output Current, 200 mA/div
Time Base: 20 ns/div

Figure 24. Load Regulation for V_{OUT} = 3.3 V



(V_{IN} = 5 V, L = 3.3 H, C_{OUT} = 10 μFx2)
Upper Trace: Output Dynamic Voltage, 50 mV/div
Lower Trace: Output Current, 200 mA/div
Time Base: 10 ns/div

Figure 25. Load Regulation for V_{OUT} = 1.2 V



(V_{IN} = 5 V, L = 3.3 H, C_{OUT} = 10 μF x 2)
Upper Trace: Output Dynamic Voltage, 50 mV/div
Lower Trace: Output Current, 200 mA/div
Time Base: 10 ns/div

Figure 26. Load Regulation for V_{OUT} = 1.2 V

DETAILED OPERATING DESCRIPTION

Introduction

The NCP1596A is a current−mode buck converter with switching frequency at 1.5 MHz. High operation frequency can reduce the capacitor value and PCB area. Also, more features are built in this converter.

1. Internal 1 ms soft−start to avoid inrush current at startup.
2. Internal cycle by cycle current limit provides an output short circuit protection.
3. Internal compensation. No external compensation components are necessary.
4. Thermal shutdown protects the devices from over heat.
5. 100% duty cycle allowed. Speed up transient load response.

The upper feature can provide more cost effective solutions to applications. A simple function block diagram and timing diagram are shown in Figure 1 and Figure 2.

Soft−Start and Current Limit

A soft start circuit is internally implemented to reduce the in−rush current during startup. This helps to reduce the output voltage over−shoot.

The current limit is set to allow peak switch current in excess of 2 A. The intended output current of the system is 1.5 A. The ripple current is calculated to be approximately 350 mA with a 3.3 μH inductor. Therefore, the peak current at 1.5 A output will be approximately 1.7 Amps. A 2.5 Amp set point will allow for transient currents during load step. The current limit circuit is implemented as a cycle−by−cycle current limit. Each on−cycle is treated as a separate situation. Current limiting is implemented by monitoring the P−channel switch current buildup during conduction with a current limit comparator. The output of the current limit comparator resets the PWM latch, immediately terminating the current cycle. When output loading is short circuit, device will auto restart with soft−start.

Error Amplifier and Slope Compensation

A fully internal compensated error amplifier is provided inside NCP1596A. No external circuitry is needed to stabilize the device. The error amplifier provides an error signal to the PWM comparator by comparing the feedback voltage (800 mV) with internal voltage reference of 1.2 V.

Current mode converter can exhibit instability at duty cycles over 50%. A slope compensation circuit is provided inside NCP1596A to overcome the potential instability. Slope compensation consists of a ramp signal generated by the synchronization block and adding this to the inductor current signal. The summed signal is then applied to the PWM comparator.

Thermal Shutdown

Internal Thermal Shutdown circuitry is provided to protect the integrated circuit in the event when maximum junction temperature is exceeded. When activated, typically at 180°C, the shutdown signal will disable the P−channel switch. The thermal shutdown circuit is designed with 30°C of hysteresis. This means that the switching will not start until the die temperature drops by this amount. This feature is provided to prevent catastrophic failures from accidental device overheating. **It is not intended as a substitute for proper heat sinking**. NCP1596A is contained in the thermally enhanced QFN package.

Under Voltage Lockout (UVLO)

UVLO function is used to ensure the logic level correctly when input voltage is very low. In NCP1596A, the UVLO level is set to 3.5 V. If the input voltage is less than 3.5 V, the converter will shutdown itself automatically.

Low Power Shutdown Mode (EN)

NCP1596A can be disabled whenever the EN pin is tied to ground. During the shutdown mode, the internal reference, oscillator and driver control circuits will be turn off, the device only consume 1 μA typically and output voltage will be discharge to zero by the external resistor divider. EN pin has an internal pull−up current source, which typical value is 500 nA.

Power Saving Pulse−Frequency−Modulation (PFM) Control Scheme

While the converter loading decreases, the converter enters the Discontinues−conduction−mode (DCM) operation. In DCM operation, the on−time (T_{on}) of the integrated switch for each switching cycle will decrease when the output current decreases. In order to maintain a high converter efficiency at light load condition. A minimum T_{on} is set to 70 ns. It can make sure a minimum fixed power send to output. To avoid a higher switch loss occurs when without loading apply. This control scheme can reduce the switching loss at light load and improve the conversion efficiency.

APPLICATION INFORMATION

Output Voltage Selection

The output voltage is programmed through an external resistor divider connect from V_{OUT} to FB then to GND.

For internal compensation and noise immunity, the resistor from FB to GND should be in 10 k to 20 k ranges. The relationship between the output voltage and feedback resistor is given by:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) \quad \text{(eq. 1)}$$

V_{OUT}: Output voltage
V_{FB}: Feedback Voltage
R1: Feedback resistor from V_{OUT} to FB.
R2: Feedback resistor from FB to GND.

Input Capacitor Selection

In the PWM buck converter, the input current is pulsating current with switching noise. Therefore, a bypass input capacitor must choose for reduce the peak current drawn from the power supply. For NCP1596A, low ESR ceramic capacitor of 10 μF should be used for most of cases. Also, the input capacitor should be placed as close as possible to the V_{CCA} pin for effective bypass the supply noise.

Inductor Selection

The inductor parameters are including three items, which are DC resistance, inductor value and saturation current. Inductor DC resistance will effect the convector overall efficiency, low DC resistor value can provide a higher efficiency. Thus, inductor value are depend on the inductor ripple current, input voltage, output voltage, output current and operation frequency, the inductor value is given by:

$$\Delta_{IL} = \frac{V_{OUT}}{L \times F_{SW}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad \text{(eq. 2)}$$

ΔIL : peak to peak inductor ripple current
L: inductor value
FSW: switching frequency

After selected a suitable value of the inductor, it should be check out the inductor saturation current. The saturation current of the inductor should be higher than the maximum load plus the ripple current.

$$\Delta_{IL(MAX)} = \Delta_{IOUT(MAX)} + \frac{\Delta_{IL}}{2} \quad \text{(eq. 3)}$$

$\Delta_{IL(MAX)}$: Maximum inductor current
$\Delta_{IOUT(MAX)}$: Maximum output current

Output Capacitor Selection

Output capacitor value is based on the target output ripple voltage. For NCP1596A, the output capacitor is required a ceramic capacitors with low ESR value. Assume buck converter duty cycle is 50%. The output ripple voltage in PWM mode is given by:

$$\Delta_{VOUT} \approx \Delta_{IL} \times \left(\frac{1}{4 \times FSW \times C_{OUT}} + ESR\right) \quad \text{(eq. 4)}$$

In general, value of ceramic capacitor using 20 μF should be a good choice.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

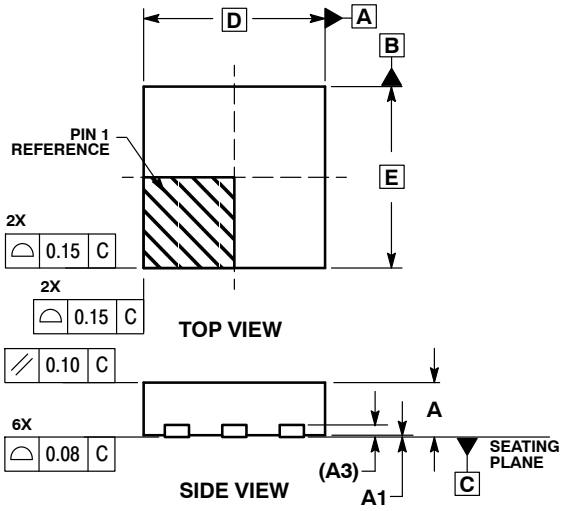


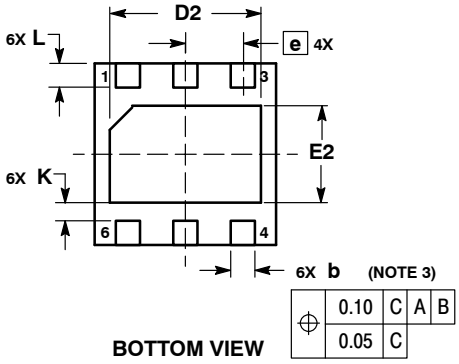
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SCALE 2:1

DFN6 3*3 MM, 0.95 PITCH
CASE 506AH−01
ISSUE O

DATE 17 NOV 2004

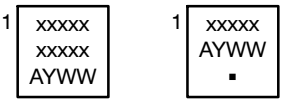




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.35	0.40	0.45
D		3.00 BSC	
D2	2.40	2.50	2.60
E		3.00 BSC	
E2	1.50	1.60	1.70
e		0.95 BSC	
K	0.21	---	---
L	0.30	0.40	0.50

GENERIC MARKING DIAGRAM*

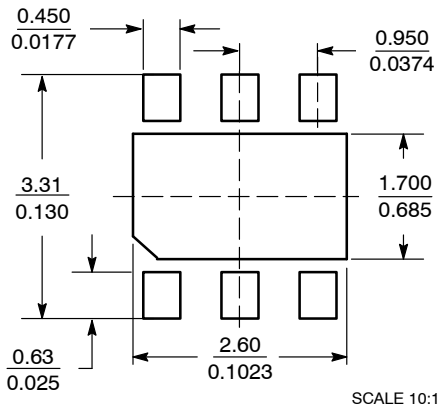


Standard **Pb−Free**

xxxxx	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



SCALE 10:1 (mm / inches)

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**DFN6 3*3 MM, 0.95 PITCH, SINGLE FLAG**	**PAGE 1 OF 1**

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