NCP1599

Buck Regulator - Synchronous

1 MHz, 3 A

The NCP1599 is a fixed 1 MHz, high−output−current, synchronous PWM converter that integrates a low−resistance, high−side P−channel MOSFET and a low−side N−channel MOSFET. The NCP1599 utilizes internally compensated current mode control to provide good transient response, ease of implementation, and excellent loop stability.

The NCP1599 includes an internally fixed switching frequency (Fsw), and an internal soft−start to limit inrush current.

Other features include cycle−by−cycle current limiting, short−circuit protection, power saving mode and thermal shutdown.

Features

- Internal 140 mΩ High−Side P−Channel and 90 mΩ Low−Side N−Channel MOSFET
- Fixed 1 MHz Switching Frequency
- Cycle−by−Cycle Current Limiting
- Hiccup Mode Short−Circuit Protection
- Overtemperature Protection
- Internal Soft−Start
- Start−up with Pre−Biased Output Load
- Adjustable Output Voltage Down to 0.8 V
- Power Saving Mode During Light Load
- These are Pb−Free Devices

Applications

- DSP Power
- Hard Disk Drivers
- Computer Peripherals
- Home Audio
- Set−Top Boxes
- Networking Equipment
- LCD TV
- Wireless and DSL/Cable Modem
- USB Power Devices

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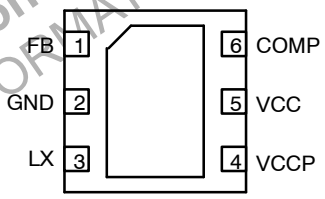
DFN6
CASE 506AH

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NCP1599MNTWG	DFN6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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BLOCK DIAGRAM

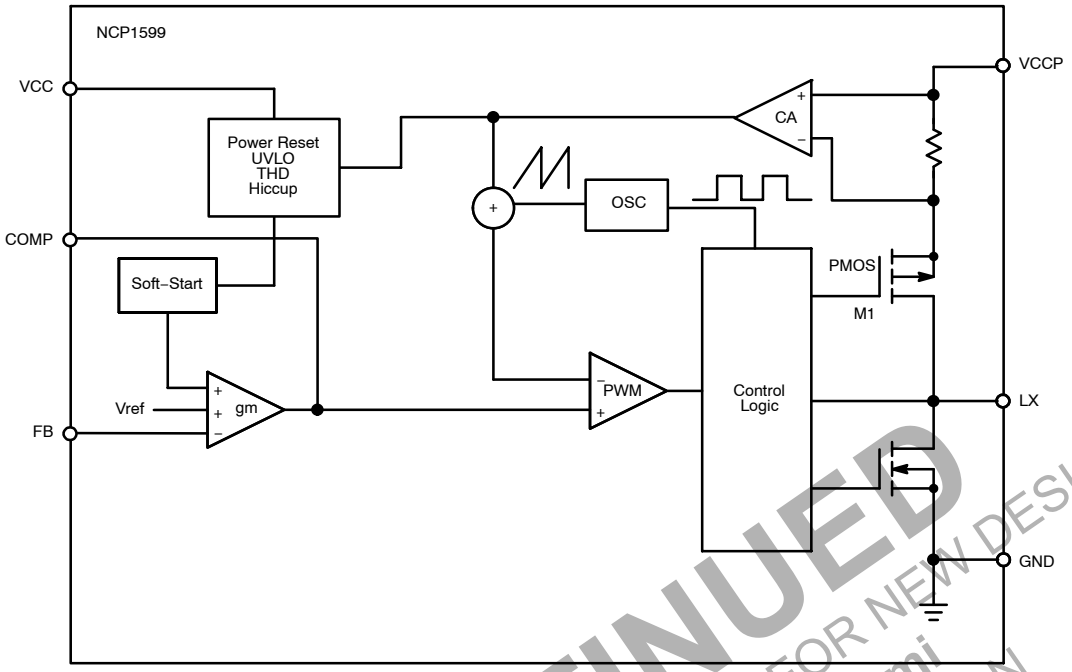


Figure 1. Block Diagram

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PIN DESCRIPTIONS

Pin No	Symbol	Description
1	FB	Feedback input pin of the Error Amplifier. Connect a resistor divider from the converter's output voltage to this pin to set the converter's output voltage.
2	GND	Ground pin. Connect to thermal pad.
3	LX	The drains of the internal MOSFETs. The output inductor should be connected to this pin.
4	V_{CCP}	Power input for the power stage
5	V_{CC}	Input supply pin for internal bias circuitry. A 0.1 μF ceramic bypass capacitor is preferred to connect to this pin.
6	COMP	Output of the Gm Amplifier and compensation node. Connect a series R−C network from this pin to GND for control loop regulation.
EP	PAD	Exposed pad of the package provides both electrical contact to the ground and good thermal contact to the PCB. This pad must be soldered to the PCB for proper operation.

APPLICATION CIRCUIT

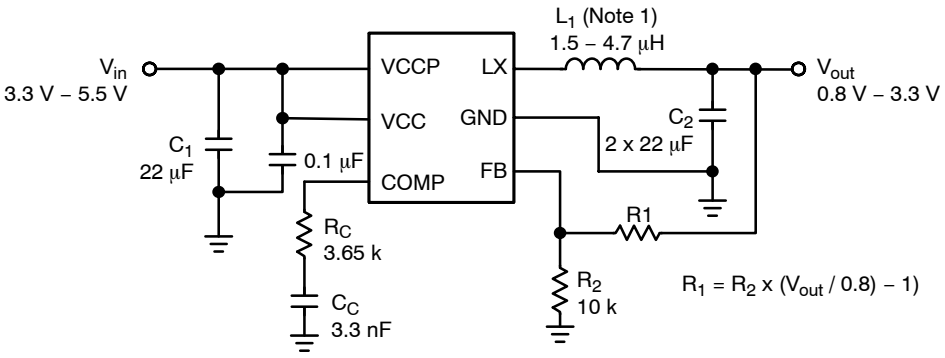


Figure 2. NCP1599 Application Circuit

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ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Power Supply Pin (Pin 4, 5) to GND	V_{in}	6.5 −0.3 (DC) −1.0 (t < 100 ns)	V
LX to GND		V_{in} + 0.7 V_{in} + 1.0 (t < 20 ns) −0.7 (DC) −5.0 (t < 100 ns)	V
All other pins		6.0 −0.3 (DC) −1.0 (t < 100 ns)	V
Operating Temperature Range	T_A	−40 to +85	°C
Junction Temperature	T_J	−40 to +150	°C
Storage Temperature Range	T_S	−55 to +150	°C
Thermal Resistance Junction−to−Air (Note 2)	$R_{\theta JA}$	68.5	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. See External Component Reference Data for inductor selection.
2. $R_{\theta JA}$ measured on approximately 1x1 inch sq. of 1 oz. Copper.

EXTERNAL COMPONENT REFERENCE DATA

V_{OUT} (V)	I_{OUT} Max (A)	Inductor (L1)	C_{IN} Min (C1) (μF)	C_{OUT} (C2) (μF)	R1 (kΩ)	R2 (kΩ)	Rc (kΩ)	Cc (nF)
3.3	3	2.2 μH	22 μF	2 X 22 μF	31.6	10	3.4 – 6.81	2.2 – 3.3
	1–2	3.3 μH					3.65 – 10	2.2 – 3.3
2.5	3	2.2 μH	22 μF	2 X 22 μF	21.5	10	3.4 – 4.99	2.2 – 3.3
	2	3.3 μH					3.4 – 6.81	2.2 – 3.3
	1	4.7 μH					3.4 – 6.81	2.2 – 3.3
1.8	3	1.5 μH	22 μF	2 X 22 μF	12.7	10	3.4 – 6.81	2.2 – 3.3
	2	2.2 μH					3.4 – 4.99	2.2 – 3.3
	1	3.3 μH					3.4 – 6.81	2.2 – 3.3
1.5	3	1.5 μH	22 μF	2 X 22 μF	8.87	10	3.4 – 6.81	2.2 – 3.3
	2	2.2 μH					3.4 – 4.99	2.2 – 3.3
	1	3.3 μH					3.4 – 4.99	2.2 – 3.3
1.2	3	1.5 μH	22 μF	2 X 22 μF	5.11	10	3.4 – 6.81	2.2 – 3.3
	2	2.2 μH					3.4 – 4.99	2.2 – 3.3
	1	3.3 μH					3.4 – 4.99	2.2 – 3.3
0.9	3	1.5 μH	22 μF	2 X 22 μF	1.24	10	3.4 – 6.81	2.2 – 3.3
	2	2.2 μH					3.4 – 4.99	2.2 – 3.3
	1	3.3 μH					3.4 – 4.99	2.2 – 3.3

NOTE: This table shows the recommended components for six common output voltages. Compensation components are given in a range of values that one may use to stabilize the NCP1599 over a range of output voltages and currents. Figure 2 also shows a recommended schematic.
Please note that input lead lengths and traces should be as short as possible, especially for high bandwidth crossover frequencies. Input capacitance may have to increase at higher bandwidths and currents as well.

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ELECTRICAL CHARACTERISTICS (V_{in} = 3.0 V – 5.5 V, V_{out} = 1.2 V, T_J = +25°C for typical value; –40°C < T_J < +125°C for min/max values unless noted otherwise)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{in} Input Voltage Range	V_{in}		3.0		5.5	V
V_{CC} UVLO Threshold			2.3	2.75	2.99	V
UVLO Hysteresis				500		mV
V_{CC} Quiescent Current	I_{inVCC}	V_{in} = 5.0 V, V_{FB} = 1.5 V, (No Switching)		1.8	2.2	mA
V_{CCP} Quiescent Current	I_{inVCCP}	V_{in} = 5.0 V,V_{FB} = 1.5 V, (No Switching)		39		μA
FEEDBACK VOLTAGE						
Reference Voltage	V_{FB}	V_{FB} = V_{COMP}	0.788	0.800	0.812	V
Feedback Input Bias Current	I_{FB}	V_{FB} = 0.8 V		10	100	nA
Feedback Voltage Line Regulation		V_{FB} = V_{COMP}, V_{in} = 2.7 V to 6.0 V			0.03	%/V
GM AMPLIFIER						
Gm Amp Open Loop Voltage Gain (Note 3)	AV_{gm}		55			dB
Gm Amp Transconductance (Note 3)	gm_{COMP}	V_{FB} > 0.75 V, ΔI_{COMP}= ± 10 μA		1000		μA/V
PWM						
Maximum Duty Cycle (Regulating)			82			%
Minimum Controllable ON Time (Note 3)					50	ns
CURRENT SENSE AMPLIFIER						
Current Sense to COMP Transconductance (Note 3)	gm_{POWER}			5.0		A/V
PULSE−BY−PULSE CURRENT LIMIT						
Pulse−by−Pulse Current Limit (Note 4)	I_{LIM}	V_{in} = 4.0 V – 5.5 V	3.83	4.18	4.54	A
Pulse−by−Pulse Current Limit (Soft−Start) (Note 4)	I_{LIMSS}	V_{in} = 4.0 V – 5.5 V	4.12	4.40	4.72	A
OSCILLATOR						
Oscillator Frequency	F_{SW}		0.87	1.0	1.13	MHz
MOSFET						
High Side MOSFET ON Resistance	$R_{DS(on)}$ HS	I_{DS} = 100 mA, V_{GS} = 5 V		140	175	mΩ
High Side MOSFET Leakage (Note 3)		V_{SW} = 0 V			10	μA
Low Side MOSFET ON Resistance	$R_{DS(on)}$ LS	I_{DS} = 100 mA, V_{GS} = 5 V		90	100	mΩ
Low Side MOSFET Leakage (Note 3)		V_{SW} = 5 V			10	μA
SOFT−START						
Soft−Start Ramp Time (Note 3)	t_{SS}	F_{SW} = 1 MHz		1.0		ms
Hiccup Timer (Note 3)				2.0		ms
THERMAL SHUTDOWN						
Thermal Shutdown Threshold				170		°C
Thermal Shutdown Hysteresis				40		°C

3. Guaranteed by design.
4. Current limit operation not guaranteed below V_{in} = 4.0 V.

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TYPICAL OPERATING CHARACTERISTICS

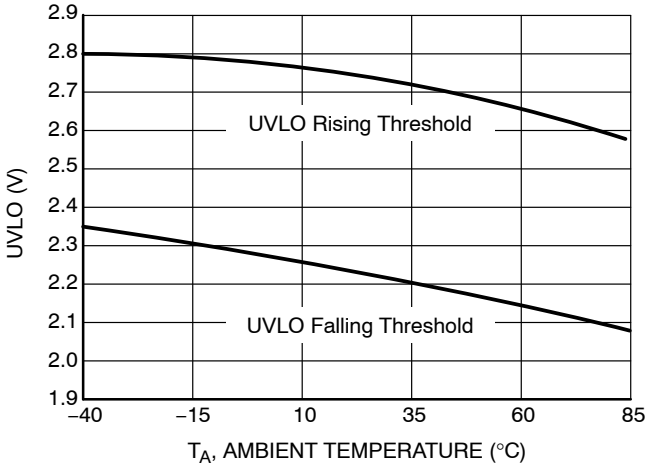


Figure 3. Undervoltage Lockout vs. Temperature

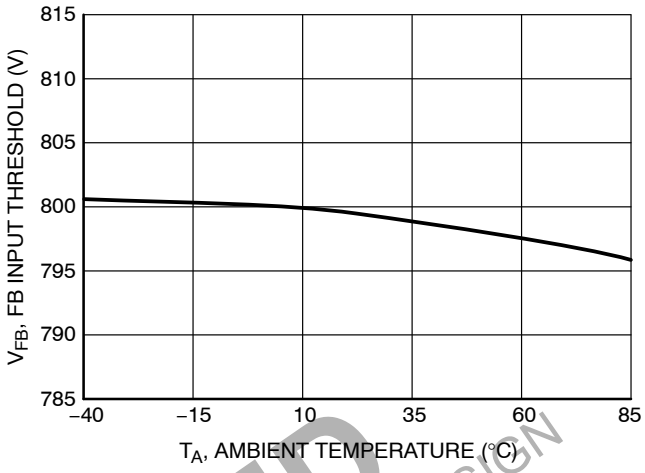


Figure 4. Feedback Input Threshold vs. Temperature

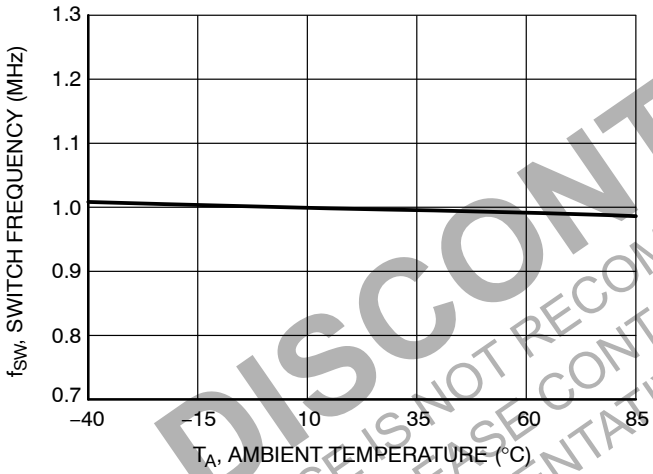


Figure 5. Switching Frequency vs. Temperature

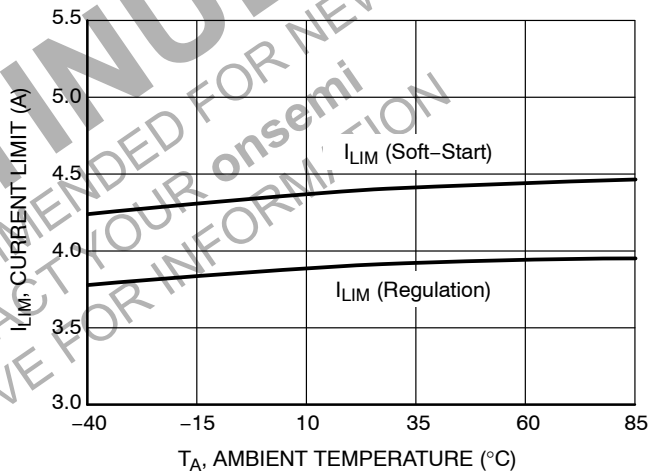


Figure 6. Current Limit vs. Temperature

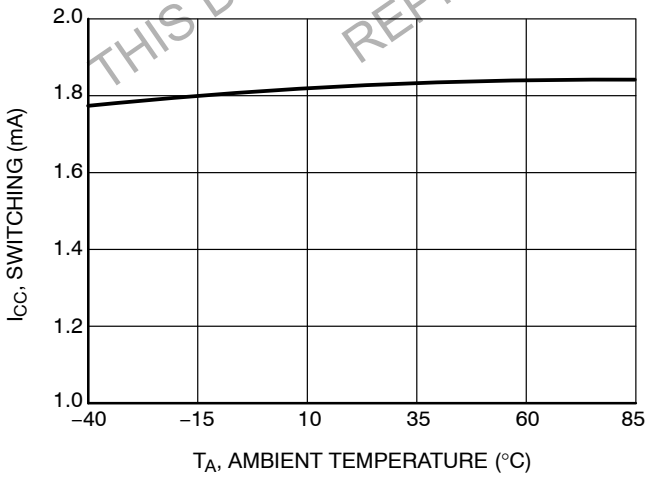


Figure 7. Quiescent Current Into V_{CC} vs. Temperature

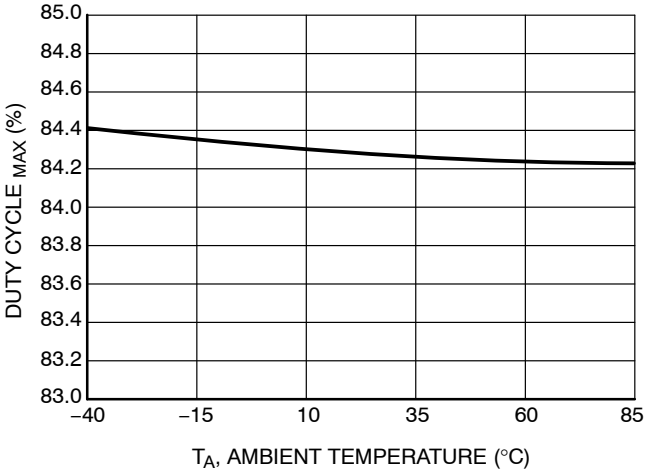


Figure 8. Maximum Duty Cycle vs. Temperature

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TYPICAL OPERATING CHARACTERISTICS

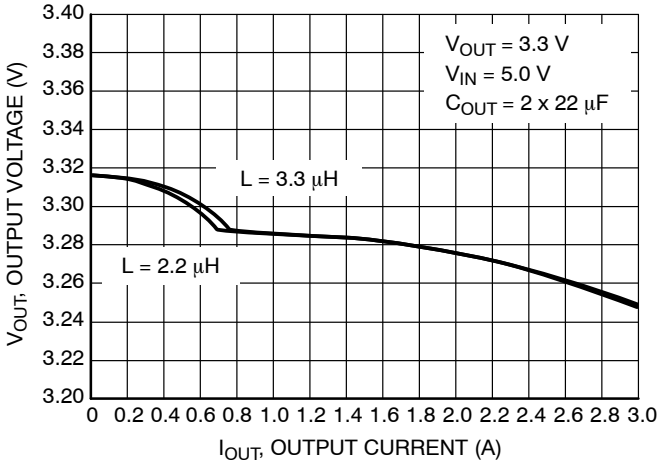


Figure 9. Load Regulation for V_{OUT} = 3.3 V

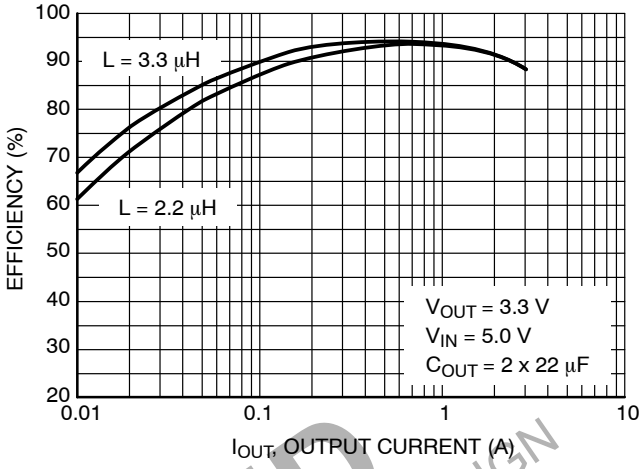


Figure 10. Efficiency vs. Output Current for V_{OUT} = 3.3 V

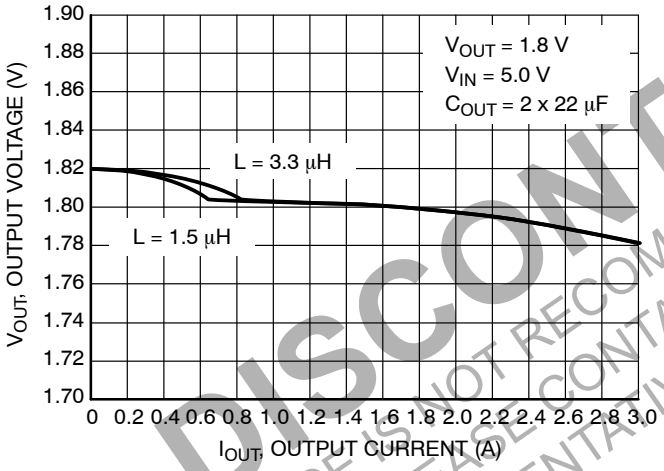


Figure 11. Load Regulation for V_{OUT} = 1.8 V

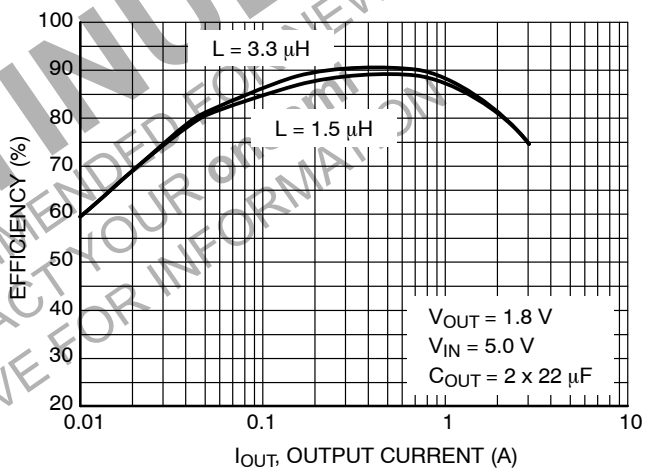


Figure 12. Efficiency vs. Output Current for V_{OUT} = 1.8 V

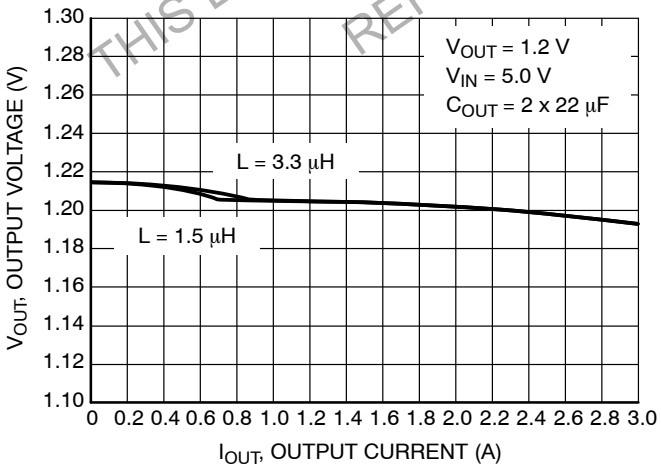


Figure 13. Load Regulation for V_{OUT} = 1.2 V

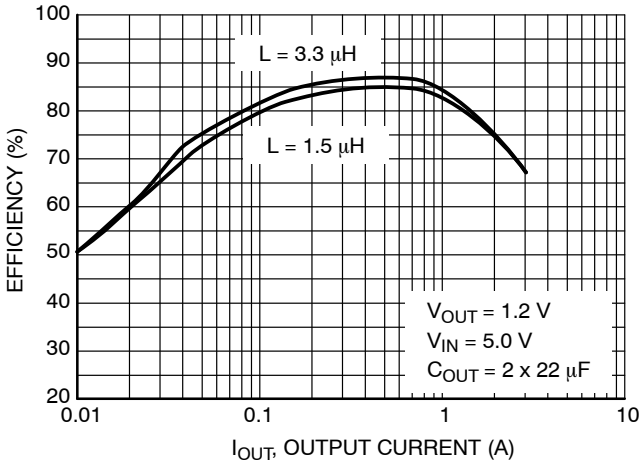
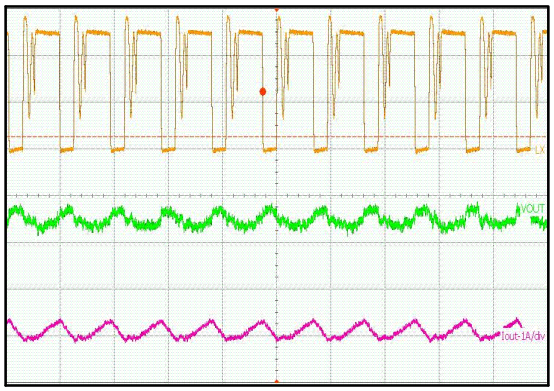


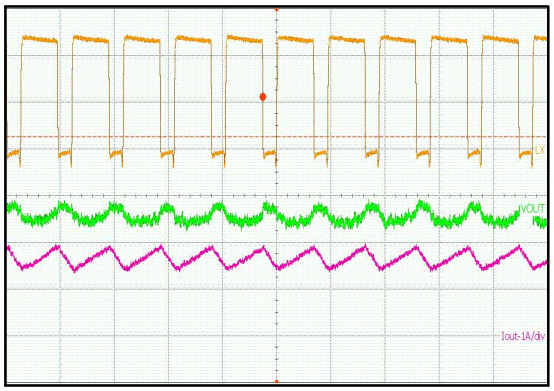
Figure 14. Efficiency vs. Output Current for V_{OUT} = 1.2 V

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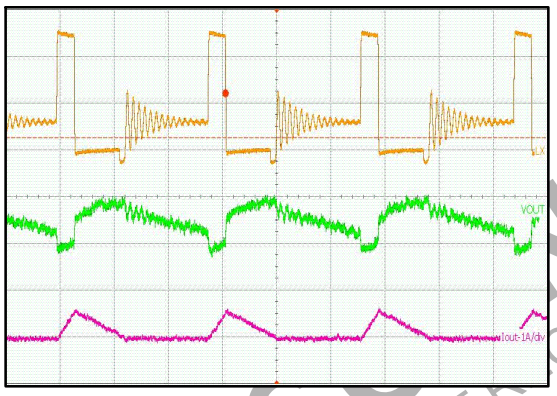
(V_{IN} = 5 V, I_{LOAD} = 120 mA, L = 2.2 μH, C_{OUT} = 2 x 22 μF)
Upper Trace: L_X Pin Switching Waveform, 2 V/div
Middle Trace: Output Ripple Voltage, 20 mV/div
Lower Trace: Inductor Current, 1 A/div
Time Scale: 1.0 μs/div

Figure 15. DCM Switching Waveform for V_{OUT} = 3.3 V



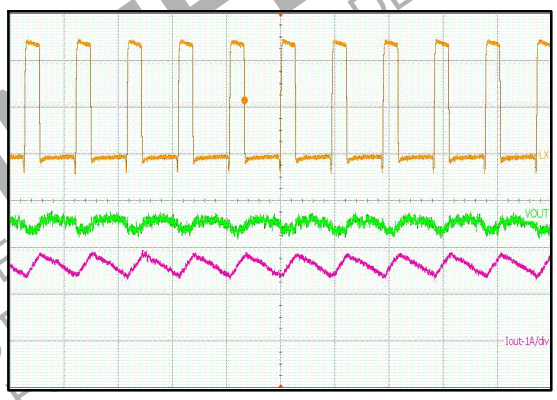
(V_{IN} = 5 V, I_{LOAD} = 1.5 A, L = 2.2 μH, C_{OUT} = 2 x 22 μF)
Upper Trace: L_X Pin Switching Waveform, 2 V/div
Middle Trace: Output Ripple Voltage, 20 mV/div
Lower Trace: Inductor Current, 1 A/div
Time Scale: 1.0 μs/div

Figure 16. CCM Switching Waveform for V_{OUT} = 3.3 V



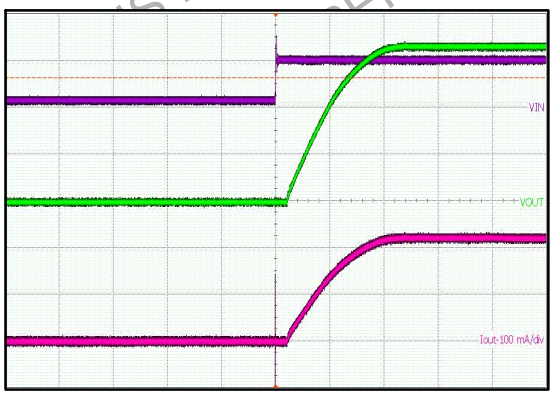
(V_{IN} = 5 V, I_{LOAD} = 120 mA, L = 2.2 μH, C_{OUT} = 2 x 22 μF)
Upper Trace: L_X Pin Switching Waveform, 2 V/div
Middle Trace: Output Ripple Voltage, 20 mV/div
Lower Trace: Inductor Current, 200 mA/div
Time Scale: 1.0 μs/div

Figure 17. DCM Switching Waveform for V_{OUT} = 1.2 V



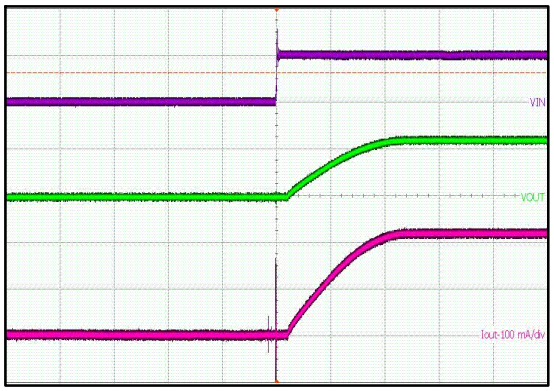
(V_{IN} = 5 V, I_{LOAD} = 1.5 A, L = 2.2 μH, C_{OUT} = 2 x 22 μF)
Upper Trace: L_X Pin Switching Waveform, 2 V/div
Middle Trace: Output Ripple Voltage, 20 mV/div
Lower Trace: Inductor Current, 1 A/div
Time Scale: 1.0 μs/div

Figure 18. CCM Switching Waveform for V_{OUT} = 1.2 V



(V_{IN} = 5 V, I_{LOAD} = 200 mA, L = 2.2 μH, C_{OUT} = 2 x 22 μF)
Upper Trace: VIN Pin Voltage, 5 V/div
Middle Trace: Output Voltage, 1 V/div
Lower Trace: Input Current, 100 mA/div
Time Scale: 500 μs/div

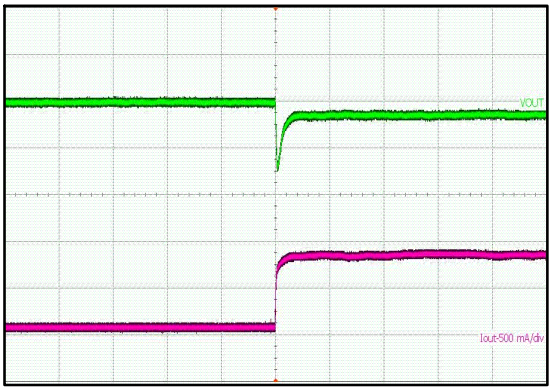
Figure 19. Soft−Start Waveforms for V_{OUT} = 3.3 V



(V_{IN} = 5 V, I_{LOAD} = 200 mA, L = 2.2 μH, C_{OUT} = 2 x 22 μF)
Upper Trace: VIN Pin Voltage, 5 V/div
Middle Trace: Output Voltage, 1 V/div
Lower Trace: Input Current, 100 mA/div
Time Scale: 500 μs/div

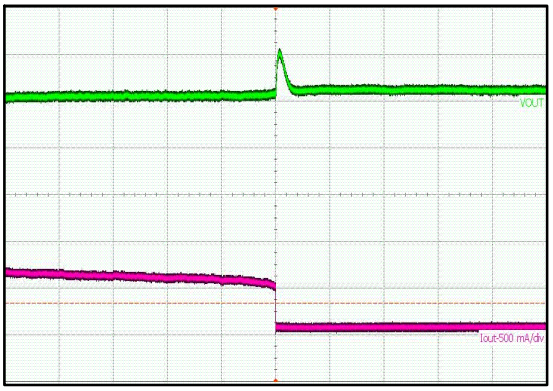
Figure 20. Soft−Start Waveforms for V_{OUT} = 1.2 V

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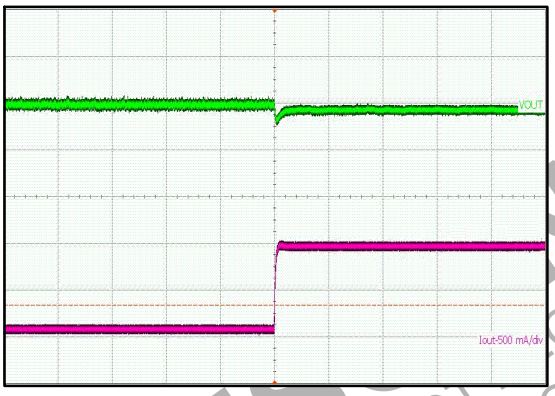
(V_{IN} = 5 V, I_{LOAD} = 100 mA, L = 2.2 μH, C_{OUT} = 2 x 22 μF)
Upper Trace: Output Dynamic Voltage, 100 mV/div
Lower Trace: Output Current, 500 mA/div
Time Scale: 200 μs/div

Figure 21. Transient Response for V_{OUT} = 3.3 V



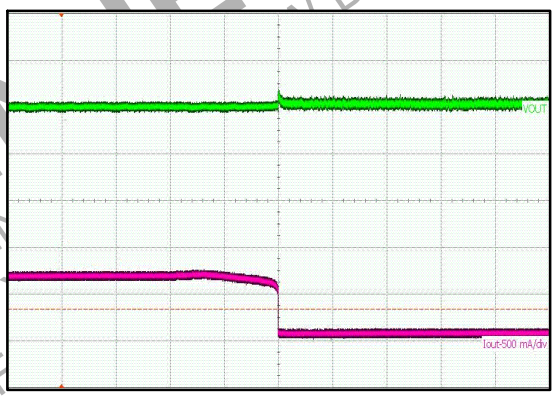
(V_{IN} = 5 V, I_{LOAD} = 100 mA, L = 2.2 μH, C_{OUT} = 2 x 22 μF)
Upper Trace: Output Dynamic Voltage, 100 mV/div
Lower Trace: Output Current, 500 mA/div
Time Scale: 200 μs/div

Figure 22. Transient Response for V_{OUT} = 3.3 V



(V_{IN} = 5 V, I_{LOAD} = 100 mA, L = 2.2 H, C_{OUT} = 2 x 22 μF)
Upper Trace: Output Dynamic Voltage, 100 mV/div
Lower Trace: Output Current, 500 mA/div
Time Scale: 200 μs/div

Figure 23. Transient Response for V_{OUT} = 1.2 V



(V_{IN} = 5 V, I_{LOAD} = 100 mA, L = 2.2 H, C_{OUT} = 2 x 22 μF)
Upper Trace: Output Dynamic Voltage, 100 mV/div
Lower Trace: Output Current, 500 mA/div
Time Scale: 200 μs/div

Figure 24. Transient Response for V_{OUT} = 1.2 V

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DESIGN

DETAILED DESCRIPTION

Overview

The NCP1599 is a synchronous PWM controller that incorporates all the control and protection circuitry necessary to satisfy a wide range of applications. The NCP1599 employs current mode control to provide good transient response, simple compensation, and excellent stability. The features of the NCP1599 include a precision reference, fixed 1 MHz switching frequency, a transconductance error amplifier, an integrated high−side P−channel MOSFET and low−side N−Channel MOSFET, internal soft−start, and very low shutdown current. The protection features of the NCP1599 include internal soft−start, pulse−by−pulse current limit, hiccup mode short−circuit protection, and thermal shutdown.

Reference Voltage

The NCP1599 incorporates an internal reference that allows output voltages as low as 0.8 V. The tolerance of the internal reference is guaranteed over the entire operating temperature range of the controller. The reference voltage is trimmed using a test configuration that accounts for error amplifier offset and bias currents.

Oscillator Frequency

A fixed precision oscillator is provided. The oscillator frequency range is 1 MHz with ±13% variation.

Transconductance Error Amplifier

The transconductance error amplifier's primary function is to regulate the converter's output voltage using a resistor divider connected from the converter's output to the FB pin of the controller, as shown in the applications Schematic. A series RC compensation network must be connected from the error amplifier's output (COMP pin) to GND to stabilize the converter. In some applications, a lower value capacitor may be connected from the COMP pin to GND to reduce the loop gain at higher frequencies. However, if this capacitor is too large the phase margin of the converter will be reduced. If a Fault occurs, the COMP pin is immediately pulled to GND and PWM switching is inhibited.

Internal Soft−Start

To limit the startup inrush current, an internal soft start circuit is used to ramp up the reference voltage from 0 V to its final value linearly. The internal soft start time is 1 ms typically.

Output MOSFETs

The NCP1599 includes low $R_{DS(on)}$, both high−side P−channel and low−side N−channel MOSFETs capable of delivering up to 3.0 A of current. When the controller is disabled or during a Fault condition, the controller's output stage is tri−stated by turning OFF both the upper and lower MOSFETs.

Adaptive Dead Time Gate Driver

In a synchronous buck converter, a certain dead time is required between the low side drive signal and high side drive signal to avoid shoot through. During the dead time, the body diode of the low side FET freewheels the current. The body diode has much higher voltage drop than that of the MOSFET, which reduces the efficiency significantly. The longer the body diode conducts, the lower the efficiency. In NCP1599, the drivers and MOSFETs are integrated in a single chip. The parasitic inductance is minimized. Adaptive dead time control method is used in NCP1599 to prevent the shoot through from happening and minimizing the diode conduction loss at the same time.

Pulse Width Modulation

A high−speed PWM comparator, capable of pulse widths as low as 50 ns, is included in the NCP1599. The inverting input of the comparator is connected to the output of the error amplifier. The non−inverting input is connected to the the current sense signal. At the beginning of each PWM cycle, the CLK signal sets the PWM flip−flop and the upper MOSFET is turned ON. When the current sense signal rises above the error amplifier's voltage then the comparator will reset the PWM flip−flop and the upper MOSFET will be turned OFF.

Power Save Mode

If the load current decreases, the converter will enter power save mode operation automatically. During power save mode, the converter skips switching and operates with reduced frequency, which minimizes the quiescent current and maintain high efficiency.

Current Sense Amplifier

The NCP1599 monitors the current in the upper MOSFET. The current signal is required by the PWM comparator, the pulse−by−pulse current limiter, and the hiccup mode/over current counter.

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PROTECTIONS

Undervoltage Lockout (UVLO)

The undervoltage lockout feature prevents the controller from switching when the input voltage is too low to power the internal power supplies and reference. Hysteresis must be incorporated in the UVLO comparator to prevent resistive drops in the wiring or PCB traces from causing ON/OFF cycling of the controller during heavy loading at power up or power down.

The UVLO threshold allows steady−state operation at input voltages as low as 3.3 V. However, the current limit at these input voltage levels may not function appropriately due to increased R_{DSon}. This could cause excessive heating and possible device failure.

Overcurrent Protection (OCP)

NCP1599 detects high side switch current and then compares to a voltage level representing the overcurrent threshold limit. If the current through the high side FET exceeds the overcurrent threshold limit for seven consecutive switching cycles, overcurrent protection is triggered.

Once the overcurrent protection occurs, hiccup mode engages. First, hiccup mode turns off both FETs and discharges the internal compensation network at the COMP pin. Next, the IC waits typically 2 ms and then resets the overcurrent counter. After this reset, the circuit attempts another normal soft−start. During soft−start, the overcurrent protection threshold is increased to prevent false overcurrent detection while charging the output capacitors. The hiccup mode scheme reduces input supply current and power dissipation during a short−circuit. It also allows for much improved system up−time by allowing auto−restart upon removal of a temporary short−circuit.

Pre−Bias Startup

In some applications the controller will be required to start switching when its output capacitors are charged anywhere from slightly above 0 V to just below the regulation voltage. This situation occurs for a number of reasons: the converter's output capacitors may have residual charge on them or the converter's output may be held up by a low current standby power supply. NCP1599 supports pre−bias start up by holding the low side FETs off till soft start ramp reaches the FB Pin voltage.

Thermal Shutdown

The NCP1599 protects itself from over heating with an internal thermal monitoring circuit. If the junction temperature exceeds the thermal shutdown threshold the voltage at the COMP pin will be pulled to GND and both the upper and lower MOSFETs will be shut OFF.

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APPLICATION INFORMATION

Programming the Output Voltage

The output voltage is set using a resistive voltage divider from the output voltage to FB pin (see Figure 25). So the output voltage is calculated according to Eq.1.

$$V_{out} = V_{FB} \cdot \frac{R_1 + R_2}{R_2} \quad \text{(eq. 1)}$$

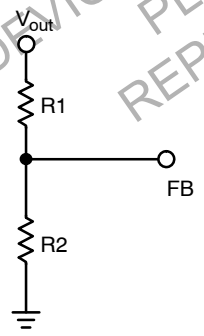


Figure 25. Output divider

Inductor Selection

The inductor is the key component in the switching regulator. The selection of inductor involves trade−offs among size, cost and efficiency. The inductor value is selected according to the equation 2.

$$L = \frac{V_{out}}{f \cdot I_{ripple}} \cdot \left(1 - \frac{V_{out}}{V_{in(max)}}\right) \quad \text{(eq. 2)}$$

Where V_{out} − the output voltage;
f − switching frequency, 1.0 MHz;
I_{ripple} − Ripple current, usually it's 20% − 30% of output current;
$V_{in(max)}$ − maximum input voltage.

Choose a standard value close to the calculated value to maintain a maximum ripple current within 30% of the maximum load current. If the ripple current exceeds this 30% limit, the next larger value should be selected.

The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be about 30% higher. For robust operation in fault conditions (start−up or short circuit), the saturation current should be high enough. To keep the efficiency high, the series resistance (DCR) should be less than 0.1 Ω, and the core material should be intended for high frequency applications.

Output Capacitor Selection

The output capacitor acts to smooth the dc output voltage and also provides energy storage. So the major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is

related to capacitance and the ESR. The minimum capacitance required for a certain output ripple can be calculated by Equation 4.

$$C_{OUT(min)} = \frac{I_{ripple}}{8 \cdot f \cdot V_{ripple}} \quad \text{(eq. 3)}$$

Where V_{ripple} is the allowed output voltage ripple.

The required ESR for this amount of ripple can be calculated by equation 5.

$$ESR = \frac{V_{ripple}}{I_{ripple}} \quad \text{(eq. 4)}$$

Based on Equation 2 to choose capacitor and check its ESR according to Equation 3. If ESR exceeds the value from Eq.4, multiple capacitors should be used in parallel.

Ceramic capacitors can be used in most of the applications. In addition, both surface mount tantalum and through−hole aluminum electrolytic capacitors can be used as well.

Maximum Output Capacitor

NCP1599 family has internal 1 ms fixed soft−start and overcurrent limit. It limits the maximum allowed output capacitor to startup successfully. The maximum allowed output capacitance can be determined by the equation:

$$C_{out(max)} = \frac{I_{lim(min)} - I_{load(max)} - \frac{\Delta i_{p-p}}{2}}{V_{out}/T_{SS(min)}} \quad \text{(eq. 5)}$$

Where $T_{SS(min)}$ is the minimum soft−start period (1ms); D_{iPP} is the current ripple.

This is assuming that a constant load is connected. For example, with 3.3 V/2.0 A output and 20% ripple, the maximum allowed output capacitance is 546 μF.

Input Capacitor Selection

The input capacitor can be calculated by Equation 6.

$$C_{in(min)} = I_{out(max)} \cdot D_{max} \cdot \frac{1}{f \cdot V_{in(ripple)}} \quad \text{(eq. 6)}$$

Where $V_{in(ripple)}$ is the required input ripple voltage.

$$\Delta_{max} = \frac{V_{out}}{V_{in(min)}} \text{ is the maximum duty cycle.} \quad \text{(eq. 7)}$$

Compensation Design

The NCP1599 is a current mode controller, therefore there are two feedback loops. The inner feedback loop derives its feedback from the sensed inductor current, while the outer loop monitors the output voltage.

The compensation network is designed around the power components, or the power stage. An isolated schematic of the error amplifier and the various compensation components is shown in Figure 26. The error amplifier in conjunction with the compensation network makes up the compensator network. The purpose of the compensator network is to stabilize the control loop and achieve high performance in terms of the transient response, audio susceptibility and output impedance. Specifically, the compensator is added to increase low frequency magnitude, extend the 0 dB frequency (crossover frequency), and improve the phase characteristic.

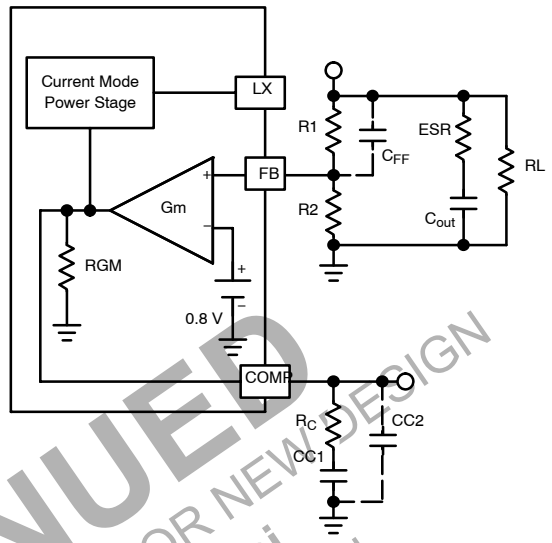


Figure 26. NCP1599 Compensation Components

There are several different types of compensation that can be used to improve the frequency response of the control loop. To determine which compensation scheme to use, some information about the power stage is needed. Use $V_{in} = V_{in(min)}$ and $R = R_{min}$ ($I_{out(max)}$) when calculating compensation components.

The DC gain of the voltage feedback loop is given by:

$$A_{DC} = R \times G_{CS} \times A_{EA} \times \frac{V_{FB}}{V_{out}} \quad \text{(eq. 8)}$$

Where AEA is the error amplifier voltage gain, 560 V/V (55 db), G_{CS} is the current sense transconductance, 5.0 A/V, and R is the load resistor value.

The power stage has one pole due to the output capacitor C_{out} and the load resistor R. It's located at:

$$f_{p1} = \frac{1}{2\pi \cdot C_{out} \cdot R} \quad \text{(eq. 9)}$$

The power stage may have a zero of importance, if the output capacitor has a large capacitance and/or a high ESR value. The zero, due to the ESR and capacitance of the output capacitor, is located at:

$$f_{ESRZ} = \frac{1}{2\pi \cdot C_{out} \cdot R_{ESR}} \quad \text{(eq. 10)}$$

A compensator is designed to achieve improved performance and stability. The NCP1599 will typically require only a single resistor and capacitor for compensation, but depending on the power stage it could require three or four external components.

First, a target crossover frequency (fc) for the loop gain must be selected. The crossover frequency is the bandwidth

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of the converter. A higher bandwidth generally corresponds to faster response times and lower overshoots to load transients. However, the bandwidth should not be much higher than 1/10 the switching frequency. The NCP1599 operates with a 1.0 MHz switching frequency, so it is recommended to choose a crossover frequency between 40 kHz − 100 kHz. The schematic of the NCP1599 compensator is shown in Figure 2. The default design uses Rc and C_{C1} to form a lag (Type 2) compensator. The C_{C2} capacitor can be added to form an additional pole that is typically used to cancel out the ESR zero of the output capacitor. Finally, if extra phase margin is needed, the C_{FF} capacitor can be added (this does not help at low output voltages, see below). The strategy taken here for choosing Rc and C_{C1} is to set the crossover frequency with Rc, and set the compensator zero with C_{C1}.

Using the selected target crossover frequency, fc, set Rc to:

$$R_C = \frac{2\pi \cdot f_C \cdot C_{out}}{Gm_{EA} \cdot G_{CS}} \cdot \frac{V_{out}}{V_{FB}} \Omega \quad \text{(eq. 11)}$$

f_C = Crossover frequency in Hertz (50kHz − 200kHz is recommended).

The zero, due to the compensation capacitor (Cc1) and the compensation resistor (Rc), is located at:

$$f_{Z1} = \frac{1}{2\pi \times C_{C1} \times R_C} \quad \text{(eq. 12)}$$

When fast transient responses are desired, f_{Z1} should be placed as high as possible, however it should not be higher than the selected crossover frequency fc. The guideline proposed here is to choose C_{C1} such that f_{Z1} falls somewhere between the power pole f_{P1} and 1⁄2 decade before the selected crossover frequency fc:

$$\frac{3.16}{2\pi R_C f_C} \le C_{C1} \le \frac{1}{2\pi f_{p1} R_C} \quad \text{(eq. 13)}$$

The compensation capacitor (Cc1) and the output resistor of error amplifier R_{GM} creates another pole of the system, and it's located at:

$$f_{p2} = \frac{1}{2\pi \times C_{C1} \times R_{GM}}, \quad \text{(eq. 14)}$$

Where $R_{GM} = 66 \bullet 10^3\ \Omega$.

In this compensation scheme, the pole created by C_{C2} is used to cancel out the zero created by the ESR of the output capacitor. This pole is located at:

$$f_{p3} = \frac{1}{2\pi \cdot C_{C2} \cdot \frac{R_C R_{GM}}{R_C + R_{GM}}}, \quad \text{(eq. 15)}$$

For the typical case, use C_{C2} if:

$$f_{ESR} < \frac{f_S}{2} \quad \text{(eq. 16)}$$

$$C_{C2} = \frac{R_{GM} + R_C}{2\pi f_{ESR} R_{GM} R_C} \quad \text{(eq. 17)}$$

A feed−forward capacitor is recommended for most designs. The large resistor value and the parasitic capacitance of the FB Pin can cause a high frequency pole that can reduce the overall system phase margin. By placing a feed−forward capacitor C_{FF}, these effects can be significantly reduced. C_{FF} will provide a positive phase shift (lead) that can be used to increase phase margin. However, it is important to note that the effectiveness of C_{FF} decreases with output voltage. This is due to the fact that the frequency of the zero f_{zff} and pole f_{pff} get closer together as the output voltage is reduced.

The frequency of the feed−forward zero and pole are:

$$f_{Zff} = \frac{1}{2\pi R_{FB1} C_{ff}} \quad \text{(eq. 18)}$$

$$f_{pff} = \frac{1}{2\pi R_{FB1} C_{ff}} \frac{R_{FB1} + R_{FB2}}{R_{FB2}} = f_{Zff} \frac{V_{out}}{V_{FB}} \quad \text{(eq. 19)}$$

Power Dissipation

The NCP1599 is available in thermally enhanced 6−pin, DFN package. When the die temperature reaches +185°C, the NCP1599 shuts down (see the *Thermal−Overload Protection* section). The power dissipated in the device is the sum of the power dissipated from supply current (PQ), power dissipated due to switching the internal power MOSFET (P_{SW}), and the power dissipated due to the RMS current through the internal power MOSFET (PON). The total power dissipated in the package must be limited so the junction temperature does not exceed its absolute maximum rating of +150°C at maximum ambient temperature. Calculate the power lost in the NCP1599 using the following equations:

1. High side MOSFET

The conduction loss in the top switch is:

$$P_{HSON} = I^2_{RMS_HSFET} \times R_{DS(on)HS} \quad \text{(eq. 20)}$$

Where:

$$I_{RMS_FET} = \sqrt{\left(I_{out}^2 + \frac{\Delta I_{PP}^2}{12}\right) \times D} \quad \text{(eq. 21)}$$

ΔI_{PP} is the peak−to−peak inductor current ripple.

The power lost due to switching the internal power high side MOSFET is:

$$P_{HSSW} = \frac{V_{in} \cdot I_{out} \cdot \left(t_r + t_f\right) \cdot f_{SW}}{2} \quad \text{(eq. 22)}$$

t_r and t_f are the rise and fall times of the internal power MOSFET measured at SW node.

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2. Low side MOSFET

The power dissipated in the top switch is:

$$P_{LSON} = I_{RMS_LSFET}^{2} \cdot R_{DS(on)LS} \quad \text{(eq. 23)}$$

Where:

$$I_{RMS_LSFET} = \sqrt{\left(I_{out}^{2} + \frac{\Delta I_{PP}^{2}}{12}\right) \cdot (1 - D)} \quad \text{(eq. 24)}$$

ΔI_{PP} is the peak−to−peak inductor current ripple.

The switching loss for the low side MOSFET can be ignored.

The power lost due to the quiescent current (I_Q) of the device is:

$$P_Q = V_{in} \cdot I_Q \quad \text{(eq. 25)}$$

I_Q is the switching quiescent current of the NCP1599.

$$P_{TOTAL} = P_{HSON} + P_{HSSW} + P_{LSON} + P_Q \quad \text{(eq. 26)}$$

Calculate the temperature rise of the die using the following equation:

$$T_J = T_C + \left(P_{TOTAL} \cdot \theta_{JC}\right) \quad \text{(eq. 27)}$$

θ_{JC} is the junction−to−case thermal resistance equal to 1.7°C/W. T_C is the temperature of the case and T_J is the junction temperature, or die temperature. The case−to−ambient thermal resistance is dependent on how well heat can be transferred from the PC board to the air. Solder the underside−exposed pad to a large copper GND plane. If the die temperature reaches the thermal shutdown threshold the NCP1599 shuts down and does not restart again until the die temperature cools by 30°C.

Layout

As with all high frequency switchers, when considering layout, care must be taken in order to achieve optimal electrical, thermal and noise performance. To prevent noise both radiated and conducted, the high speed switching current path must be kept as short as possible. Shortening the current path will also reduce the parasitic trace inductance of approximately 25 nH/inch. At switch off, this parasitic inductance produces a flyback spike across the NCP1599 switch. When operating at higher currents and input voltages, with poor layout, this spike can generate voltages across the NCP1599 that may exceed its absolute maximum rating. A ground plane should always be used under the switcher circuitry to prevent interplane coupling and overall noise.

The COMP and FB components should be kept as far away as possible from the switch node. The ground for these components should be separated from the switch current path. Failure to do so will result in poor stability or subharmonic like oscillation.

Board layout also has a significant effect on thermal resistance. Reducing the thermal resistance from the ground pin and exposed pad onto the board will reduce die temperature and increase the power capability of the NCP1599. This is achieved by providing as much copper area as possible around the exposed pad. Adding multiple thermal vias under and around this pad to an internal ground plane will also help. Similar treatment to the inductor pads will reduce any additional heating effects.

Derating

The following graph shows the maximum output current of the NCP1599 with a typical 4−layer PCB layout vs input voltage (V_{in}) and output current (I_{out}). The maximum allowable current is 3 A. The maximum junction temperature (T_J) of the device, so the "thermal limit" shows when maximum T_J is reached. The maximum duty cycle of the NCP1599 is also shown. The PCB used for this data is the standard evaluation board (NCP1599GEVB) and is available at www.onsemi.com.

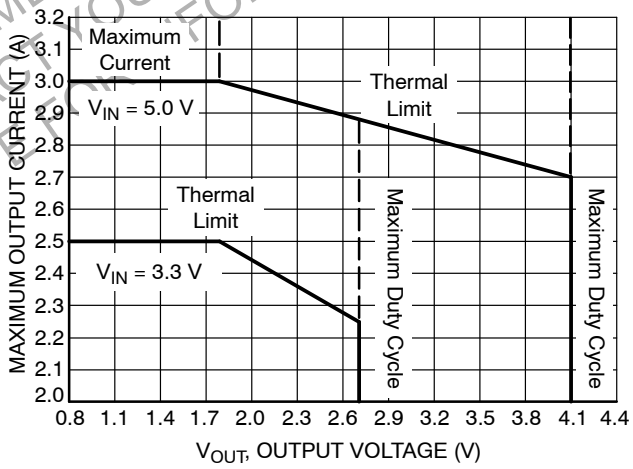


Figure 27. Derating Curves

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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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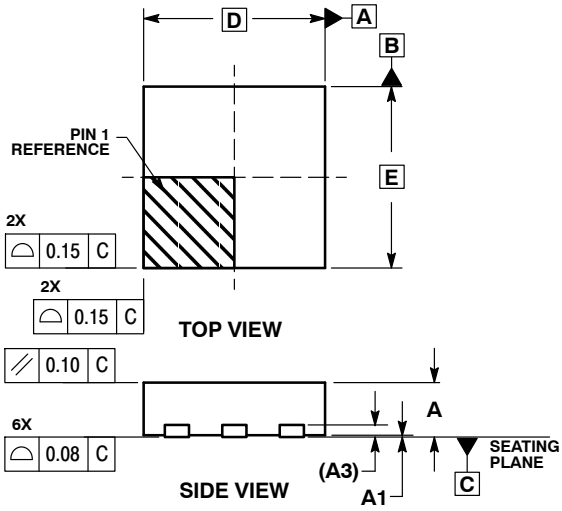


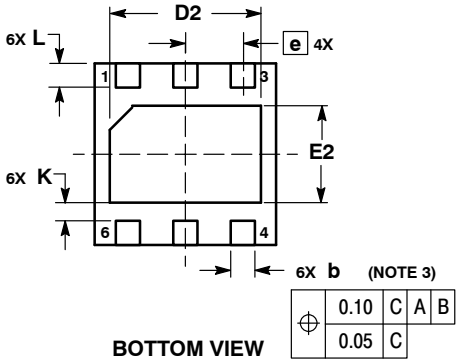
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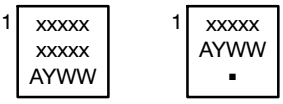




NOTES:
1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMESNION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3		0.20 REF	
b	0.35	0.40	0.45
D		3.00 BSC	
D2	2.40	2.50	2.60
E		3.00 BSC	
E2	1.50	1.60	1.70
e		0.95 BSC	
K	0.21	---	---
L	0.30	0.40	0.50

GENERIC MARKING DIAGRAM*

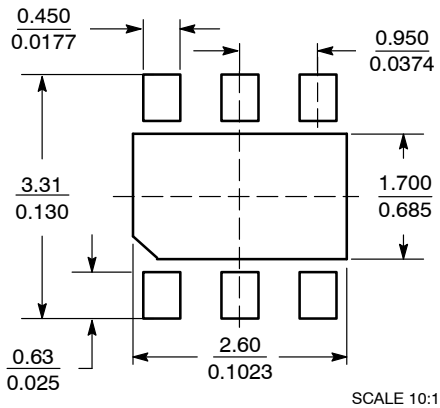


Standard **Pb−Free**

XXXXX	= Specific Device Code
A	= Assembly Location
Y	= Year
WW	= Work Week
▪	= Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking.
Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

SOLDERING FOOTPRINT*



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*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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