NCP2823 Series

Audio Power Amplifier, 3.0 W, Filterless, Class D

The NCP2823A/B are cost effective mono audio power amplifiers designed for portable electronic devices. NCP2823A is optimized for 8 Ω operation and NCP2823B can operate with speaker impedance down to 4.0 Ω. For Instance, NCP2823B is capable of delivering 3 W of continuous average power to a 4.0 Ω from a 5.0 V supply in a Bridge Tied Load (BTL) configuration. Under the same conditions, NCP2823A can provide 1.5 W to an 8.0 Ω BTL load with less than 10% THD+N. For cellular handsets or PDAs it offers space and cost savings because no output filter is required when using inductive transducers. With more than 90% efficiency and very low shutdown current, it increases the lifetime of your battery and drastically lowers the junction temperature.

NCP2823 processes analog inputs with a pulse width modulation technique that lowers output noise and THD. The device allows independent gain while summing signals from various audio sources. Thus, in cellular handsets, the earpiece, the loudspeaker and even melody ringer can be driven with a single NCP2823. Due to its low 26 μV noise floor, A−weighted, clean listening is guaranteed no matter the load sensitivity.

Features

- Optimized PWM Output Stage: Filterless Capability
- Externally gain setting
- Low consumption: 1.8 mA for NCP2823A
- High efficiency: up to 92%
- Large Output Power Capability:
  - 3 W @ V_P = 5.0 V, R_L = 4 Ω, THD+N < 10%
  - 3 W @ V_P = 5.5 V, R_L = 4 Ω, THD+N < 1%
- High PSRR: up to −77 dB
- Fully Differential Capability: RF immunity
- Thermal and Auto recovery Short−Circuit Protection
- CMRR (−80 dB) Eliminates Two Input Coupling Capacitors
- Pin to Pin compatible with NCP2820 Flip−Chip
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- Audio Amplifier for
  - Cellular Phones
  - Digital Cameras
  - Personal Digital Assistant and Portable Media Player
  - GPS

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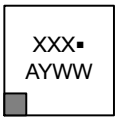
MARKING DIAGRAM



1

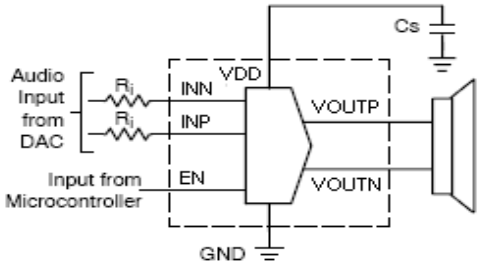
9−PIN FLIP−CHIP CSP
FC SUFFIX
CASE 499AL

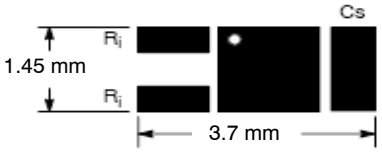


XXX = QTA for NCP2823A
= PMA for NCP2823B
= TPG for NCP2823A with backside laminate
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information on page 10 of this data sheet.





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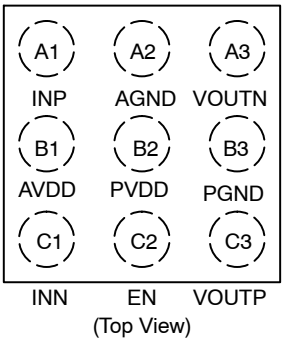


Figure 1. Pin Description

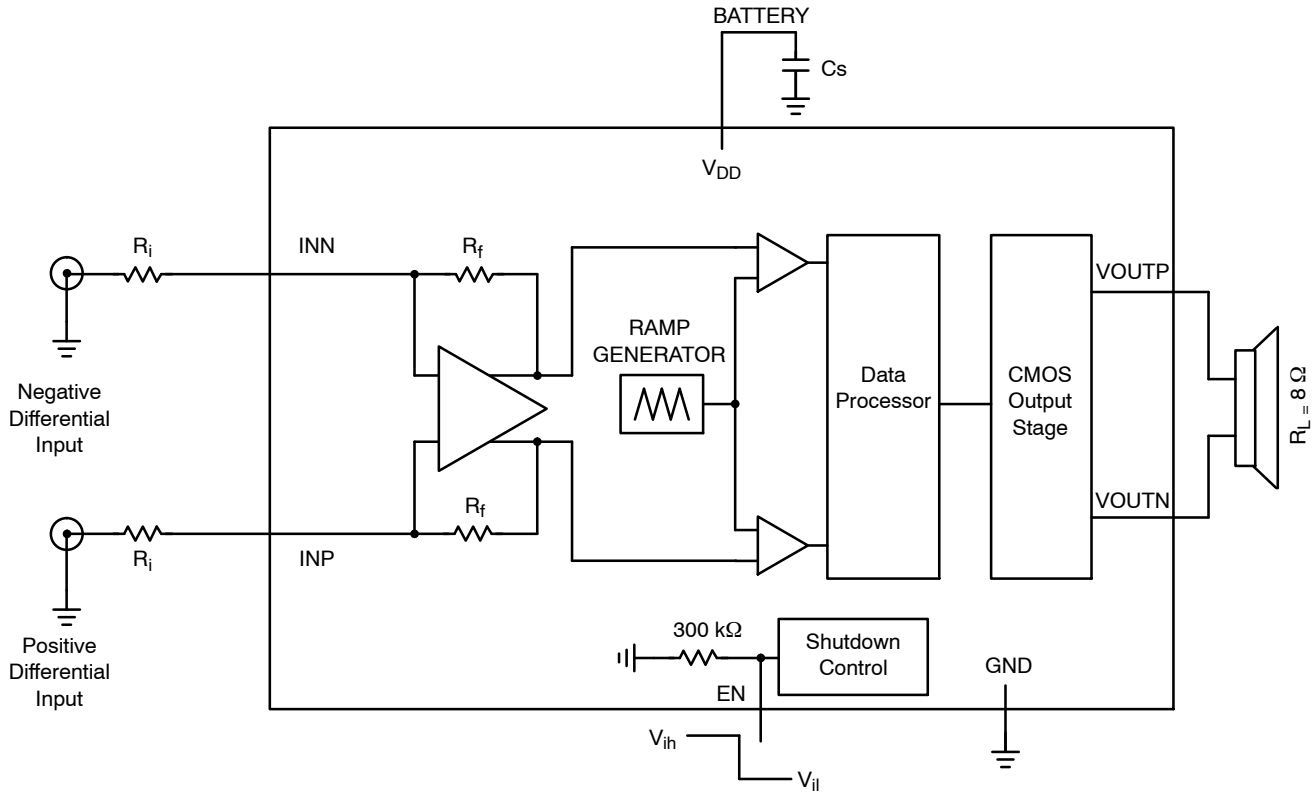


Figure 2. Simplified Block Diagram

PIN FUNCTION DESCRIPTION

Pin	Pin Name	Type	Description
A1	INP	INPUT	Positive Differential Input
C1	INN	INPUT	Negative Differential Input
B2	PVDD	POWER	Power Supply: This pin is the power supply of the device. A 4.7 μF ceramic capacitor or larger must bypass this input to the ground. This capacitor should be placed as close a possible to this input.
B1	AVDD	POWER	Analog Power Supply: This pin must be connected to PVDD.
C3	VOUTP	OUTPUT	Positive output Special care must be observed at layout level. See the Layout recommendations.
A3	VOUTN	OUTPUT	Negative output: Special care must be observed at layout level. See the Layout recommendations.
C2	EN	INPUT	Enable: When a High logic is applied to this pin, the device is activated
B3	PGND	POWER	Power Ground: This pin is the power ground and carries the high switching current. A high quality ground must be provided to avoid any noise spikes/uncontrolled operation. Care must be observed to avoid high−density current flow in a limited PCB copper track.
A2	AGND	POWER	Analog Ground: This pin is the analog ground of the device and must be connected to GND plane.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
AVDD, PVDD Pins: Power Supply Voltage (Note 2)	V_P	−0.3 to +6.0	V
INP/N ,Pins: Input (Note 2)	$V_{INP/N}$	−0.3 to +V_{DD}	V
Digital Input/Output: EN Pin: Input Voltage Input Current	 V_{DG} I_{DG}	 −0.3 to V_{DD} +0.3 1	 V mA
Human Body Model (HBM) ESD Rating are (Note 3)	ESD HBM	2000	V
Machine Model (MM) ESD Rating are (Note 3)	ESD MM	200	V
WCSP 1.5 x 1.5 mm package (Notes 6 and 7) Thermal Resistance Junction−to−Case	$R_{\theta JC}$	90	°C/W
Operating Ambient Temperature Range	T_A	−40 to +85	°C
Operating Junction Temperature Range	T_J	−40 to +125	°C
Maximum Junction Temperature (Note 6)	T_{JMAX}	+150	°C
Storage Temperature Range	T_{STG}	−65 to +150	°C
Moisture Sensitivity (Note 5)	MSL	Level 1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum electrical ratings are defined as those values beyond which damage to the device may occur at T_A = 25°C.
2. According to JEDEC standard JESD22−A108B.
3. This device series contains ESD protection and passes the following tests:
   Human Body Model (HBM) +/−2.0 kV per JEDEC standard: JESD22−A114 for all pins.
   Machine Model (MM) +/−200 V per JEDEC standard: JESD22−A115 for all pins.
4. Latch up Current Maximum Rating: ±100 mA per JEDEC standard: JESD78 class II.
5. Moisture Sensitivity Level (MSL): 1 per IPC/JEDEC standard: J−STD−020A.
6. The thermal shutdown set to 150°C (typical) avoids irreversible damage on the device due to power dissipation.
7. The $R_{\theta CA}$ is dependent on the PCB heat dissipation. The maximum power dissipation (PD) is dependent on the min input voltage, the max output current and external components selected.

$$R_{\theta CA} = \frac{125 - T_A}{P_D} - R_{\theta JC}$$

ELECTRICAL CHARACTERISTICS Min and Max Limits apply for T_A between −40°C to +85°C and for V_{DD} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25 °C and V_{DD} = 3.6 V. (see Note 8)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
GENERAL PERFORMANCES						
V_P	Operational Power Supply		2.5		5.5	V
F_{OSC}	Oscillator Frequency		250	300	350	kHz
I_{DD}	Supply current	NCP2823A V_P = 3.6 V, No Load NCP2823B V_P = 3.6 V, No Load		 1.8 2.6	 2.4 4.6	mA
I_{sd}	Shutdown current	V_{ENL} = V_{ENR} = 0 V		0.01	1	μA
T_{ON}	Turn ON Time	EN rising edge		7.4		ms
T_{OFF}	Turn Off Time	EN falling edge		4		ms
Z_{sd}	Class D Output impedance in shutdown mode	V_{ENL} = 0 V		20		kΩ
$R_{DS(ON)}$	Static drain−source on−state resistance of power Mosfets			300		mΩ
η	Efficiency	NCP2823A, V_P = 3.6 V, Po = 600 mW, RL = 8 Ω, F = 1 kHz		92		%
		NCP2823B, V_P = 3.6 V, Po = 1 W, RL = 4 Ω, F = 1 kHz		90		
Av	Voltage gain		285 kΩ / Ri	300 kΩ / Ri	315 kΩ / Ri	V/V
F_{LP}	−3 dB Cut off Frequency of the Built in Low Pass Filter			30		kHz
T_{SD}	Thermal Shut Down Protection			150		°C
T_{SDH}	Thermal Shut Down Hysteresis			10		°C
V_{IH}	Rising Voltage Input Logic High		1.2	–	V_{DD}	V
V_{IL}	Falling Voltage Input Logic Low			–	0.4	V
R_{PLD}	Pull Down Resistor			250		kΩ
AUDIO PERFORMANCES						
v_{oo}	Output offset			0.3		mV
PSRR	Power supply rejection ratio	F = 217 Hz, Input ac grounded		−77		dB
		F = 1 kHz, Input ac grounded		−63		
SNR	Signal to noise ratio	V_P = 5 V, Pout = 600 mW (A. Weighted)		97		dB
CMRR	Common mode rejection ratio	Input shorted together V_{IC} = 1 V_{pp}, f = 217 Hz		−80		dB
Vn	Output Voltage noise	Input ac grounded, Av = 0 dB, No weighting		35		μV
		Input ac grounded, Av = 0 dB, A. Weighted		26		

8. Performances guaranteed over the indicated operating temperature range by design and/or characterization, production tested at T_J = T_A = 25°C.

ELECTRICAL CHARACTERISTICS Min and Max Limits apply for T_A between −40°C to +85°C and for V_{DD} between 2.5 V to 5.5 V (Unless otherwise noted). Typical values are referenced to T_A = + 25 °C and V_{DD} = 3.6 V. (see Note 8)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
AUDIO PERFORMANCES								
Po	Output Power	NCP2823A RL = 8 Ω F = 1 kHz	THD+N < 1%	V_P = 5 V		1.5		W
				V_P = 3.6 V		0.7		
				V_P = 2.5 V		0.22		
			THD+N < 10%	V_P = 5 V		1.8		
				V_P = 3.6 V		0.87		
				V_P = 2.5 V		0.4		
		NCP2823B RL = 4 Ω F = 1 kHz	THD+N < 1%	V_P = 5 V		1.72		
				V_P = 3.6 V		1.2		
				V_P = 2.5 V		0.58		
			THD+N < 10%	V_P = 5 V		3		
				V_P = 3.6 V		1.57		
				V_P = 2.5 V		0.71		
THD+N	Total harmonic distortion plus noise	V_P = 3.6 V, Av = 6 dB, Po = 0.5 W				0.1		%
		V_P = 5 V, Av = 6 dB, Po = 1 W				0.08		

8. Performances guaranteed over the indicated operating temperature range by design and/or characterization, production tested at T_J = T_A = 25°C.

TYPICAL OPERATING CHARACTERISTICS

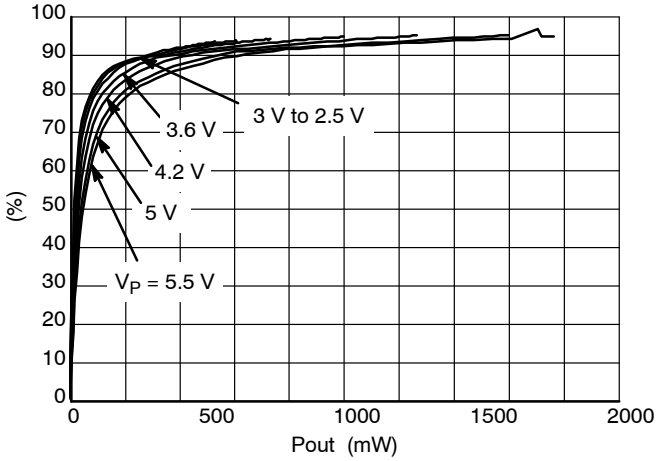


Figure 3. Efficiency vs P_{out}

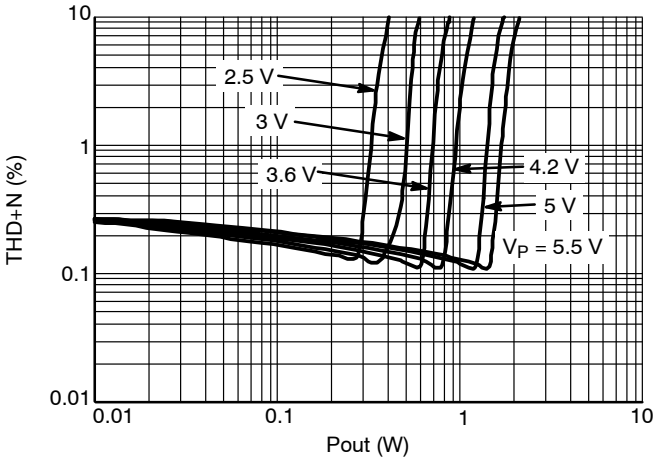


Figure 4. NCP2823A/B, THD+N vs P_{out}, R_L = 8 Ω

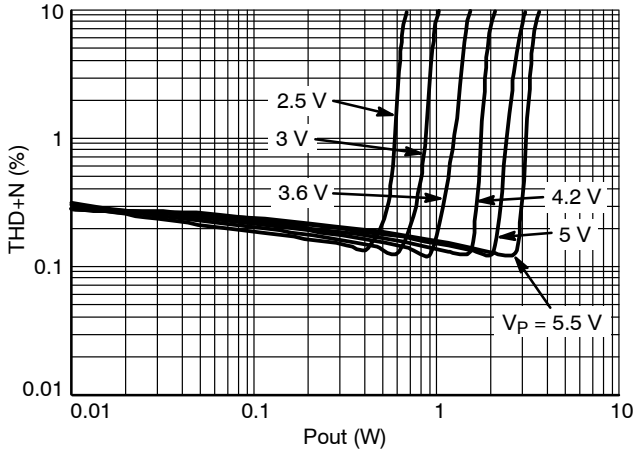


Figure 5. NCP2823B, THD+N vs Pout, R_L = 4 Ω

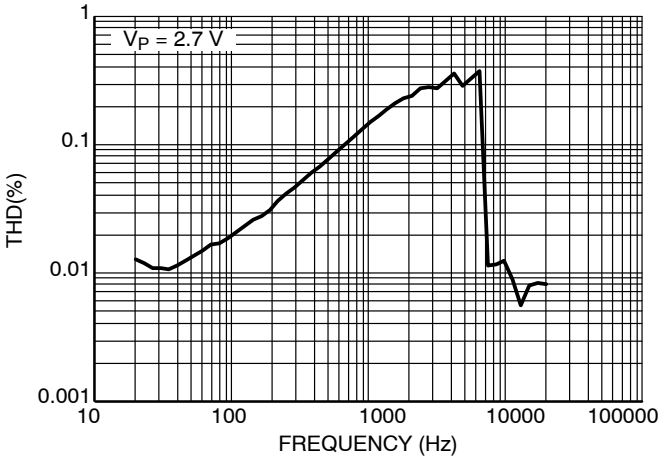


Figure 6. THD+N vs Frequency P_{out} = 150 mW, R_L = 8 Ω

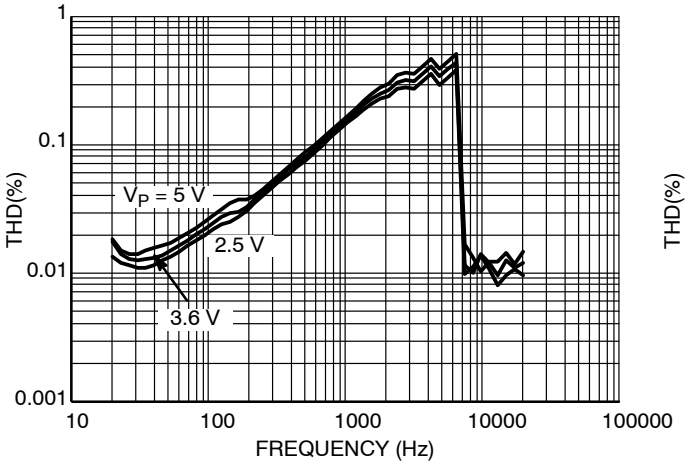


Figure 7. THD+N vs Frequency P_{out} = 250 mW, R_L = 8 Ω

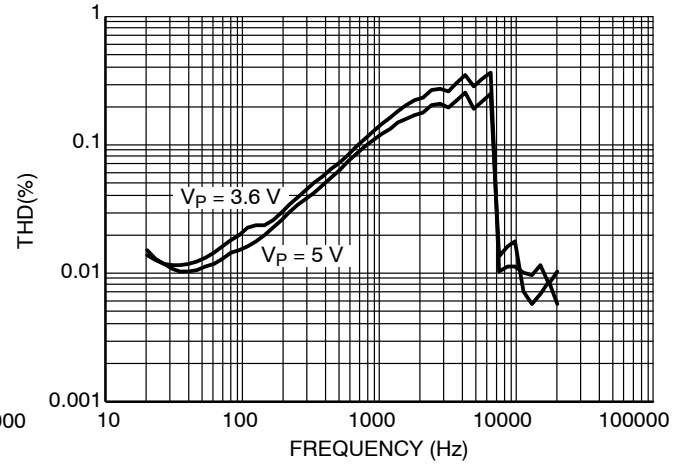


Figure 8. THD+N vs Frequency P_{out} = 500 mW, R_L = 8 Ω

TYPICAL OPERATING CHARACTERISTICS

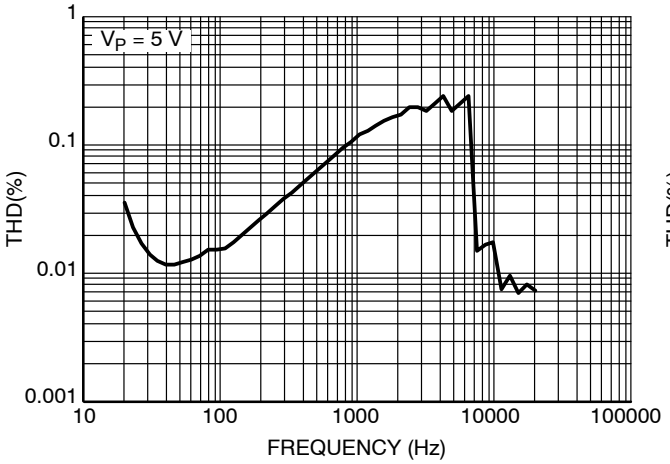


Figure 9. THD+N vs Frequency P_{out} = 1 W, R_L = 8 Ω

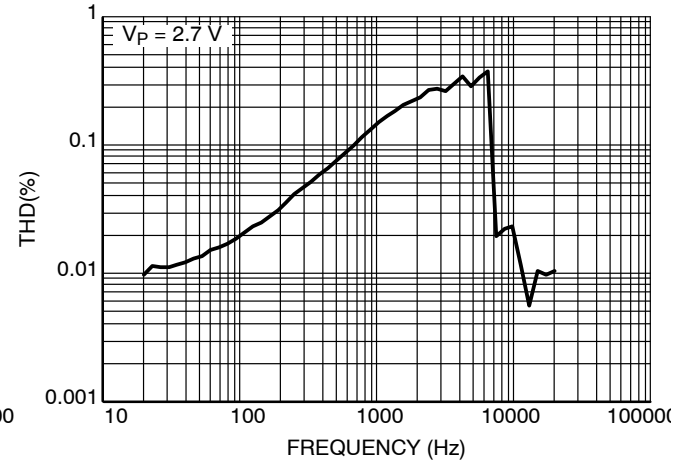


Figure 10. THD+N vs Frequency P_{out} = 300 mW, R_L = 4 Ω

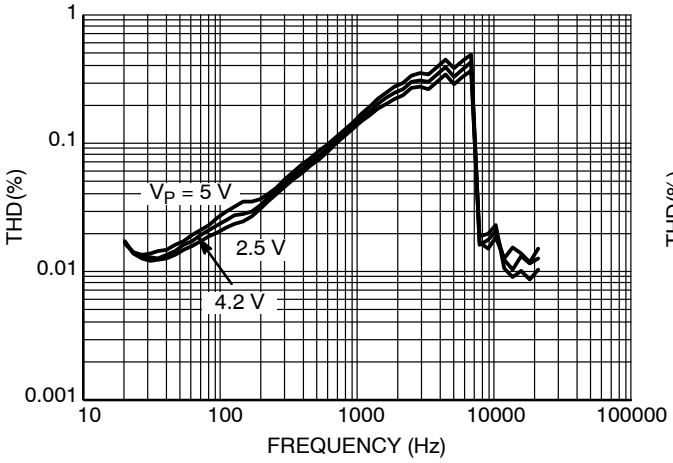


Figure 11. THD+N vs Frequency P_{out} = 500 mW, R_L = 4 Ω

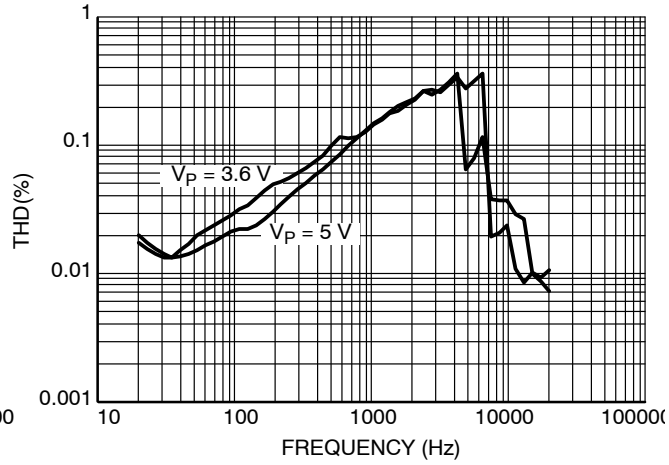


Figure 12. THD+N vs Frequency P_{out} = 1 W, R_L = 4 Ω

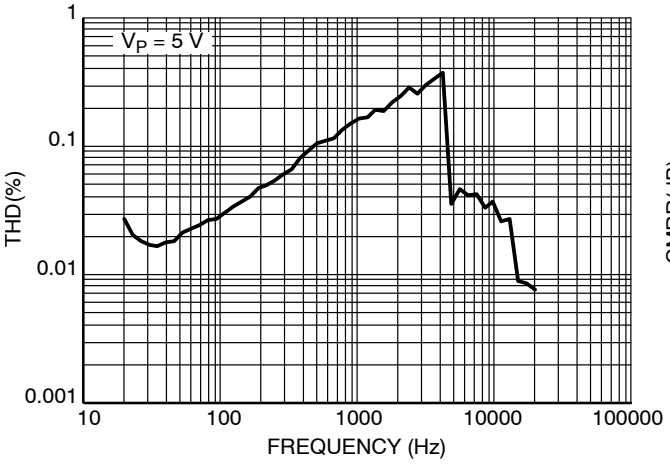


Figure 13. THD+N vs Frequency P_{out} = 2 W, R_L = 4 Ω

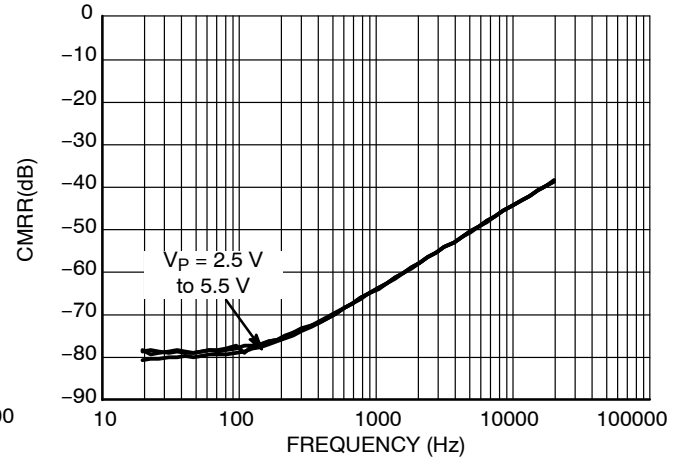


Figure 14. CMRR vs Frequency, V_{ipp} = 1 V_{pp}, R_L = 8 Ω

TYPICAL OPERATING CHARACTERISTICS

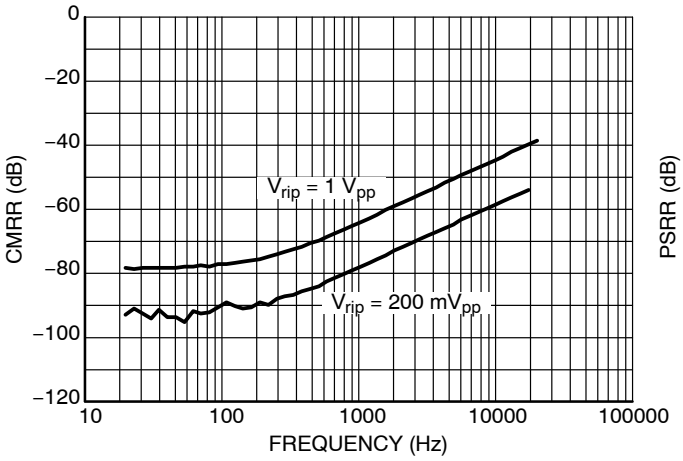


Figure 15. CMRR vs Frequency vs V_P

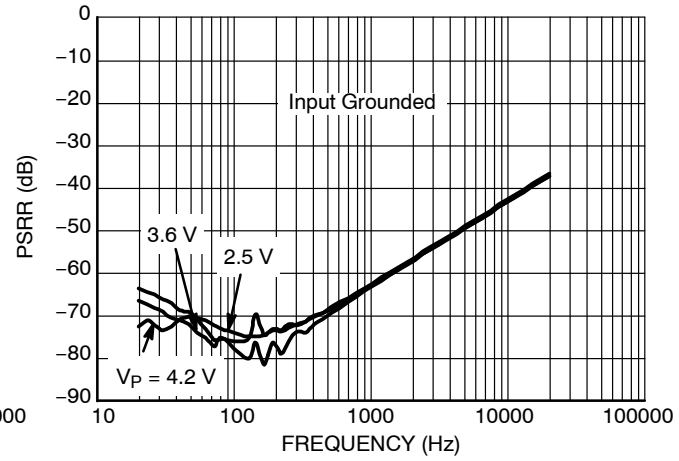


Figure 16. PSRR vs Frequency

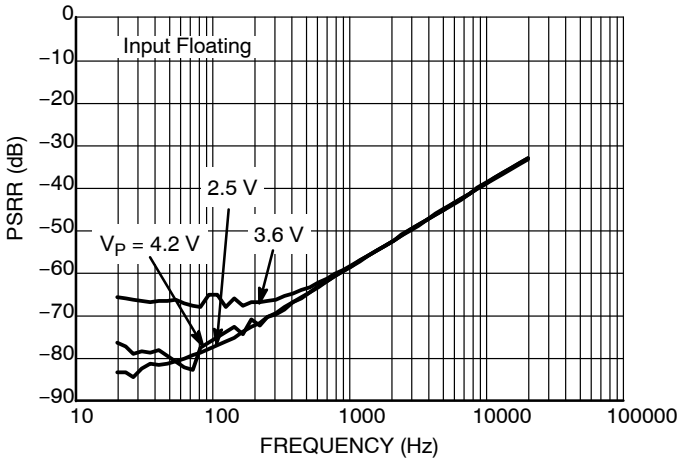


Figure 17. PSRR vs Frequency

DETAIL OPERATING DESCRIPTION

General Description

The basic structure of the NCP2823A/B is composed of one analog pre−amplifier, a pulse width modulator and an H−bridge CMOS power stage. The first stage is externally configurable with gain−setting resistor Ri and the internal fixed feedback resistor Rf (the closed−loop gain is fixed by the ratios of these resistors). The load is driven differentially through two output stages. The differential PWM output signal is a digital image of the analog audio input signal. The human ear is a band pass filter regarding acoustic waveforms, which the typical cut off values are 20 Hz and 20 kHz. Thus, the user will hear only the amplified audio input signal within the frequency range. The switching frequency and its harmonics are fully filtered. The inductive parasitic element of the loudspeaker helps to guarantee a superior distortion value.

Power Amplifier

The output PMOS and NMOS transistors of the amplifier have been designed to deliver a maximum output power before clipping. The channel resistance (Ron) of the NMOS and PMOS transistors is typically 0.3 Ω.

Gain Selection

The preamplifier stage amplifies the input signal. The gain is fully configurable by external resistors.

The gain setting is given by the following equation:

$$Av = \frac{300\ k\Omega}{Ri} \qquad \text{(eq. 1)}$$

Turn On and Turn Off Transitions

In order to reduce “pop and click” noises during transition, the output power in the load must not be established or cutoff suddenly. When logic high is applied to the Enable pin, the internal biasing voltage rises quickly and, 4 ms later, once the output DC level is around the common mode voltage, the gain is established slowly (5.0 ms). Thus, the total turn on time to get full power to the load is 7.4 ms (typical). The device has the same behavior when it is turned−off by a logic low on the Enable pin. No power is delivered to the load 4 ms after a falling edge on the shutdown pin. Due to the fast turn on and off times, the shutdown signal can be used as a mute signal as well.

Shutdown Function

The device enters shutdown mode when the Enable signal is low. During the shutdown mode, the DC Shutdown current of the circuit does not exceed 1 μA.

The NCP2823A/B has an internal resistor (R_{PLD} = 250 kΩ) connected between GND and Enable. The purpose of this resistor is to eliminate any unwanted state changes when the Enable pin is floating.

30 kHz Built−in Low Pass Filter

This filter allows connecting directly a DAC or a CODEC to the NCP2823 input without increasing the output noise by mixing frequency with the DAC/CODEC output frequency. Consequently, optimized operation with DACs or CODECs is guaranteed without additional external components.

Power Supply Bypassing

The NCP2823 requires a correct decoupling of the power supply in order to guarantee the best operation in terms of audio performances. To achieve these performances, it is necessary to place a 4.7 μF low ESR ceramic capacitor as close as possible to the PVDD pin in order to reduce high frequency transient spikes due to parasitic inductance (see Layout considerations).

Input Capacitors C_{in}

Thanks to its fully differential architecture the NCP2823 does not require input capacitors. However, it is possible to use input capacitors when the differential source is not biased or in single ended configuration. In this case it is necessary to take into account the corner frequency which can influence the low frequency response of the NCP2823. The following equation will help choose the adequate input capacitor.

$$f_C = \frac{1}{2 \cdot \pi \cdot Ri \cdot C_{in}} \qquad \text{(eq. 2)}$$

Over Current Protection

This protection allows detecting an over current in the H−Bridge. When the current is higher than 2A for the NCP2823B or 1A for the NCP2823A, the H−Bridge is positioned in high impedance. When the short circuit is removed or the current is lower, the NCP2823 goes back to normal operation. This protection avoids over current due to a bad assembly (Output shorted together, to V_{DD} or to ground).

Layout Recommendations

For Efficiency and EMI standpoints, it is strongly recommended to use Power and ground plane in order to reduce parasitic resistance and inductance.

For the same reason, it is recommended to keep the output traces short and well shielded in order to avoid them to act as antenna.

The EMI Level is strongly dependent upon the application. However, ferrite beads placed close to the NCP2823 will reduce EMI radiation when it is needed.

Ferrite value is strongly dependent upon the application.

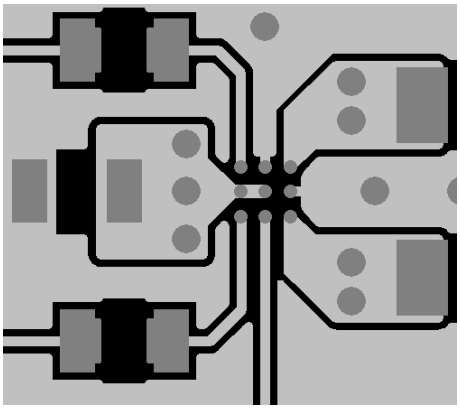


Figure 18. PCB Layout example

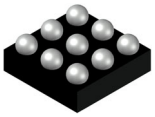
ORDERING INFORMATION

Device	Package	Shipping†
NCP2823AFCT2G	WLCSP9 (Pb−Free)	3000 / Tape & Reel
NCP2823AFCCT2G	WLCSP9 (Backside Laminate Coating) (Pb−Free)	3000 / Tape & Reel
NCP2823BFCT1G	WLCSP9 (Pb−Free)	3000 / Tape & Reel
NCP2823BFCT2G	WLCSP9 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

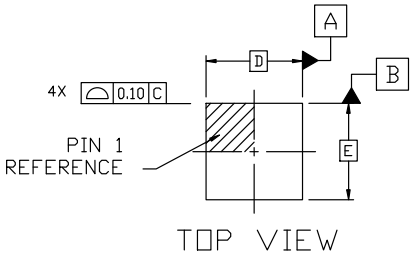
Demo Board Available:

NCP2823AGEVB/D and NCP2823BGEVB/D evaluation board configure the device in typical application.

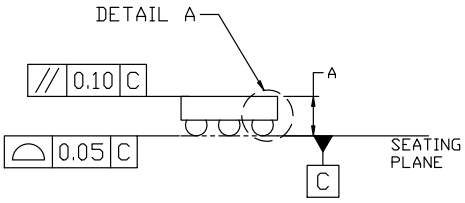


9 PIN FLIP−CHIP 1.45x1.45x0.596
CASE 499AL
ISSUE A

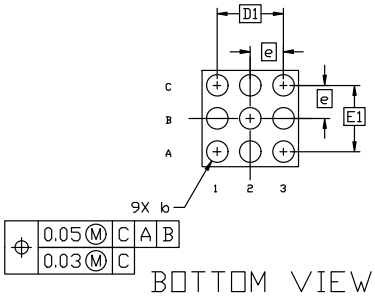
DATE 21 JUN 2022



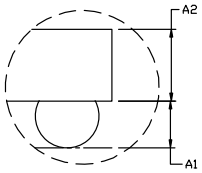
TOP VIEW



SIDE VIEW



BOTTOM VIEW

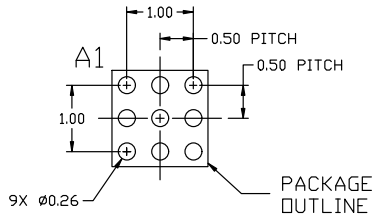


DETAIL A
SCALE 1:3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

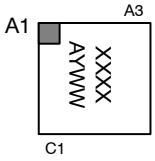
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.541	0.596	0.651
A1	0.206	0.236	0.266
A2	0.335	0.360	0.385
b	0.289	0.319	0.349
D	1.450 BSC		
D1	1.000 BSC		
E	1.450 BSC		
E1	1.000 BSC		
e	0.50 BSC		



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
G or ▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**9 PIN FLIP−CHIP 1.45x1.45x0.596**		**PAGE 1 OF 1**

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