# NCP398

# USB Type-C VCONN Overvoltage Protection IC

The NCP398 is an overvoltage protection device. It protects VCONN against overvoltages in applications where VCONN is directly derived from the VBUS supply.

At power up, the integrated power MOSFET is automatically controlled to reduce inrush current. The IC continuously monitors undervoltage, overvoltage and thermal events. In case of overvoltage, a very high speed comparator opens the power MOSFET instantaneously.

The part is enabled through the $\overline{EN}$ pin. A high level on this pin allows forcing off the internal switch and drastically decreases the current consumption of the NCP398 core.

### Features

- Over−voltage Protection up to + 28 V
- On−chip Low $R_{dson}$ NMOS Transistors: Typical 200 mΩ
- Over−voltage Lockout (OVLO)
- Shutdown $\overline{EN}$ Input
- Output Discharge Path
- WLCSP4 Package 0.84 x 0.84 mm, 0.4p
- UDFN6 Package 2 x 2 mm, 0.65p
- These Parts are ROHS Devices

### Typical Applications

- Type−C USB
- Smartphones
- Tablets

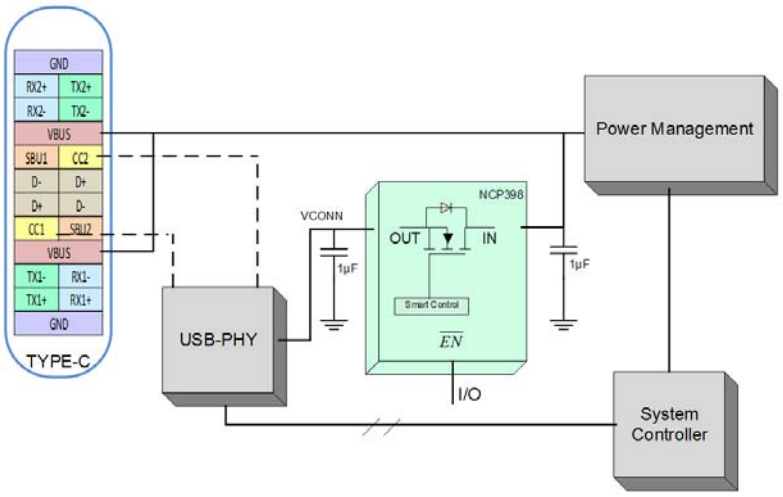


**Figure 1. Typical Application Circuit**

**ON Semiconductor®**

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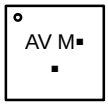
### MARKING DIAGRAMS



**UDFN6**
**CASE 517AB**




AV = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

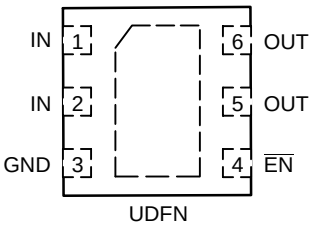


**WLCSP4**
**CASE 567MN**

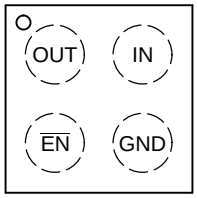



AA = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week

### PIN CONNECTIONS




UDFN




WLCSP

(Top Views)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 11 of this data sheet.

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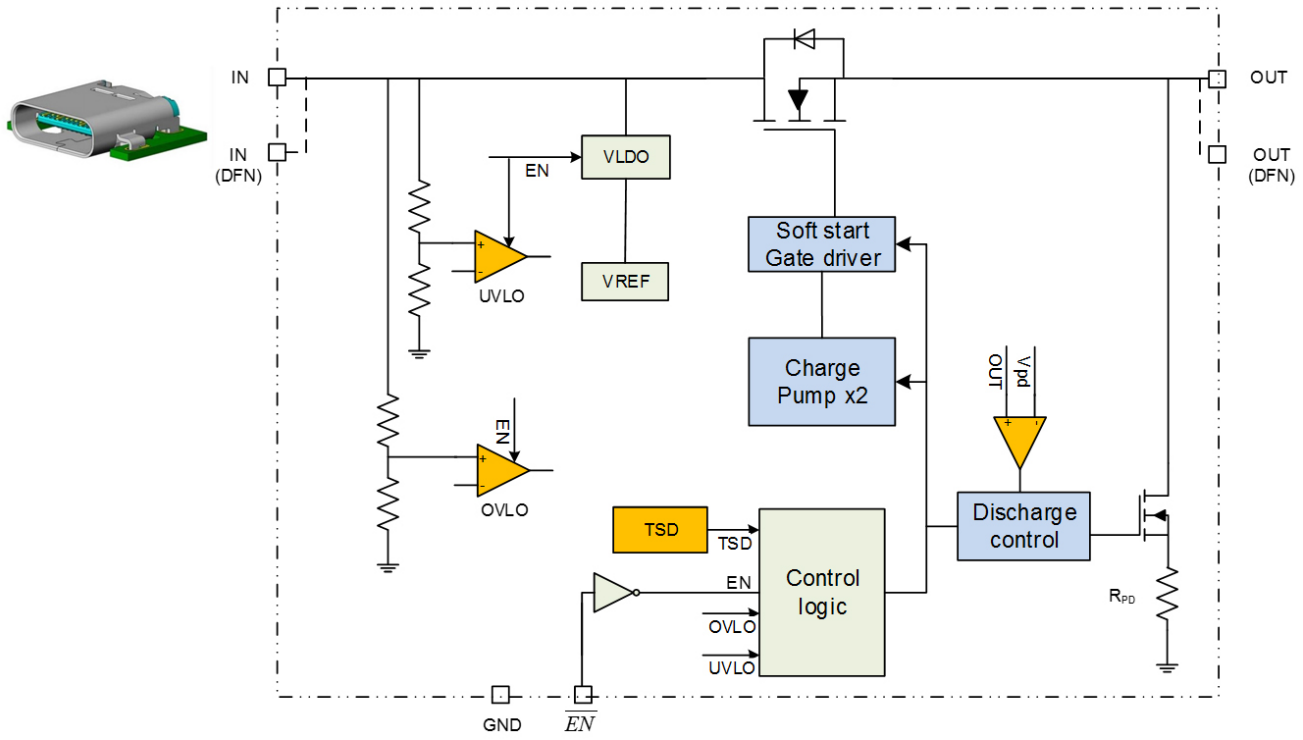



**Figure 2. Simplified Block Diagram, WLCSP and UDFN Packages**

**Table 1. CSP PINOUT DESCRIPTION**

| Pin | Pin Name | Type | Description |
|---|---|---|---|
| A1 | OUT | OUTPUT | Output voltage pin.<br>The OUT pin must be connected to the circuitry that is to be protected (VCONN rail). |
| B1 | $\overline{EN}$ | I/O | Enable pin bar.<br>The device enters in shutdown mode when this pin is tied high in which case the output is disconnected from the input. |
| A2 | IN | POWER | Input voltage pin.<br>The IN pin must be connected to the input power supply (VBUS). |
| B2 | GND | POWER | Ground.<br>Must be connected to the system GND plane. |

**Table 2. DFN PINOUT DESCRIPTION**

| Pin | Pin Name | Type | Description |
|---|---|---|---|
| 1,2 | IN | POWER | Input voltage pins.<br>The two IN pins must be hardwired together and are connected to the input power supply (VBUS). |
| 3 | GND | POWER | Ground.<br>Must be connected to the system GND plane. |
| 5,6 | OUT | POWER | Output voltage pins.<br>The two OUT pins must be hardwired together and are connected to the circuitry that is to be protected (VCONN rail). |
| 4 | $\overline{EN}$ | I/O | Enable pin bar.<br>The device enters in shutdown mode when this pin is tied high in which case the output is disconnected from the input. |
| 7 | PAD | POWER | DFN package back side pad. Must be connected to ground plane for thermal dissipation optimization. |

**Table 3. MAXIMUM RATINGS**

| Rating | | Symbol | Value | Unit |
|---|---|---|---|---|
| Minimum Voltage (All to GND) | | $V_{MIN}$ | −0.3 | V |
| Maximum Voltage (Ins to GND) | | $V_{INMAX}$ | 29 | V |
| Maximum Voltage (All others to GND) | | $V_{MAX}$ | 7 | V |
| Maximum DC current | | $I_{MAX}$ | 0.8 | A |
| Thermal Resistance, Junction to Air | WLCSP (Note 1)<br>DFN (Note 1) | $R_{\theta JA}$ | 170<br>145 | °C/W |
| Operating Ambient Temperature Range | | $T_A$ | −40 to +85 | °C |
| Storage Temperature Range | | $T_{STG}$ | −65 to +150 | °C |
| Junction Operating temperature | | $T_J$ | +125 | °C |
| Human Body Model (HBM) ESD Rating are (Note 2) | | ESD HBM | 2 | kV |
| Charged Device Model (CDM) ESD Rating are (Note 2) | | ESD CDM | 1 | kV |
| Latch Up Current (Note 3) | | $I_{LU}$ | 100 | mA |
| Moisture Sensitivity | | MSL | Level 1 | |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The $R_{\theta JA}$ is highly dependent on the PCB heat sink area. As example UDFN6 $R_{\theta JA}$ is 220°C/W with 50 $mm^2$ (copper 35 μm, 1 oz) and 145°C/W with 200 $mm^2$ (copper 35 μm, 2 oz).
2. Human Body Model, 100 pF discharged through a 1.5 kΩ resistor following specification JESD22/A114, Charged Device Model (CDM) per JEDEC standard: JESD22−C101 Class IV.
3. Latch Up Current per JEDEC standard: JESD78 class II.

**Table 4. ELECTRICAL CHARACTERISTICS**
Min / Max limits values (−40°C < $T_A$ < +85°C) and $V_{IN}$ = +5 V (Unless otherwise noted). Typical values are $T_A$ = +25°C.

| Characteristics | Symbols | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Input Voltage Range | $V_{IN}$ | | − | − | 28 | V |
| Under Voltage Lockout | UVLO | Vin rising | 2.4 | − | 2.8 | V |
| Under Voltage Lockout Hysteresis | $UVLO_{HYST}$ | Vin falling | − | 50 | − | mV |
| Over voltage Lockout Threshold | OVLO (Note 4) | Vin rising | 5.50 | 5.65 | 5.80 | V |
| Over voltage Lockout Threshold hysteresis | $OVLO_{HYST}$ | Vin falling | − | 115 | − | mV |
| Vin versus Vout Resistance | $R_{DSON}$ | Vin = 5 V, $\overline{EN}$ = low, 25°C, WLCSP | − | 190 | 220 | mΩ |
| | | –40°C < $T_J$ < 85°C, WLCSP | − | 230 | 260 | |
| | | Vin = 5 V, $\overline{EN}$ = low, 25°C, UDFN | − | 230 | 260 | |
| | | –40°C < $T_J$ < 85°C, UDFN | − | 270 | 300 | |
| Supply Quiescent Current | $I_{DD}$ | No load. $\overline{EN}$ = low | − | 40 | 60 | μA |
| OFF current | $I_{OFF}$ | $\overline{EN}$ = high | − | − | 1.5 | μA |
| Standby current | $I_{STB}$ | Vin = 2.4 V | − | − | 2.5 | μA |
| Output Discharge path | $R_{PD}$ | From $\overline{EN}$ = low to high or Vin < UVLO – hysteresis to Vout = $V_{PD}$ | 8 | 10 | 12 | kΩ |
| Output Discharge path level | $V_{PD}$ | Vout falling | − | 0.63 | − | V |
| **$\overline{EN}$** | | | | | | |
| $\overline{EN}$ Voltage High | $V_{IH}$ | | 1.2 | − | − | V |
| $\overline{EN}$ Voltage Low | $V_{IL}$ | | − | − | 0.4 | V |
| $\overline{EN}$ Input Leakage Current | $I_{\overline{EN}}$ | 0 < $V_{\overline{EN}}$ < 5.5 V | −1 | 0 | +1 | μA |
| **TIMINGS** | | | | | | |
| Ton Time | $T_{ON}$ | Vin valid, From $\overline{EN}$ high to low, 90% Vout | − | 0.3 | 1 | ms |
| Disable Time | $T_{OFF}$ | From $\overline{EN}$ low to high, to 90% Vout. $R_{LOAD}$ 100 Ω | − | 10 | − | μs |
| OVLO Turn Off Time | $T_{OVLO}$ | Vin exceeding $V_{OVLO}$ at 2 V/μs to Vout starts decreasing. $R_{LOAD}$ 100 Ω | − | 100 | − | ns |
| **TSD** | | | | | | |
| Thermal shutdown | TSD | | − | 150 | − | °C |
| Thermal shutdown rearming | TSD rearm | | − | 125 | − | °C |

4. Please contact your ON representative for additional OVLO thresholds.
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

### Operation

The NCP398 device provides overvoltage protection when a wrong input supply is connected or voltage ringing appears on the input line. The internal NMOS Fet is soft start controlled to limit inrush current into the load (capacitors, IC wake up).

The device integrates an enable control pin, undervoltage and overvoltage comparators, and output discharge path to eliminate residual voltage after the turn off.

### Timings Chronogram and States Description

The phase 1 sections described below are respectively the OFF state ($\overline{EN}$ high) and the standby state (VIN < UVLO) of the device. When Vin is below the undervoltage comparator (UVLO) or $\overline{EN}$ is tied high, NCP398 will be in this state.

Phase 2 corresponds to the defined time for the gate driver soft start. Referring to the electrical parameter, this phase is aligned to Ton time.

Phase 3 is the normal operation, with Vin valid, the part enabled and there is no fault.

The behavior during an overvoltage condition is detailed in the phase number 4.

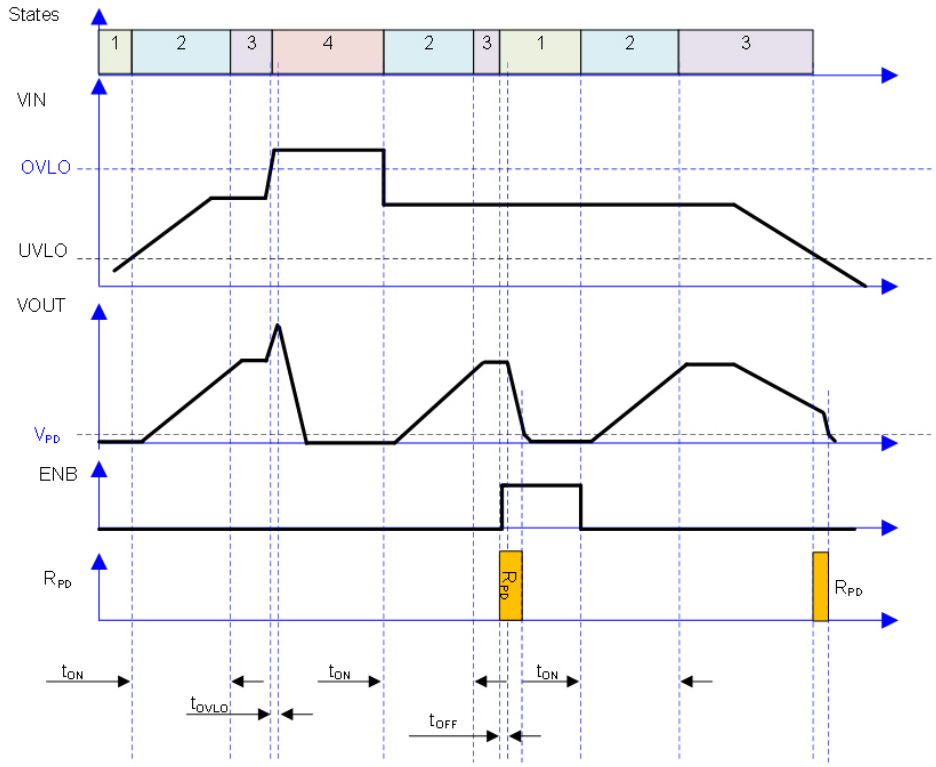



**Figure 3. Timings Diagram**

### Enable Bar Pin ($\overline{EN}$)

The part is enabled through the $\overline{EN}$ pin. In some diagrams and figures, ENB refers to $\overline{EN}$. A high level on this pin allows forcing off the internal switch and drastically decreases the current consumption of the NCP398 core. To exit the OFF state, the $\overline{EN}$ pin must be tied low.

### Under−voltage Lockout (UVLO)

To ensure proper operation under any conditions, the device integrates an under−voltage lock out (UVLO) comparator. This block has a built−in hysteresis to provide noise immunity to transient conditions.

### Over−voltage Lockout (OVLO)

To protect connected systems on $V_{OUT}$ pin from over−voltage, a second comparator, over−voltage lock out (OVLO), is embedded. During over−voltage condition, the output remains disabled until the input voltage drops below the OVLO – comparator hysteresis.

### Auto Discharge − $R_{PD}$

When disabling the NCP398 the output gets automatically discharged by means of the internal pull down resistor Rpd. Once reaching the Vpd level the discharge path is disabled. The auto−discharge is also engaged when Vin drops below the UVLO threshold. The auto−discharge ensures a proper power cycling of peripherals connected to the output of the NCP398.

### Thermal Shutdown Protection

In case of internal overheating, the integrated thermal shutdown (TSD) protection will open the internal NMOS FET in order to instantaneously decrease the device temperature.

Embedded hysteresis allows reengaging the NMOS FET when the junction temperature decreases.

This OFF−ON cycle is repeated until the fault event disappears.

## TYPICAL CHARACTERISTICS

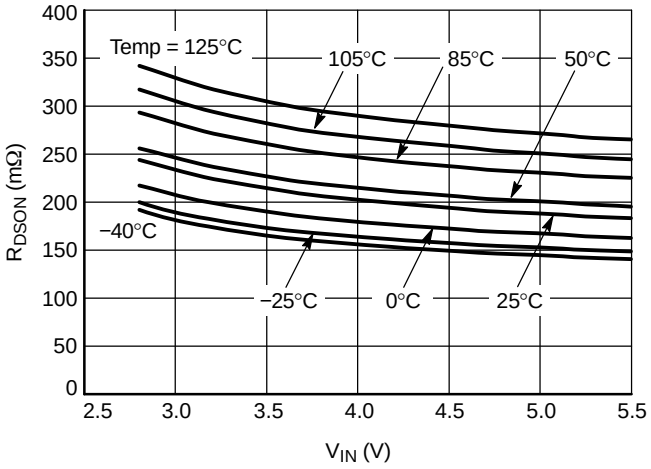



**Figure 4. Ron vs. Vin, Overtemperature**

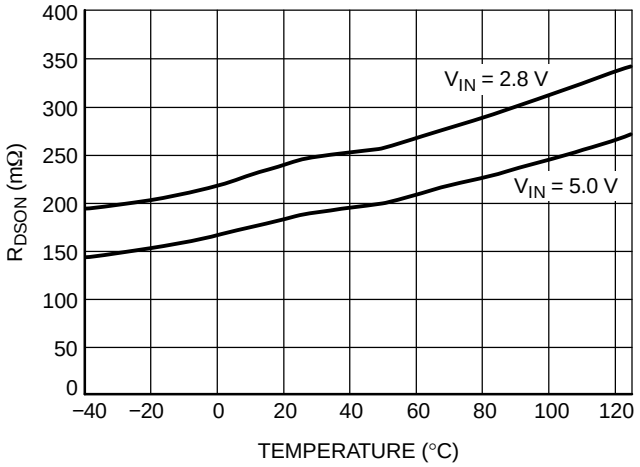



**Figure 5. Ron vs. Temperature, at Fixed Vin Voltage**

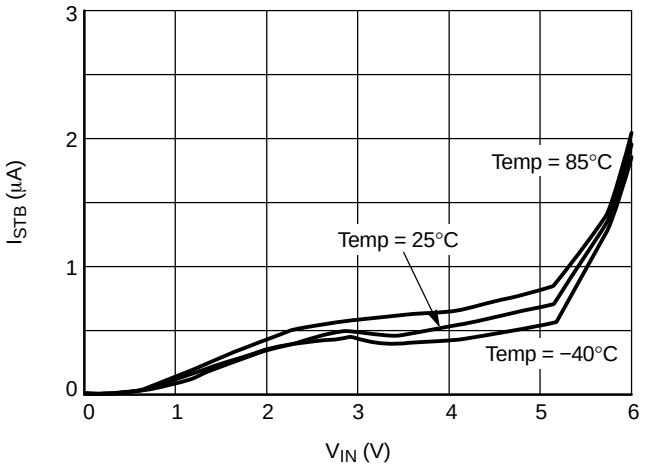



**Figure 6. Standby Current vs. Vin, Over Temperature**

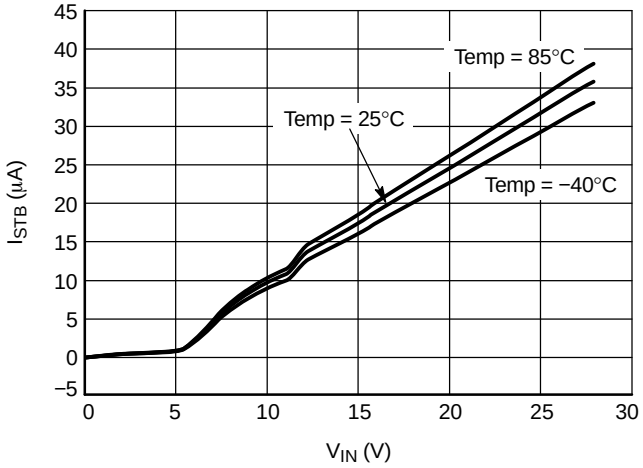



**Figure 7. Standby Current vs. Vin, Over Temperature**

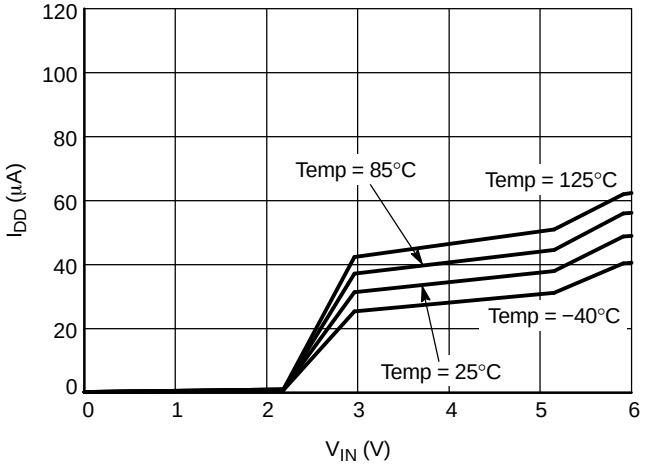



**Figure 8. Quiescent Current vs. Vin, Over Temperature**

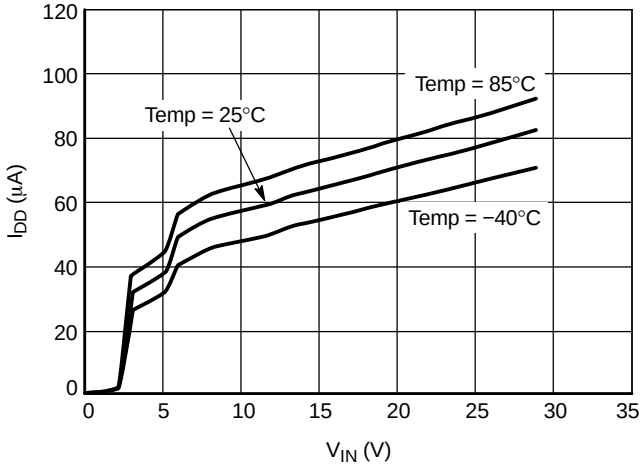



**Figure 9. Quiescent Current vs. Vin, Over Temperature**

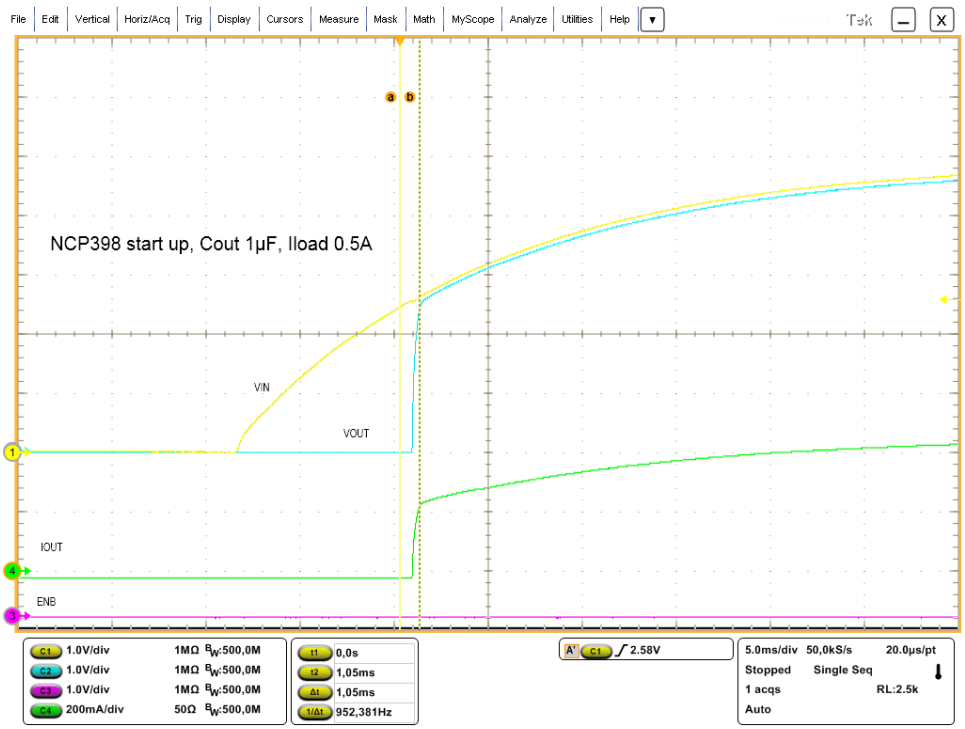



**Figure 10. Soft Start Up On Load, Vin: yellow, Vout: blue, $\overline{EN}$: pink, IOUT: green**

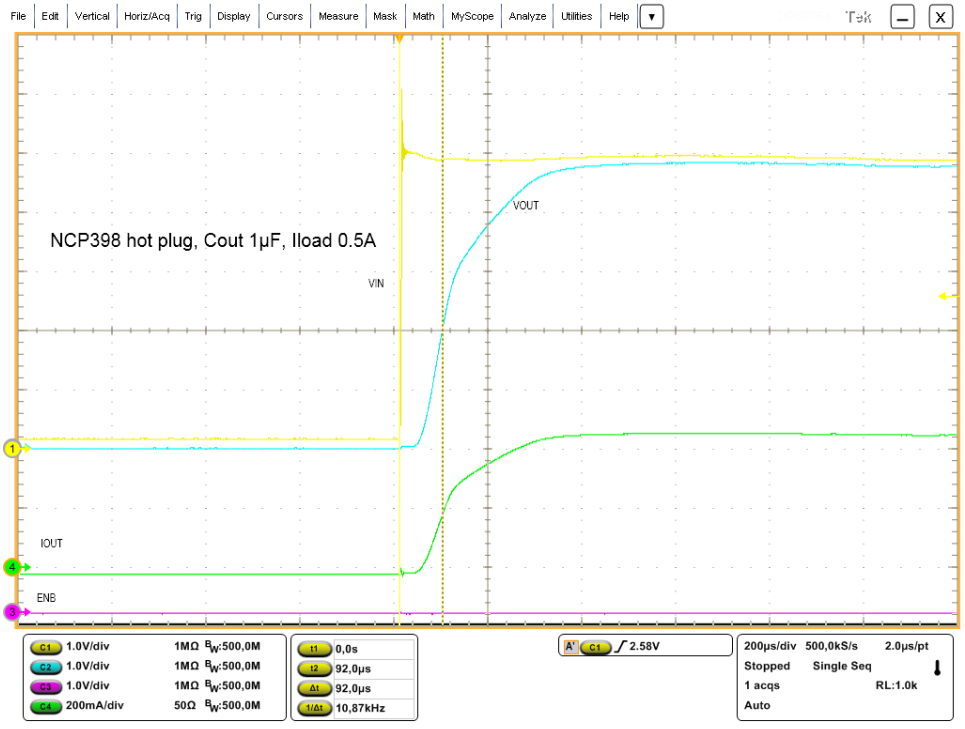



**Figure 11. Hot Plug On Load, Vin: yellow, Vout: blue, $\overline{EN}$: pink, IOUT: green**

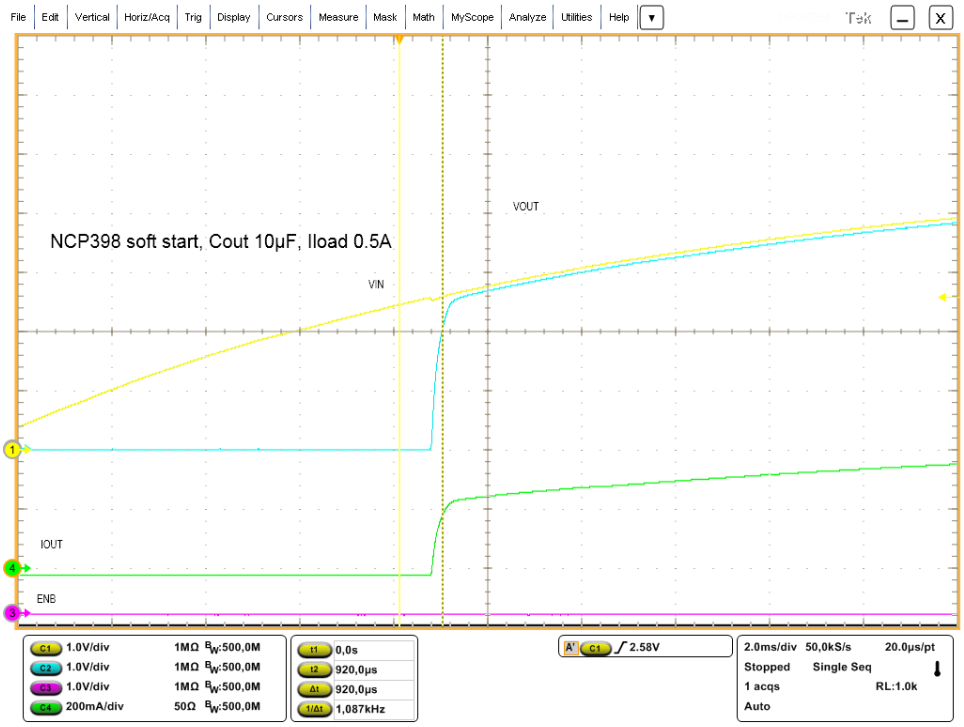



**Figure 12. Soft Start On Cout 10 µF, 500 mA, Vin: yellow, Vout: blue, $\overline{EN}$: pink, IOUT: green**

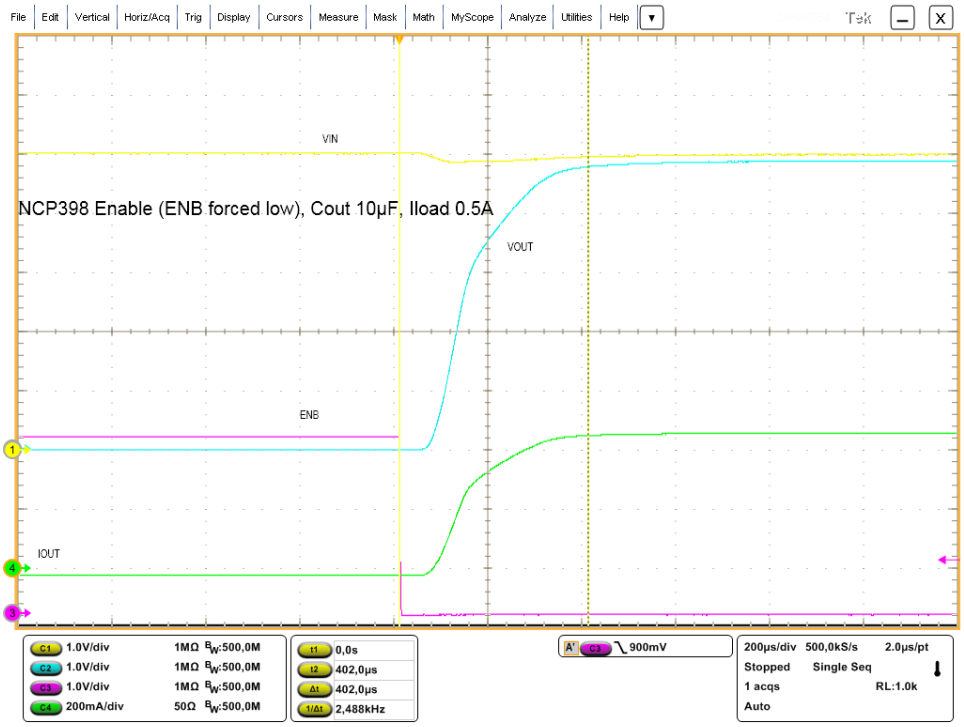



**Figure 13. NCP398 Enable (ENB forced low) Vin: yellow, Vout: blue, $\overline{EN}$: pink, IOUT: green**

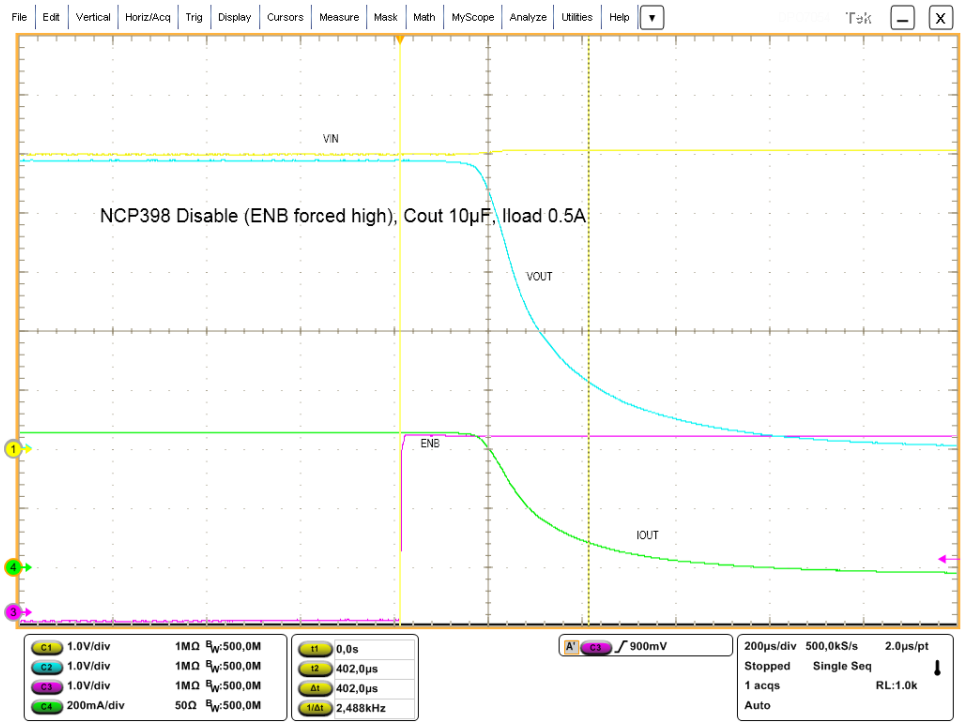



**Figure 14. NCP398 Disable (ENB forced high) Vin: yellow, Vout: blue, $\overline{EN}$: pink, IOUT: green**

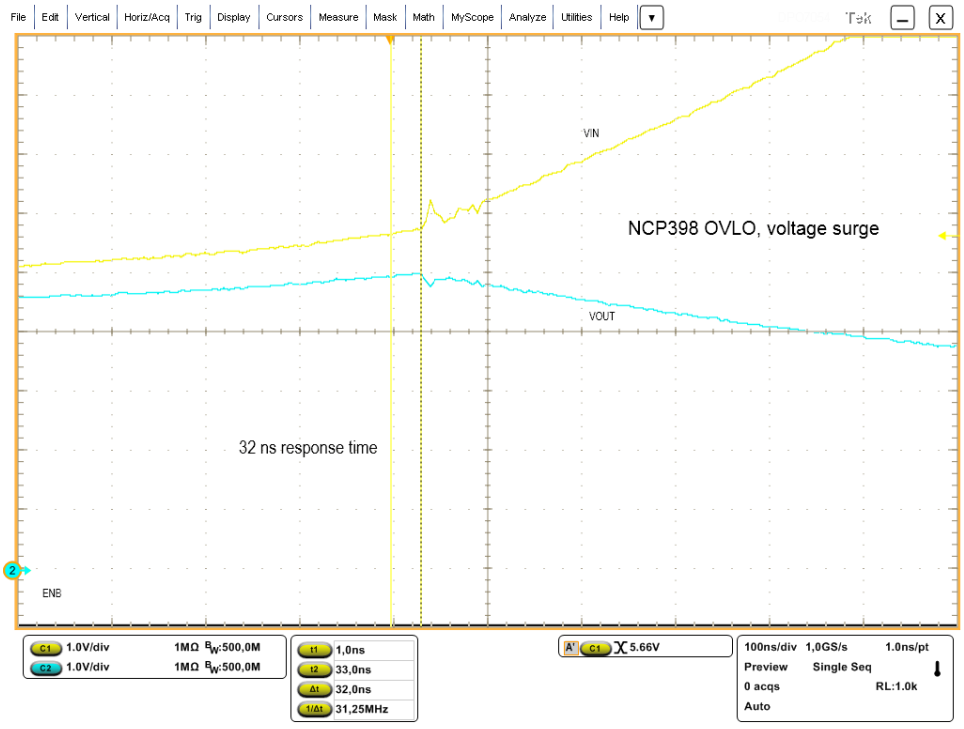



**Figure 15. NCP398 Overvoltage Time Response, Vin: yellow, Vout: blue**

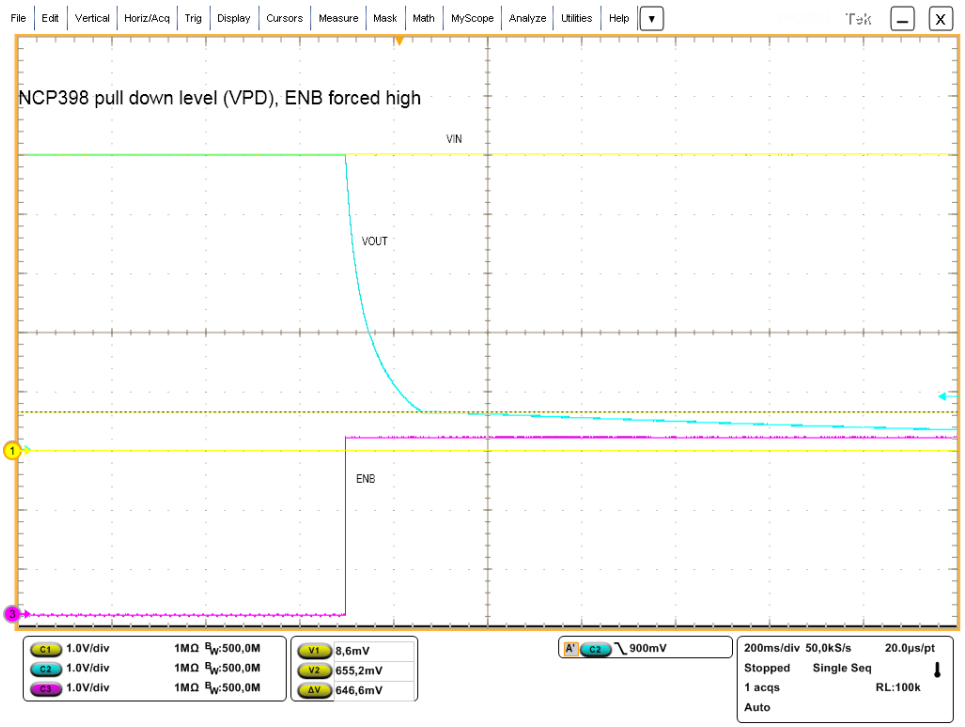



**Figure 16. NCP398 Pull Down Level (following disable) Vin: yellow, Vout: blue, $\overline{EN}$: pink**

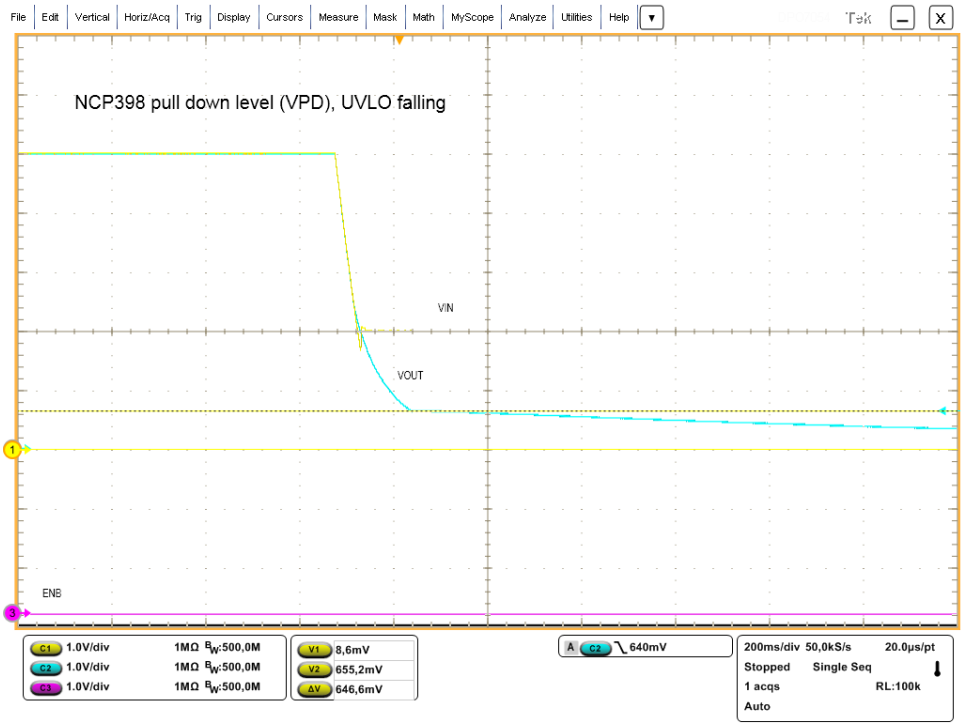



**Figure 17. NCP398 Pull Down Level (following UVLO) Vin: yellow, Vout: blue, $\overline{EN}$: pink**

## ORDERING INFORMATION

| Device | Marking | Package | Shipping† |
|---|---|---|---|
| NCP398FCCT1G | AA | WLCSP4 0.84x0.84 mm | 3000 Tape / Reel |
| NCP398MUTBG | AV | UDFN6 2x2 mm | 3000 Tape / Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

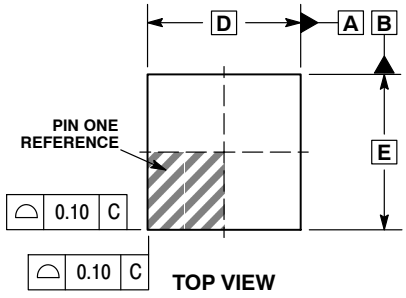
ON Semiconductor®



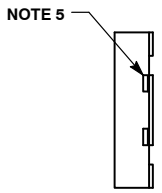
SCALE 4:1

**UDFN6 2x2, 0.65P**
CASE 517AB
ISSUE C

DATE 10 APR 2013



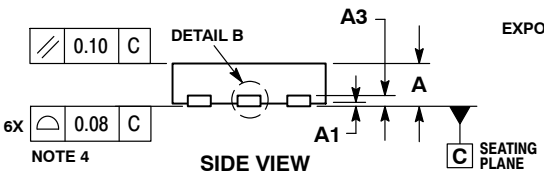

TOP VIEW



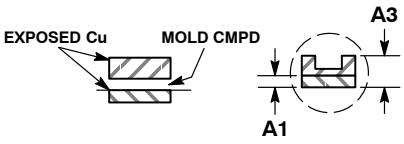

END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TIE BARS MAY BE VISIBLE IN THIS VIEW AND ARE CONNECTED TO THE THERMAL PAD.

| DIM | MILLIMETERS MIN | MAX |
|---|---|---|
| A | 0.45 | 0.55 |
| A1 | 0.00 | 0.05 |
| A3 | 0.127 REF | |
| b | 0.25 | 0.35 |
| D | 2.00 BSC | |
| D2 | 1.50 | 1.70 |
| E | 2.00 BSC | |
| E2 | 0.80 | 1.00 |
| e | 0.65 BSC | |
| L | 0.25 | 0.35 |
| L1 | --- | 0.15 |




SIDE VIEW




DETAIL B
ALTERNATE
CONSTRUCTIONS

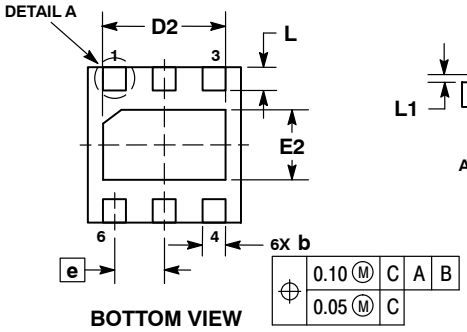
GENERIC
MARKING DIAGRAM*



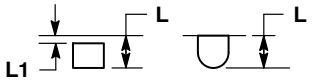

XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

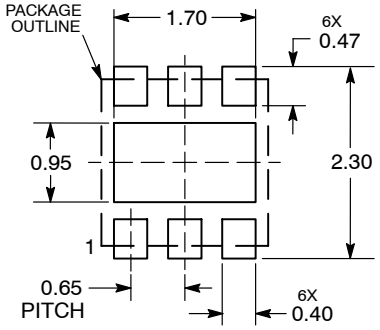



BOTTOM VIEW




DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

RECOMMENDED
SOLDERING FOOTPRINT*




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| DOCUMENT NUMBER: | 98AON22162D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
|---|---|---|
| DESCRIPTION: | UDFN6 2X2, 0.65P | PAGE 1 OF 1 |

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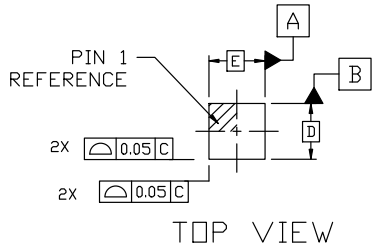
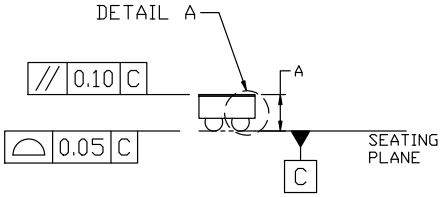
**WLCSP4, 0.84x0.84x0.554**
CASE 567MN
ISSUE B

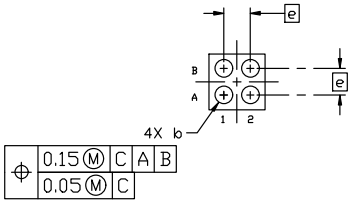
DATE 14 JUN 2022



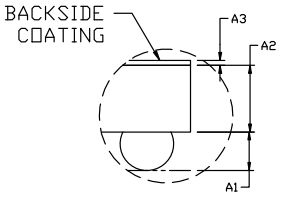

TOP VIEW




SIDE VIEW




BOTTOM VIEW

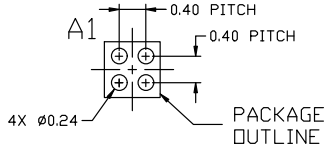



DETAIL A
SCALE 1:3

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO DATUM C.
4. COPLANARITY APPLIES TO THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. DATUM C, THE SEATING PLANE, IS DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.

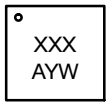
| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.509 | 0.554 | 0.599 |
| A1 | 0.174 | 0.194 | 0.214 |
| A2 | 0.310 | 0.335 | 0.360 |
| A3 | 0.025 BSC | | |
| b | 0.239 | 0.269 | 0.299 |
| D | 0.84 BSC | | |
| E | 0.84 BSC | | |
| e | 0.40 BSC | | |




RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC**
**MARKING DIAGRAM***




A = Assembly Location
Y = Year
W = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
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