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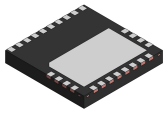
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Enhanced Mode GaN Power Switch with Integrated Driver

650 V, 150 mΩ, 11 A, TQFN26

NCP58920



TQFN26 8x8, 0.8P
CASE 518AG

The NCP58920 integrates a high−performance, high frequency, Silicon (Si) driver and a 650 V, 150 mΩ Gallium−Nitride (GaN) High Electron Mobility Transistors (HEMT) in a single switch structure. The powerful combination of the Si Driver and power GaN HEMT Switch provides superior performance compared to discrete solution GaN HEMT and external driver. The NCP58920 integrated implementation significantly reduces circuit and package parasitics while enables more compact design.

Features

- 650 V 150 mΩ GaN HEMT with Integrated Driver
- 30 ns Typical Driver Propagation Delay
- 8x8 mm TQFN26 Package Minimizes Parasitic Inductances
- 2.75 mm Creepage Distance for Maximum Reliability
- Driver Turn−on Process is Adjustable Via External Resistor, which Enables EMI Optimization under Hard Switching Conditions
- GDS Logic Input, that Switches Driver Strength to Easy Accompanying with QR Flyback Controllers
- 6.0 V Driver Clamp Voltage Regulator
- TTL Compatible Schmitt Trigger and Rail−to−Rail PWM Input
- UVLO Protections for VDD and VDR Supplies
- Up to 200 V/ns dV/dt Slew Rate Transient Immunity
- 20 V Maximum VDD Ratings
- Pb−Free, Halogen Free and RoHS Compliant

Typical Applications

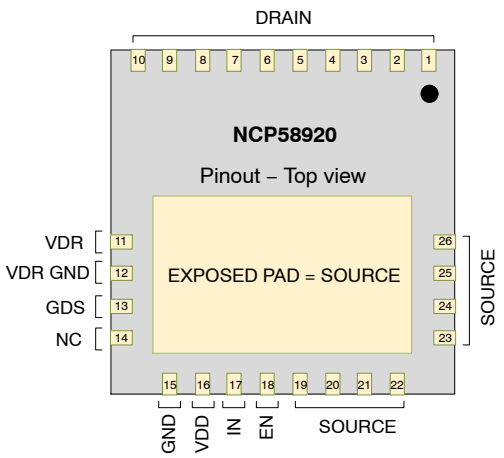
- Power Conversion
- High Power Density Power Supplies
- All Double−ended Topologies: Half−bridges, Full−bridge, LLC
- Active Clamp Flyback, QR Flyback
- High−Voltage Synchronous Buck Converter
- High−Voltage Synchronous Boost Converter
- Synchronous PFC Stage
- Totem Pole PFC

MARKING DIAGRAM



58920 = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 20 of this data sheet.

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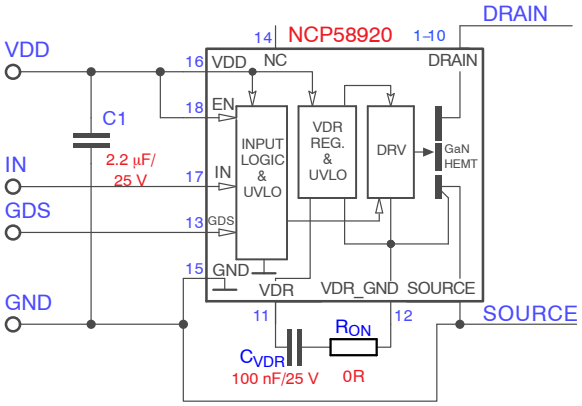


Figure 1. Minimum Application Schematic for Single Switch

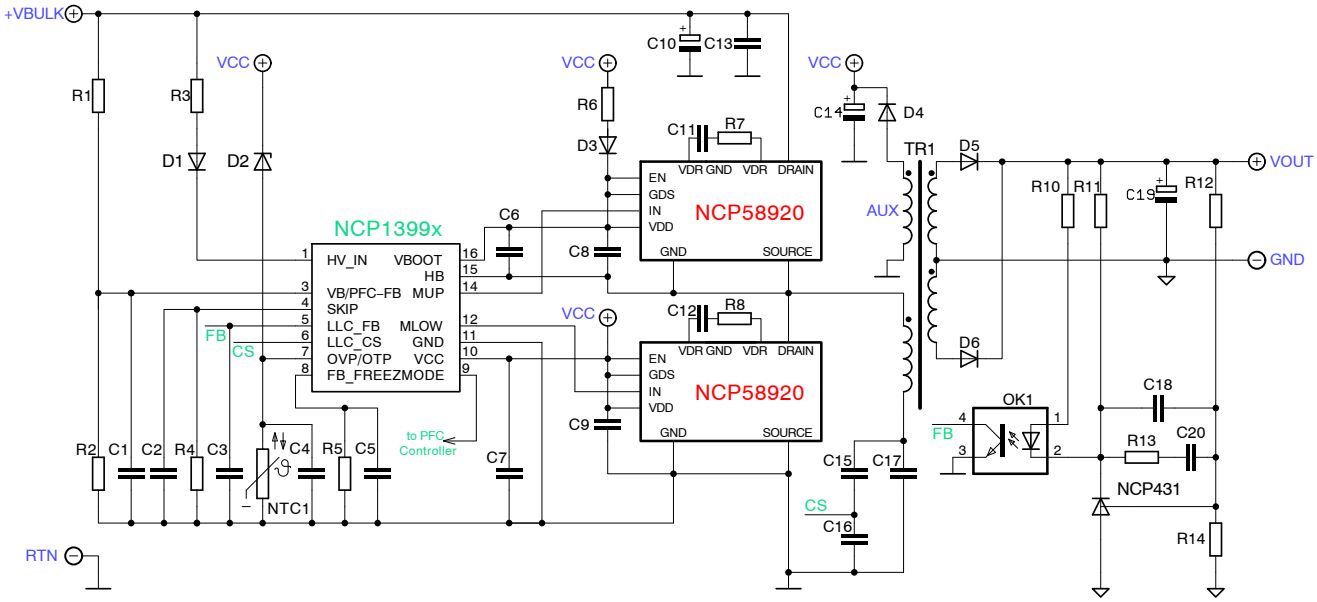


Figure 2. Application Schematic – HB LLC–Converter

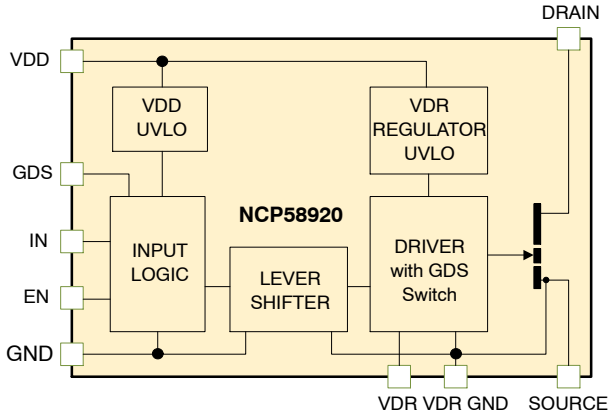


Figure 3. Simplified Block Diagram

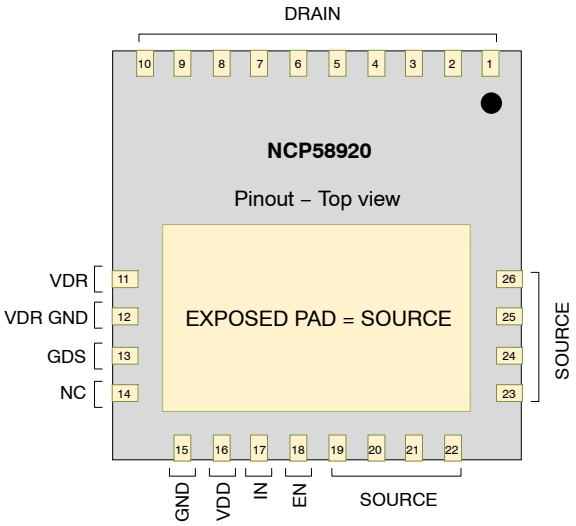


Figure 4. Pin Connection

PIN DESCRIPTION

Pin No.	Pin Name	Function	Pin Description
1 – 10	DRAIN	GaN Power Switch Drain	Power path connection for the GaN Switch DRAIN
19 – 22, 23 – 26,	SOURCE	GaN Power Switch Source	Power path connection for the GaN Switch SOURCE
11	VDR	Driver clamp regulator decoupling	Connect driver clamp regulator decoupling capacitor between VDR pin and VDR GND pin. To reduce turn−on slew rate is possible connect resistor in series with driver decoupling capacitor.
12	VDR GND	GaN Kelvin source and driver ground	Use this pin as return path for VDR decoupling capacitor. Do not connect to SOURCE or GND pin
13	GDS	Gate Drive Strength	According to GDS pin input level (low/ high) driver change Gate Drive Strength, thus turn−on slew rate. GDS pin can be used as interface to controller.
14	NC	Not connected	Not connected, (Note 1)
15	GND	Input circuitries signal ground	Input signals should be referred to this pin
16	VDD	Driver supply input	Driver accepts up to VDD up to 20 V. Connect VDD decoupling capacitor between VDD and SGND pins.
17	IN	Driver input	Driver signal input is 3.3 V logic compatible
18	EN	Logic input signal to enable the operation	Pull this pin high to allow device switching

1. NC Pad might be connected to trace to retain connection compatibility with NCP58921 in case of needed scalability.

ABSOLUTE MAXIMUM RATING

Rating	Symbol	Value	Unit
Supply Voltage Range, Referenced to GND (Note 2)	V_{DD}	−0.3 to 20	V
IN, EN and GDS Inputs Voltage Range, Referenced to GND	IN, EN, GDS	−0.3 to V_{DD} + 0.3	V
Driver−regulator decoupling, Referenced to VDR_GND	VDR	−0.3 to 6.5	V
Transient Drain−to−Source Voltage, For < 1 μs	$V_{DS(tran)}$	850	V
Allowable Drain−to−Source Voltage slew rate, Device is off	dV_{DS}/dt	200	V/ns
Continuous Drain Current, T_{case} = 25°C	I_{DS}	11	A
Continuous Drain Current, T_{case} = 100°C	I_{DS}	7.2	A
Pulsed Drain Current, T_{case} = 25°C, Pulse−width < 50 μs	$I_{DS-pulse}$	19	A
Maximum Junction Temperature	$T_{J(max)}$	150	°C
Storage Temperature Range	T_{STG}	−65 to 150	°C
ESD Capability, Charged Device Model (Note 3)	ESD_{CDM}	750	V
ESD Capability, Human Body Model (Note 3)	ESD_{HBM}	2.0	kV
Lead Temperature Soldering Reflow (SMD Styles Only), Pb−Free Versions (Note 4)	T_{SLD}	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
3. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latch−up Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
4. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Characteristics, TQFN26, 8x8 mm (Note 5) Thermal Resistance, Junction−to−Case (Exposed pad) Thermal Reference, Junction−to−Top Case Thermal Resistance, Junction−to−Air	 $R_{\theta JC}$ $R_{\Psi JL}$ $R_{\theta JA}$	 1.42 14 19	°C/W

5. Values based on copper area of 645 mm^2 (or 1 in^2) of 2 oz copper thickness, two layers FR4 PCB substrate with black mask.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage Range, (Note 7)	V_{DD}	9	18	V
IN, EN and GDS Inputs Voltage Range, Referenced to GND	IN, EN, GDS		18	V
VDR GND to GND − DC Offset Voltage	$V_{VDR\ GND} - V_{GND}$	−3.5	+3.5	V
Operation Junction Temperature	T_J	−40	+150	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. Maximum Recommended Operating Drain−to−Source Voltage or DC Bus Voltage must be considered voltage overshoots due to parasitic inductance in power loop. See page Application Drain−to−Source Voltage and its maximum recommended value.
7. The minimum V_{DD} Supply Voltage should be high enough above UVLO−off level to avoid unwanted device turn−off during dynamic operation.
8. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C.
9. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
10. $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while VDS is rising from 0 V to the stated V_{DS}.
11. $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while VDS is rising from 0 V to the stated V_{DS}.
12. The parameter is not tested in the production; value is guaranteed by the design.

ELECTRICAL CHARACTERISTICS

V_{DD} = 15 V, C_{VDD} = 1 μF, C_{VDR} = 0.1 μF, for typical values T_A = 25°C, V_{BUS} = 400 V, unless otherwise noted. (Note 8)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
GaN TRANSISTOR OUTPUT						
Maximum DRAIN Voltage	IN = 0 V, I_{DSS} < 18 μA	$V_{DS(max)}$	650			V
DRAIN−SOURCE Non−synchronous Drop Voltage	I_D = −1 A	V_{DSNS}	−4.5			V
DRAIN Leakage Current	V_{DS} = 650V, T_J = 25°C, IN = 0 V	I_{DLK}		0.2	7	μA
	V_{DS} = 650V, T_J = 150°C, IN = 0 V, (Note 9)	I_{DLK}		3.5		μA
DRAIN−SOURCE On State Resistance	I_D = 3.2 A, 500 μs, T_J = 25°C,	$R_{DS(on)}$		150		mΩ
	I_D = 3.2 A, 500 μs, T_J = 150°C, (Note 9)	$R_{DS(on)}$		310		mΩ
Output Capacitance	IN = 0 V; V_{DS} = 400 V, f = 100 kHz	C_{OSS}		20		pF
Output Capacitance Energy Related	(Notes 10, 12)	$C_{OSS(er)}$		30		pF
Output Capacitance Time Related	(Notes 11, 12)	$C_{OSS(tr)}$		47		pF
Output Charge	V_{DS} = 400 V, V_{IN} = 0 V, (Note 12)	Q_{OSS}		19		nC
Energy Stored in Output Capacitance	IN = 0 V, V_{DS} = 400 V, (Note 12)	E_{OSS}		2.4		μJ
Reverse Recovery Charge	(Note 12)	Q_{RR}		0		nC
POWER SUPPLY SECTION (VDD)						
Quiescent Current	V_{EN} = 0 V, V_{DD} = 15 V	I_{DDQ1}		55	75	μA
	V_{EN} = 5 V, V_{DD} = 15 V,	I_{DDQ2}		54	75	μA
Supply Current, Device Idle + EN Input Current	V_{EN} = 15V, V_{DD} = 15 V, V_{IN} = 0 V	$I_{DDQ1+ EN}$		100		μA
Operating VDD Supply Current	V_{EN} = 5V, V_{GDS} = 0V, V_{DD} = 15V, f_{IN} = 500 kHz, 50% DC			1.1	2.3	mA
UVLO ON Threshold	VDD Rising	V_{UVLO_R}		8.5	9	V
UVLO OFF Threshold	VDD Falling	V_{UVLO_F}	7.5	8		V
UVLO Hysteresis		V_{UVLO_HYST}		0.5		V
UVLO Filter Delay Time	VDD Rising	$t_{UVLO_DEL_R}$		3		μs
UVLO Filter Delay Time	VDD Falling	$t_{UVLO_DEL_F}$		3.2		μs
IN, EN INPUTS						
IN Input High−Logic−Level Voltage	IN / EN Rising	V_{IN_H}		2.1	2.5	V
IN Input Low−Logic−Level Voltage	IN / EN Falling	V_{IN_L}	1.2	1.5		V
Logic Input Voltage Hysteresis		V_{IN_HYST}		0.6		V
High−Level Logic Input Bias Current	V_{IN} = 5 V / V_{EN} = 5 V	I_{IN+}		15.3		μA
Input Pull−down Resistance	V_{IN} = 5 V / V_{EN} = 5 V	R_{IN}	250	327	400	kΩ
GDS INPUT						
High−Level Logic Input Voltage	GDS Rising	V_{GDS_H}		1.62	1.8	V
Low−Level Logic Input Voltage	GDS Falling	V_{GDS_L}	1.1	1.24		V
Logic Input Voltage Hysteresis		V_{GDS_HYST}		0.38		V
Input Pull−up Current Source	Current source referred to internal 5 V	I_{GDS_PULLUP}		1.08		μA
Driver SRC Resistance ("Weak" driving level or low slew rate),	V_{GDS} = LOW, (Note 12)	R_{SRC_weak}		300		Ω
Driver SRC Resistance ("Strong" driving level or higher slew rate)	V_{GDS} = HIGH, (Note 12)	R_{SRC_strong}		10		Ω

ELECTRICAL CHARACTERISTICS (continued)
V_{DD} = 15 V, C_{VDD} = 1 μF, C_{VDR} = 0.1 μF, for typical values T_A = 25°C, V_{BUS} = 400 V, unless otherwise noted. (Note 8)

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit
GATE DRIVER REGULATOR SECTION						
V_{DR} – V_{VDR_GND} Regulated Voltage	0 mA < $I_{O,DR}$ < 10 mA	V_{DR}	5.7	6	6.5	V
VDR UVLO ON Threshold	VDR Rising	V_{UVTH_R}		5.5	5.6	V
VDR UVLO OFF Threshold	VDR Falling	V_{UVTH_F}	4.6	5		V
VDR UVLO Hysteresis		V_{UVTH_HYST}		0.5		V
TIMING CHARACTERISTICS						
Switching Frequency		f_{SW}			1	MHz
Switch Maximal Turn−On time	(Note 13)	$t_{ON(MAX)}$			1	ms
Switch Minimal Turn−On time		$t_{ON(MIN)}$	25			ns
Switch Minimal Turn−Off time		$t_{OFF(MIN)}$	25			ns
Driver to Switch Turn−on Propagation Delay	(Note 14)	t_{PD_ON}		16		ns
Driver to Switch Turn−off Propagation Delay	(Note 14)	t_{PD_OFF}		16		ns
Switch Drain to Source Rise Time	R_{ON} = 0 Ω, I_L = 5 A, (Note 14)	t_R		6		ns
Switch Drain to Source Fall Time	R_{ON} = 0 Ω, I_D = 5 A, (Note 14)	t_F		7		ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
13. Internally limited by driver, do not use switch for continuous DC conduction.
14. Refer to Figure 37 and Figure 38.

TYPICAL CHARACTERISTICS

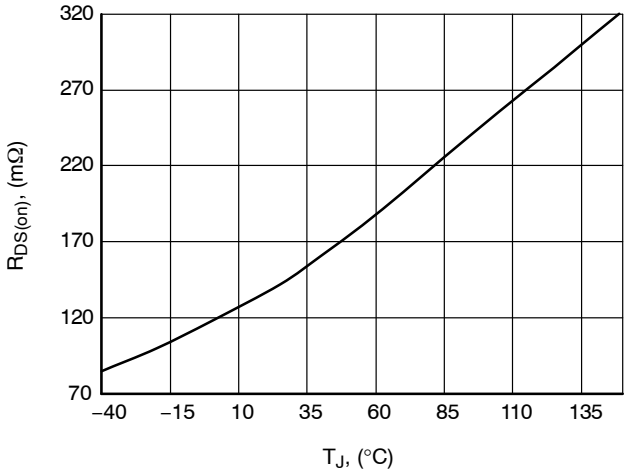


Figure 5. $R_{DS(on)}$ Drain−Source Turn−On Resistance vs. Temperature

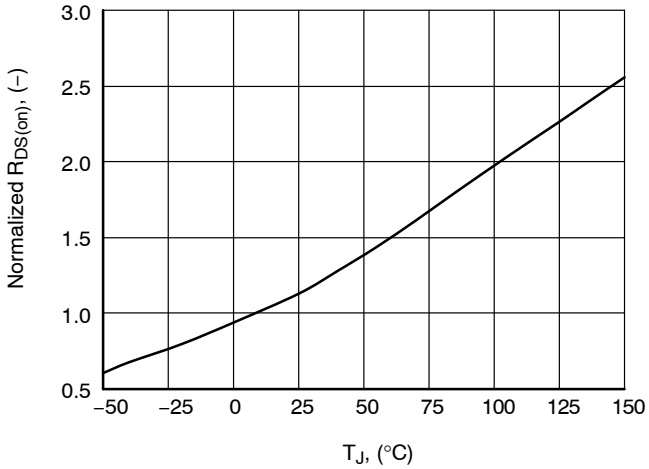


Figure 6. Normalized $R_{DS(on)}$ vs. Temperature

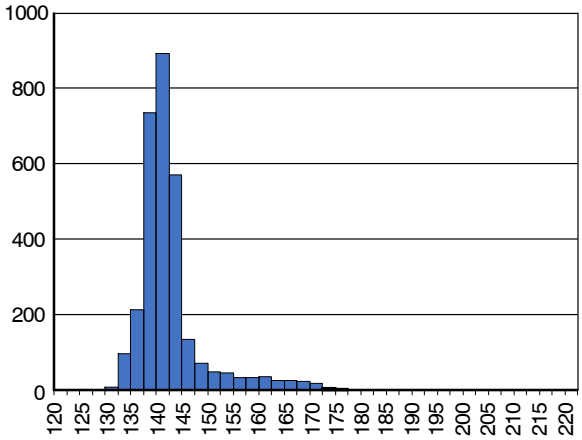


Figure 7. RDS(on) Histogram

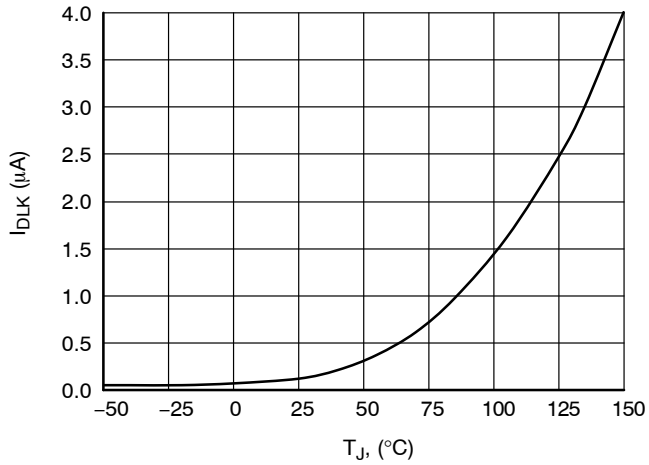


Figure 8. I_{DLK} Drain−Source Leakage Current vs. Drain−Source Voltage

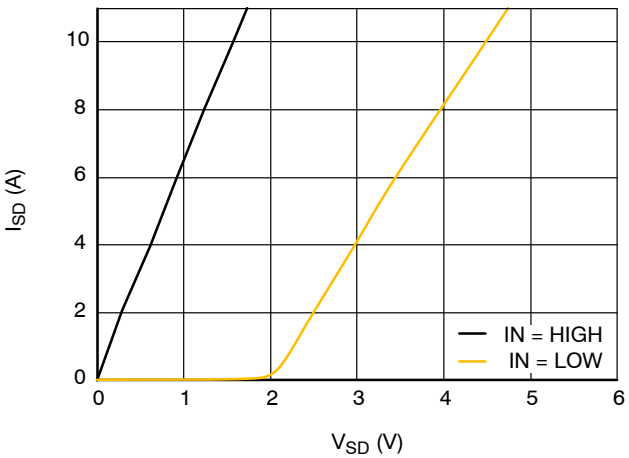


Figure 9. Typical VSD Drop vs. IDS and IN = 0 V at T_J = 25°C

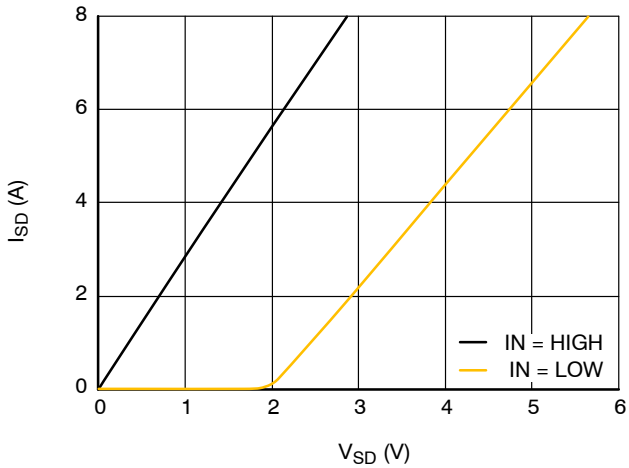


Figure 10. Typical VSD Drop vs. IDS and IN = 0 V at T_J = 150°C

TYPICAL CHARACTERISTICS (continued)

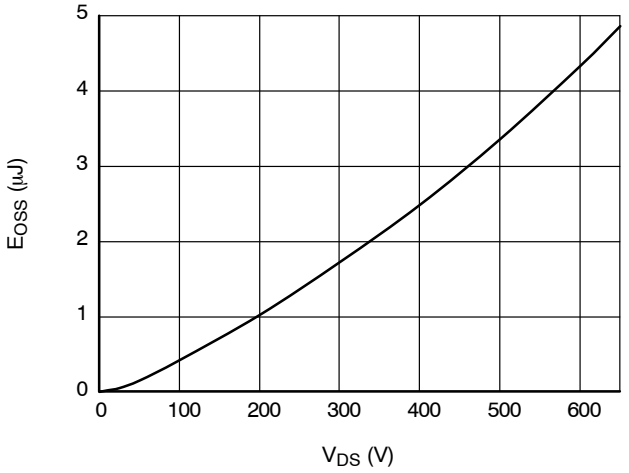


Figure 11. Output Capacitance Stored Energy vs. Drain−Source Voltage

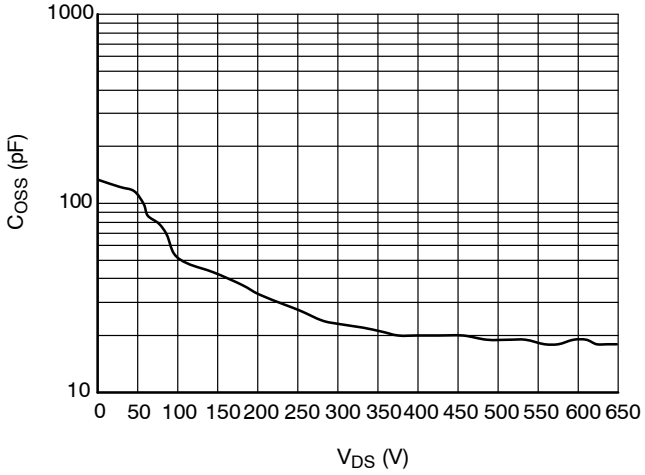


Figure 12. Output Capacitance vs. Drain−Source Voltage

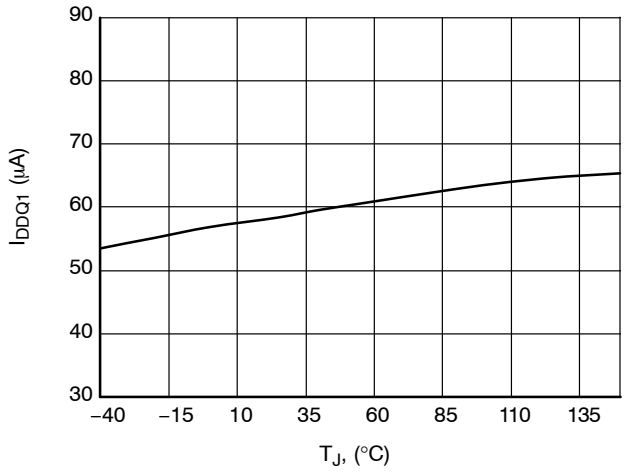


Figure 13. I_{DDQ1} Quiescent Supply Current vs. Temperature, VDD = 15 V, EN = 0 V, IN = 0 V

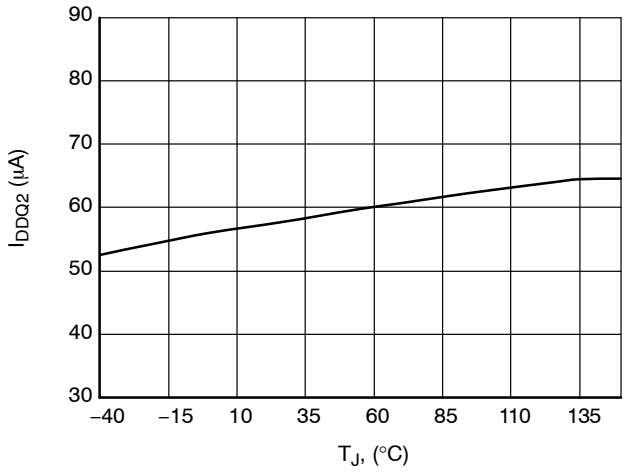


Figure 14. I_{DDQ2} Quiescent Supply Current vs. Temperature, VDD = 15 V, EN = 5 V, IN = 0 V

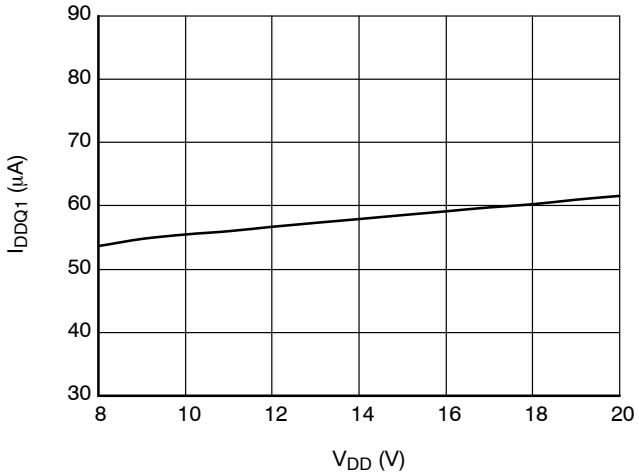


Figure 15. I_{DDQ1} Quiescent Supply Current vs. VDD Supply Voltage, IN = 0 V

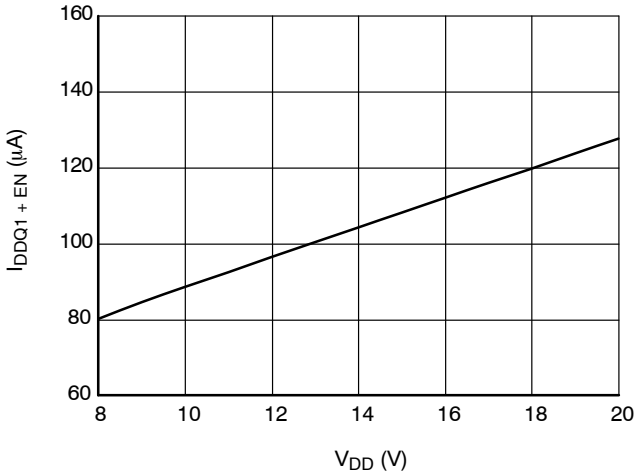


Figure 16. I_{DDQ1} + I_{EN} Supply Current vs. VDD Supply Voltage, EN = VDD, IN = 0 V

TYPICAL CHARACTERISTICS (continued)

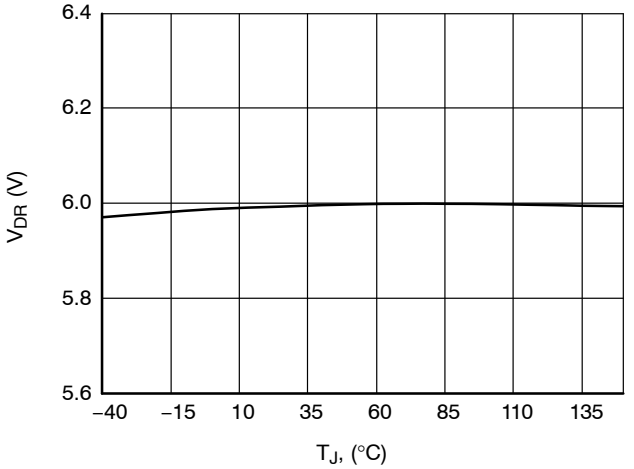


Figure 17. V_{DR} Driver Voltage vs. Temperature, IN = 0, R_{ON} = 0

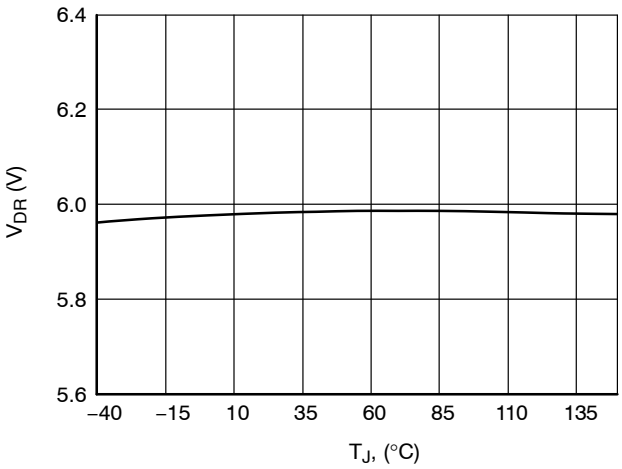


Figure 18. V_{DR} Driver Voltage vs. Temperature, IN = 0, R_{ON} = 0, External Load 10 mA

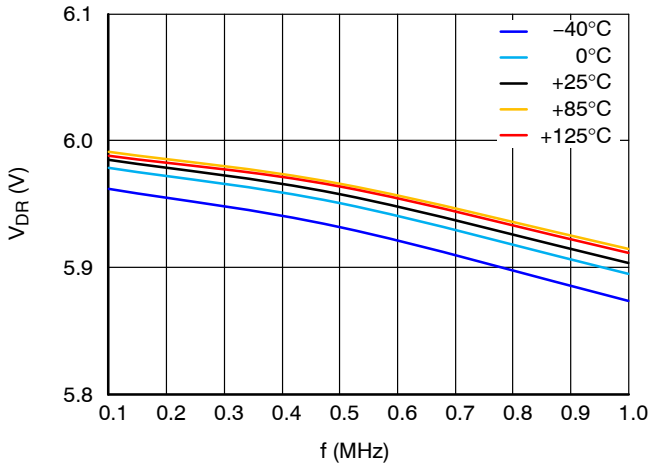


Figure 19. V_{DR} Driver Voltage vs. Frequency, R_{ON} = 0 Ω

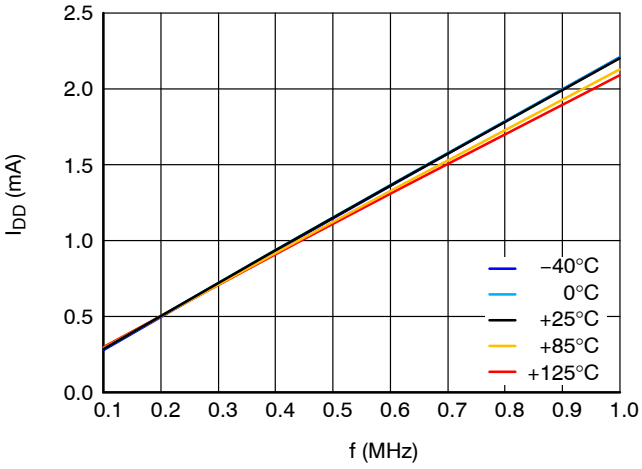


Figure 20. I_{DD} Supply Current vs. Frequency, R_{ON} = 0 Ω, Open Drain

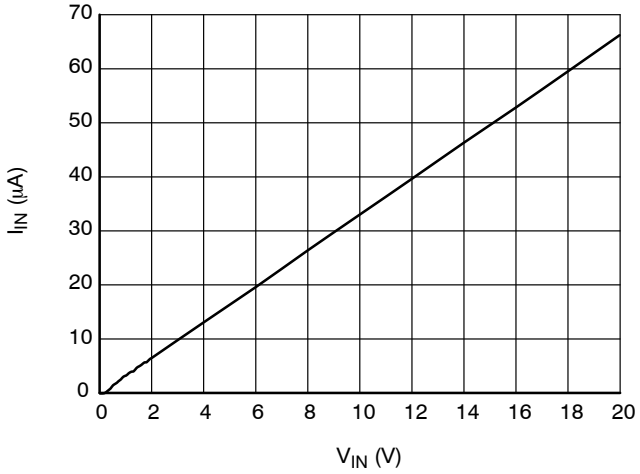


Figure 21. I_{IN} IN Input Current vs. V_{IN} Input Voltage, 25°C

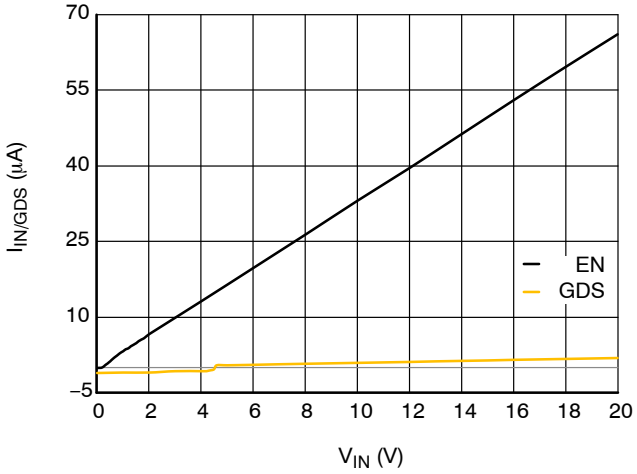


Figure 22. I_{EN}, I_{GDS} EN & GDS Input Current vs. V_{EN} Input Voltage, 25°C

TYPICAL CHARACTERISTICS (continued)

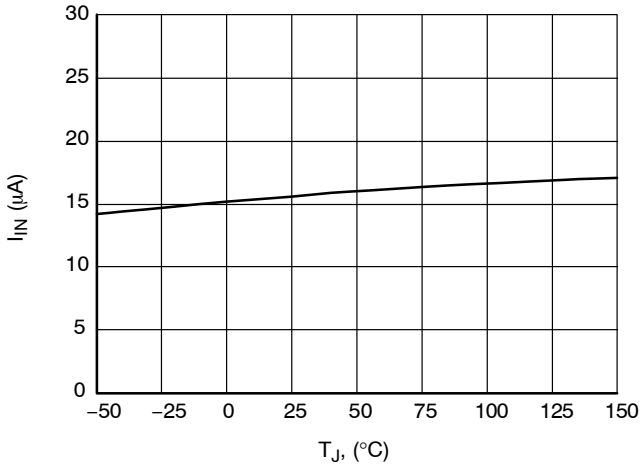


Figure 23. I_{IN} IN Input Current vs. Temperature, V_{IN} = 5 V

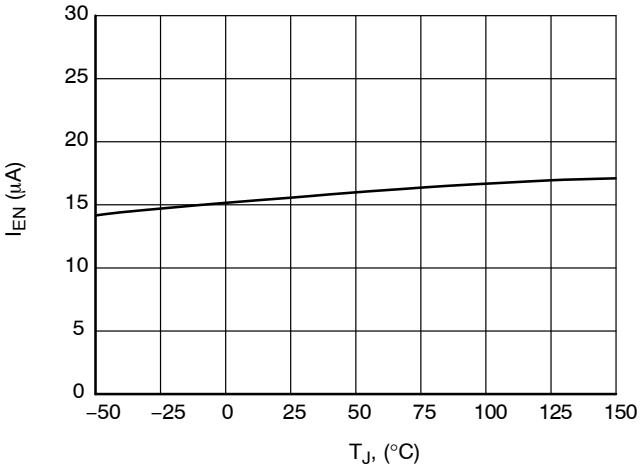


Figure 24. I_{EN} EN Input Current vs. Temperature, V_{IN} = 5 V

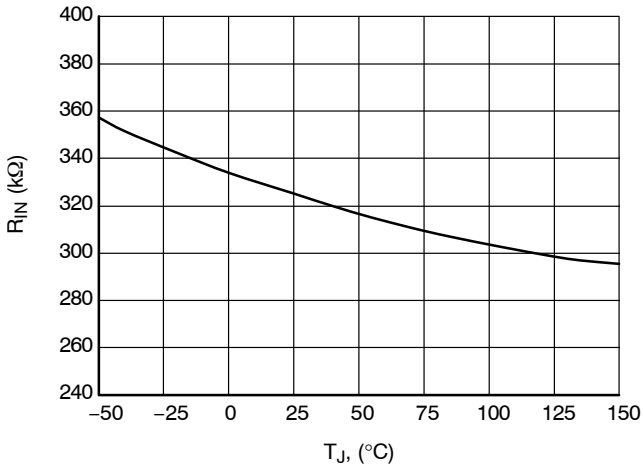


Figure 25. R_{IN} IN Input Resistance vs. Temperature

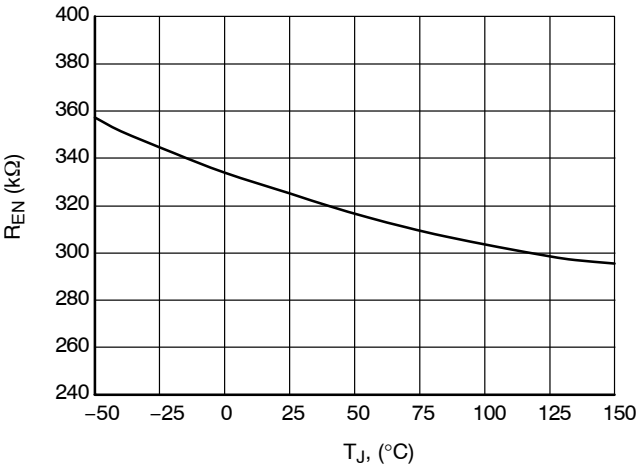


Figure 26. R_{EN} EN Input Resistance vs. Temperature

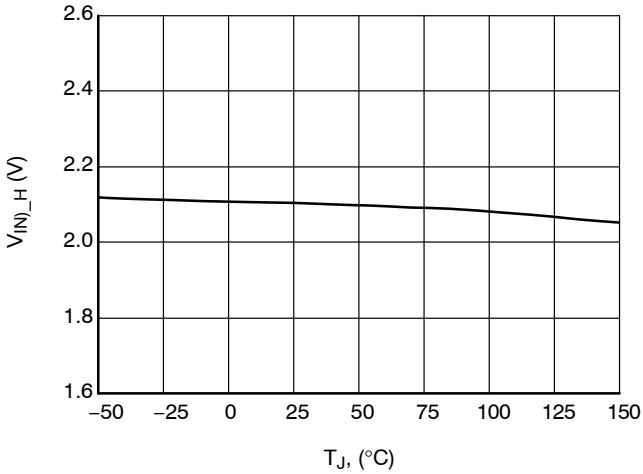


Figure 27. V_{IN_H} IN Input Threshold vs. Temperature

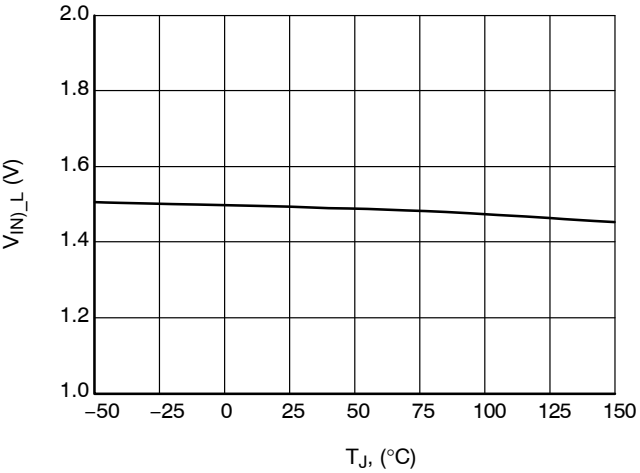


Figure 28. V_{IN_L} IN Input Threshold vs. Temperature

TYPICAL CHARACTERISTICS (continued)

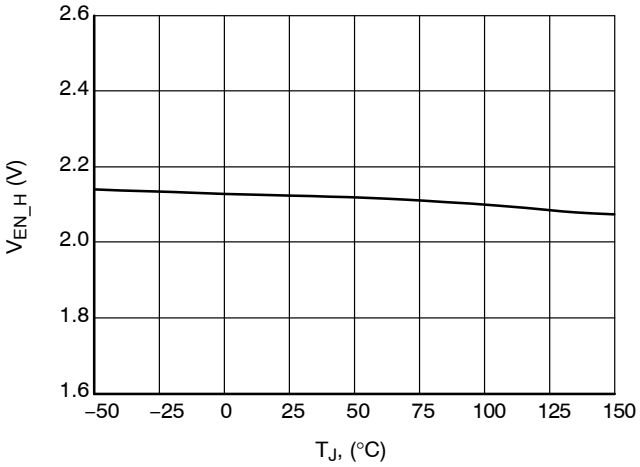


Figure 29. V_{EN_H} EN Input Threshold vs. Temperature

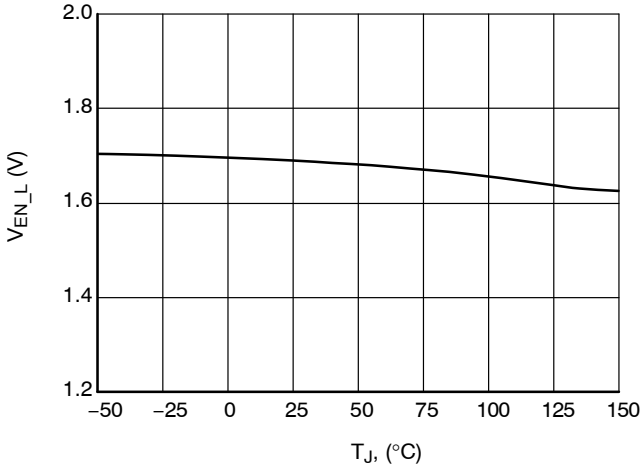


Figure 30. V_{EN_L} EN Input Threshold vs. Temperature

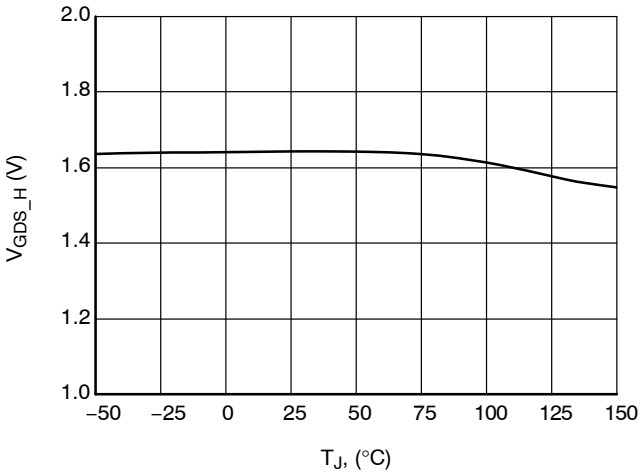


Figure 31. V_{GDS_H} GDS Input Threshold vs. Temperature

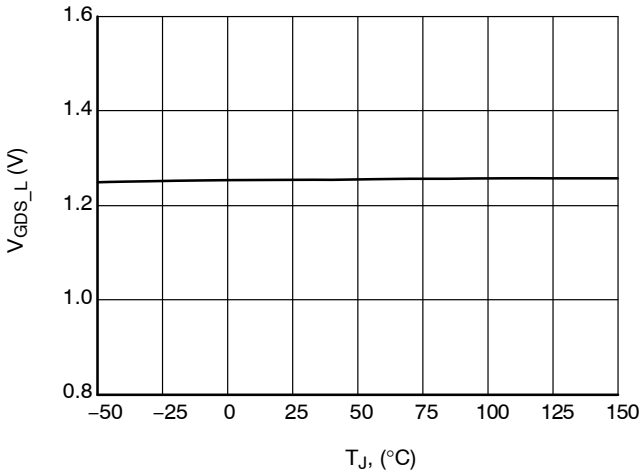


Figure 32. V_{GDS_L} GDS Input Threshold vs. Temperature

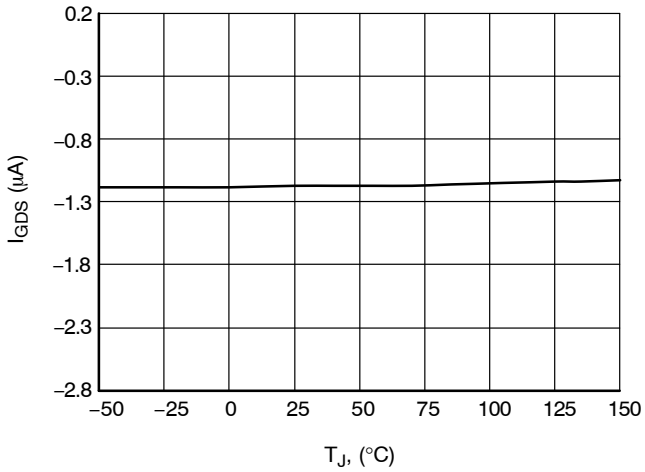


Figure 33. IGDS Input GDS Current vs. Temperature, VGDS = 15 V

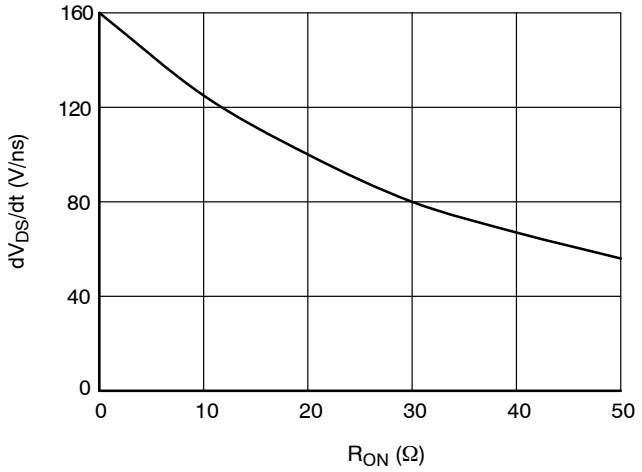


Figure 34. Half−bridge Turn−On dv/dt vs. RON resistance

TYPICAL CHARACTERISTICS (continued)

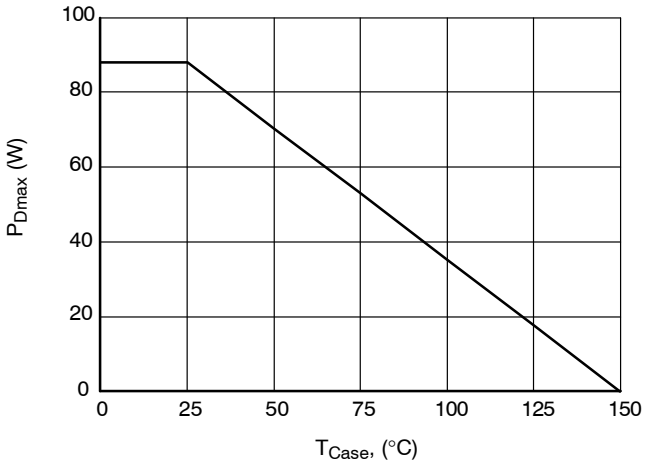


Figure 35. Power Derating vs. Case Temperature

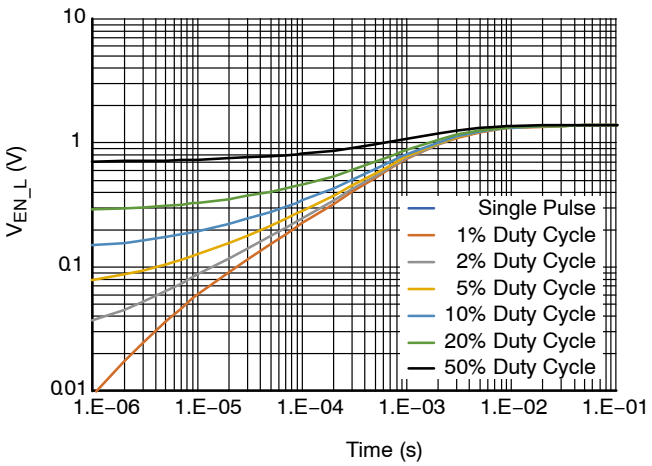


Figure 36. Transient Thermal Impedance

DEFINITIONS

General

All measurements are performed using short pulse low duty cycle techniques to maintain junction temperature as close as possible to ambient temperature.

Switching Test Circuit

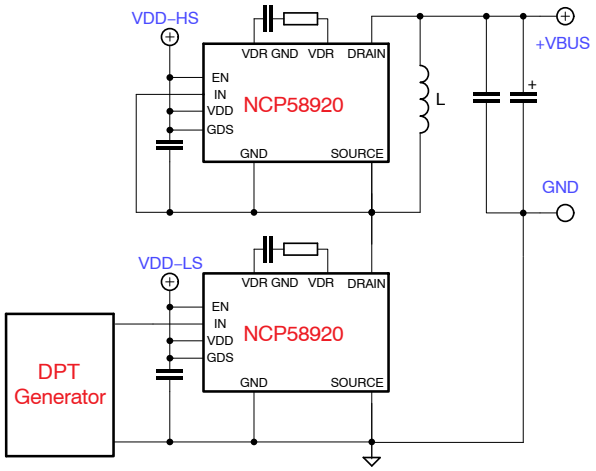


Figure 37. Half−bride Stage Arranged as Double−pulse tester Circuit

A typical approach to determine timing parameters of switching devices is to test them in double−pulse tester or use double−pulse testing technique. The half−bridge is a basic switching structure adopted in a wide range of converter topologies, that is easy to convert into double−pulse tester. Figure 37 shows principle schematic diagram of circuit (double−pulse test) that is used to measure switching parameters. The low−side device NCP58920 is the part that actively switching. When the device is turned on, the Inductor current is built to the certain level. The inductor current for this switching interval is almost the same as Drain current and its level is basically related to +VBUS Voltage, Inductance, and turn−on pulse width (the initial current must be considered). When Low−Side device is turned−off, inductor current cannot be interrupted (or cannot change direction), so the high−side device NCP58920 naturally turns−on, operates in third quadrant and its function is the same as freewheeling diode which enables inductor current re−circulation. Operation in the third quadrant should be well considered to avoid generating excessive losses and thus device overheating. Dedicated sequence of pulses creates operating conditions that are sufficient for generating switching waveforms and measuring required parameters. The specific timing measurement is shown in Figure 38.

Timing Characterization Reference

The timing of the turn−on transition is composed of two parameters: Driver to Switch Turn−on propagation delay, Switch V_{DS} Voltage fall time. The first one component is the propagation delay of the driver from when the input goes high, measured at 50%, to when the GaN HEMT starts turning−on, while its V_{DS} voltage drops to 90% of +VBUS. The fall time is the time that takes for Switch V_{DS} Voltage to slew between 90 percent and 10 percent of +VBUS voltage. The R_{ON} (Turn−on) resistor value has significant impact on Turn−on slew rate while the Turn−on propagation delay influence is minor. The timing definition of the turn−off transition also has two components; Driver to Switch Turn−off propagation delay and V_{DS} Voltage rise time. Reference levels are the same, however difference lays in opposite order. For better explanation reference waveform is depicted in Figure 38.

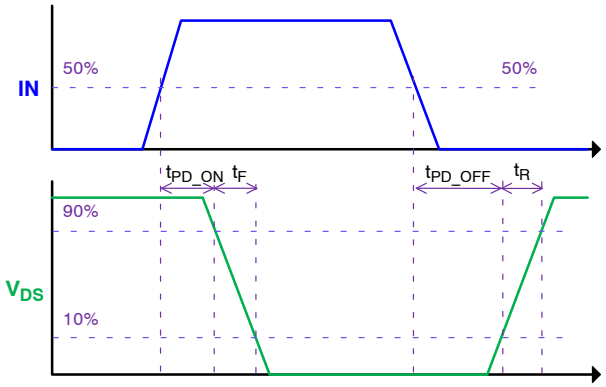


Figure 38. Measurement Reference for Determining Timing

High Speed Measurement Practice

In general, the GaN HEMTs have a significantly faster switching performance than Silicon and Silicon−Carbide MOSFETs. It's essential to use proper measuring techniques to evade the parasitic elements introduced by test equipment, that may distort device parameters and lead to inaccurate measurement results. A long probing ground wire inserts undesired inductance into the probe measurement path, which results in overshoot and ringing linked to the rising and falling edges of the measured signals. Minimizing the length of the ground loop is important especially for signals which have very high dv/dt level. At least, it's recommended to use so called "pigtail" that helps to reduce probe grounding inductance and thus provides more accurate measurement. Further, it's advised to use an oscilloscope and a probe with BW more than 350 MHz, while it should be considered edge slope time distortion approximately 1.5 ns.

Maximum Package Power Dissipation

The power dissipation level is maximum allowed power dissipation for package or power dissipation at which the junction temperature reaches its maximum operating value, whichever is lower.

APPLICATIONS INFORMATION

NCP58920 Application Drain−to−Source Voltage and its Maximum Recommended Levels

The NCP58920 has been designed to offer design margin to withstand transient and continuous voltage levels that are typically seen in single switch topologies, such as quasi−resonant (QR) flyback applications. The various voltage levels and recommended margins in a typical QR flyback converter is described using Figure 39. $V_{DS(TRAN)}$ rating is the voltage level of events that occur on a non−repetitive basis (occasional event), such as line surge, lightning strikes, start−up, over−current, short−circuit, load transient, and output voltage transition. $V_{DS(TRAN)}$ = 850 V ensures device robustness and derating is not required for non−repetitive events when the transient time duration is <100 μs. After the device is turned off, the energy stored in parasitic inductances (stray and leakage inductance of transformer and PCB layout) creates overshoot voltage stress $V_{DS}(t)$ that is applied to Drain−Source terminals. It is necessary to design a clamp circuit that limits V_{DS} continuous overshoot to $V_{DS(max)}$ 650 V level under the worst case steady−state operating conditions. After consuming energy from parasitic inductances, the device V_{DS} will drop to the level given by sum of the bus voltage and the reflected output voltage which is shown in Figure 39 as $V_{PLATEAU}$. It is recommended to design the system in such way that $V_{PLATEAU}$ level is maximally 69% of $V_{DS(max)}$ = 650 V, thus $V_{PLATEAU}$ ≤450 V. The recommended DC Bus voltage, $V_{PLATEAU}$ (in Figure 39) is not guaranteed spec.

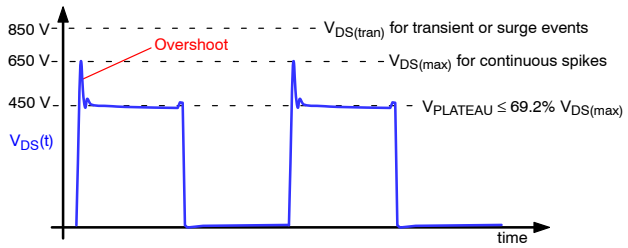


Figure 39. Drain−to−Source Voltage Definition

Minimum Schematic Diagram

The NCP58920 is an Integrated Device containing Power GaN HEMT Switch and Silicon Integrated Control Circuit that is equipped with dedicated two Quadrant Clamped Regulator, Driver, Level Shifter, and Input Logic circuitries. Device features VDD & VDR UVLO. Refer to following sections to gather more information. In Figure 1 is depicted minimum component circuit of a single switch, while typical application circuit Half−bridge LLC Stage is shown in Figure 2.

Benefits Integrated Driver GaN

Integrating the driver and GaN HEMT into one package is a logical step in development. Short Kelvin−connection between GaN switch and driver diminishes coupling link from Source common inductance of power terminal and minimizes the inductances between the driver output and GaN switch Gate terminals. Integrated solution offers clean driving waveforms, higher dv/dt immunity and simplified PCB design layout as well as reduces required PCB area.

VDD Supply Voltage

A DC voltage applied to VDD provides bias for the digital inputs, internal logic circuitries as well as providing bias directly to the internal driver voltage regulator (VDR) and subsequently to the driver. The GaN HEMT is driven by high−speed driver thus it requires higher current level during short charging interval of gate capacitance. This supply current is delivered through an internal regulator, from VDD bypass capacitor C_{VDD}, that is required to decouple V_{DD} Supply Voltage. C_{VDD} must be connected directly between the VDD and GND pins. The C_{VDD} capacitor should be a ceramic capacitor at least with capacitance 1 μF, located as close as possible to supply pins to properly filter out all glitches while device is switching. Use series resistance 3 – 30 Ω which forms low−pass filter that limits I_{DD} peak current and minimizes noise passing through the supply rails. Also, ferrite−bead may be adopted. Under−Voltage Lock Out (UVLO) is important for protecting device and power stage against running with insufficient supply voltage. The NCP58920 includes UVLO thresholds of V_{UVLO_R} > 8.5 V, ON and V_{UVLO_F} < 8 V, OFF, making it well suited for +12 V bias rails. UVLO protection is also implementing delay filters (refer to Electrical characteristic table) that avoid unwanted UVLO protection trigger due to noise or glitch of VDD bias voltage.

GND Signal Ground, VDR GND and SOURCE

The GND is the reference ground for internal control logic and all digital inputs. The GND and VDR_GND are two Driver IC grounds, that are separated by bidirectional level shifter structure that can handle DC offset ±3.5 V (see rating section). VDR_GND is interconnected with GaN SOURCE internally and VDR_GND is practically Kelvin−SOURCE of power switch. It's NOT ALLOWED to supply device while GND is separated from VDR_GND or SOURCE. It is forbidden to connect VDR_GND to SOURCE. Two connections are allowed:

1. GND may be connected to SOURCE for lower power application up to 500 W. When GND is tied to SOURCE, it must be done in place where no power−loop (Drain) current flows (Exposed pad corner that is close to GND pin) to ensure the noise injection into control signal is minimized.

2.GND may be connected to VDR_GND especially in high−power applications that feature high di/dt level, and this may overstress level shifter. That's the main reason for merging GND with VDR_GND.

VDR Internal Driver Regulator

The NCP58920 includes an internal linear driver regulator (VDR) dedicated to providing a tightly regulated, 6 V gate drive amplitude level to the GaN HEMT. The VDR regulator is fed directly from VDD, providing the most direct interface to the internal GaN HEMT Switch. This assures the lowest possible parasitic inductance, required to avoid ringing gate drive circuit. The VDR regulator is referenced between VDR and the VDR GND (Kelvin−Source). Source current for the GaN HEMT is provided from the charge stored in the CVDR connected between VDR and VDR GND. The recommended value of the CVDR capacitor is 100 nF. As CVDR capacitor is recommended to use multi−layer ceramic capacitor (MLCC) while preferred dielectric material is X7R. The VDR regulator also includes dedicated UVLO thresholds of V_{UVTH_R} > 5.5 V, ON and V_{UVTH_F} < 5 V, OFF which protects GaN HEMT against running in higher level of $R_{DS(on)}$ resistance.

NCP58920 Turn−on Slew−rate (dv/dt) Adjustment

The NCP58920 enables Turn−on Slew−rate (dv/dt) adjustment via R_{ON} resistance in series with VDR decoupling C_{VDR} capacitor (refer to Figure 1) Recommended VDR decoupling capacitor is Multi−Layer Ceramic Capacitor (MLCC) X7R material. CVDR capacitance is 100 nF, higher voltage rating than 25 V provides better thermal/ voltage stability. Always, append series resistance (R_{ON}) that allows to set turn−on slew rate and permits application debugging. Recommended starting R_{ON} value is 33 Ω. RON resistance level depends on application requirements as well as operating frequency, however 100 Ω should be considered as maximum value. Users ought to thoroughly check switching performance for R_{ON} value in given application and conditions. The reason is that PCB layout parasitic capacitance as well as inductor parasitic capacitance and power loop stray inductance impact switching behavior.

IN − Device PWM Input

The IN Input is the PWM input with Schmitt trigger, Transistor−Transistor Logic (TTL) compatible and it's internally pulled low to GND (see parametric table) such that corresponding driver input is defaulted to the inactive state. The TTL input thresholds provide buffer and logic level translation functions capable of operating from a variety of PWM signals up to VDD level of the NCP58920. TTL levels permit the input to be driven from a range of input logic signal levels for which a voltage greater than 2.1 V typically is considered logic high. Both input thresholds meet industry−standard TTL−logic defined thresholds and are therefore independent of VDD voltage. A typical hysteresis voltage of 0.6 V is dedicated to driver IN input (similarly EN Input). For optimal high−speed switching performance, the driving signal for the TTL inputs should have fast rising and falling edges with a slew rate that results in a reasonable rise time and fall time, so maximally few percent of switching period. Switching power systems contain a lot of noise level, so due to this is recommended to implement a low−pass RC filter that filters out noise coming from switching events. The RC filter must have small time constant which introduces only minor time delay that response impact is minimal. The RC Resistor value may be in range 10 – 100 Ω, further RC capacitor capacitance range might be up to several hundreds of pF, however their combination must give short time constant. It should be noted that IN input is edge sensitive while EN input is level sensitive, for better understanding refer to Figure 40.

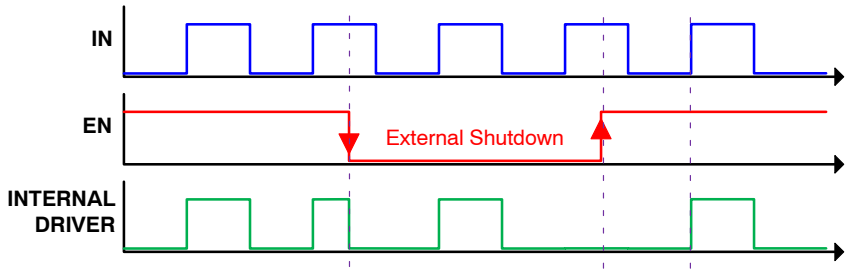


Figure 40. EN/IN Inputs Timing Behavior

EN − Device Enable Input

EN is internally pulled low to GND, so the driver is always defaulted to a disabled or iddle status. Similarly, as IN Input, the EN is a Schmitt trigger TTL compatible input. Pulling the EN pin above 2.1 V typically enables the output, placing device into an active ready state. Due to the nature of high−speed switching associated with GaN power stages, and for improved noise immunity, it is recommended to connect the EN pin to VDD through a 100 Ω pull−up resistor or directly to VDD. EN pin has fast response and noise may be caught by device input circuitries then GaN switch could be prematurely turned−off. For applications where the EN pin is actively controlled, the EN pin can be driven directly but should be bypassed with at least 1 nF decoupling capacitor which is placed as close as possible to device EN pin. Also, as in previous case, EN input series resistance helps to form RC filter that filter out unwanted noise. As it is shown in Figure 40, if EN is pulled low during normal operation, the driver output is immediately disabled, even terminating an active IN pulse mid –cycle during the

on−time. When EN is toggled high, during normal operation, a cycle−by−cycle, edge−triggered logic function is employed to prevent shortened, erroneous control pulses from being processed by the output. This behavior is highlighted in Figure 40, where EN transitions high at the same time the IN−input pulse is high. In this way, the NCP58920 is intelligent by waiting until the next rising edge to process the full input signal to the output driver stage.

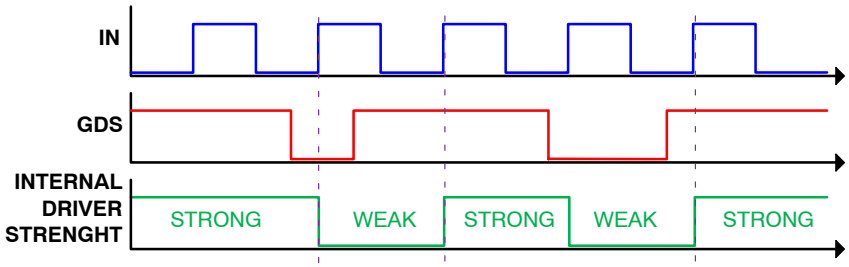


Figure 41. GDS Input Timing Behavior

GDS Input − Gate Drive Strenght

Similarly, as EN Input, the GDS is a Schmitt trigger input, which typically high and low levels are 1.6 and 1.2 V, respectively. GDS Input Gate Drive Strength sets Driver turn−on resistance. If the GDS pin is at low−level, then turn−on resistance is approximately 300 Ω. If GDS is pulled to high−level, then turn−on resistance is 10 Ω. When GDS is controlled externally, use a small filter to filter out noise that may come from high−speed switching. If GDS feature is not needed and driver strength should be set to high level, then it's better to pull−up GDS pin to VDD via low impedance <100 Ω − same approach as in case of EN pin. The NCP58920 GDS feature is dedicated for accompanying device with Active Clamped Flyback controller NCP51568. In a such implementation is GDS input controlled based on NCP1568 FB signal, which sets "Low Driver Strength" for low FB levels (during burst mode or light−load mode) and "High Driver Strength" for power level, that pushes FB signal level above high threshold. GDS Input is level sensitive, and its proper level must be set approximately 15 ns before PWN (IN) signal edge comes. Once driver strength is confirmed by PWM rising edge, its level is kept until next PWM rising edge is introduced. GDS signal does not have any impact during mid−cycle change or after active level cycle change. GDS Input timing dependency is depicted in Figure 41.

Boot−strap Circuit

Typically, boot−strap supply is not fully recommended for Hard−switched applications as these are characteristic with high dv/dt level as well as big noise level, that may strongly affect operation. For lowering VDD supply noise caused by bootstrapping, it's possible to use independent capacitor that is connected to low−side VDD supply via resistor while SOURCE is used for capacitor ground. As bootstrap diode, implement soft−recovery diode with low capacitance and low reverse recovery charge Q_{RR} like NHP160. Also, add series resistance to limit peak current. Another good option for how to reduce current peak is a ferrite bead (100 Ω @ 100 MHz). A higher resistance bootstrap resistor as well as shorter dead−time may help to prevent overcharge high side floating supply. If low side is supplied more than 16 V, it's suggested to add Zener diode clamp to limit bootstrap supply voltage and avoid overstressing or even destruction of high−side circuitry. Further, it helps to separate NCP58920 VDD supply terminal and Level Shifter or Isolator VCC supply pin with resistor to avoid charge exchange and thus current spikes between decoupling capacitor, especially during switching transition. It's recommended to evaluate bootstrapping solution and adjust component values with respect to application. To summarize above use following pars and approach at application developing phase:

- Bootstrap diodes; NVRHP160, NVRHP260 or ES1JFL
- Bootstrap resistor 5 – 10 Ω or ferrite bead with recommended impedance at least 100 Ω @ 100 MHz.
- Short Dead−time < 150 ns, prevent staying device too long in 3rd quadrant.
- Use Zener diode clamp (MMSZ18T1G) or regulator for high side.
- Measure bootstrap current peak and check bootstrap diode commutation especially during dead−time phase.

Half−Bridge Stage Decoupling

Use at least one high−voltage 100 nF MLCC for Half−Bridge Stage $+V_{BUS}$ supply decoupling. However, it's strongly recommended to implement more capacitors, same or mixture multiple values to ensure more advanced filtering. It should be noted that minimum capacitance should be more than 100 nF, while lower capacitance is deployed, there is high risk of capacitor damage as it might not accept energy stored in power loop stray inductance.

Soft−Switched Application

For soft switching topologies like CrM TP PFC, ZVS Buck or Boost Converters, the NCP51530 can be used as level shifter. A similar solution may be implemented for LLCs NCP1399x family, and its internal HB driver provides level shifting same way as NC51530. High−side portion of converter can be supplied via bootstrap circuit while

appropriate bootstrap components and dead−time should be used as mentioned in Boot−strap circuit section.

Hard−Switched Application

For hard−switched application CCM PFC, CCM Buck or Boost Converters is highly recommended to use digital isolator such as NCP51561. Also, it's recommended to implement floating supply or insulated DC/DC converter for High−Side portion, especially when application is being developed or debugged. Bootstrap supplying for High−Side was tested up to 1 kW in CCM TP PFC and must be noted that proper PCB layout is necessary. Follow recommendation for boot−strap circuit from previous text. Hard−Switched applications generate high noise levels, that may impact input signal. Use input RC filter to filter out noise and glitches caused by Hard Switching event.

General Rules for PCBs

Use at least 2 oz or 70 μm copper thickness PCB, however preferred copper thickness is 2.5 – 3 oz (90 – 105 μm) due to thermal performance. 2−layers PCB is the minimum for lower power application <400 W. PCB thermal resistance, application surface and related heat spreading capability must be well−thought−out. PCB layout design complexity must be considered and if it's too high switch to 4−layers. 4−layers PCB is preferred minimum for application that has higher power > 400 W. Use thermal vias for exposed pads to transfer heat from device to opposite side of PCB and further to heatsink if needed. For applications where power losses dominate it's recommended to mount device on Insulated Metal Substrate board (IMS). From an electrical point of view, it is important to design power loops using flux cancelation loop. For Half−Bridge power loop use flux cancelation technique that is depicted in Figure 42 and Figure 43. Do not create unreasonable big structure, keep Half−Bridge stage compact, the best is to place both half−bridge switches in one line with decoupling MLCC capacitors as in Figure 42. +VBUS or +VBULK ceramic bypass capacitors must be close to the DRAIN of high−side switch or SOURCE of low−side switch. Return trace should be as short and direct as possible. This reduces power loop area thus power loop stray inductance that minimize switching node overshoots. Switching node and return−GND trace overlay area should be small as possible, so it won't add too much parasitic capacitance that increase switching losses, however this is not always possible. All high−current power loop coppers traces, such as +VBUS or +VBULK, SW and SOURCE – power GND; should be short and wide enough to keep low parasitic inductance and resistance. This helps achieve a more stable and evenly distributed current flow, along with better heat radiation and system performance.

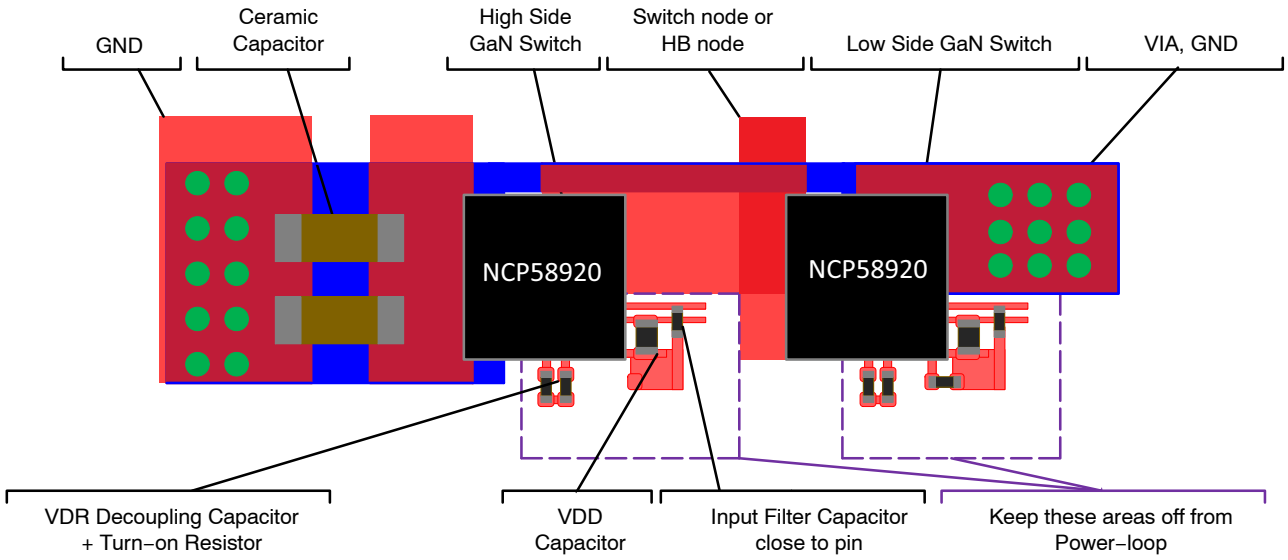


Figure 42. Half−Bridge Stage PCB Layout Recommendation

General Rules for Placing and Routing Surrounding Components

First do not mix power loop together with supply rails or input control signal traces. Supply decoupling and filter capacitors should be placed as close to device as possible (see Figure 42). NCP58920 GND must be connected to Source or VDR_GND in the shortest possible way. If GND is tied with SOURCE, then it should be in the corner of exposed pad that is located next GND pad. The VDR regulator components (C_{VDR}, R_{ON}) must be kept away from power traces especially DRAIN voltage. Minimize area of VDR regulator parts as well as traces and do not short VDR_GND to Source. Under surrounding components place shielding ground connected to device GND at one place close to GND pad. Shielding layer mustn't conduct current from power loop (DRAIN−SOURCE).

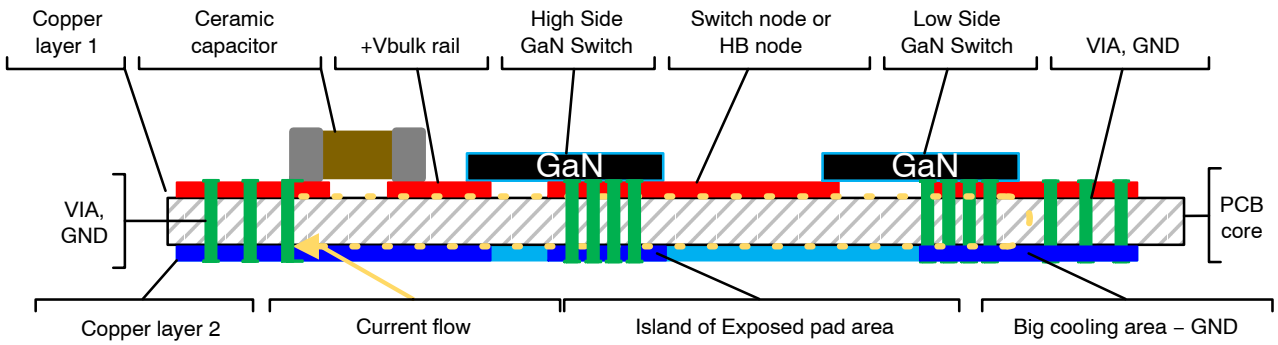


Figure 43. Half−Bridge Stage PCB Layout Cut View

Thermal Guidelines

Power device like NCP58920 may dissipate significant amounts of power losses. It's helpful to estimate power dissipation level and calculate maximal thermal resistance of entire cooling chain for allowable temperature rise or maximum junction temperature T_{jmax}. Proper PCB layout design and cooling chain design ensure that device will operate within acceptable temperature limits in the final application.

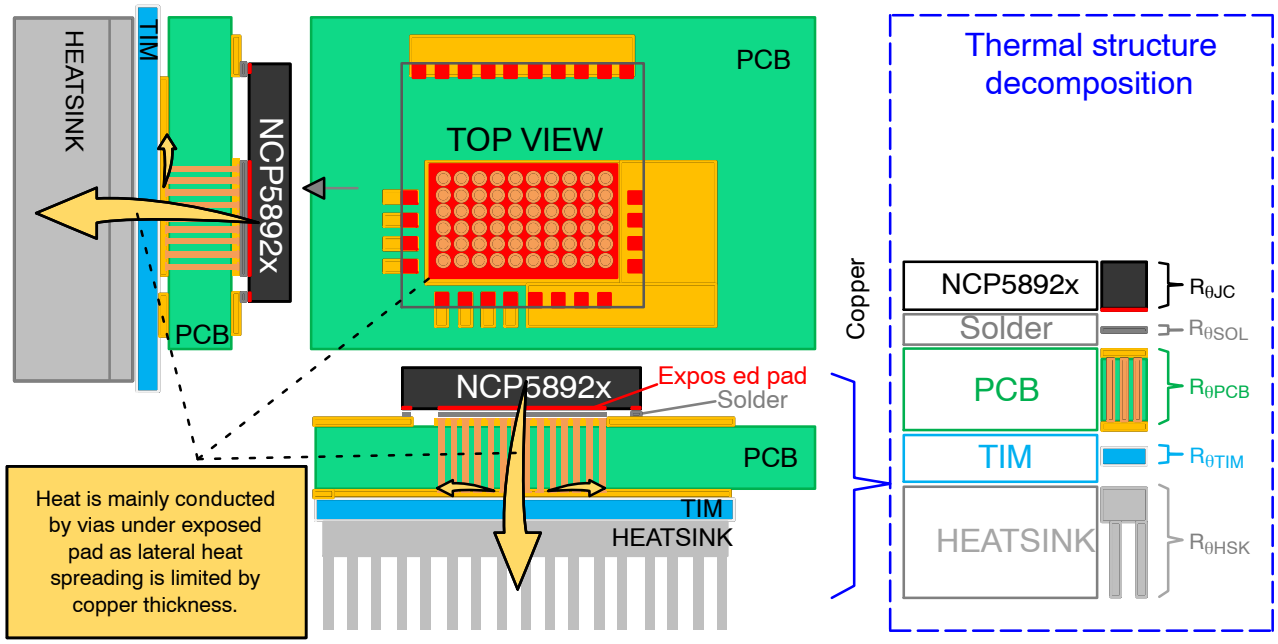


Figure 44. Heat−flux Through PCB Vias

NCP58920 is bottom cooled device and generated heat is extracted from its exposed pad through subsequent cooling chain parts. Typical case is device mounted on the PCB as shows Figure 44. In this figure is depicted device mounted on PCB and Thermal structure decomposition as well as it demonstrates heat flux directions and level by simplified way. Basically, heat is taken away from exposed pad, then passing through solder joint and the PCB vias to the opposite site of PCB where is distributed into copper plane, however, lateral heat spreading is limited. Further heat goes through Thermal Interface Material (TIM) and then continues to the heatsink where is released to the ambient. As mentioned previously, the spreading effect is limited due to transferring heat through thermal vias that are practically thermally insulated by PCB laminate which has typically tiny thermal conductivity 0.2 W/mK (FR4 laminate). Despite the high copper thermal conductivity 396 W/mK (at 350 K, ~ +77°C), with respect to amount of main heat flow level, the lateral heat spreading within planes is limited by the PCB copper thickness due to very small ratio between copper thickness and area dimension. Thus, heat flow mainly passes perpendicularly through PCB plane thanks to copper vias and afterwards heat is removed by heatsink. Applicating simplifications afore stated and using scheme from Figure 44, it's easy to calculate 1−dimennsional thermal resistance for each unknow part. Overall cooling chain thermal resistance (Junction to Ambient) $R_{\theta JA}$ is given by sum of elements in thermal structure as following:

$$R_{\theta JC} + R_{\theta SOL} + R_{\theta PCB} + R_{\theta TIM} + R_{\theta HSK} \quad \text{(eq. 1)}$$

where, $R_{\theta JC}$ device junction to case thermal resistance, $R_{\theta SOL}$ solder layer thermal resistance, $R_{\theta PCB}$ printed circuit board thermal resistance, $R_{\theta TIM}$ TIM thermal resistance and $R_{\theta HSK}$ heatsink thermal resistance. Thermal resistance of the device is shown in THERMAL CHARACTERISTICS table. Below is list of three the most used solder alloys and their thermal conductivity data (at 85°C), that can be used for calculation.

- Lead−free Solder alloys:
  - Sn96.5−Ag3.5 k = 78 W/mK,
  - Sn95.6−Ag3.5−Cu0.9 k = 60 W/mK,
  - Sn96.2−Ag2.5−Cu0.8−Sb0.5 k = 57 W/mK.
- Lead containing Solder alloys:
  - Sn63−Pb37 k = 51W/mK,
  - Sn62−Pb36−Ag2 k = 50 W/mK,
  - Pb50−In50 k = 22 W/mK.

In case you need some specific solder alloy, refer to its vendor or manufacturer to obtain necessary characteristics. Solder layer thermal resistance $R_{\theta SOL}$ is proportional to solder layer thickness hSOL and inverse proportional to solder area A_{SOL} and solder thermal conductivity k_{SOL}. $R_{\theta SOL}$ can be calculated as following:

$$R_{\theta SOL} = h_{SOL} / (A_{SOL} \times k_{SOL}) \quad \text{(eq. 2)}$$

Let's assume that solder layer is 100 μm, exposed pad area 24.64 mm^2 and conductivity 60 W/mK, then solder layer thermal resistance $R_{\theta SOL}$ is 0.068°C/W, so this value can be considered as negligible. Similarly, thermal interface material thermal resistance $R_{\theta TIM}$ can be computed same way as in equation 2, thus:

$$R_{\theta TIM} = h_{TIM} / (A_{TIM} \times k_{TIM}) \quad \text{(eq. 3)}$$

and again, h_{TIM} is TIM mounting thickness, k_{TIM} thermal conductivity while A_{TIM} area is limited copper plane area around thermal vias under device. Let's consider TIM thickness 0.5 mm with thermal conductivity 3.8 W/mK and active area is same as exposed pad. Then TIM layer thermal resistance $R_{\theta TIM}$ is 5.34°C/W, this value is quite significant and TIM layer optimalization is big question. For half TIM layer thickness (0.25 mm/ 3.8 W/mK) thermal resistance is halved. Summarizing the afore stated, to calculate realistic thermal resistance numbers, the size of material area (A_{SOL}, A_{TIM}) associated with heat transfer should be same as device exposed pad (flag) area.

Thermal Resistance Calculations

Continuing with calculations, we know thermal resistance of Device, Solder, TIM and Heatsink, however PCB thermal resistance $R_{\theta PCB}$ is still required to develop entire cooling chain thermal resistance level. We can look at PCB from two perspectives. The first one is PCB thermal resistance from device to ambient as parallel path and its level is typically high, and it has minor impact to overall thermal resistance, especially when speak about small compact PCB. The second one is PCB thermal resistance from side where device is mounted to the opposite site, practically local thermal resistance of thermal vias under device exposed pad that significantly contributes to main cooling path thermal resistance. The most straightforward way to estimate thermal resistance of PCB portion with multiple thermal vias is to calculate single via thermal resistance and then divide it by number of active vias. To compute thermal resistance of single via use following equations eq4:

$$R_{\theta VIA} = h_{PCB} / \left(\frac{\pi}{4} \left(\left(d_{drill} + h_{plt} \right)^2 - d_{drill}^2 \right) \times k_{Cu} \right) \quad \text{(eq. 4)}$$

where h_{PCB} is PCB height value (typically 1.575 mm), d_{drill} is via drill diameter, h_{plt} is copper layer plating thickness (typically 1 oz or 35 μm) and k_{Cu} is copper thermal conductivity. For afore mentioned copper thermal conductivity, via height 1.575 mm, via drill 0.3 mm and copper plating 35 μm, the $R_{\theta VIA}$ equals to 109°C/W. To simplify whole process of computing, the chart in Figure 45 can be used for reading via thermal resistance for given setup. Furthermore, linear scaling works very well for fitting to other inputs. For example, halved PCB height gives half of thermal resistance.

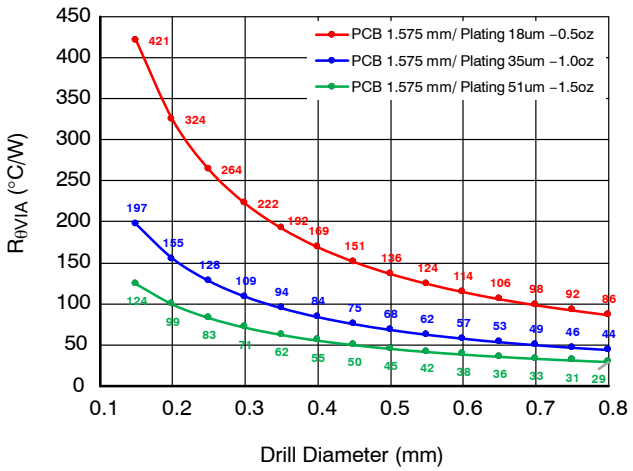


Figure 45. $R_{\theta VIA}$ Thermal Resistance of Via vs. Manufacturing Parameters

Considering thermal resistance for given number n of actively heat transferring vias $R_{\theta nVIAS}$ can be calculated as:

$$R_{\theta nVIAS} = R_{\theta VIA}/n \quad \text{(eq. 5)}$$

So, for 40 active vias with $R_{\theta VIA}$ = 109°C/W per each via (via height 1.575 mm, via drill 0.3 mm, copper plating 35 μm), we obtain PCB thermal resistance under exposed pad $R_{\theta PCB}$ = 2.73°C/W. It should not be forgotten that vias contributing on main portion of heat transfer are located under device exposed pad only. To estimate cooling chain thermal resistance, let's assume that heatsink thermal resistance is $R_{\theta HSK}$ = 3.0°C/W and other values are already calculated or defined. Using equation 1, it can be obtained junction to ambient thermal resistance $R_{\theta JA} \approx$ 12.6°C/W.

Then device maximum power dissipation level P_{Dmax} can be estimated as:

$$P_{Dmax} = (T_J - T_a)/ R_{\theta JA} \quad \text{(eq. 6)}$$

where, T_J is junction temperature and T_a is ambient temperature. The junction temperature may user define up to 150°C. However, it's recommended to keep safety margin (25 – 30°C) that covers all manufacturing tolerances and prevent unwanted device overheating. For selected junction temperature T_J = 120°C, ambient temperature T_a = 60°C and $R_{\theta JA}$ = 12.6°C/W, device may dissipate up to 4.76 W.

Thermal Vias Considerations

The minimum recommendation for thermal vias pattern is at least 60 vias of 0.3 mm drill that all of them are located under exposed pad. In Figure 46 are depicted 4 thermal vias pattern that were deployed to establish $R_{\theta PCB}$ levels. For the same manufacturing condition, PCB thermal resistance top to bottom is given mainly by thermal vias under exposed pad area as was mentioned in previous section. First three patterns in Figure 46 a), b), and c) use 0.3 mm drill with 0.8/0.4 mm pitch, while pattern d) uses 0.15 mm drill with 0.4 mm pitch. All patterns use same 35 μm copper plating level. For first three patterns, the minor variation of thermal resistance was measured, and their thermal resistance is approximately $R_{\theta PCB}$ = 2.3°C/W while pattern d) with denser vias pitch offers additional improvement of thermal resistance which is $R_{\theta PCB}$ = 2.0°C/W. NCP58920 on PCB with pattern d) mounted on 1.0°C/W fanned heatsink (using screws) via 6.0 W/mK TIM (40016005) achieves $R_{\theta JA}$ = 5.6°C/W.

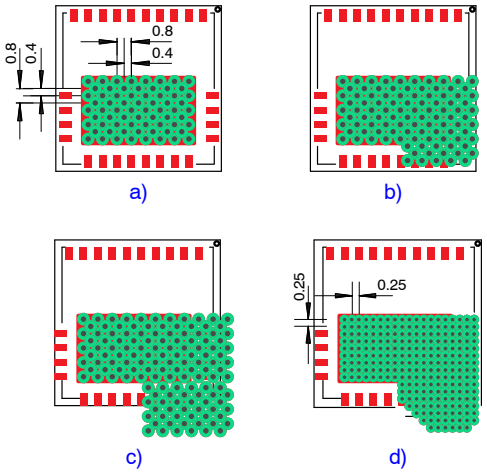
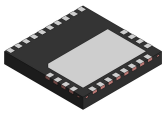


Figure 46. Recommended Thermal Vias Arrangement

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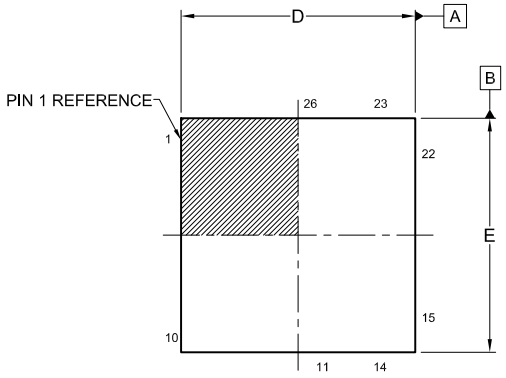
Device	Package	Shipping†
NCP58920MNTWG	TQFN26 8x8, 0.8P (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

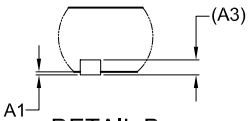


TQFN26 8x8, 0.8P
CASE 518AG
ISSUE B

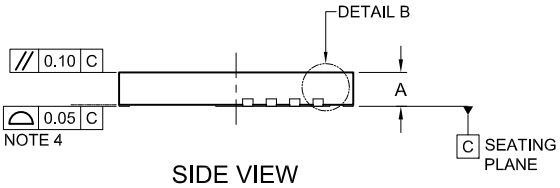
DATE 29 NOV 2022



TOP VIEW



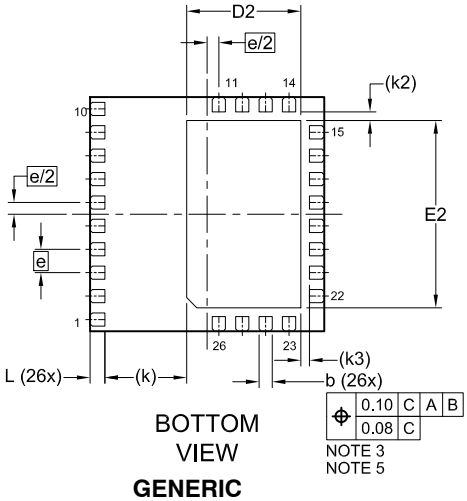
DETAIL B
SCALE: 2X



SIDE VIEW

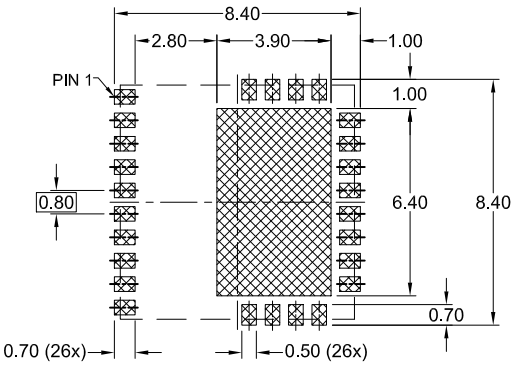
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO THE EXPOSED PAD AND ALL TERMINALS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A1	0.00	---	0.05
A3		0.254 REF	
b	0.40	0.45	0.50
D	7.90	8.00	8.10
D2	3.80	3.90	4.00
E	7.90	8.00	8.10
E2	6.30	6.40	6.50
e		0.80 BSC	
e/2		0.40 BSC	
L	0.40	0.50	0.60
k		2.80 REF	
k2		0.30 REF	
k3		0.30 REF	



BOTTOM VIEW

NOTE 3
NOTE 5



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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