FlexRay® Transceiver, Clamp 30

NCV7381C

NCV7381C is a high−temperature single−channel FlexRay transceiver compliant with FlexRay Electrical Physical Layer Specification Rev. 3.0.1, capable of communicating at speeds of up to 10 Mbit/s. It provides differential transmit and receive capability between a wired FlexRay communication medium on one side and a protocol controller and a host on the other side.

NCV7381C mode control functionality is optimized for nodes permanently connected to car battery.

It offers excellent EMC and ESD performance.

KEY FEATURES

General

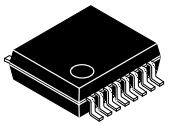
- Compliant with FlexRay Electrical Physical Layer Specification Rev 3.0.1
- FlexRay Transmitter and Receiver in Normal−power Modes for Communication up to 10 Mbit/s
- Support of 60 ns Bit Time
- FlexRay Low−power Mode Receiver for Remote Wakeup Detection
- Excellent Electromagnetic Susceptibility (EMS) Level over Full Frequency Range. Very Low Electromagnetic Emissions (EME)
- Bus Pins Protected against >10 kV System ESD Pulses
- Safe Behavior under Missing Supply or No Supply Conditions
- Interface Pins for a Protocol Controller and a Host (TxD, RxD, TxEN, RxEN, STBN, BGE, EN, ERRN)
- INH Output for Control of External Regulators
- Local Wakeup Pin WAKE
- TxEN Timeout
- BGE Feedback
- Supply Pins V_{BAT}, V_{CC}, V_{IO} with Independent Voltage Ramp Up:
  - V_{BAT} Supply Parametrical Range from 5.5 V to 50 V
  - V_{CC} Supply Parametrical Range from 4.75 V to 5.25 V
  - V_{IO} Supply Parametrical Range from 2.3 V to 5.25 V
- Compatible with 14 V and 28 V Systems
- Operating Ambient Temperature −40°C to +150°C (T_{AMB_Class0})
- Increased Operating Junction Temperature
- Junction Temperature Monitoring with Two Levels
- SSOP−16 Package
- This Device is Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Quality

- AEC−Q100 Qualified and PPAP Capable

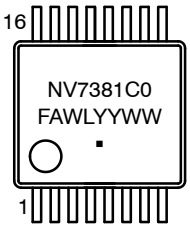
FlexRay Functional Classes

- Bus Driver Voltage Regulator Control
- Bus Driver – Bus Guardian Interface
- Bus Driver Logic Level Adaptation
- Bus Driver Remote Wakeup



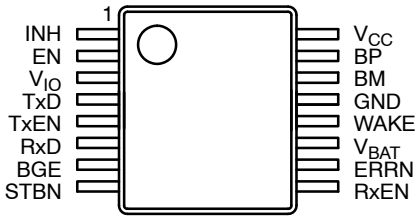
SSOP 16
CASE 565AE

MARKING DIAGRAM



F = Fab Location
A = Assembly Location
WL = Wafer Lot
YYWW = Year / Work Week
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 24 of this data sheet.

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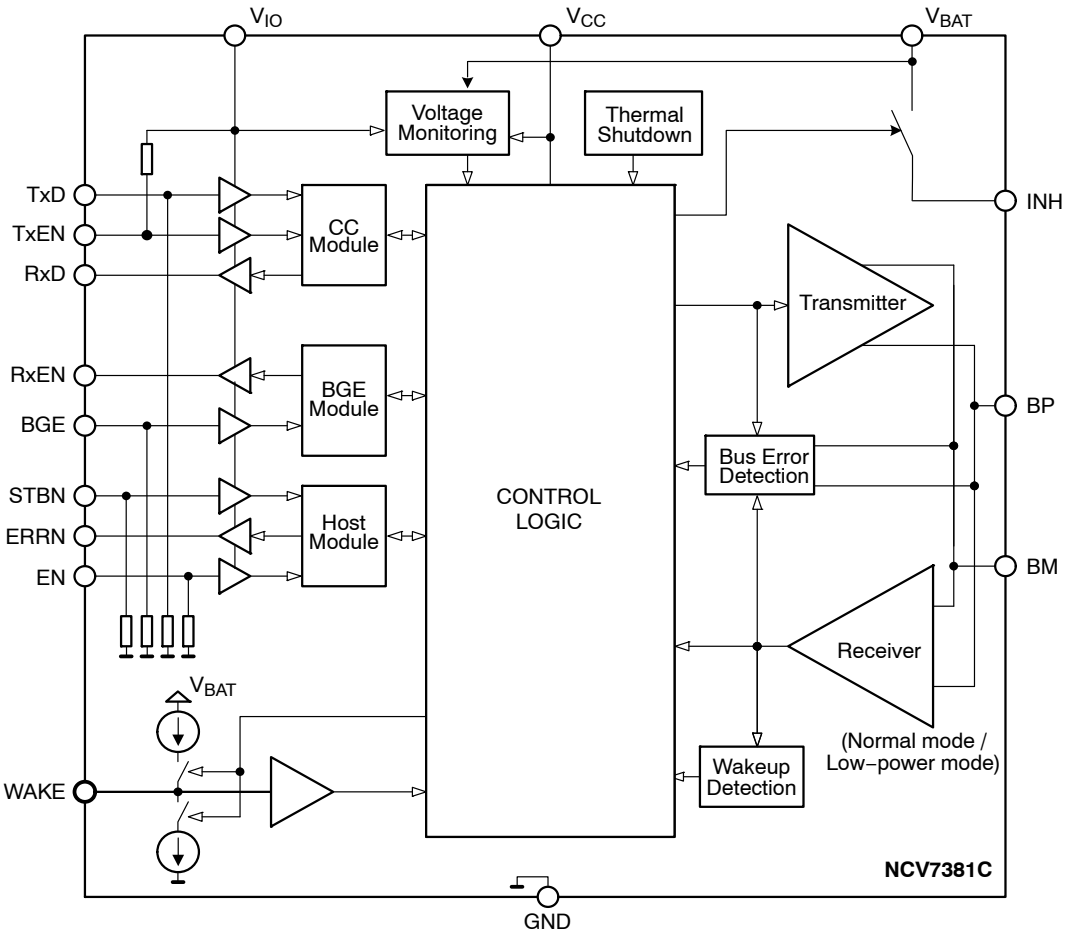


Figure 1. Block Diagram

PIN FUNCTION DESCRIPTION

Pin Number	Pin Name	Pin Type	Pin Function
1	INH	high−voltage analog output	External regulator control output
2	EN	digital input	Mode control input; internal pull−down resistor
3	V_{IO}	supply	Supply voltage for digital pins level adaptation
4	TxD	digital input	Data to be transmitted; internal pull−down resistor
5	TxEN	digital input	Transmitter enable input; when High transmitter disabled; internal pull−up resistor
6	RxD	digital output	Receive data output
7	BGE	digital input	Bus guardian enable input; when Low transmitter disabled; internal pull−down resistor
8	STBN	digital input	Mode control input; internal pull−down resistor
9	RxEN	digital output	Bus activity detection output; when Low bus activity detected
10	ERRN	digital output	Error diagnosis and status output
11	V_{BAT}	supply	Battery supply voltage
12	WAKE	high−voltage analog input	Local wakeup input; internal pull−up or pull−down (depends on voltage at pin WAKE)
13	GND	ground	Ground connection
14	BM	high−voltage analog input/output	Bus line minus
15	BP	high−voltage analog input/output	Bus line plus
16	V_{CC}	supply	Bus driver core supply voltage; 5 V nominal

APPLICATION INFORMATION

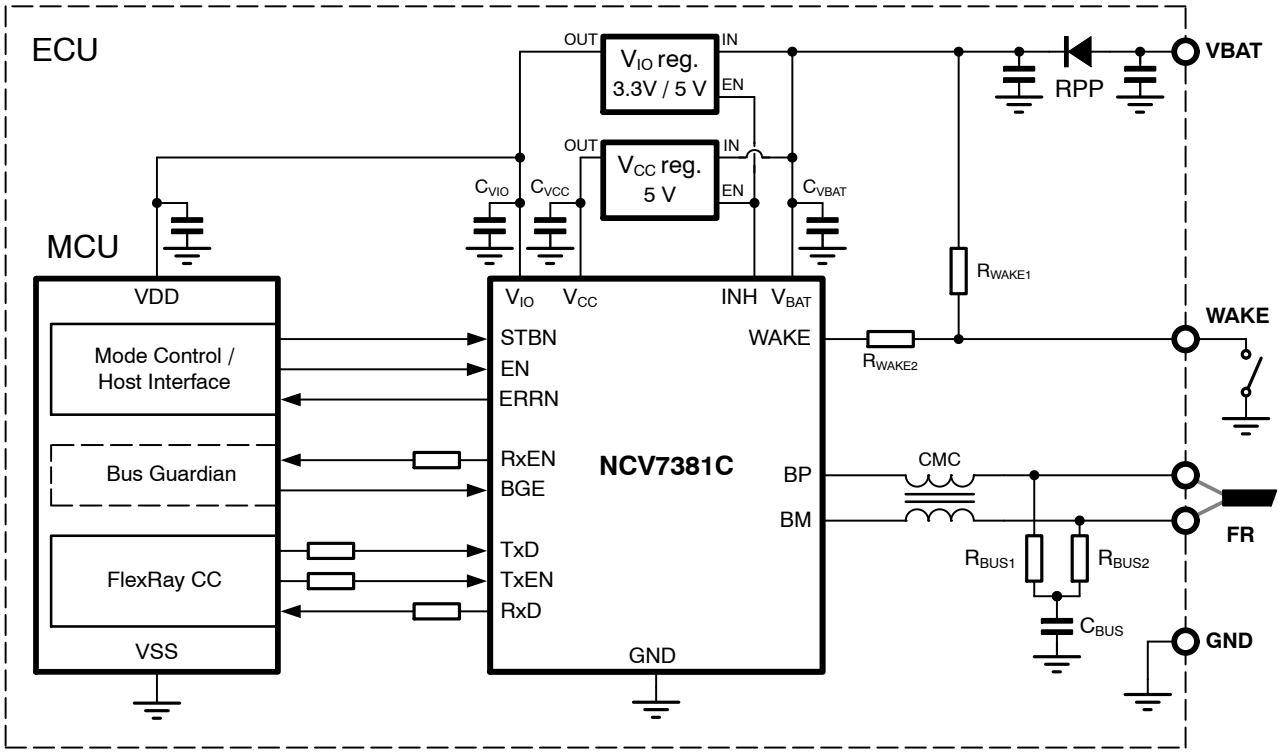


Figure 2. Application Diagram

RECOMMENDED EXTERNAL COMPONENTS FOR THE APPLICATION DIAGRAM

Component	Function	Min	Typ	Max	Unit
C_{VBAT}	Decoupling capacitor on battery line, ceramic		100		nF
C_{VCC}	Decoupling capacitor on V_{CC} supply line, ceramic		100		nF
C_{VIO}	Decoupling capacitor on V_{IO} supply line, ceramic		100		nF
R_{WAKE1}	Pull−up resistor on WAKE pin		33		kΩ
R_{WAKE2}	Serial protection resistor on WAKE pin		3.3		kΩ
R_{BUS1}	Bus termination resistor (Note 1)		47.5		Ω
R_{BUS2}	Bus termination resistor (Note 1)		47.5		Ω
C_{BUS}	Common−mode stabilizing capacitor, ceramic (Note 2)		4.7		nF
CMC	Common−mode choke		100		μH

1. Tolerance ±1%, type 0805
2. Tolerance ±20%, type 0805

MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Units
$uV_{BAT-MAX}$	Battery voltage power supply		−0.3	50	V
uV_{CC-MAX}	5 V Supply voltage		−0.3	5.5	V
uV_{IO-MAX}	Supply voltage for V_{IO} voltage level adaptation		−0.3	5.5	V
$uDigIn_{MAX}$	DC voltage at digital inputs (BGE, EN, STBN, TxD, TxEN)		−0.3	5.5	V
$uDigOut_{MAX}$	DC voltage at digital outputs (ERRN, RxD, RxEN)		−0.3	V_{IO}+0.3	V
$iDigOut_{IN-MAX}$	Digital output pins input current (V_{IO} = 0 V)		−10	+10	mA
uBM_{MAX}	DC voltage at pin BM		−50	50	V
uBP_{MAX}	DC voltage at pin BP		−50	50	V
$uDiff_{MAX}$	Maximum DC voltage between any two pins		−50	50	V
$uINH_{MAX}$	DC voltage at pin INH		−0.3	V_{BAT}+0.3	V
$iINH_{MAX}$	INH pin maximum load current		−10	−	mA
$uWAKE_{MAX}$	DC voltage at WAKE pin		−0.3	V_{BAT}+0.3	V
T_{J_MAX}	Junction temperature		−40	175	°C
T_{STG}	Storage Temperature Range		−55	150	°C
MSL	Moisture Sensitivity Level		2		−
T_{SLD}	Lead Soldering Temperature, Reflow (Note 3)		−	260	°C
$uESD_{IEC}$	System HBM on pins BP and BM (as per IEC 61000−4−2; 150 pF / 330 Ω)		−10	+10	kV
$uESD_{EXT}$	Component HBM on pins BP, BM, V_{BAT} and WAKE (as per EIA−JESD22−A114−B; 100 pF / 1500 Ω)		−6	+6	kV
$uESD_{INT}$	Component HBM on all other pins (as per EIA−JESD22−A114−B; 100 pF / 1500 Ω)		−4	+4	kV
uV_{TRAN}	Voltage transients, pins BP, BM, V_{BAT} and WAKE. According to ISO7637−2, Class C (Note 4)	test pulses 1	−100	−	V
		test pulses 2a	−	+75	V
		test pulses 3a	−150	−	V
		test pulses 3b	−	+100	V
	Voltage transients, pin V_{BAT}. According to ISO7637−2	test pulse 5 Load Dump	−	50	V
	Overvoltage, pin V_{BAT}, according to ISO16750−2	Jump Start	−	50	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. For more information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D
4. Test is carried out according to setup in *FlexRay Physical Layer EMC Measurement Specification, Version 3.0*. This specification is referring to ISO7637.

RECOMMENDED OPERATING RANGES

Symbol	Parameter	Min	Max	Units
uV_{BAT-OP}	Battery voltage power supply (Note 5)	5.5	50	V
uV_{CC-OP}	Supply voltage 5 V	4.75	5.25	V
uV_{IO-OP}	Supply voltage for V_{IO} voltage level adaptation	2.3	5.25	V
$uWAKE_{OP}$	DC voltage at WAKE pin	0	V_{BAT}	V
$uDigIO_{OP}$	DC voltage at digital pins (EN, TxD, TxEN, RxD, RxEN, BGE, STBN, ERRN)	0	V_{IO}	V
$uINH_{OP}$	DC voltage at pin INH	0	V_{BAT}	V
T_{AMB}	Ambient temperature (Note 6)	−40	150	°C
T_{J_OP}	Junction temperature	−40	155	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

5. For $T_J \le 130°C$, full functionality is guaranteed from 5.1 V. For more details see $uBDUVV_{BAT}$ parameter.
6. The specified range corresponds to T_{AMB_Class0}

THERMAL CHARACTERISTICS

Symbol	Rating	Value	Unit
$R_{\theta JA_1}$	Thermal Resistance Junction−to−Air, JEDEC 1S0P PCB	78	°C/W
$R_{\theta JA_2}$	Thermal Resistance Junction−to−Air, JEDEC 2S2P PCB	69	°C/W

ELECTRICAL CHARACTERISTICS

V_{BAT} = 5.5 V to 50 V, V_{CC} = 4.75 V to 5.25 V, V_{IO} = 2.3 V to 5.25 V, C_{VBAT} = 100 nF, C_{VCC} = 100 nF, C_{VIO} = 100 nF, for typical values T_A = 25°C, for min/max values T_J = −40°C to 155°C; unless otherwise noted. All voltages are referenced to GND (pin 13). Positive currents flow into the respective pin.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CURRENT CONSUMPTION						
$iV_{BAT-NORM}$	Current consumption from V_{BAT}	Normal−power modes	−	0.65	1.25	mA
iV_{BAT-LP}		Low−power modes	−	−	75	μA
		Sleep mode, V_{IO} = V_{CC} = 0 V	−	−	80	μA
		Low−power modes, V_{IO} = V_{CC} = 0 V, V_{BAT} = 12 V, T_J < 85°C (Note 7)	−	−	55	μA
$iV_{CC-NORM-IDLE}$	Current consumption from V_{CC}	Normal mode − bus signals Idle	5.0	−	15	mA
$iV_{CC-NORM-ACTIVE}$		Normal mode − bus signals Data_0/1; R_{BUS} = No Load	10	−	37	mA
		Normal mode − bus signals Data_0/1; R_{BUS} = 40 to 55 Ω	25	−	72	mA
iV_{CC-REC}		Receive−only mode	2.0	−	10	mA
iV_{CC-LP}		Low−power modes, T_J < 85°C (Note 7)	−	−	8.0	μA
$iV_{IO-NORM}$	Current consumption from V_{IO}	Normal−power modes	−	−	1.0	mA
iV_{IO-LP}		Low−power modes, T_J < 85°C (Note 7)	−	−	6.0	μA
$iTot_{-LP}$	Total current consumption − Sum from all supply pins	Low−power modes	−	−	100	μA
		Sleep mode, V_{IO} = V_{CC} = 5.0 V, V_{BAT} = 12 V, T_J < 85°C (Note 7)	−	−	65	μA
		Sleep mode, V_{IO} = V_{CC} = 5.0 V, V_{BAT} = 12 V, T_J < 25°C (Note 7)	−	−	55	μA
TRANSMITTER CHARACTERISTICS						
$uBDTx_{active}$	Differential voltage |uBP − uBM| when sending symbol “Data_0” or “Data_1”	R_{BUS} = 40 to 55 Ω; C_{BUS} = 100 pF Parameters defined in Figure 3	600	−	2000	mV
$uBDTx_{Idle}$	Differential voltage |uBP − uBM| when driving signal “Idle”		0	−	30	mV

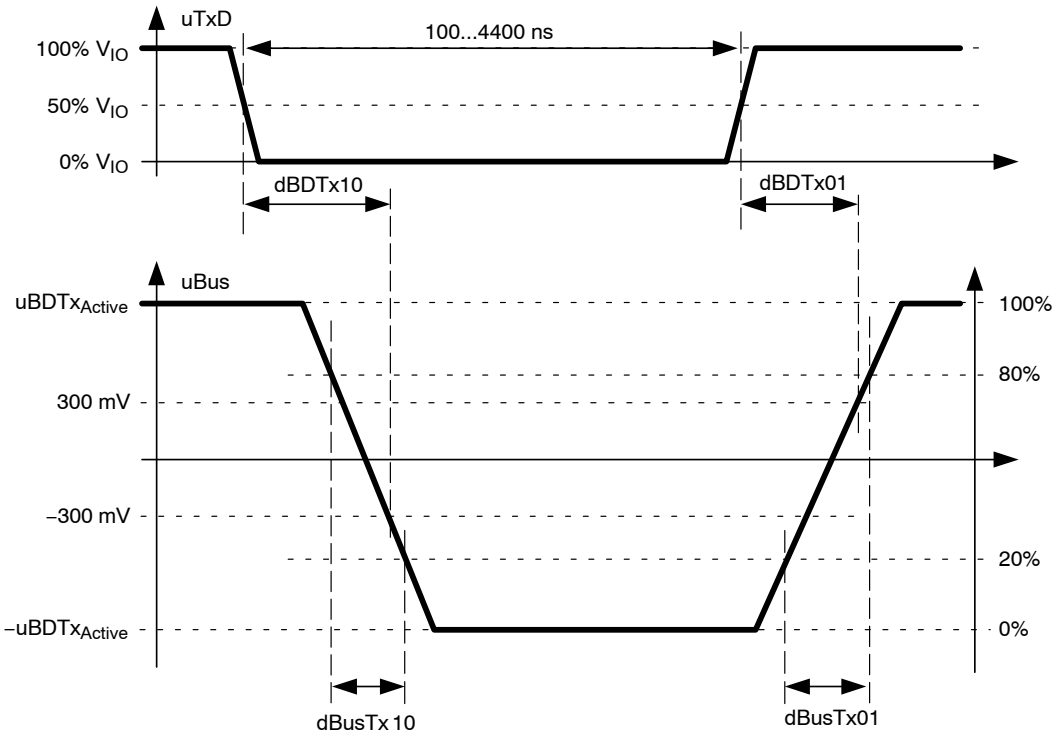
ELECTRICAL CHARACTERISTICS

V_{BAT} = 5.5 V to 50 V, V_{CC} = 4.75 V to 5.25 V, V_{IO} = 2.3 V to 5.25 V, C_{VBAT} = 100 nF, C_{VCC} = 100 nF, C_{VIO} = 100 nF, for typical values T_A = 25°C, for min/max values T_J = −40°C to 155°C; unless otherwise noted. All voltages are referenced to GND (pin 13). Positive currents flow into the respective pin.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
TRANSMITTER CHARACTERISTICS						
dBDTx10	Transmitter delay, negative edge	Test setup as per Figure 17 with R_{BUS} = 40 Ω; C_{BUS} = 100 pF Sum of TxD signal rise and fall time (20% to 80% V_{IO}) of up to 9 ns Parameters defined in Figure 3	–	–	75	ns
dBDTx01	Transmitter delay, positive edge		–	–	75	ns
dBDTxAsym	Transmitter delay mismatch, |dBDTx10 – dBDTx01| (Note 8)		–	–	4.0	ns
dBusTx10	Fall time of the differential bus voltage from 80% to 20%		6.0	–	18.75	ns
dBusTx01	Rise time of the differential bus voltage from 20% to 80%		6.0	–	18.75	ns
dBusTxDif	Differential bus voltage fall and rise time mismatch |dBusTx10 – dBusTx01|		–	–	3.0	ns
dBDTxia	Transmitter delay idle –> active	Test setup as per Figure 17 with R_{BUS} = 40 Ω; C_{BUS} = 100 pF Parameters defined in Figure 4	–	–	75	ns
dBDTxai	Transmitter delay active –> idle		–	–	75	ns
dBDTxDM	Idle−active transmitter delay mismatch |dBDTxia – dBDTxai|		–	–	50	ns
dBusTxia	Transition time idle –>active		–	–	30	ns
dBusTxai	Transition time active –> idle		–	–	30	ns
$dTxEN_{LOW}$	Time span of bus activity		550	–	650	ns
dBDTxActiveMax	Maximum length of transmitter activation		650	–	2600	μs
$iBP_{BMShortMax}$ $iBM_{BPShortMax}$	Absolute maximum output current when BP shorted to BM – no time limit	$R_{ShortCircuit} \le 1\ \Omega$	–	–	60	mA
$iBP_{GNDShortMax}$ $iBM_{GNDShortMax}$	Absolute maximum output current when shorted to GND – no time limit	$R_{ShortCircuit} \le 1\ \Omega$	–	–	60	mA
$iBP_{-5VShortMax}$ $iBM_{-5VShortMax}$	Absolute maximum output current when shorted to V_{BAT} = −5 V – no time limit	$R_{ShortCircuit} \le 1\ \Omega$	–	–	60	mA
$iBP_{BAT27ShortMax}$ $iBM_{BAT27ShortMax}$	Absolute maximum output current when shorted to V_{BAT} = 27 V – no time limit	$R_{ShortCircuit} \le 1\ \Omega$	–	–	60	mA
$iBP_{BAT48ShortMax}$ $iBM_{BAT48ShortMax}$	Absolute maximum output current when shorted to V_{BAT} = 48 V – no time limit	$R_{ShortCircuit} \le 1\ \Omega$	–	–	72	mA
$R_{BDTransmitter}$	Bus interface equivalent output impedance (Bus driver simulation model parameter)		31	105	500	Ω

ELECTRICAL CHARACTERISTICS

V_{BAT} = 5.5 V to 50 V, V_{CC} = 4.75 V to 5.25 V, V_{IO} = 2.3 V to 5.25 V, C_{VBAT} = 100 nF, C_{VCC} = 100 nF, C_{VIO} = 100 nF, for typical values T_A = 25°C, for min/max values T_J = −40°C to 155°C; unless otherwise noted. All voltages are referenced to GND (pin 13). Positive currents flow into the respective pin.



NOTE: TxD signal is constant for 100..4400 ns before the first edge.
All parameters values are valid even if the test is performed with opposite polarity.

Figure 3. Transmitter Characteristics (TxEN is Low and BGE is High)

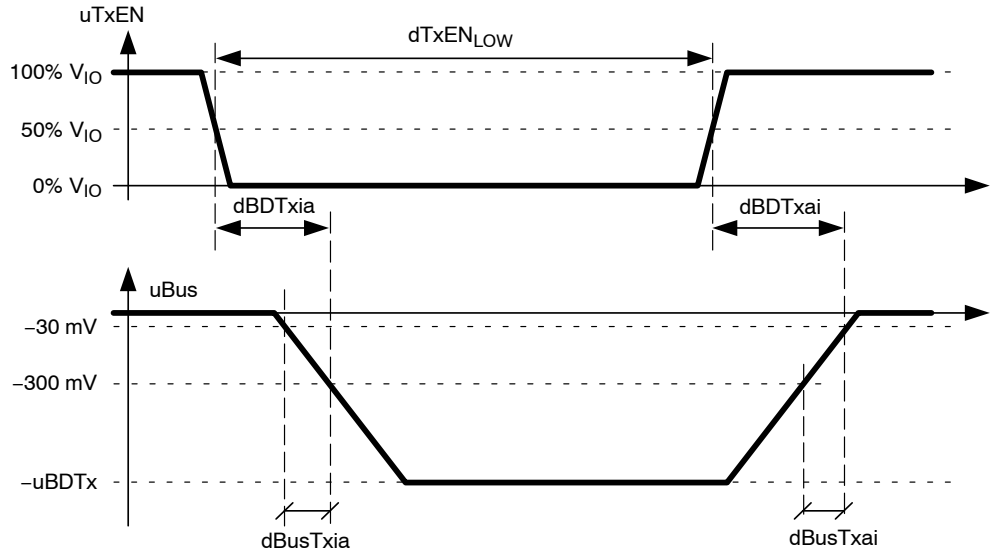


Figure 4. Transmitter Characteristics for Transitions between Idle and Active (TxD is Low)

ELECTRICAL CHARACTERISTICS

V_{BAT} = 5.5 V to 50 V, V_{CC} = 4.75 V to 5.25 V, V_{IO} = 2.3 V to 5.25 V, C_{VBAT} = 100 nF, C_{VCC} = 100 nF, C_{VIO} = 100 nF, for typical values T_A = 25°C, for min/max values T_J = −40°C to 155°C; unless otherwise noted. All voltages are referenced to GND (pin 13). Positive currents flow into the respective pin.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RECEIVER CHARACTERISTICS						
uData0	Receiver threshold for detecting Data_0	Activity detected previously |uBP − uBM| ≤ 3.0 V	−300	−	−150	mV
uData1	Receiver threshold for detecting Data_1		150	−	300	mV
|uData1| − |uData0|	Mismatch of receiver thresholds	(uBP + uBM) / 2 = 2.5 V	−30	−	30	mV
uData0_LP	Low−power receiver threshold for detecting Data_0	uV_{BAT} ≥ 7.0 V	−400	−	−100	mV
uCM	Common mode voltage range (with respect to GND) that does not disturb the receiver function and reception level parameters	uCM = (uBP + uBM) / 2 (Note 9)	−10	−	15	V
uBias	Bus bias voltage during bus state Idle in normal−power modes	R_{BUS} = 40 to 55 Ω; C_{BUS} = 100 pF (Note 10)	1800	2500	3200	mV
	Bus bias voltage during bus state Idle in low−power modes		−200	0	200	mV
R_{CM1}, R_{CM2}	Receiver common mode resistance	(Note 10)	10	−	40	kΩ
C_BP, C_BM	Input capacitance on BP and BM pin (Note 7)	f = 5.0 MHz	−	−	20	pF
C_Bus_{DIF}	Bus differential input capacitance (Note 7)	f = 5.0 MHz	−	−	5.0	pF
iBP_{LEAK} iBM_{LEAK}	Absolute leakage current when driver is off	uBP = uBM = 5.0 V All other pins = 0 V	−	−	25	μA
$iBP_{LEAKGND}$ $iBM_{LEAKGND}$	Absolute leakage current, in case of loss of GND	uBP = uBM = 0 V All other pins = 16 V	−	−	1600	μA

ELECTRICAL CHARACTERISTICS

V_{BAT} = 5.5 V to 50 V, V_{CC} = 4.75 V to 5.25 V, V_{IO} = 2.3 V to 5.25 V, C_{VBAT} = 100 nF, C_{VCC} = 100 nF, C_{VIO} = 100 nF, for typical values T_A = 25°C, for min/max values T_J = −40°C to 155°C; unless otherwise noted. All voltages are referenced to GND (pin 13). Positive currents flow into the respective pin.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
RECEIVER CHARACTERISTICS						
$uBusRx_{Data}$	Test signal parameters for reception of Data_0 and Data_1 symbols	Test signal and parameters defined in Figure 5 and Figure 6 RxD pin loaded with 25 pF capacitor	400	–	3000	mV
$dBusRx0_{BD}$			60	–	4330	ns
$dBusRx1_{BD}$			60	–	4330	ns
dBusRx10			–	–	22.5	ns
dBusRx01			–	–	22.5	ns
dBDRx10	Receiver delay, negative edge (Note 8)		–	–	75	ns
dBDRx01	Receiver delay, positive edge (Note 8)		–	–	75	ns
dBDRxAsym	Receiver delay mismatch |dBDRx10 − dBDRx01| (Note 8)		–	–	5.0	ns
uBusRx	Test signal parameters for bus activity detection		400	–	3000	mV
dBusActive			590	–	610	ns
dBusIdle			590	–	610	ns
dBusRxia			18	–	22	ns
dBusRxai			18	–	22	ns
dBDIdleDetection	Bus driver filter−time for idle detection		50	–	200	ns
dBDActivityDetection	Bus driver filter−time for activity detection		100	–	250	ns
dBDRxai	Bus driver idle reaction time		50	–	275	ns
dBDRxia	Bus driver activity reaction time		100	–	325	ns
dBDTxRxai	Idle−Loopdelay		–	–	325	ns
REMOTE WAKEUP DETECTION						
$dWU_{0Detect}$	Detection time for Wakeup Data_0 symbol		1.0	–	4.0	µs
$dWU_{IdleDetect}$	Detection time for Wakeup Idle/ Data_1 symbol		1.0	–	4.0	µs
$dWU_{Timeout}$	Maximum accepted Wakeup pattern duration		48	–	140	µs
$dWU_{Interrupt}$	Acceptance timeout for interruptions	(Note 11)	0.13	–	1.0	µs
$uV_{BAT-RWU}$	Minimum supply voltage V_{BAT} for remote wakeup events detection		–	–	5.5	V
dBDWakeup $Reaction_{remote}$	Reaction time after remote wakeup event		7.0	–	35	µs
TEMPERATURE MONITORING						
T_{JW}	Thermal warning level		125	140	155	°C
T_{JSD}	Thermal shutdown level		160	170	190	°C

ELECTRICAL CHARACTERISTICS

V_{BAT} = 5.5 V to 50 V, V_{CC} = 4.75 V to 5.25 V, V_{IO} = 2.3 V to 5.25 V, C_{VBAT} = 100 nF, C_{VCC} = 100 nF, C_{VIO} = 100 nF, for typical values T_A = 25°C, for min/max values T_J = −40°C to 155°C; unless otherwise noted. All voltages are referenced to GND (pin 13). Positive currents flow into the respective pin.

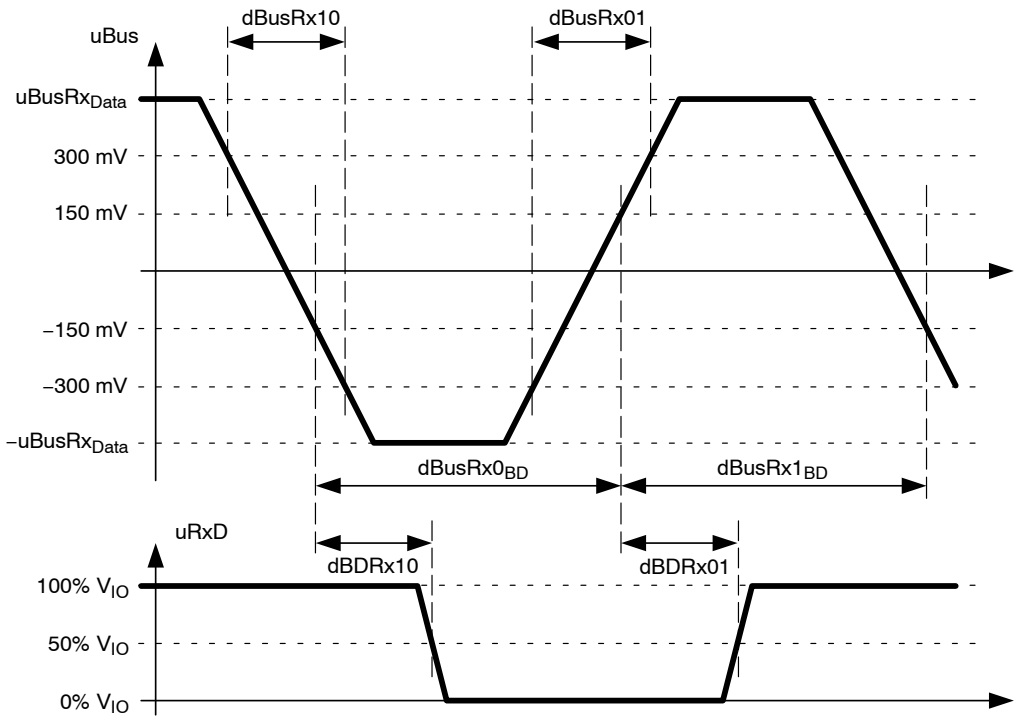


Figure 5. Receiver Characteristics

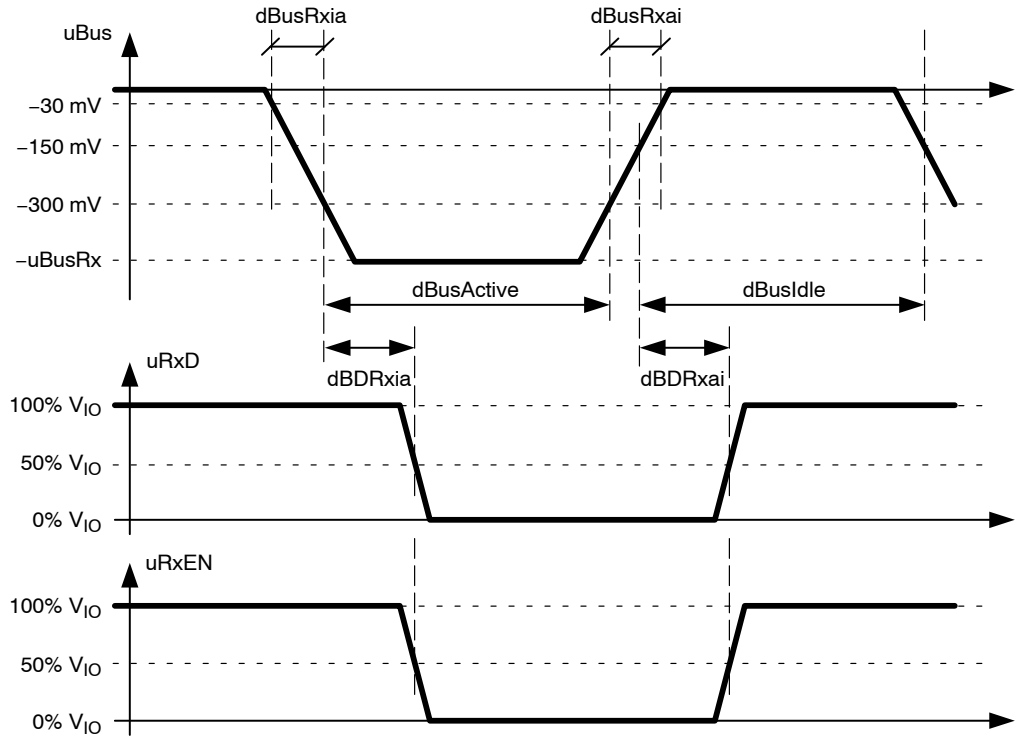


Figure 6. Parameters of Bus Activity Detection

ELECTRICAL CHARACTERISTICS

V_{BAT} = 5.5 V to 50 V, V_{CC} = 4.75 V to 5.25 V, V_{IO} = 2.3 V to 5.25 V, C_{VBAT} = 100 nF, C_{VCC} = 100 nF, C_{VIO} = 100 nF, for typical values T_A = 25°C, for min/max values T_J = −40°C to 155°C; unless otherwise noted. All voltages are referenced to GND (pin 13). Positive currents flow into the respective pin.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
WAKE PIN						
$uV_{BAT-WAKE}$	Minimum supply voltage V_{BAT} for local wakeup events detection		–	–	7.0	V
$uWAKE_{TH}$	Threshold of WAKE comparator		0.45 x V_{BAT}	0.5 x V_{BAT}	0.55 x V_{BAT}	V
dBDWakePulseFilter	WAKE pulse filter time (spike rejection)		1.0	–	500	μs
dBDWakeup $Reaction_{local}$	Reaction time after local wakeup event		14	–	50	μs
$iWAKE_{PD}$	Internal pull−down current	uWAKE = 0 V for longer than dWakePulseFilter	3.0	–	12	μA
$iWAKE_{PU}$	Internal pull−up current	uWAKE = V_{BAT} for longer than dWakePulseFilter	−12	–	−3.0	μA
INH PIN						
$uINH1_{Not_Sleep}$	Voltage on INH pin when signaling Not_Sleep	iINH = −5.0 mA uV_{BAT} > 5.5 V	uV_{BAT} − 0.6	uV_{BAT} − 0.27	uV_{BAT} − 0.1	V
$iINH1_{LEAK}$	Leakage current while signaling Sleep		−5.0	0	5.0	μA
POWER SUPPLY MONITORING						
$uBDUVV_{BAT}$	V_{BAT} undervoltage detection threshold	$T_J \le 130°C$ (Note 7)	4.0	4.79	5.1	V
		$-40°C \le T_J \le 155°C$	4.0	4.79	5.5	V
$uBDRV_{BAT}$	V_{BAT} undervoltage recovery threshold	$T_J \le 130°C$ (Note 7)	–	4.9	5.1	V
		$-40°C \le T_J \le 155°C$	–	4.9	5.5	V
$uBDUVV_{CC}$	V_{CC} undervoltage threshold		4.0	4.3	4.5	V
uUV_{IO}	V_{IO} undervoltage threshold		2.0	2.15	2.3	V
$uBDUVV_{BAT-WAKE}$	V_{BAT} undervoltage threshold for correct detection of the local wakeup		5.0	5.6	7.0	V
uUV_HYST	Hysteresis of the undervoltage detectors	V_{BAT} undervoltage detector	20	110	200	mV
		V_{CC} undervoltage detector	20	100	200	mV
		V_{IO} undervoltage detector	20	50	200	mV
		$V_{BAT-WAKE}$ undervoltage detector	20	140	200	mV
$dBDUVV_{CC}$	V_{CC} undervoltage detection time		150	350	750	ms
$dBDUVV_{IO}$	V_{IO} undervoltage detection time		150	350	750	ms
$dBDUVV_{BAT}$	V_{BAT} undervoltage detection time		350	750	1500	μs
$dBDRV_{CC}$	V_{CC} undervoltage recovery time		1.5	–	4.5	ms
$dBDRV_{IO}$	V_{IO} undervoltage recovery time		–	–	1.0	ms
$dBDRV_{BAT}$	V_{BAT} undervoltage recovery time		–	–	1.0	ms

ELECTRICAL CHARACTERISTICS

V_{BAT} = 5.5 V to 50 V, V_{CC} = 4.75 V to 5.25 V, V_{IO} = 2.3 V to 5.25 V, C_{VBAT} = 100 nF, C_{VCC} = 100 nF, C_{VIO} = 100 nF, for typical values T_A = 25°C, for min/max values T_J = −40°C to 155°C; unless otherwise noted. All voltages are referenced to GND (pin 13). Positive currents flow into the respective pin.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
HOST INTERFACE						
dBDModeChange	EN and STBN level filtering time for operating mode transition		21	–	65	µs
dGo−to−Sleep	Go−to−Sleep mode timeout		14	–	33	µs
$dReactionTime_{ERRN}$	Reaction time on ERRN pin	Error detected	–	–	33	µs
		Wakeup detected or Mode changed	–	–	1.0	µs
DIGITAL INPUT SIGNALS VOLTAGE THRESHOLDS (Pins EN, STBN, BGE, TxEN)						
$uV_{DIG-IN-LOW}$	Low level input voltage	$uV_{DIG} = uV_{IO}$	−0.3	–	$0.3 \times V_{IO}$	V
$uV_{DIG-IN-HIGH}$	High level input voltage		$0.7 \times V_{IO}$	–	5.5	V
EN PIN						
R_{PD}_EN	Pull−down resistance		50	110	200	kΩ
iEN_{IL}	Low level input current	uEN = 0 V	−1.0	0	1.0	µA
dEN_{STAT}	EN toggling period for status register read−out		2.0	–	20	µs
dEN_{STAT_L} dEN_{STAT_H}	Duration of EN Low and High level for status register read−out		1.0	–	–	µs
dEN_ERRN	Delay from EN falling edge to ERRN showing valid signal during status register read−out		–	–	1.0	µs
STBN PIN						
R_{PD}_STBN	Pull−down resistance		50	110	200	kΩ
$iSTBN_{IL}$	Low level input current	uSTBN = 0 V	−1.0	0	1.0	µA
BGE PIN						
R_{PD}_BGE	Pull−down resistance		200	320	450	kΩ
R_{PD}_BGE	Pull−down resistance		200	320	450	kΩ
$iBGE_{IL}$	Low level input current	uBGE = 0 V	−1.0	0	1.0	µA
$iBGE_{IL}$	Low level input current	uBGE = 0 V	−1.0	0	1.0	µA
TxD PIN						
uBDLogic_0	Low level input voltage		−0.3	–	$0.4 \times V_{IO}$	V
uBDLogic_1	High level input voltage		$0.6 \times V_{IO}$	–	5.5	V
R_{PD}_TxD	Pull−down resistance		5.0	11	20	kΩ
C_BDTxD	Input capacitance on TxD pin (Note 7)	f = 5.0 MHz	–	–	10	pF
$iTxD_{LI}$	Low level input current	uTxD = 0 V	−1.0	0	1.0	µA
TxEN PIN						
R_{PU}_TxEN	Pull−up resistance		50	110	200	kΩ
$iTxEN_{IH}$	High level input current	$uTxEN = V_{IO}$	−1.0	0	1.0	µA
$iTxEN_{LEAK}$	Input leakage current	uTxEN = 5.25 V, V_{IO} = 0 V	−1.0	0	1.0	µA

ELECTRICAL CHARACTERISTICS

V_{BAT} = 5.5 V to 50 V, V_{CC} = 4.75 V to 5.25 V, V_{IO} = 2.3 V to 5.25 V, C_{VBAT} = 100 nF, C_{VCC} = 100 nF, C_{VIO} = 100 nF, for typical values T_A = 25°C, for min/max values T_J = −40°C to 155°C; unless otherwise noted. All voltages are referenced to GND (pin 13). Positive currents flow into the respective pin.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL OUTPUT SIGNALS VOLTAGE LIMITS (Pins RxD, RxEN and ERRN)						
$uV_{DIG-OUT-LOW}$	Low level output voltage	$iRxD_{OL}$ = 6.0 mA $iRxEN_{OL}$ = 5.0 mA $iERRN_{OL}$ = 0.7 mA (Note 12)	0	–	0.2 × V_{IO}	V
$uV_{DIG-OUT-HIGH}$	High level output voltage	$iRxD_{OH}$ = −6.0 mA $iRxEN_{OH}$ = −5.0 mA $iERRN_{OH}$ = −0.7 mA (Note 12)	0.8 × V_{IO}	–	V_{IO}	V
$uV_{DIG-OUT-UV}$	Output voltage on a digital output when V_{IO} in undervoltage	R_{LOAD} = 100 kΩ to GND, Either V_{CC} or V_{BAT} supplied	–	–	500	mV
$uV_{DIG-OUT-OFF}$	Output voltage on a digital output when unsupplied	R_{LOAD} = 100 kΩ to GND	–	–	500	mV
RxD PIN						
$dBDRxD_{R15}$	RxD signal rise time (20%−80% V_{IO})	RxD pin loaded with 15 pF capacitor (Note 7)	–	–	6.5	ns
$dBDRxD_{F15}$	RxD signal fall time (20%−80% V_{IO})		–	–	6.5	ns
$dBDRxD_{R15}$ + $dBDRxD_{F15}$	Sum of rise and fall time (20%−80% V_{IO})		–	–	13	ns
$\lvert dBDRxD_{R15} - dBDRxD_{F15}\rvert$	Difference of rise and fall time		–	–	5.0	ns
$dBDRxD_{R25}$	RxD signal rise time (20%−80% V_{IO})	RxD pin loaded with 25 pF capacitor	–	–	8.5	ns
$dBDRxD_{F25}$	RxD signal fall time (20%−80% V_{IO})		–	–	8.5	ns
$dBDRxD_{R25}$ + $dBDRxD_{F25}$	Sum of rise and fall time (20%−80% V_{IO})		–	–	16.5	ns
$\lvert dBDRxD_{R25} - dBDRxD_{F25}\rvert$	Difference of rise and fall time		–	–	5.0	ns
$dBDRxD_{R25_10}$ + $dBDRxD_{F25_10}$	RxD signal sum of rise and fall time at TP4_CC (20%−80% V_{IO})	RxD pin loaded with 25 pF capacitor plus 10 pF at the end of a 50 Ω, 1 ns microstripline (Note 13)	–	–	16.5	ns
$\lvert dBDRxD_{R25_10} - dBDRxD_{F25_10}\rvert$	RxD signal difference of rise and fall time at TP4_CC (20%−80% V_{IO})		–	–	5.0	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Values based on design and characterization, not tested in production.
8. Guaranteed for ±300 mV and ±150 mV level of uBus.
9. Tested on a receiving bus driver. Sending bus driver has a ground offset voltage in the range of [−12.5 V to +12.5 V] and sends a 50/50 pattern.
10. Bus driver is connected to GND and uV_{CC} = 5 V and $uV_{BAT} \geq 7$ V.
11. The minimum value is only guaranteed, when the phase that is interrupted was continuously present for at least 870 ns.
12. $uV_{DIG} = uV_{IO}$. No undervoltage on V_{IO} and either V_{CC} or V_{BAT} supplied.
13. Simulation results. Simulation performed within T_{J_OP} range, according to *FlexRay Electrical Physical Layer Specification, Version 3.0.1.*

FUNCTIONAL DESCRIPTION

Operating Modes

NCV7381C can switch between several operating modes depicted in Figure 7. In Normal and Receive−only modes, the chip interconnects a FlexRay communication controller with the bus medium for full−speed communication. These two modes are also referred to as normal−power modes.

In Standby and Sleep modes, the communication is suspended and the power consumption is substantially reduced. A wakeup on the bus or through a locally monitored signal on pin WAKE can be detected and signaled to the host. Go−to−sleep mode is a temporary mode ensuring correct transition between any mode and the Sleep mode. All three modes – Standby, Sleep and Go−to−sleep – are referred to as low−power modes.

The operating mode selected is a function of the host signals STBN and EN, the state of the supply voltages and the wakeup detection. As long as all three supplies (V_{BAT}, V_{CC}, V_{IO}) remain above their respective undervoltage detection levels, the logical control by EN and STBN pins shown in Figure 7 applies. Influence of the power supplies and of the wakeup detection on the operating modes is described in subsequent paragraphs.

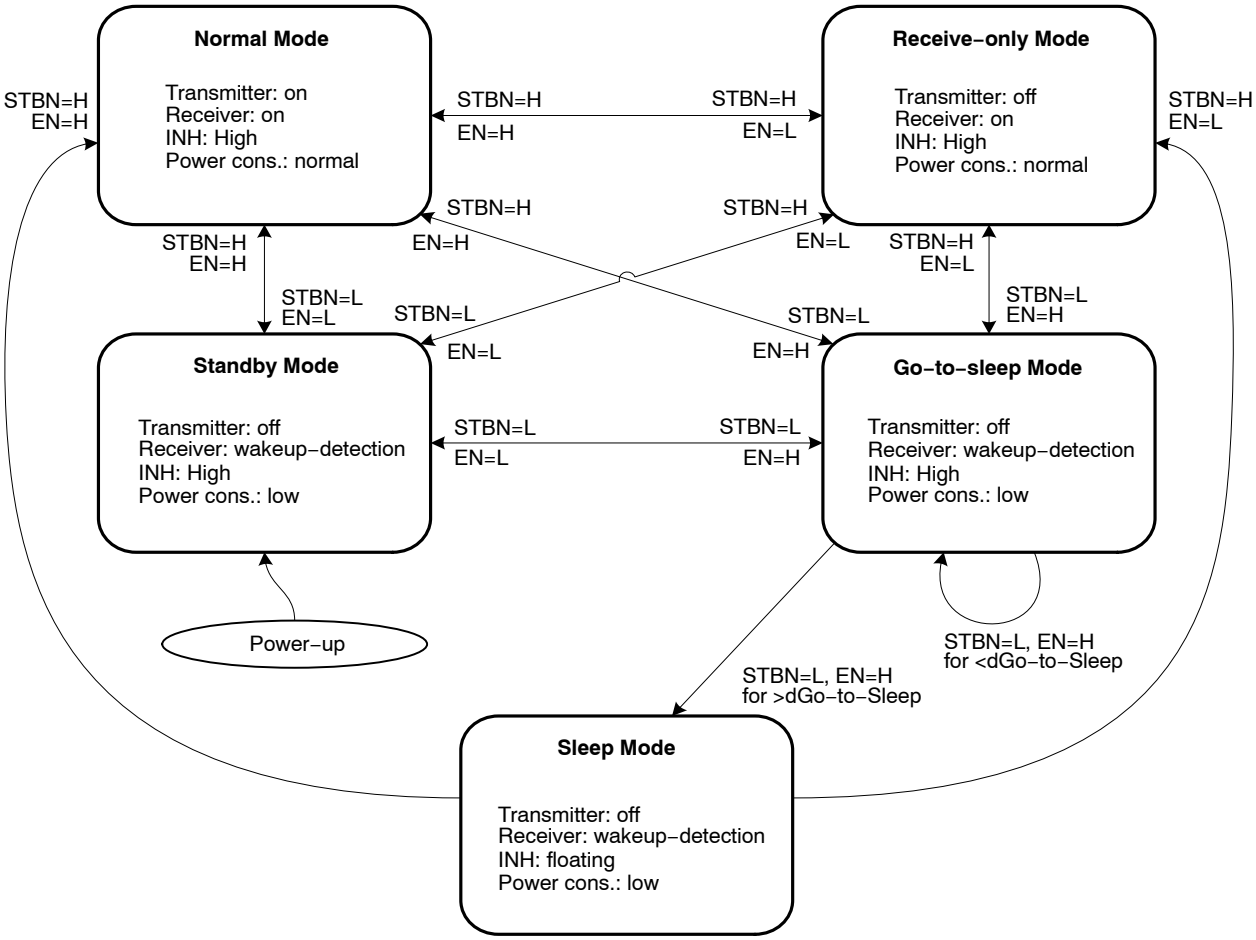


Figure 7. Operating Modes and their Control by the STBN and EN Pins

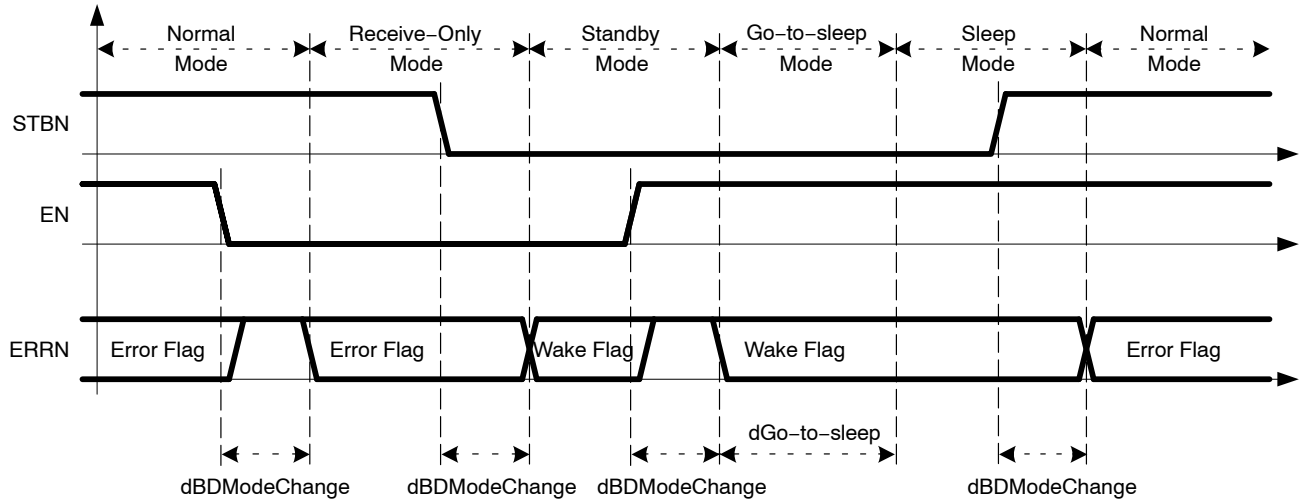


Figure 8. Timing Diagram of Operating Modes Control by the STBN and EN Pins

Power Supplies and Power Supply Monitoring

NCV7381C is supplied by three pins. V_{BAT} is the main supply both for NCV7381C and the full electronic module. V_{BAT} will be typically connected to the automobile battery through a reverse−polarity protection. V_{CC} is a 5 V low−voltage supply primarily powering the FlexRay bus driver core in a normal−power mode. V_{IO} supply serves to adapt the logical levels of NCV7381C to the host and/or the FlexRay communication controller digital signal levels. All supplies should be properly decoupled by filtering capacitors − refer to Figure 2 and Recommended External Components for the Application Diagram.

All three supplies are monitored by undervoltage detectors with individual thresholds and filtering times both for undervoltage detection and recovery − see Table Electrical Characteristics − Power Supply Monitoring Parameters.

Logic Level Adaptation

Level shift input V_{IO} is used to apply a reference voltage $uV_{DIG} = uV_{IO}$ to all digital inputs and outputs in order to adapt the logical levels of NCV7381C to the host and/or the FlexRay communication controller digital signal levels

Internal Flags

The NCV7381C control logic uses a number of internal flags (i.e. one−bit memories) reflecting important conditions or events. Table 1 summarizes the individual flags and the conditions that lead to a set or reset of the flags.

Table 1. INTERNAL FLAGS

Flag	Set Condition	Reset Condition	Comment
Local Wakeup	Low level detected on WAKE pin in a low−power mode	Low−power mode is entered	
Remote Wakeup	Remote wakeup detected on the bus in a low−power mode	Low−power mode is entered	
Wakeup	Local Wakeup flag changes to set or Remote Wakeup flag changes to set	Normal mode is entered or Low−power mode is entered or Any undervoltage flag becomes set	
Power−on	Internal power supply of the chip becomes sufficient for the operation of the control logic	Normal mode is entered	
Thermal Warning	Junction temperature is higher than *Tjw* (typ. 138°C) in a normal−power mode and V_{BAT} is not in undervoltage	(Junction temperature is below *Tjw* in a normal−power mode or the status register is read in a low−power mode) and V_{BAT} is not in undervoltage	The thermal warning flag has no influence on the bus driver function
Thermal Shutdown	Junction temperature is higher than *Tjsd* (typ. 172°C) in a normal−power mode and V_{BAT} is not in undervoltage	Junction temperature is below *Tjsd* in a normal−power mode and falling edge on TxEN and V_{BAT} is not in undervoltage	The transmitter is disabled as long as the thermal shutdown flag is set
TxEN Timeout	TxEN is Low for longer than dBDTxActiveMax (typ. 1.5 ms) and bus driver is in Normal mode	TxEN is High or Normal mode is left	The transmitter is disabled as long as the timeout flag is set
Bus Error	Transmitter is enabled and Data on bus are different from TxD signal (sampled after each TxD edge)	(Transmitter is enabled and Data on bus are identical to TxD signal) or Transmitter is disabled	The bus error flag has no influence on the bus driver function
V_{BAT} Undervoltage	V_{BAT} is below the undervoltage threshold for longer than $dBDUVV_{BAT}$	V_{BAT} is above the undervoltage threshold for longer than $dBDRV_{BAT}$ or Wake flag becomes set	
V_{CC} Undervoltage	V_{CC} is below the undervoltage threshold for longer than $dBDUVV_{CC}$	V_{CC} is above the undervoltage threshold for longer than $dBDRV_{CC}$ or Wake flag becomes set or V_{BAT} undervoltage is recovered	
V_{IO} Undervoltage	V_{IO} is below the undervoltage threshold for longer than dUV_{IO}	V_{IO} is above the undervoltage threshold for longer than $dBDRV_{IO}$ or Wake flag becomes set or V_{BAT} undervoltage is recovered	
Error	Any of the following status bits is set: • Bus error • Thermal Warning • Thermal Shutdown • TxEN Timeout • V_{BAT} Undervoltage • V_{CC} Undervoltage • V_{IO} Undervoltage	All of the following status bits are reset: • Bus error • Thermal Warning • Thermal Shutdown • TxEN Timeout • V_{BAT} Undervoltage • V_{CC} Undervoltage • V_{IO} Undervoltage	

Operating Mode Changes Caused by Internal Flags

Changes of some internal flags described in Table 1 can force an operating mode transition complementing or overruling the operating mode control by the digital inputs STBN and EN which is shown in Figure 7:

- Setting the V_{BAT} and/or VIO undervoltage flag causes a transition to Sleep mode
- Setting the V_{CC} undervoltage flag, while the bus driver is not in Sleep, causes a transition to Standby mode
- In case a Wake flag is set, the NCV7381C transitions to Standby mode, all undervoltage flags are cleared and the corresponding undervoltage detection timers are reset. The restart of the undervoltage detection timers allows the external power supplies to ramp−up and stabilize properly if, for example, they were previously switched off during Sleep mode
- In case the V_{BAT} is recovered from undervoltage condition, the operating mode control of the chip by digital inputs STBN and EN is re−enabled, all undervoltage flags are cleared and the corresponding undervoltage detection timers are reset
- In case the V_{CC} and V_{IO} are both recovered from undervoltage while V_{BAT} is not in undervoltage condition, the operating mode control by digital inputs STBN and EN is re−enabled.

NOTE: The operating mode control state machine is not reset when an undervoltage condition is detected. Thus if Sleep mode was requested by the host prior to undervoltage condition detection and the EN pin was set Low in Sleep mode, the device stays in Sleep once the undervoltage is recovered, although STBN and EN pins are both set Low, which is otherwise considered a Standby mode request.

FlexRay Transceiver

NCV7381C contains a fully−featured FlexRay transceiver compliant with Electrical Physical Layer Specification Rev. 3.0.1. The transmitter part translates logical signals on digital inputs TxEN, BGE and TxD into appropriate bus levels on pins BP and BM. A transmission cannot be started with Data_1. In case the transmitter is enabled for longer than *dBDTxActiveMax*, the TxEN Timeout flag is set and the current transmission is disabled. The receiver part monitors bus pins BP and BM and signals the detected levels on digital outputs RxD and RxEN. The different bus levels are defined in Figure 9. The function of the transceiver and the related digital pins in different operating modes is detailed in Table 2 and Table 3.

- The transmitter can only be enabled if the activation of the transmitter is initiated in Normal mode.
- The receiver function is enabled by entering a normal−power mode.

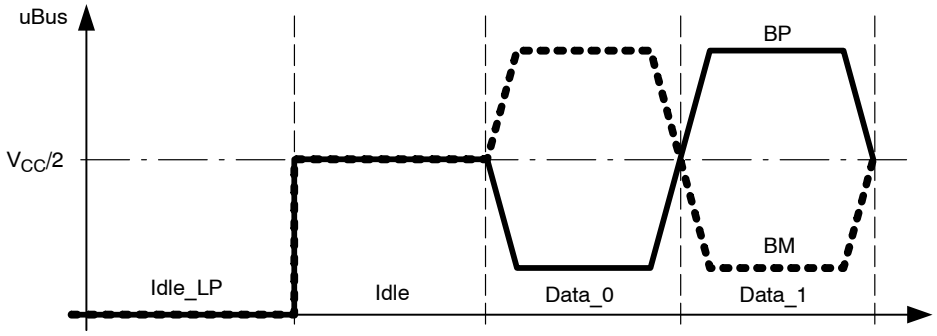


Figure 9. FlexRay Bus Signals

Table 2. TRANSMITTER FUNCTION AND TRANSMITTER−RELATED PINS

Operating Mode	BGE	TxEN	TxD	Transmitted Bus Signal
Standby, Go−to−sleep, Sleep	x	x	x	Idle_LP
Receive−only	x	x	x	Idle
Normal	0	x	x	Idle
	1	1	x	Idle
	1	0	0	Data_0
	1	0	1	Data_1

Table 3. RECEIVER FUNCTION AND RECEIVER−RELATED PINS

Operating Mode	Signal on Bus	Wake flag	RxD	RxEN
Standby, Go−to−sleep, Sleep	x	not set	High	High
	x	set	Low	Low
Normal, Receive−only	Idle	x	High	High
	Data_0	x	Low	Low
	Data_1	x	High	Low

Bus Guardian Interface

The interface consists of the BGE digital input signal allowing a Bus Guardian unit to disable the transmitter and of the RxEN digital output signal used to signal whether the communication signal is Idle or not.

Bus Driver Voltage Regulator Control

NCV7381C provides a high−voltage output pin INH which can be used to control an external voltage regulator (see Figure 2). The pin INH is driven by a switch to V_{BAT} supply. In Normal, Receive−only, Standby and Go−to−Sleep modes, the switch is activated thus forcing a High level on pin INH. In the Sleep mode, the switch is open and INH pin remains floating. If a regulator is directly controlled by INH, it is then active in all operating modes with the exception of the Sleep mode.

Bus Driver Remote Wakeup Detection

During a low−power mode and under the presence of V_{BAT} voltage, a low−power receiver constantly monitors the activity on bus pins BP and BM. A valid remote wakeup is detected when either a wakeup pattern or a dedicated wakeup frame is received. A valid remote wakeup is also detected when wakeup pattern has been started in normal−power mode already.

A wakeup pattern is composed of two Data_0 symbols separated by Data_1 or Idle symbols. The basic wakeup pattern composed of Data_0 and Idle symbols is shown in Figure 10; the wakeup pattern composed of Data_0 and Data_1 symbols – referred to as “alternative wakeup pattern” − is depicted in Figure 11.

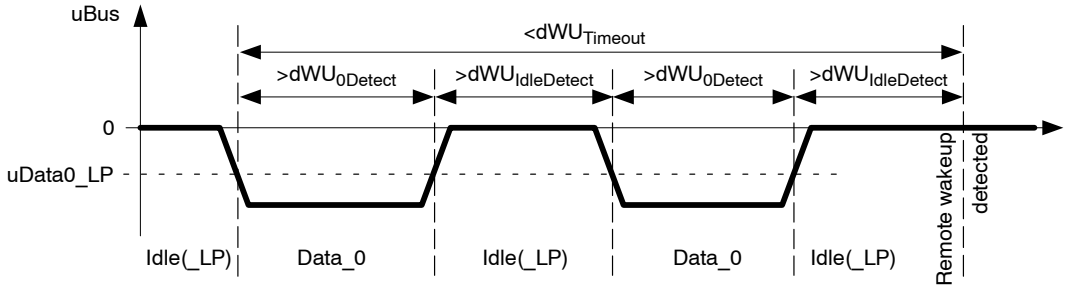


Figure 10. Valid Remote Wakeup Pattern

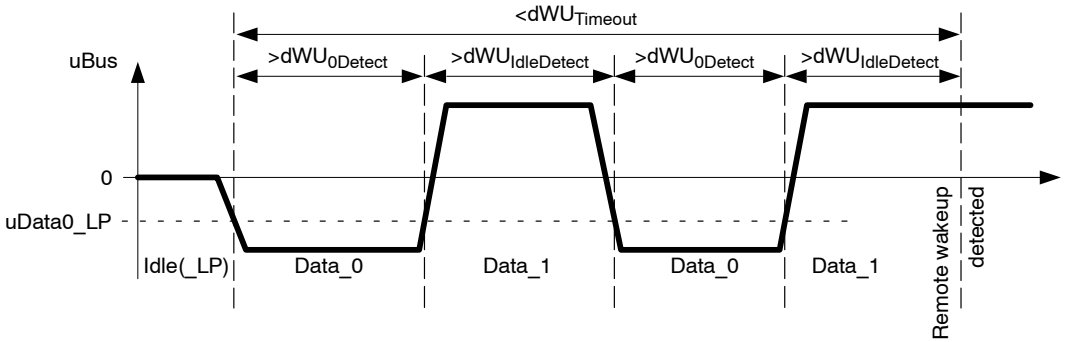


Figure 11. Valid Alternative Remote Wakeup Pattern

A remote wakeup will be also detected if NCV7381C receives a full FlexRay frame at 10 Mbit/s with the following payload data:

0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,
0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,
0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0x00, 0x00, 0x00, 0x00, 0x00,
0xFF, 0xFF, 0xFF, 0xFF, 0xFF, 0xFF

The wakeup pattern, the alternative wakeup pattern and the wakeup frame lead to identical wakeup treatment and signaling.

Local Wakeup Detection

The high−voltage input WAKE is monitored in low−power modes and under the condition of sufficient V_{BAT} supply level. If a falling edge is recognized on WAKE pin, a local wakeup is detected. In order to avoid false wakeups, the Low level after the falling edge must be longer than *dWakePulseFilter* in order for the wakeup to be valid. The WAKE pin can be used, for example, for switch or contact monitoring.

Internal pull−up and pull−down current sources are connected to WAKE pin in order to minimize the risk of parasitic toggling. The current source polarity is automatically selected based on the WAKE input signal polarity – when the voltage on WAKE stays stable High (Low) for longer than *dWakePulseFilter*, the internal current source is switched to pull−up (pull−down).

ERRN Pin and Status Register

Provided V_{IO} supply is present together with either V_{BAT} or V_{CC}, the digital output ERRN indicates the state of the internal “Error” flag when in Normal mode and the state of the internal “Wake” flag when in Standby, Go−to−Sleep or Sleep. In Receive−only mode ERRN indicates either the state of the internal “Error” or the wakeup source (See Table 4).

The polarity of the indication is reversed – ERRN pin is pulled Low when the “Error” flag is set. The signaling on pin ERRN functions in all operating modes.

Table 4. SIGNALING ON ERRN PIN

STBN	EN	Conditions	Error flag	Wake flag	ERRN
High	High	–	not set	x	High
			set	x	Low
High	Low	EN has been set to High after previous wakeup	not set	x	High
			set	x	Low
		EN has not been set to High after previous wakeup	x	Set local	High
			x	Set remote	Low
Low	x	–	x	not set	High
			x	set	Low

Additionally, a full set of internal bits referred to as status register can be read through ERRN pin with EN pin used as a clock signal – the status register content is described in Table 5 while an example of the read−out waveforms is shown in Figure 12 and Figure 13. The individual status bits are channeled to ERRN pin with reversed polarity (if a status bit is set, ERRN is pulled Low) at the falling edge on EN pin (the status register starts to be shifted only at the second falling edge). As long as the EN pin toggling period falls in the dEN_{STAT} range, the operating mode is not changed and the read−out continues. As soon as the EN level is stable for more than *dBDModeChange*, the read−out is considered as finished and the operating mode is changed according the current EN value. At the same time, the status register bits S4 to S10 are reset provided the particular bits have been read−out and the corresponding flags are not set any more – see Table 5. The status register read−out always starts with bit S0 and the exact number of bits shifted to ERRN during the read−out is not relevant.

Table 5. STATUS REGISTER

Bit Number	Status Bit Content	Note	Reset after Finished Read−out
S0	Local wakeup flag	reflects directly the corresponding flag	no
S1	Remote wakeup flag		
S2	not used; always High		no
S3	Power−on status	the status bit is set if the corresponding flag was set previously (the respective High level of the flag is latched in its status counter−part)	yes, if the corresponding flag is reset and the bit was read−out
S4	Bus error status		
S5	Thermal shutdown status		
S6	Thermal warning status		
S7	TxEN Timeout status		
S8	V_{BAT} Undervoltage status		
S9	V_{CC} Undervoltage status		
S10	V_{IO} Undervoltage status		
S11	BGE Feedback	Normal mode: BGE pin logical state (Note 14) Other modes: Low	–
S12−S15	not used; always Low		no
S16−S23	Version of the NCV7381C analog part	fixed values identifying the production masks version	no
S24−S31	Version of the NCV7381C digital part		

14. The BGE pin state is latched during status register read−out at rising edge of the EN pin.

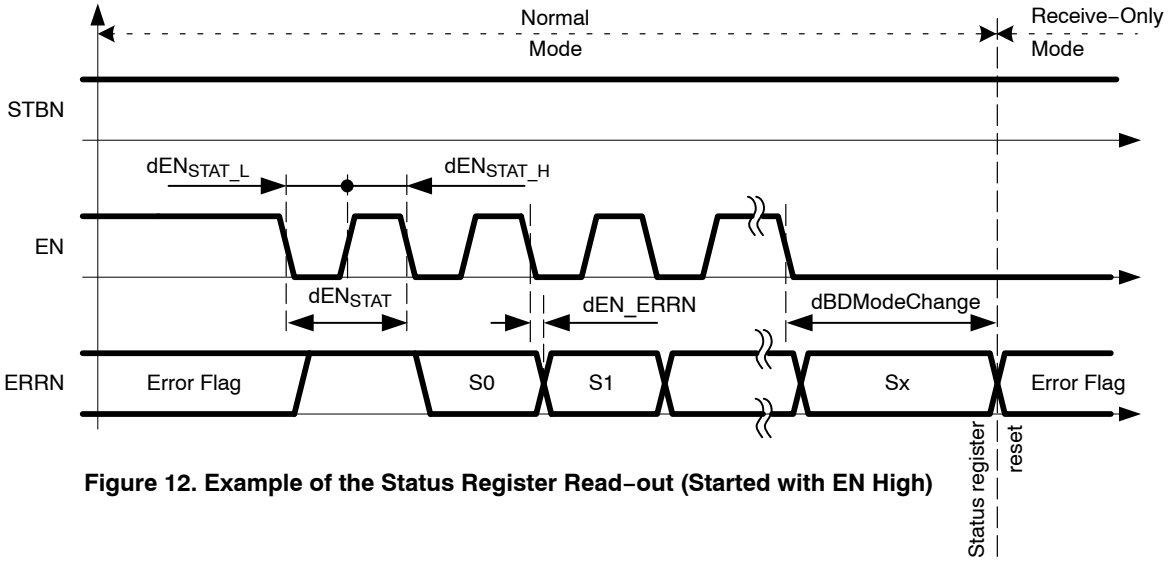


Figure 12. Example of the Status Register Read−out (Started with EN High)

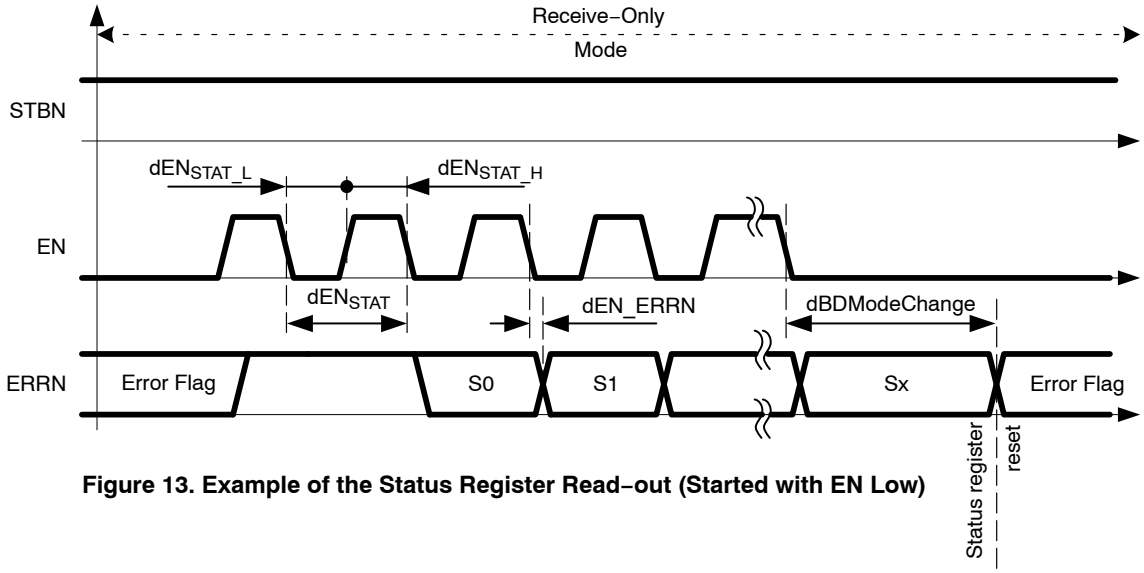


Figure 13. Example of the Status Register Read−out (Started with EN Low)

TYPICAL CHARACTERISTICS

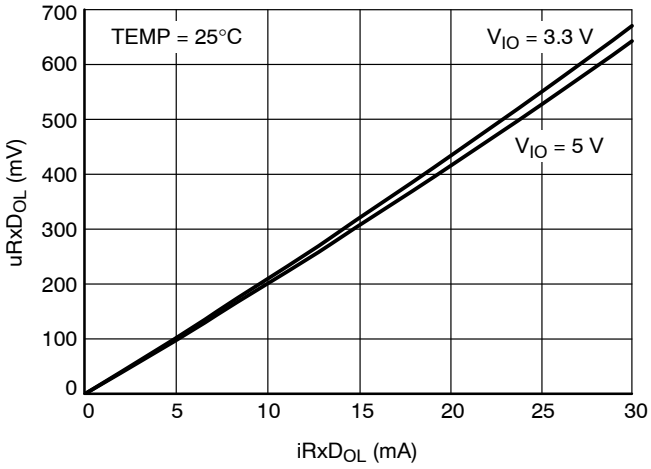


Figure 14. RxD Low Output Characteristic

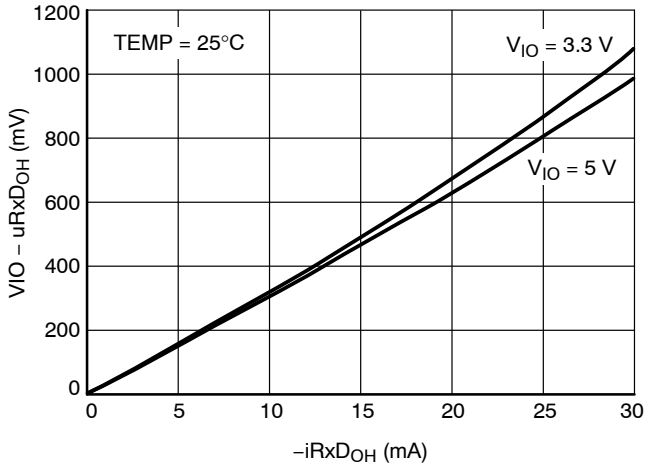


Figure 15. RxD High Output Characteristic

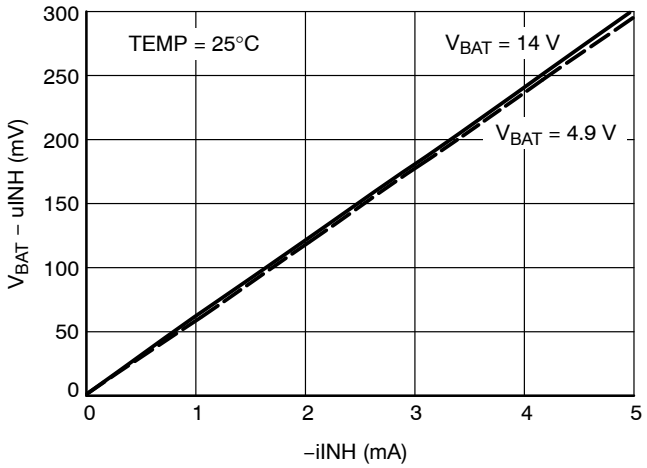


Figure 16. INH Not_Sleep Output Characteristic

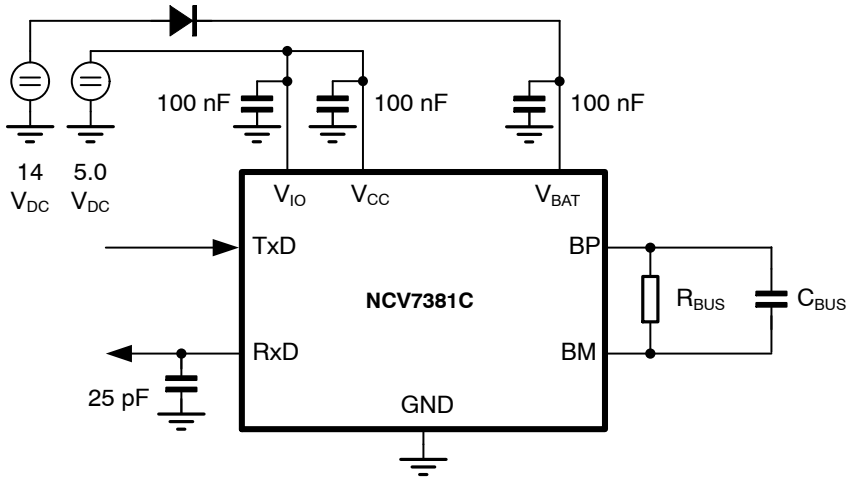


Figure 17. Test Setup for Dynamic Characteristics

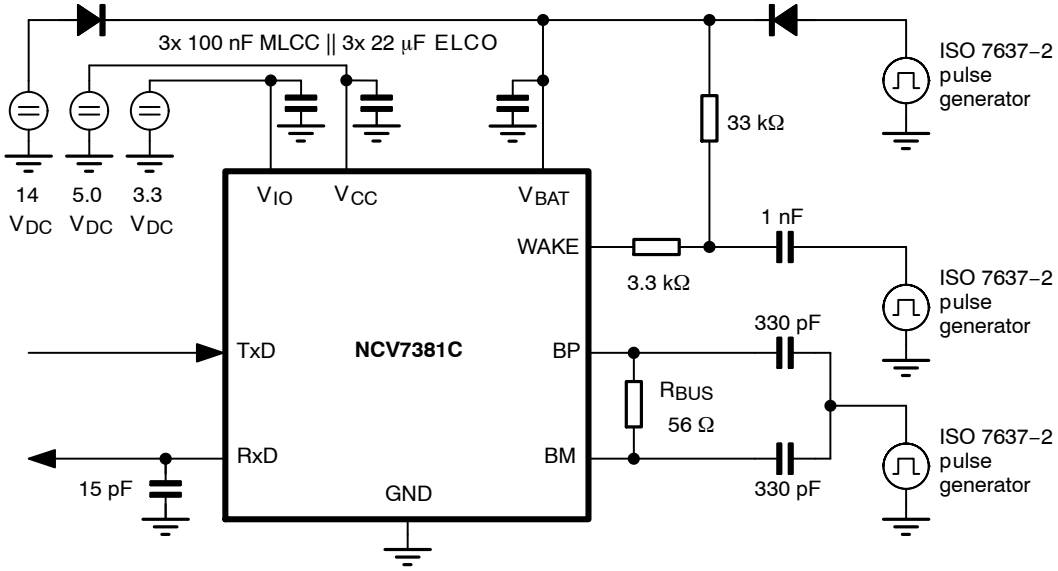


Figure 18. Test Setup for Measuring the Transient Immunity

ORDERING INFORMATION

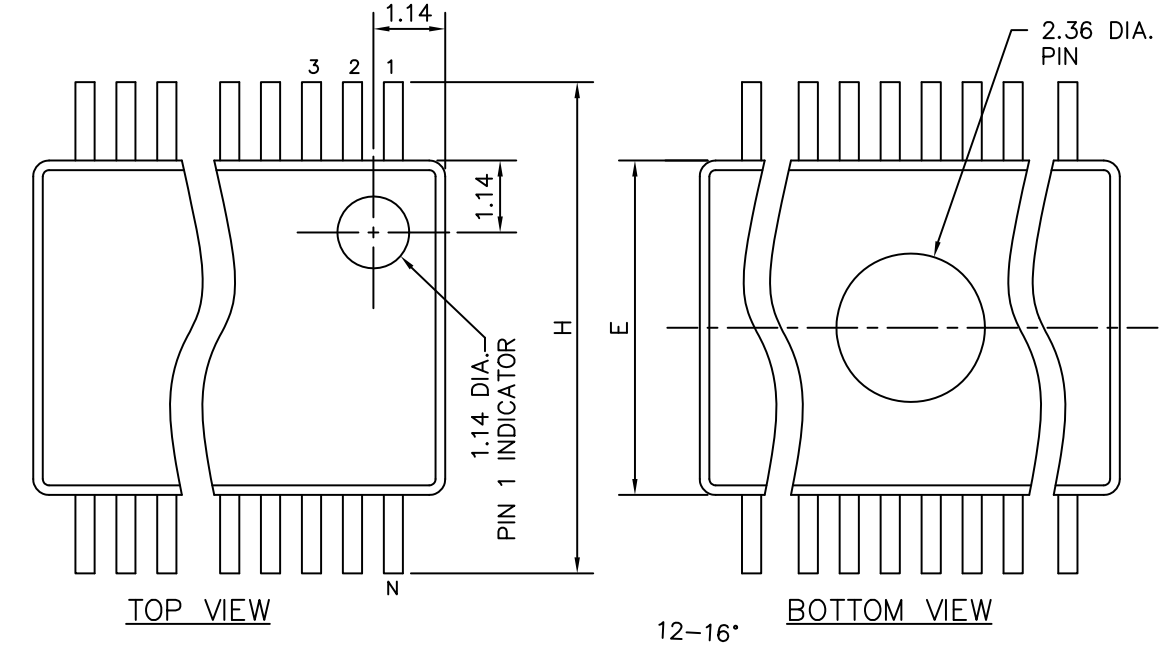
Part Number	Description	Package	Container†	
			Type	Quantity
NCV7381CDP0R2G	FlexRay Transceiver, Clamp 30, High Temperature	SSOP 16 GREEN	Tape & Reel	2000

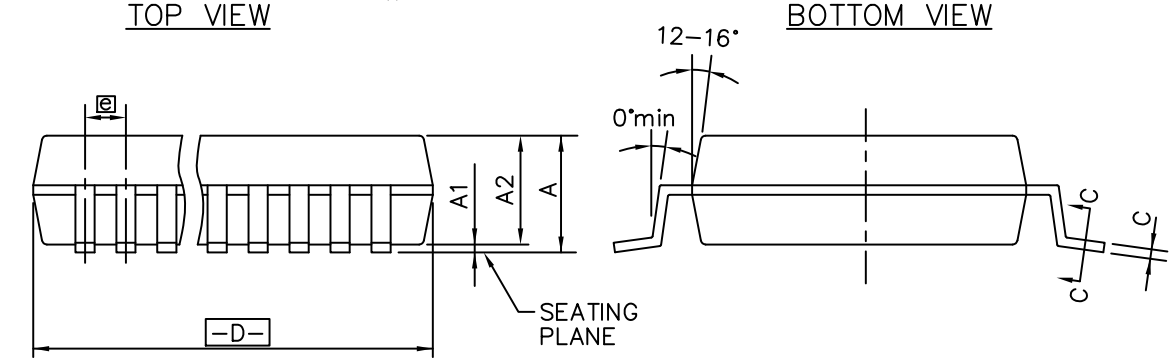
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FlexRay is a trademark of ASML Netherlands B.V.

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DATE 19 SEP 2008





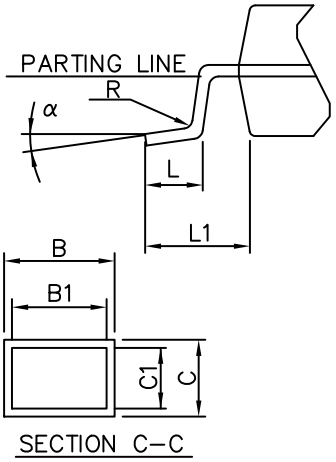


TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS			NOTE	NOTE VARIATIONS	1 D			2 N
	MIN.	NOM.	MAX.			MIN.	NOM.	MAX.	
A	1.73	1.86	1.99			2.87	3.00	3.13	8
A_1	0.05	0.13	0.21		AA	6.07	6.20	6.33	14
A_2	1.68	1.73	1.78		AB	6.07	6.20	6.33	16
B	0.25	–	0.38		AC	7.07	7.20	7.33	20
B1	0.25	0.30	0.33		AD	8.07	8.20	8.33	24
C	0.09	–	0.20		AE	10.07	10.20	10.33	28
C1	0.09	0.15	0.16		AF	10.07	10.20	10.33	30
D	SEE VARIATIONS			1					
E	5.20	5.30	5.38						
e	0.65 BSC								
H	7.65	7.80	7.90						
L	0.63	0.75	0.95						
L1	1.25 REF.								
N	SEE VARIATIONS			2					
α	0°	4°	8°						
R	0.09	0.15	–						

NOTE:
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.20mm on D PER SIDE.

ISSUE	REVISION	DATE
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