# NSBC115TPDP6

# Complementary Bias Resistor Transistors R1 = 100 kΩ, R2 = ∞ kΩ

## NPN and PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base−emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

### Features

- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS

($T_A$ = 25°C both polarities Q1 (PNP) and Q2 (NPN), unless otherwise noted)

| Rating | Symbol | Max | Unit |
|---|---|---|---|
| Collector−Base Voltage | $V_{CBO}$ | 50 | Vdc |
| Collector−Emitter Voltage | $V_{CEO}$ | 50 | Vdc |
| Collector Current − Continuous | $I_C$ | 100 | mAdc |
| Input Forward Voltage | $V_{IN(fwd)}$ | 40 | Vdc |
| Input Reverse Voltage<br>−NPN<br>−PNP | $V_{IN(rev)}$ | <br>6<br>5 | Vdc |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### ORDERING INFORMATION

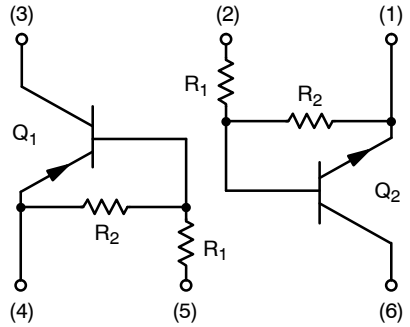
| Device | Package | Shipping† |
|---|---|---|
| NSBC115TPDP6T5G | SOT−963 | 8,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

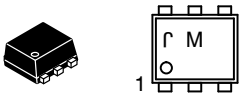
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### PIN CONNECTIONS




### MARKING DIAGRAMS




**SOT−963**
**CASE 527AD**

J = Specific Device Code
M = Date Code*

*Date Code orientation may vary depending upon manufacturing location.

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## THERMAL CHARACTERISTICS

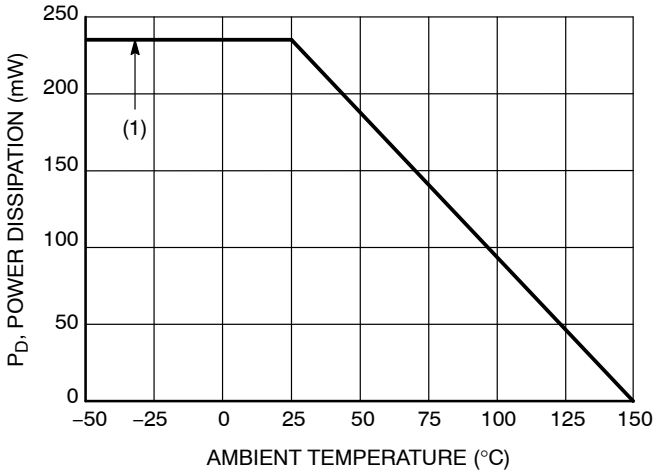
| Characteristic | Symbol | Max | Unit |
|---|---|---|---|
| **NSBC115TPDP6 (SOT−963) One Junction Heated** | | | |
| Total Device Dissipation<br>$T_A$ = 25°C (Note 1)<br>(Note 2)<br>Derate above 25°C (Note 1)<br>(Note 2) | $P_D$ | <br>231<br>269<br>1.9<br>2.2 | <br>mW<br><br>mW/°C |
| Thermal Resistance, (Note 1)<br>Junction to Ambient (Note 2) | $R_{\theta JA}$ | 540<br>464 | °C/W |
| **NSBC115TPDP6 (SOT−963) Both Junction Heated** (Note 3) | | | |
| Total Device Dissipation<br>$T_A$ = 25°C (Note 1)<br>(Note 2)<br>Derate above 25°C (Note 1)<br>(Note 2) | $P_D$ | <br>339<br>408<br>2.7<br>3.3 | <br>mW<br><br>mW/°C |
| Thermal Resistance, (Note 1)<br>Junction to Ambient (Note 2) | $R_{\theta JA}$ | 369<br>306 | °C/W |
| Junction and Storage Temperature Range | $T_J$, $T_{stg}$ | −55 to +150 | °C |

1. FR−4 @ 100 $mm^2$, 1 oz. copper traces, still air.
2. FR−4 @ 500 $mm^2$, 1 oz. copper traces, still air.
3. Both junction heated values assume total power is sum of two equally powered channels.

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C both polarities $Q_1$ (PNP) and $Q_2$ (NPN), unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Collector−Base Cutoff Current ($V_{CB}$ = 50 V, $I_E$ = 0) | $I_{CBO}$ | – | – | 100 | nAdc |
| Collector−Emitter Cutoff Current ($V_{CE}$ = 50 V, $I_B$ = 0) | $I_{CEO}$ | – | – | 500 | nAdc |
| Emitter−Base Cutoff Current ($V_{EB}$ = 6.0 V, $I_C$ = 0) | $I_{EBO}$ | – | – | 0.1 | mAdc |
| Collector−Base Breakdown Voltage ($I_C$ = 10 μA, $I_E$ = 0) | $V_{(BR)CBO}$ | 50 | – | – | Vdc |
| Collector−Emitter Breakdown Voltage (Note 4) ($I_C$ = 2.0 mA, $I_B$ = 0) | $V_{(BR)CEO}$ | 50 | – | – | Vdc |
| **ON CHARACTERISTICS** | | | | | |
| DC Current Gain (Note 4) ($I_C$ = 5.0 mA, $V_{CE}$ = 10 V) | $h_{FE}$ | 160 | 350 | – | |
| Collector−Emitter Saturation Voltage (Note 4) ($I_C$ = 10 mA, $I_B$ = 1.0 mA) | $V_{CE(sat)}$ | – | – | 0.25 | Vdc |
| Input Voltage (off) ($V_{CE}$ = 5.0 V, $I_C$ = 100 μA) (NPN)<br>($V_{CE}$ = 5.0 V, $I_C$ = 100 μA) (PNP) | $V_{i(off)}$ | –<br>– | 0.6<br>0.62 | –<br>– | Vdc |
| Input Voltage (on) ($V_{CE}$ = 0.2 V, $I_C$ = 1.0 mA) (NPN)<br>($V_{CE}$ = 0.2 V, $I_C$ = 1.0 mA) (PNP) | $V_{i(on)}$ | –<br>– | 1.0<br>1.0 | –<br>– | Vdc |
| Output Voltage (on) ($V_{CC}$ = 5.0 V, $V_B$ = 3.5 V, $R_L$ = 1.0 kΩ) | $V_{OL}$ | – | – | 0.2 | Vdc |
| Output Voltage (off) ($V_{CC}$ = 5.0 V, $V_B$ = 0.25 V, $R_L$ = 1.0 kΩ) | $V_{OH}$ | 4.9 | – | – | Vdc |
| Input Resistor | R1 | 70 | 100 | 130 | kΩ |
| Resistor Ratio | $R_1/R_2$ | – | – | – | |

4. Pulsed Condition: Pulse Width = 300 msec, Duty Cycle ≤ 2%.




(1) SOT−963; 100 mm$^2$, 1 oz. copper trace

**Figure 1. Derating Curve**

## TYPICAL CHARACTERISTICS – NPN TRANSISTOR
## NSBC115TPDP6

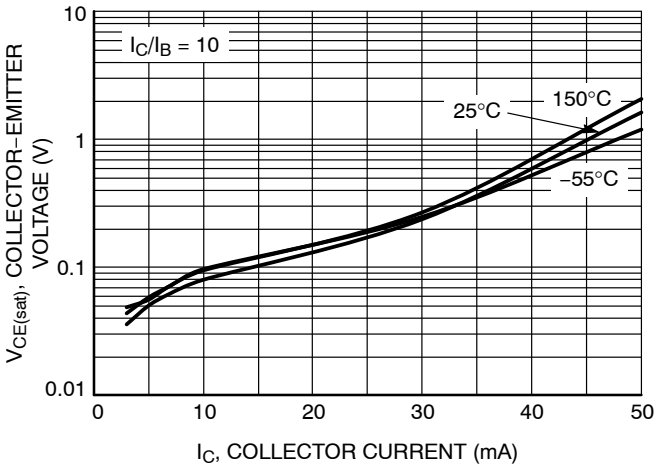



**Figure 2. $V_{CE(sat)}$ vs. $I_C$**

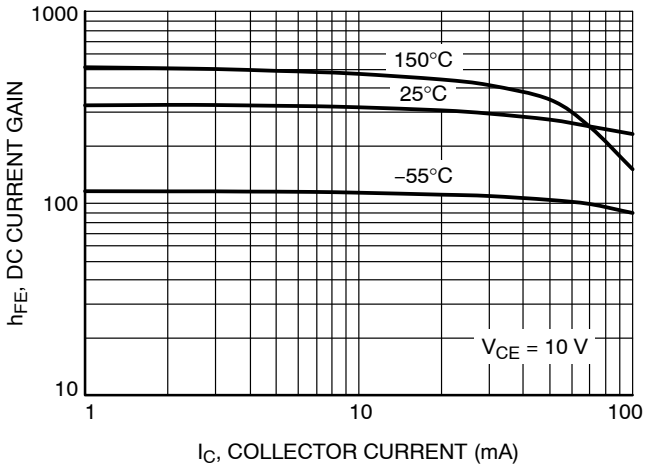



**Figure 3. DC Current Gain**

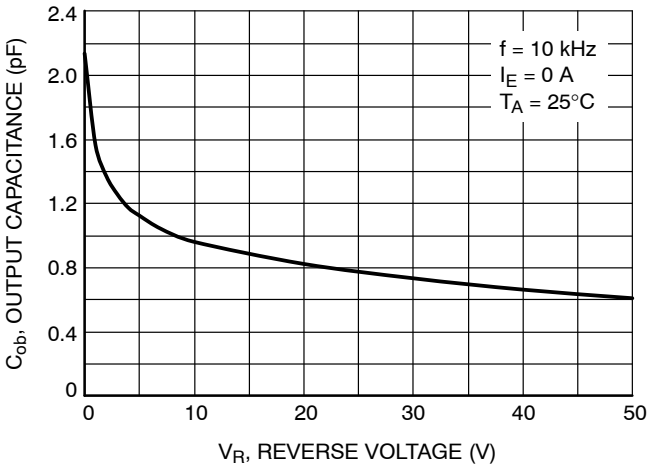



**Figure 4. Output Capacitance**

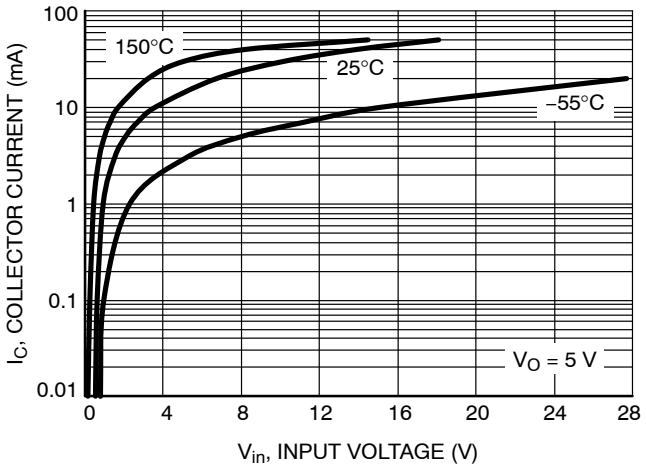



**Figure 5. Output Current vs. Input Voltage**

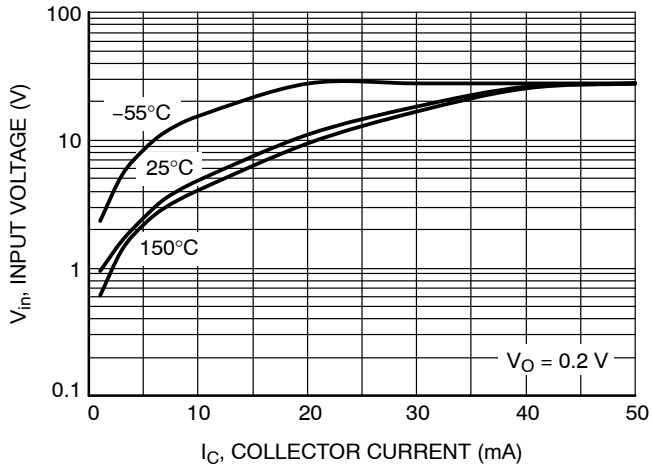



**Figure 6. Input Voltage vs. Output Current**

## TYPICAL CHARACTERISTICS – PNP TRANSISTOR
## NSBC115TPDP6

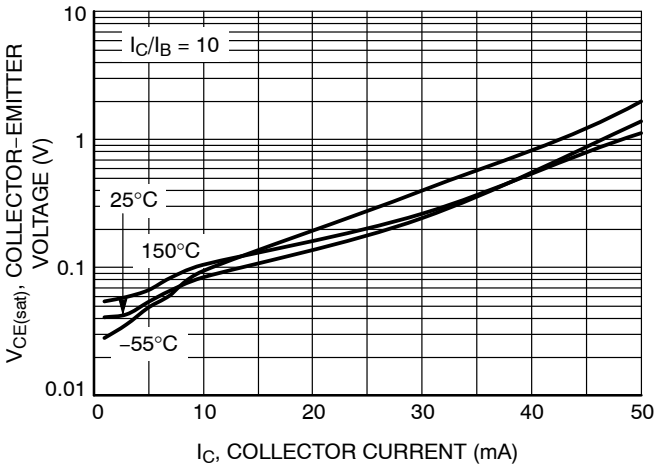



**Figure 7. $V_{CE(sat)}$ vs. $I_C$**

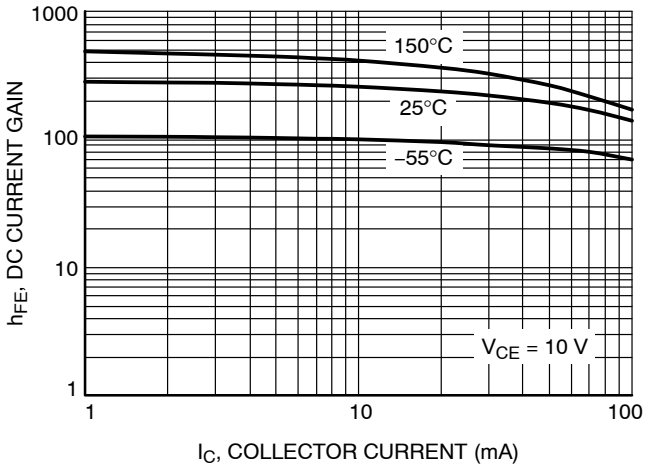



**Figure 8. DC Current Gain**

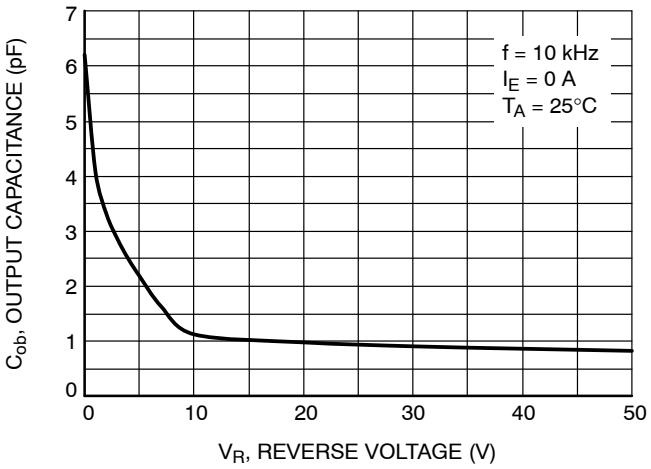



**Figure 9. Output Capacitance**

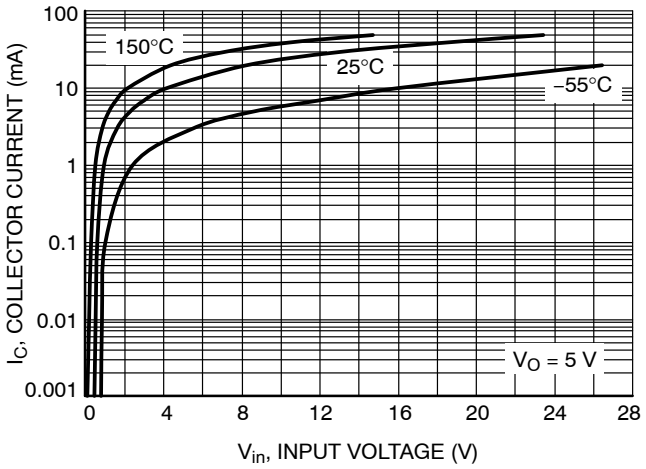



**Figure 10. Output Current vs. Input Voltage**

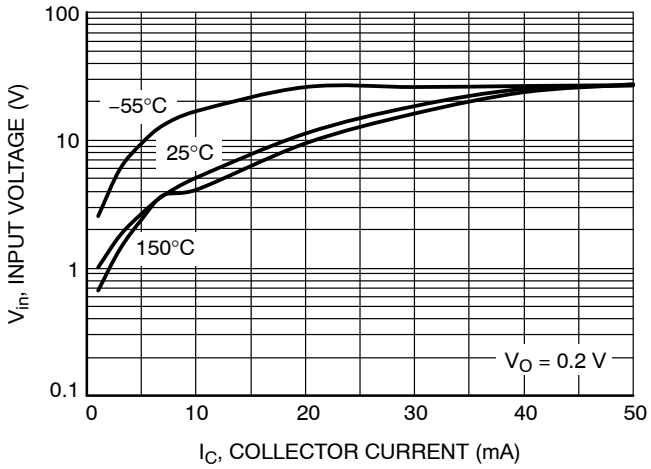
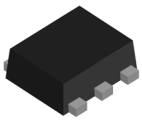



**Figure 11. Input Voltage vs. Output Current**

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

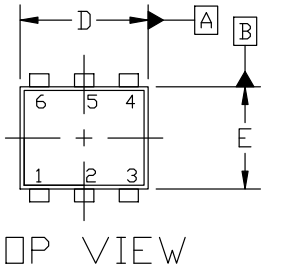


**SOT−963 1.00x1.00x0.37, 0.35P**
CASE 527AD
ISSUE F

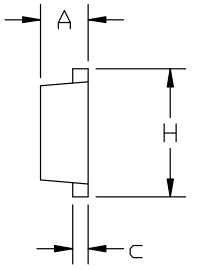
DATE 20 FEB 2024

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

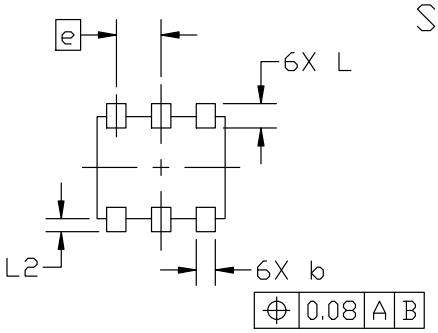
| | MILLIMETERS | | |
|---|---|---|---|
| DIM | MIN. | NOM. | MAX. |
| A | 0.34 | 0.37 | 0.40 |
| b | 0.10 | 0.15 | 0.20 |
| c | 0.07 | 0.12 | 0.17 |
| D | 0.95 | 1.00 | 1.05 |
| E | 0.75 | 0.80 | 0.85 |
| e | 0.35 BSC | | |
| H | 0.95 | 1.00 | 1.05 |
| L | 0.19 REF | | |
| L2 | 0.05 | 0.10 | 0.15 |



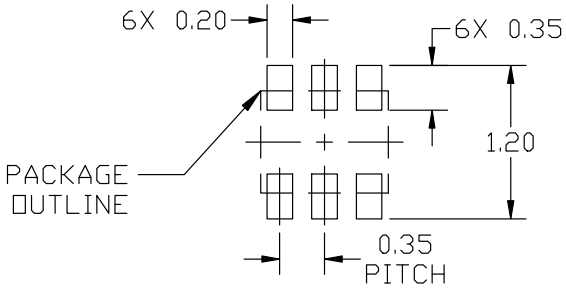

TOP VIEW




SIDE VIEW




BOTTOM VIEW




RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

STYLE 1:
PIN 1. EMITTER 1
2. BASE 1
3. COLLECTOR 2
4. EMITTER 2
5. BASE 2
6. COLLECTOR 1

STYLE 2:
PIN 1. EMITTER 1
2. EMITTER2
3. BASE 2
4. COLLECTOR 2
5. BASE 1
6. COLLECTOR 1

STYLE 3:
PIN 1. CATHODE 1
2. CATHODE 1
3. ANODE/ANODE 2
4. CATHODE 2
5. CATHODE 2
6. ANODE/ANODE 1

STYLE 4:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. CATHODE
3. ANODE
4. ANODE
5. CATHODE
6. CATHODE

STYLE 6:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

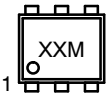
STYLE 7:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. ANODE
6. CATHODE

STYLE 8:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 9:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 10:
PIN 1. CATHODE 1
2. N/C
3. CATHODE 2
4. ANODE 2
5. N/C
6. ANODE 1

**GENERIC MARKING DIAGRAM***




XX = Specific Device Code
M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| DOCUMENT NUMBER: | 98AON26456D | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
|---|---|---|
| DESCRIPTION: | SOT−963 1.00x1.00x0.37, 0.35P | PAGE 1 OF 1 |

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