# NTB25P06, NVB25P06

# MOSFET – P-Channel, D²PAK
## -60 V, -27.5 A

Designed for low voltage, high speed switching applications and to withstand high energy in the avalanche and commutation modes.

### Features
- AEC Q101 Qualified – NVB25P06
- These Devices are Pb–Free and are RoHS Compliant

### Typical Applications
- PWM Motor Controls
- Power Supplies
- Converters
- Bridge Circuits

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Drain–to–Source Voltage | $V_{DSS}$ | –60 | V |
| Gate–to–Source Voltage<br>– Continuous<br>– Non–Repetitive ($t_p \le 10$ ms) | <br>$V_{GS}$<br>$V_{GSM}$ | <br>±15<br>±20 | <br>V<br>Vpk |
| Drain Current<br>– Continuous @ $T_A$ = 25°C<br>– Single Pulse ($t_p \le 10$ μs) | <br>$I_D$<br>$I_{DM}$ | <br>27.5<br>80 | <br>A<br>Apk |
| Total Power Dissipation @ $T_A$ = 25°C | $P_D$ | 120 | W |
| Operating and Storage Temperature Range | $T_J$, $T_{stg}$ | –55 to +175 | °C |
| Single Pulse Drain–to–Source Avalanche Energy – Starting $T_J$ = 25°C ($V_{DD}$ = 25 V, $V_{GS}$ = 10 V, $I_{L(pk)}$ = 20 A, L = 3 mH, $R_G$ = 25 Ω) | $E_{AS}$ | 600 | mJ |
| Thermal Resistance<br>– Junction–to–Case<br>– Junction–to–Ambient (Note 1)<br>– Junction–to–Ambient (Note 2) | <br>$R_{\theta JC}$<br>$R_{\theta JA}$<br>$R_{\theta JA}$ | <br>1.25<br>46.8<br>63.2 | °C/W |
| Maximum Lead Temperature for Soldering Purposes, (1/8″ from case for 10 s) | $T_L$ | 260 | °C |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

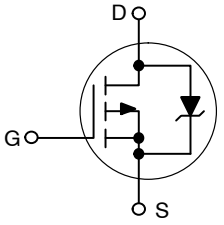
1. When surface mounted to an FR4 board using 1″ pad size (Cu Area 1.127 in²).
2. When surface mounted to an FR4 board using the minimum recommended pad size (Cu Area 0.412 in²).

**ON Semiconductor®**

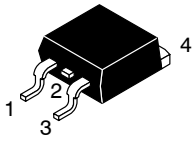
**http://onsemi.com**

| $V_{(BR)DSS}$ | $R_{DS(on)}$ TYP | $I_D$ MAX |
|---|---|---|
| –60 V | 65 mΩ @ –10 V | –27.5 A |

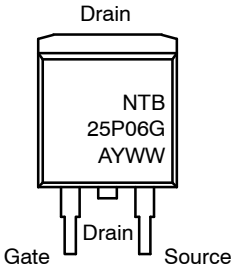
**P–Channel**




**MARKING DIAGRAM & PIN ASSIGNMENT**




**D²PAK**
**CASE 418B**




| | |
|---|---|
| A | = Assembly Location |
| Y | = Year |
| WW | = Work Week |
| G | = Pb–Free Package |

**ORDERING INFORMATION**

| Device | Package | Shipping† |
|---|---|---|
| NTB25P06T4G | D²PAK (Pb–Free) | 800 / Tape & Reel |
| NVB25P06T4G | D²PAK (Pb–Free) | 800 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

© Semiconductor Components Industries, LLC, 2011

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| Drain−to−Source Breakdown Voltage (Note 3)<br>($V_{GS}$ = 0 V, $I_D$ = −250 μA)<br>(Positive Temperature Coefficient) | | $V_{(BR)DSS}$ | <br>−60<br>− | <br>−<br>64 | <br>−<br>− | V<br><br>mV/°C |
| Zero Gate Voltage Drain Current<br>($V_{GS}$ = 0 V, $V_{DS}$ = −60 V, $T_J$ = 25°C)<br>($V_{GS}$ = 0 V, $V_{DS}$ = −60 V, , $T_J$ = 150°C) | | $I_{DSS}$ | <br>−<br>− | <br>−<br>− | <br>−10<br>−100 | μA |
| Gate−Body Leakage Current ($V_{GS}$ = ±15 V, $V_{DS}$ = 0 V) | | $I_{GSS}$ | − | − | ±100 | nA |
| **ON CHARACTERISTICS** (Note 3) | | | | | | |
| Gate Threshold Voltage<br>($V_{DS}$ = $V_{GS}$, $I_D$ = −250 μA)<br>(Negative Threshold Temperature Coefficient) | | $V_{GS(th)}$ | <br>−2.0<br>− | <br>−2.8<br>6.2 | <br>−4.0<br>− | V<br><br>mV/°C |
| Static Drain−Source On−State Resistance<br>($V_{GS}$ = −10 V, $I_D$ = −12.5 A)<br>($V_{GS}$ = −10 V, $I_D$ = −25 A) | | $R_{DS(on)}$ | <br>−<br>− | <br>0.065<br>0.070 | <br>0.075<br>0.082 | Ω |
| Forward Transconductance<br>($V_{DS}$ = −10 V, $I_D$ = −12.5 A) | | gFS | <br>− | <br>13 | <br>− | Mhos |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Input Capacitance | ($V_{DS}$ = −25 V, $V_{GS}$ = 0 V, F = 1.0 MHz) | $C_{iss}$ | − | 1200 | 1680 | pF |
| Output Capacitance | | $C_{oss}$ | − | 345 | 480 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | − | 90 | 180 | |
| **SWITCHING CHARACTERISTICS** (Notes 3 & 4) | | | | | | |
| Turn−On Delay Time | ($V_{DD}$ = −30 V, $I_D$ = −25 A, $V_{GS}$ = −10 V $R_G$ = 9.1 Ω) | $t_{d(on)}$ | − | 14 | 24 | ns |
| Rise Time | | $t_r$ | − | 72 | 118 | ns |
| Turn−Off Delay Time | | $t_{d(off)}$ | − | 43 | 68 | ns |
| Fall Time | | $t_f$ | − | 190 | 320 | ns |
| Gate Charge | ($V_{DS}$ = −48 V, $I_D$ = −25 A, $V_{GS}$ = −10 V) | $Q_T$ | − | 33 | 50 | nC |
| | | $Q_1$ | − | 6.5 | − | |
| | | $Q_2$ | − | 15 | − | |
| **BODY−DRAIN DIODE RATINGS** (Note 3) | | | | | | |
| Diode Forward On−Voltage | ($I_S$ = −25 A, $V_{GS}$ = 0 V)<br>($I_S$ = −25 A, $V_{GS}$ = 0 V, $T_J$ = 150°C) | $V_{SD}$ | <br>− | <br>−1.8<br>−1.4 | <br>−2.5<br>− | V |
| Reverse Recovery Time | ($I_S$ = −25 A, $V_{GS}$ = 0 V, $dI_S/dt$ = 100 A/μs) | $t_{rr}$ | − | 70 | − | ns |
| | | $t_a$ | − | 50 | − | |
| | | $t_b$ | − | 20 | − | |
| Reverse Recovery Stored Charge | | $Q_{RR}$ | − | 0.2 | − | μC |

3. Indicates Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

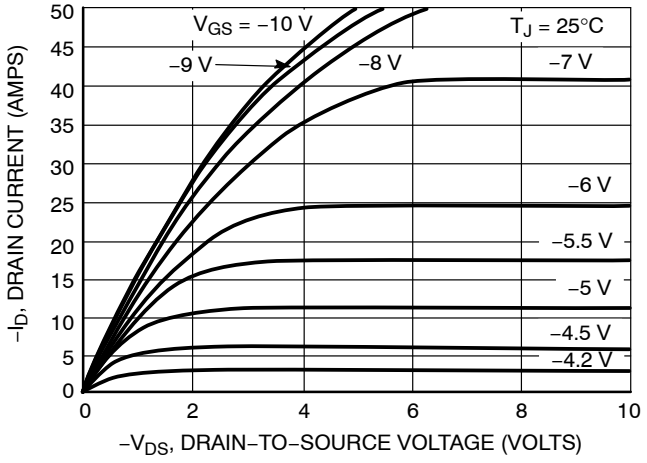



**Figure 1. On−Region Characteristics**

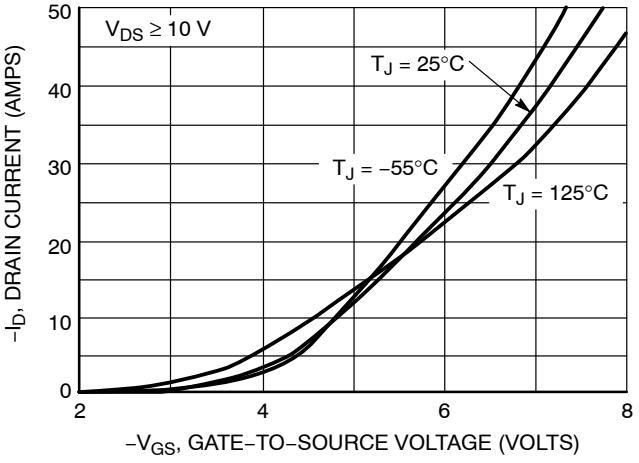



**Figure 2. Transfer Characteristics**

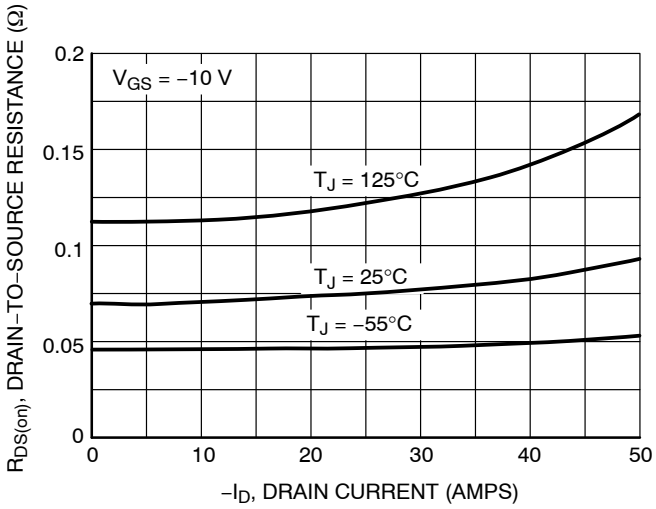



**Figure 3. On−Resistance vs. Drain Current and Temperature**

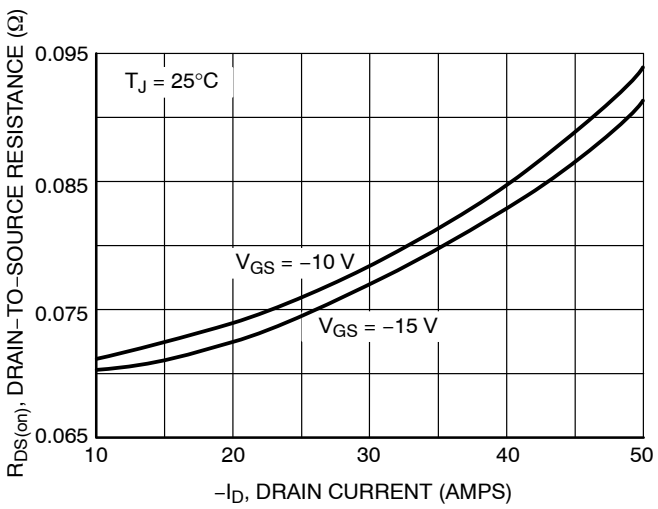



**Figure 4. On−Resistance vs. Drain Current and Gate Voltage**

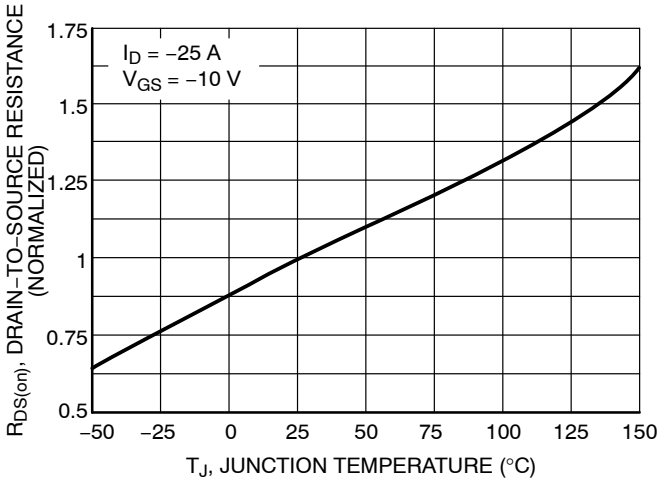



**Figure 5. On−Resistance Variation with Temperature**

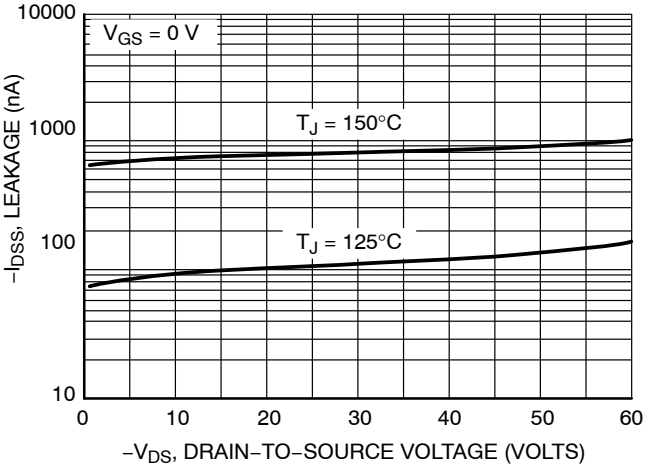



**Figure 6. Drain−to−Source Leakage Current vs. Voltage**

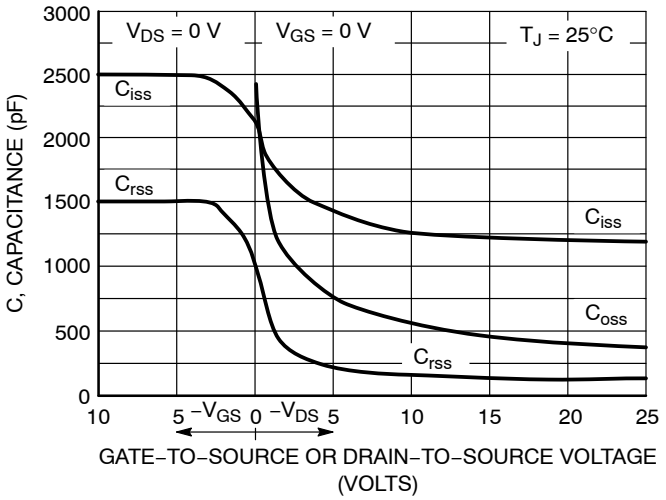



**Figure 7. Capacitance Variation**

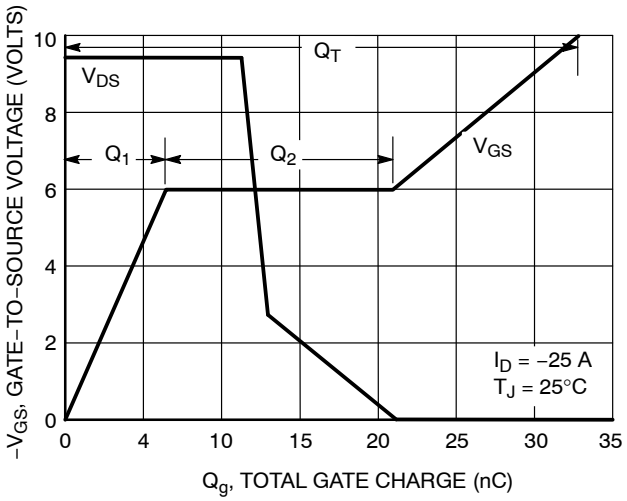



**Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge**

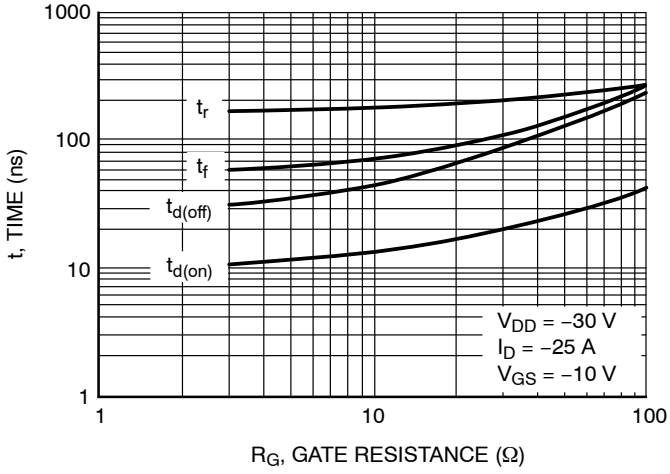



**Figure 9. Resistive Switching Time Variation vs. Gate Resistance**

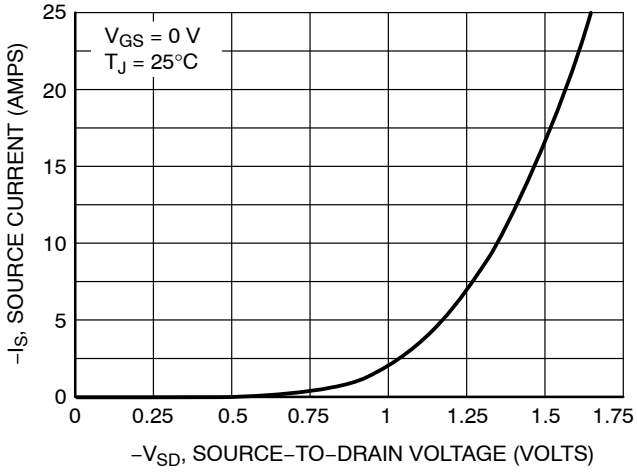



**Figure 10. Diode Forward Voltage vs. Current**

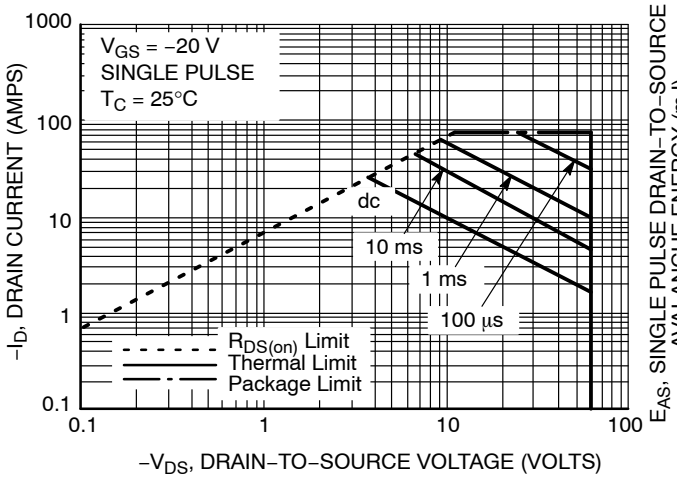



**Figure 11. Maximum Rated Forward Biased Safe Operating Area**

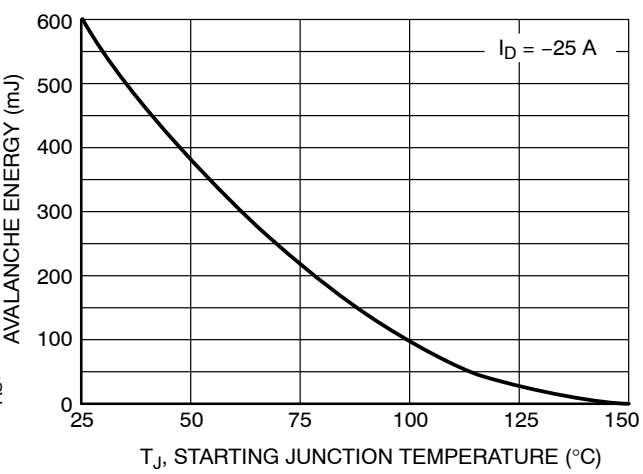
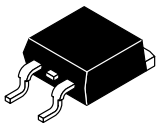


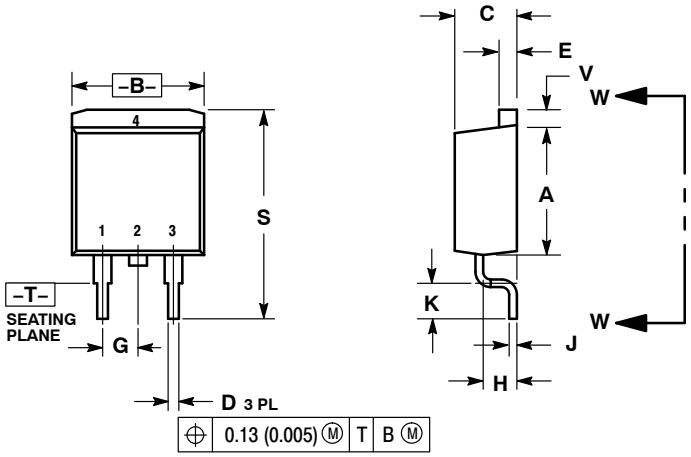

**Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature**



**D²PAK 3**
CASE 418B–04
ISSUE L

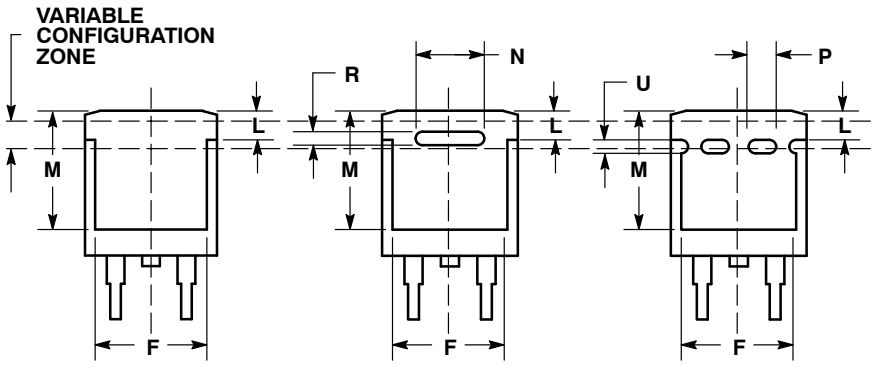
DATE 17 FEB 2015

**SCALE 1:1**




NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B–01 THRU 418B–03 OBSOLETE, NEW STANDARD 418B–04.

| | INCHES | | MILLIMETERS | |
|---|---|---|---|---|
| DIM | MIN | MAX | MIN | MAX |
| A | 0.340 | 0.380 | 8.64 | 9.65 |
| B | 0.380 | 0.405 | 9.65 | 10.29 |
| C | 0.160 | 0.190 | 4.06 | 4.83 |
| D | 0.020 | 0.035 | 0.51 | 0.89 |
| E | 0.045 | 0.055 | 1.14 | 1.40 |
| F | 0.310 | 0.350 | 7.87 | 8.89 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.080 | 0.110 | 2.03 | 2.79 |
| J | 0.018 | 0.025 | 0.46 | 0.64 |
| K | 0.090 | 0.110 | 2.29 | 2.79 |
| L | 0.052 | 0.072 | 1.32 | 1.83 |
| M | 0.280 | 0.320 | 7.11 | 8.13 |
| N | 0.197 REF | | 5.00 REF | |
| P | 0.079 REF | | 2.00 REF | |
| R | 0.039 REF | | 0.99 REF | |
| S | 0.575 | 0.625 | 14.60 | 15.88 |
| V | 0.045 | 0.055 | 1.14 | 1.40 |




VIEW W–W 1 | VIEW W–W 2 | VIEW W–W 3

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE

STYLE 4:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 5:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE

STYLE 6:
PIN 1. NO CONNECT
2. CATHODE
3. ANODE
4. CATHODE


**MARKING INFORMATION AND FOOTPRINT ON PAGE 2**





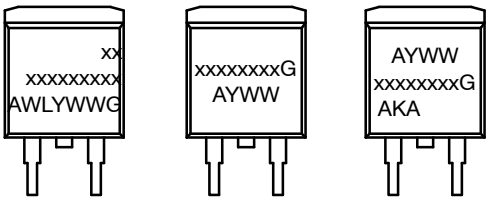
ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

**D²PAK 3**
CASE 418B−04
ISSUE L

DATE 17 FEB 2015

**GENERIC**
**MARKING DIAGRAM***

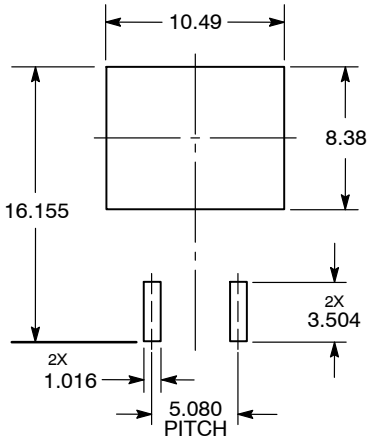



**IC** **Standard** **Rectifier**

| | |
|---|---|
| xx | = Specific Device Code |
| A | = Assembly Location |
| WL | = Wafer Lot |
| Y | = Year |
| WW | = Work Week |
| G | = Pb−Free Package |
| AKA | = Polarity Indicator |

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

**SOLDERING FOOTPRINT***




DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98ASB42761B** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| **DESCRIPTION:** | **D²PAK 3** | | **PAGE 2 OF 2** |

ON Semiconductor and ON are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

© Semiconductor Components Industries, LLC, 2019

**onsemi**, , and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent−Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as−is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales