NTJD3158C

Power MOSFET
20 V, +0.63/−0.82 A, SC−88 Complementary, ESD Protected

ON Semiconductor®

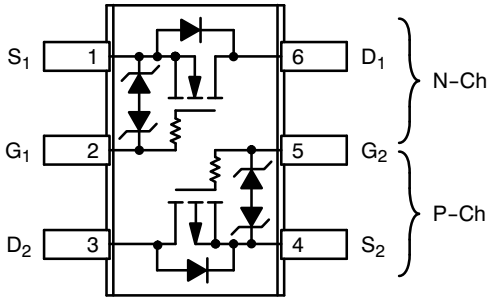
http://onsemi.com

Features
- Complementary N− and P−Channel MOSFET
- Small Size Dual SC−88 Package
- Reduced Gate Charge to Improve Switching Response
- Independently Connected Devices to Provide Design Flexibility
- This is a Pb−Free Device

Applications
- DC−DC Conversion Circuits
- Load/Power Switching with Level Shift

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max
N−Ch 20 V	375 mΩ @ 4.5 V	0.63 A
	445 mΩ @ 2.5 V	
P−Ch −20 V	300 mΩ @ −4.5 V	−0.82 A
	500 mΩ @ −2.5 V	

SC−88 (SOT−363)
(6−Leads)



(Top View)

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	20	V
Gate−to−Source Voltage			V_{GS}	±12	V
N−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	0.63	A
		T_A = 85°C		0.46	
	t ≤ 5 s	T_A = 25°C		0.72	
P−Channel Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	−0.82	A
		T_A = 85°C		−0.59	
	t ≤ 5 s	T_A = 25°C		−0.93	
Power Dissipation (Note 1)	Steady State	T_A = 25°C	P_D	0.27	W
	t ≤ 5 s			0.35	
Pulsed Drain Current	N−Ch	tp = 10 μs	I_{DM}	1.3	A
	P−Ch			−1.6	
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to 150	°C
Source Current (Body Diode)			I_S	0.46	A
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	460	°C/W
Junction−to−Ambient − t ≤ 5 s (Note 1)	$R_{\theta JA}$	357	
Junction−to−Lead (Drain) − Steady State (Note 1)	$R_{\theta JL}$	226	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

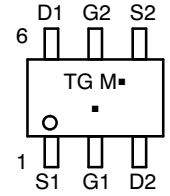
1. Surface mounted on FR4 board using 1 in sq pad size (Cu area = 1.127 in sq [1 oz] including traces).

MARKING DIAGRAM & PIN ASSIGNMENT



1

SC−88 (SOT−363)
CASE 419B
STYLE 26



TG = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NTJD3158CT1G	SC−88 (Pb−Free)	3000/Tape & Reel
NTJD3158CT4G	SC−88 (Pb−Free)	10000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	N/P	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS (Note 3)								
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	N	V_{GS} = 0 V	I_D = 250 μA	20			V
		P		I_D = −250 μA	−20			
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$					22		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	N	V_{GS} = 0 V, V_{DS} = 16 V				1.0	μA
		P	V_{GS} = 0 V, V_{DS} = −16 V				1.0	
Gate−to−Source Leakage Current	I_{GSS}	N	V_{DS} = 0 V, V_{GS} = ±12 V				±10	μA
		P	V_{DS} = 0 V, V_{GS} = ±4.5 V				±1.0	
		P	V_{DS} = 0 V, V_{GS} = ±12 V			6.0		
ON CHARACTERISTICS (Note 2)								
Gate Threshold Voltage	$V_{GS(TH)}$	N	I_D = 250 μA		0.6		1.5	V
		P	I_D = −250 μA		−0.45			
Drain−to−Source On Resistance	$R_{DS(on)}$	N	V_{GS} = 4.5 V, I_D = 0.63 A			290	375	mΩ
		P	V_{GS} = −4.5 V, I_D = −0.88 A			255	300	
		N	V_{GS} = 2.5 V, I_D = 0.40 A			360	445	
		P	V_{GS} = −2.5 V, I_D = −0.71 A			345	500	
Forward Transconductance	g_{FS}	N	V_{DS} = 4.0 V, I_D = 0.63 A			2.0		S
		P	V_{DS} = −10 V, I_D = −0.88 A			3.0		
CHARGES, CAPACITANCES AND GATE RESISTANCE								
Input Capacitance	C_{ISS}	N	f = 1 MHz, V_{GS} = 0 V	V_{DS} = 20 V		33	46	pF
		P		V_{DS} = −20 V		155		
Output Capacitance	C_{OSS}	N		V_{DS} = 20 V		13	22	
		P		V_{DS} = −20 V		25		
Reverse Transfer Capacitance	C_{RSS}	N		V_{DS} = 20 V		2.8	5.0	
		P		V_{DS} = −20 V		18		
Total Gate Charge	$Q_{G(TOT)}$	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 0.63 A			1.3	3.0	nC
		P	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −0.88 A			2.2		
Gate−to−Source Charge	Q_{GS}	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 0.63 A			0.2		
		P	V_{GS} = −4.5 V, V_{DS} = −15 V, I_D = −0.88 A			0.5		
Gate−to−Drain Charge	Q_{GD}	N	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 0.63 A			0.4		
		P	V_{GS} = −4.5 V, V_{DS} = −10 V, I_D = −0.88 A			0.65		
SWITCHING CHARACTERISTICS (Note 3)								
Turn−On Delay Time	$t_{d(ON)}$	N	V_{GS} = 4.5 V, V_{DD} = 10 V, I_D = 0.5 A, R_G = 20 Ω			83		ns
Rise Time	t_r					227		
Turn−Off Delay Time	$t_{d(OFF)}$					786		
Fall Time	t_f					506		
Turn−On Delay Time	$t_{d(ON)}$	P	V_{GS} = −4.5 V, V_{DD} = −10 V, I_D = −0.5 A, R_G = 20 Ω			5.8		
Rise Time	t_r					6.5		
Turn−Off Delay Time	$t_{d(OFF)}$					13.5		
Fall Time	t_f					3.5		
DRAIN−SOURCE DIODE CHARACTERISTICS								
Forward Diode Voltage	V_{SD}	N	V_{GS} = 0 V, T_J = 25°C	I_S = 0.23 A		0.76	1.1	V
		P		I_S = −0.48 A		−0.8	−1.2	
		N	V_{GS} = 0 V, T_J = 125°C	I_S = 0.23 A		0.63		
		P		I_S = −0.48 A		−0.66		

2. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (N−Ch) (T_J = 25°C unless otherwise noted)

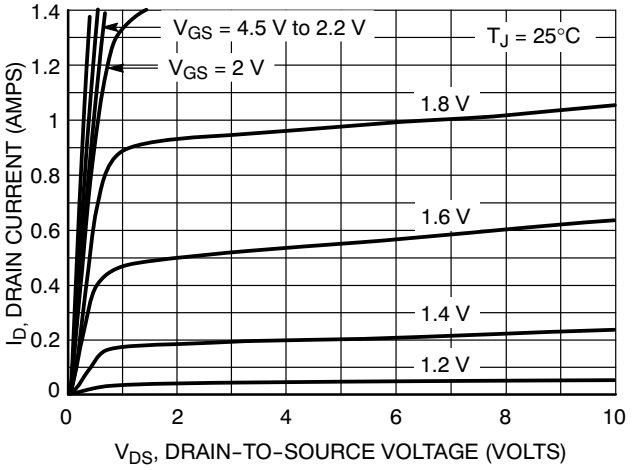


Figure 1. On−Region Characteristics

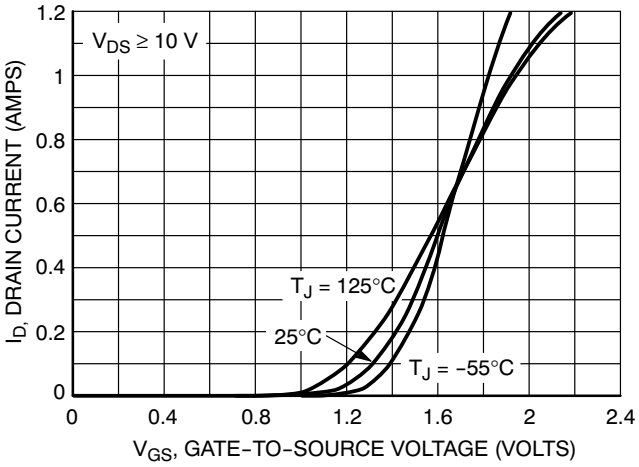


Figure 2. Transfer Characteristics

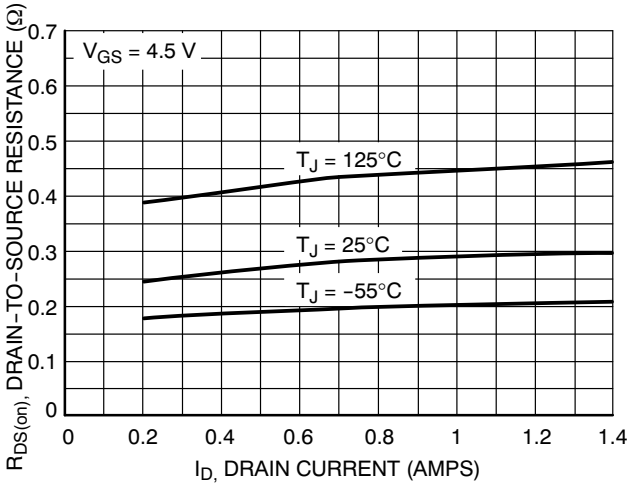


Figure 3. On−Resistance vs. Drain Current and Temperature

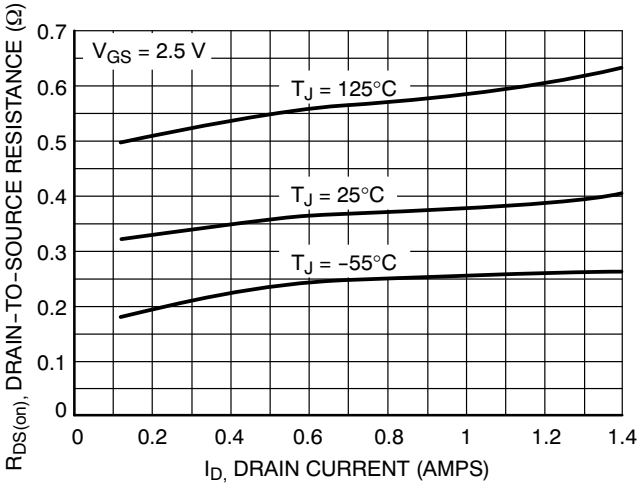


Figure 4. On−Resistance vs. Drain Current and Temperature

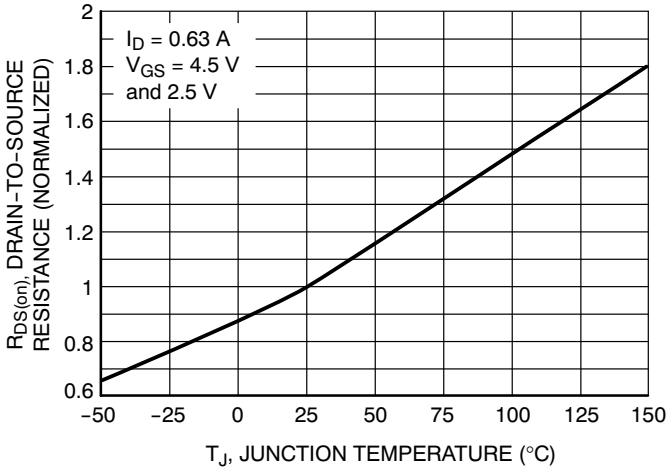


Figure 5. On−Resistance Variation with Temperature

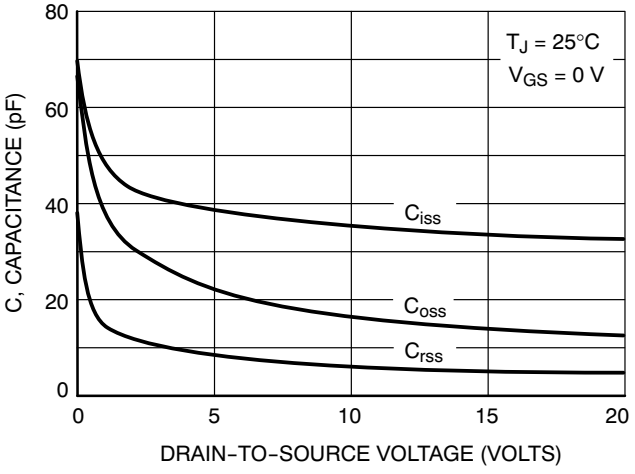


Figure 6. Capacitance Variation

TYPICAL PERFORMANCE CURVES (N−Ch) (T_J = 25°C unless otherwise noted)

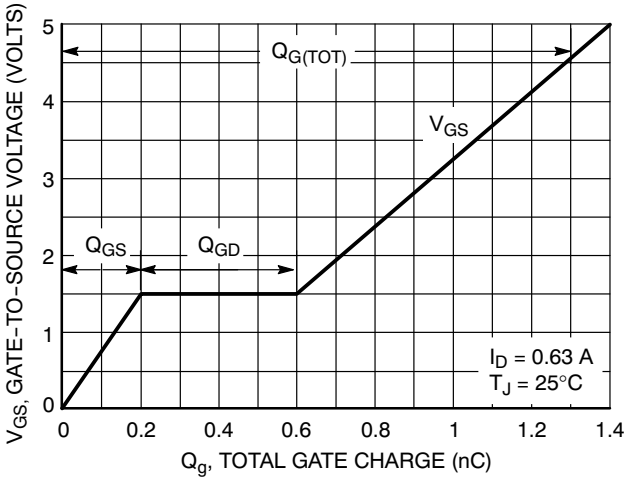


Figure 7. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

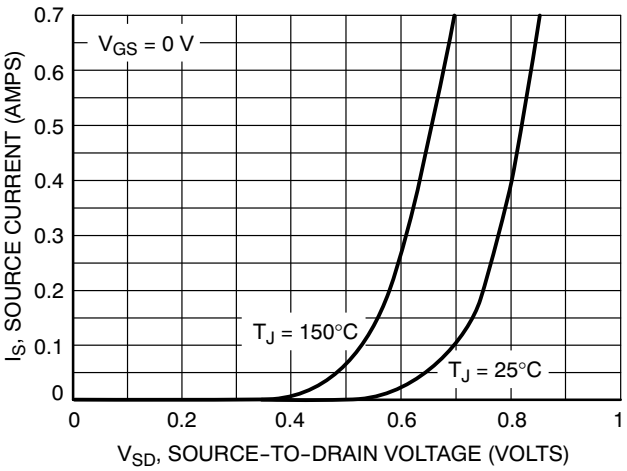


Figure 8. Diode Forward Voltage vs. Current

TYPICAL PERFORMANCE CURVES (P−Ch) (T_J = 25°C unless otherwise noted)

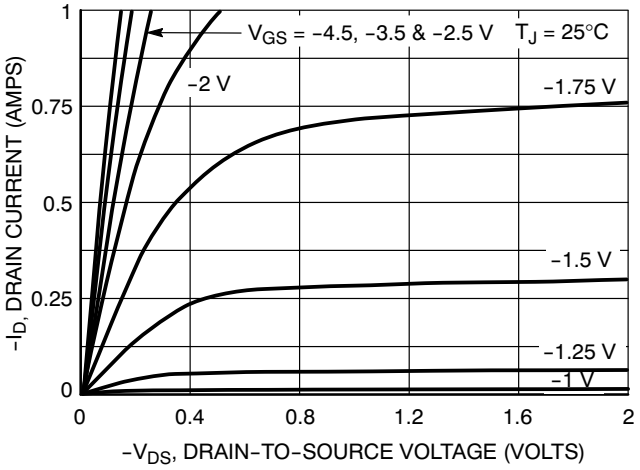


Figure 9. On−Region Characteristics

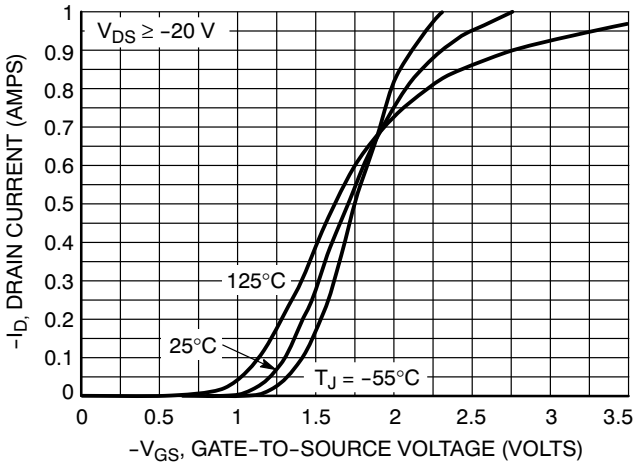


Figure 10. Transfer Characteristics

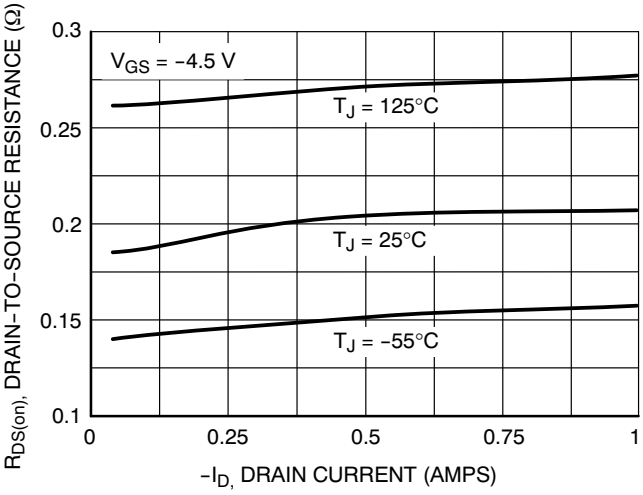


Figure 11. On−Resistance vs. Drain Current and Temperature

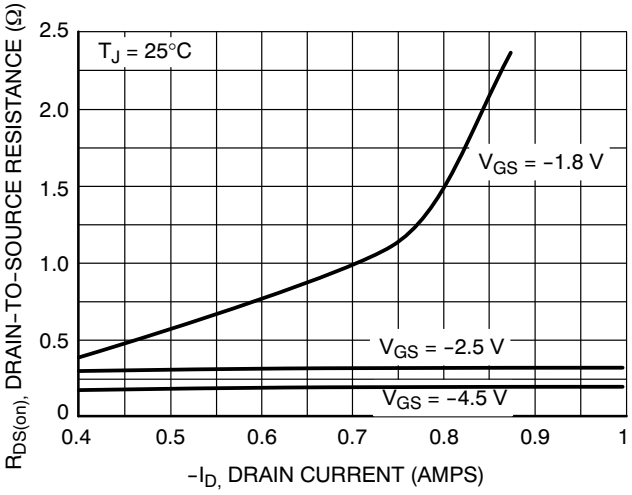


Figure 12. On−Resistance vs. Drain Current and Gate Voltage

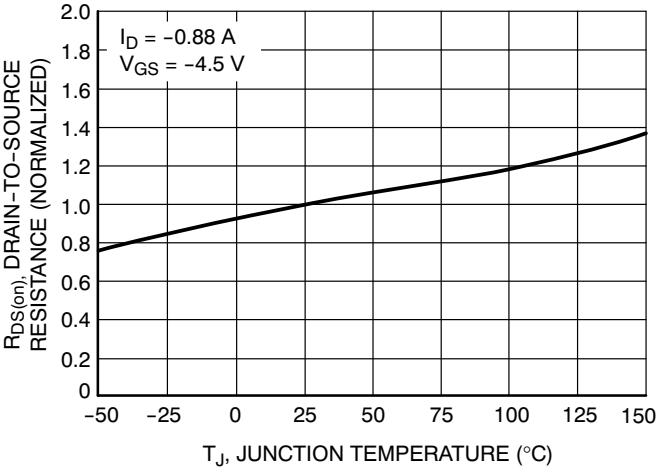


Figure 13. On−Resistance Variation with Temperature

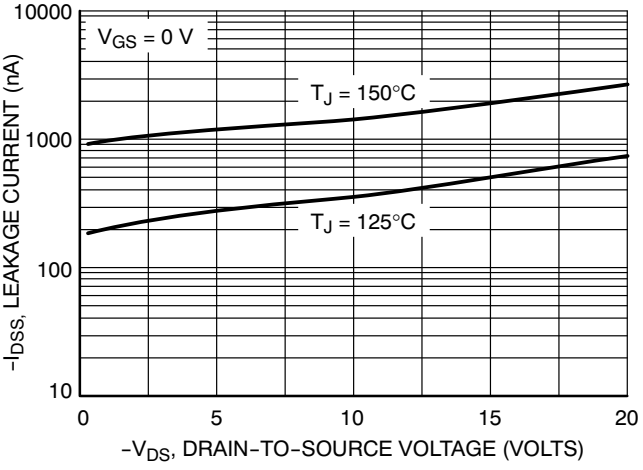


Figure 14. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES (P−Ch) (T_J = 25°C unless otherwise noted)

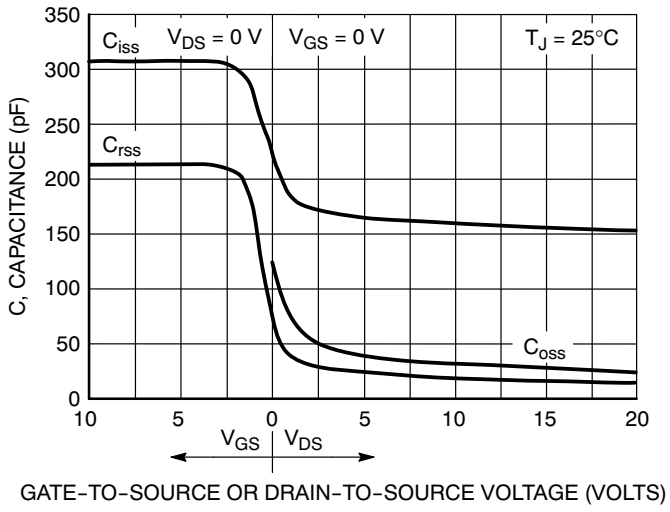


Figure 15. Capacitance Variation

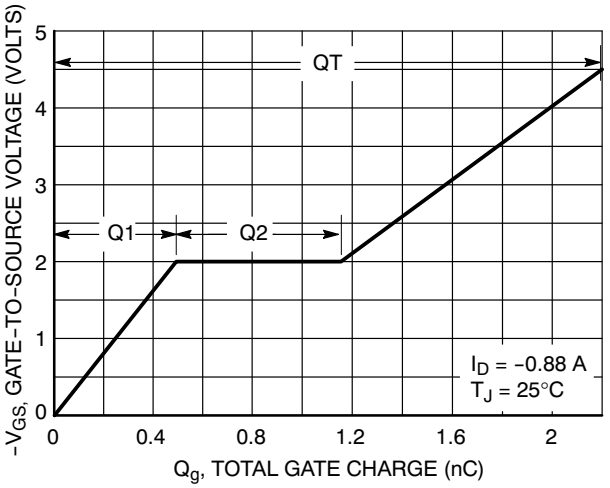


Figure 16. Gate−to−Source Voltage vs. Total Gate Charge

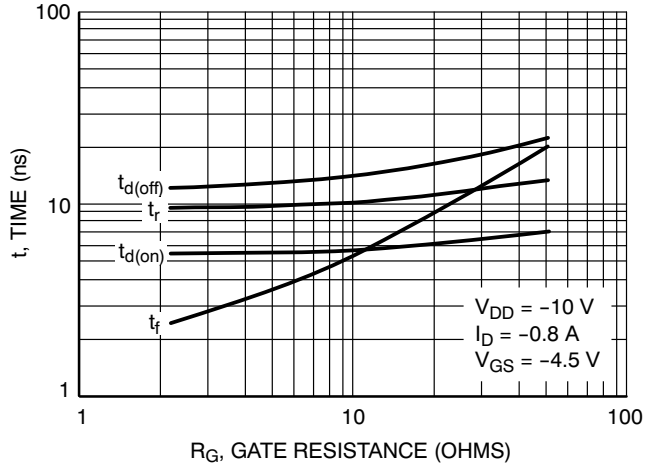


Figure 17. Resistive Switching Time Variation vs. Gate Resistance

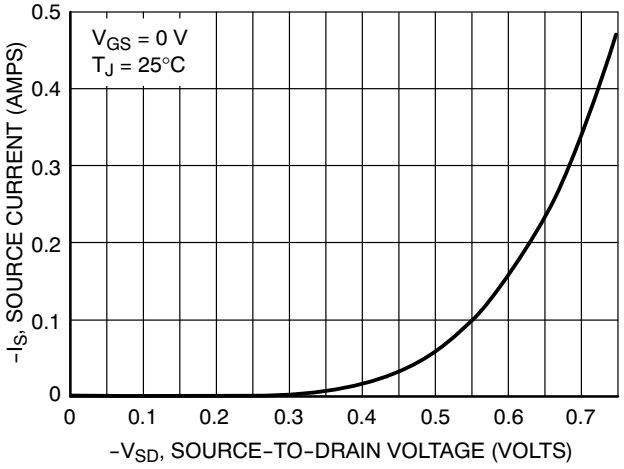
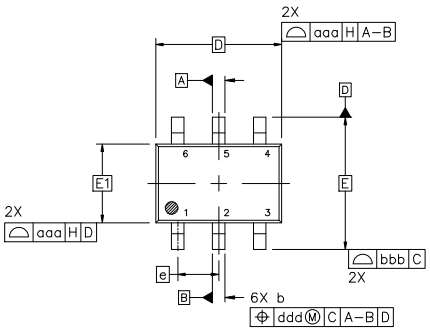


Figure 18. Diode Forward Voltage vs. Current

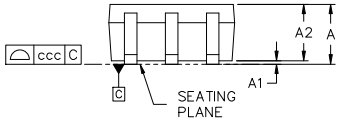


SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

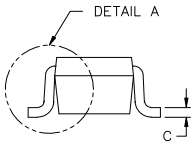
DATE 18 APR 2024



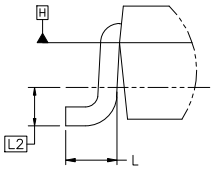
TOP VIEW



SIDE VIEW



END VIEW

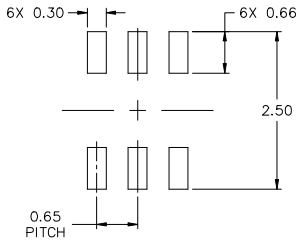


DETAIL A
SCALE 2:1

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER END.
4. DIMENSIONS D AND E1 AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AND DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.08 AND 0.15 FROM THE TIP.
7. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 TOTAL IN EXCESS OF DIMENSION b AT MAXIMUM MATERIAL CONDITION. THE DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.

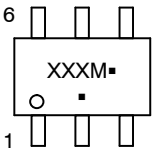
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	−−−	−−−	1.10
A1	0.00	−−−	0.10
A2	0.70	0.90	1.00
b	0.15	0.20	0.25
c	0.08	0.15	0.22
D	2.00 BSC		
E	2.10 BSC		
E1	1.25 BSC		
e	0.65 BSC		
L	0.26	0.36	0.46
L2	0.15 BSC		
aaa	0.15		
bbb	0.30		
ccc	0.10		
ddd	0.10		



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or position may vary depending upon manufacturing location.

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

STYLES ON PAGE 2

DOCUMENT NUMBER:	**98ASB42985B**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SC−88 2.00x1.25x0.90, 0.65P**		**PAGE 1 OF 2**

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SC−88 2.00x1.25x0.90, 0.65P
CASE 419B−02
ISSUE Z

DATE 18 APR 2024

STYLE 1:
PIN 1. EMITTER 2
2. BASE 2
3. COLLECTOR 1
4. EMITTER 1
5. BASE 1
6. COLLECTOR 2

STYLE 2:
CANCELLED

STYLE 3:
CANCELLED

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. COLLECTOR
4. EMITTER
5. BASE
6. ANODE

STYLE 5:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 6:
PIN 1. ANODE 2
2. N/C
3. CATHODE 1
4. ANODE 1
5. N/C
6. CATHODE 2

STYLE 7:
PIN 1. SOURCE 2
2. DRAIN 2
3. GATE 1
4. SOURCE 1
5. DRAIN 1
6. GATE 2

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. EMITTER 2
2. EMITTER 1
3. COLLECTOR 1
4. BASE 1
5. BASE 2
6. COLLECTOR 2

STYLE 10:
PIN 1. SOURCE 2
2. SOURCE 1
3. GATE 1
4. DRAIN 1
5. DRAIN 2
6. GATE 2

STYLE 11:
PIN 1. CATHODE 2
2. CATHODE 2
3. ANODE 1
4. CATHODE 1
5. CATHODE 1
6. ANODE 2

STYLE 12:
PIN 1. ANODE 2
2. ANODE 2
3. CATHODE 1
4. ANODE 1
5. ANODE 1
6. CATHODE 2

STYLE 13:
PIN 1. ANODE
2. N/C
3. COLLECTOR
4. EMITTER
5. BASE
6. CATHODE

STYLE 14:
PIN 1. VREF
2. GND
3. GND
4. IOUT
5. VEN
6. VCC

STYLE 15:
PIN 1. ANODE 1
2. ANODE 2
3. ANODE 3
4. CATHODE 3
5. CATHODE 2
6. CATHODE 1

STYLE 16:
PIN 1. BASE 1
2. EMITTER 2
3. COLLECTOR 2
4. BASE 2
5. EMITTER 1
6. COLLECTOR 1

STYLE 17:
PIN 1. BASE 1
2. EMITTER 1
3. COLLECTOR 2
4. BASE 2
5. EMITTER 2
6. COLLECTOR 1

STYLE 18:
PIN 1. VIN1
2. VCC
3. VOUT2
4. VIN2
5. GND
6. VOUT1

STYLE 19:
PIN 1. I OUT
2. GND
3. GND
4. V CC
5. V EN
6. V REF

STYLE 20:
PIN 1. COLLECTOR
2. COLLECTOR
3. BASE
4. EMITTER
5. COLLECTOR
6. COLLECTOR

STYLE 21:
PIN 1. ANODE 1
2. N/C
3. ANODE 2
4. CATHODE 2
5. N/C
6. CATHODE 1

STYLE 22:
PIN 1. D1 (i)
2. GND
3. D2 (i)
4. D2 (c)
5. VBUS
6. D1 (c)

STYLE 23:
PIN 1. Vn
2. CH1
3. Vp
4. N/C
5. CH2
6. N/C

STYLE 24:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. CATHODE
5. CATHODE
6. CATHODE

STYLE 25:
PIN 1. BASE 1
2. CATHODE
3. COLLECTOR 2
4. BASE 2
5. EMITTER
6. COLLECTOR 1

STYLE 26:
PIN 1. SOURCE 1
2. GATE 1
3. DRAIN 2
4. SOURCE 2
5. GATE 2
6. DRAIN 1

STYLE 27:
PIN 1. BASE 2
2. BASE 1
3. COLLECTOR 1
4. EMITTER 1
5. EMITTER 2
6. COLLECTOR 2

STYLE 28:
PIN 1. DRAIN
2. DRAIN
3. GATE
4. SOURCE
5. DRAIN
6. DRAIN

STYLE 29:
PIN 1. ANODE
2. ANODE
3. COLLECTOR
4. EMITTER
5. BASE/ANODE
6. CATHODE

STYLE 30:
PIN 1. SOURCE 1
2. DRAIN 2
3. DRAIN 2
4. SOURCE 2
5. GATE 1
6. DRAIN 1

Note: Please refer to datasheet for style callout. If style type is not called out in the datasheet refer to the device datasheet pinout or pin assignment.

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