NUS1204MN

Overvoltage Protection IC with Integrated MOSFET

This device represents a new level of safety and integration by combining the NCP304 overvoltage protection circuit (OVP) with a −12 V P−Channel power MOSFET. It is specifically designed to protect sensitive electronic circuitry from overvoltage transients and power supply faults. During such hazardous events, the IC quickly disconnects the input supply from the load, thus protecting the load before any damage can occur.

The OVP IC is optimized for applications using an external AC−DC adapter or a car accessory charger to power a portable product or recharge its internal batteries. It has a nominal overvoltage threshold of 4.725 V which makes it ideal for single cell Li−Ion as well as 3/4 cell NiCD/NiMH applications.

Features

- OvervoltageTurn−Off Time of Less Than 20 μs
- Accurate Voltage Threshold of 4.725 V, Nominal
- High Accuracy Undervoltage Threshold of 2.0%
- −12 V Integrated P−Channel Power MOSFET
- Low $R_{DS(on)}$ = 75 mΩ @ −4.725 V
- Low Profile 2.0 x 2.0 mm WDFN Package Suitable for Portable Applications
- Maximum Solder Reflow Temperature @ 260°C
- This device is manufactured with a Pb−Free external lead finish only.

Benefits

- Provide Battery Protection
- Integrated Solution Offers Cost and Space Savings
- Integrated Solution Improves System Reliability

Applications

- Portable Computers and PDAs
- Cell Phones and Handheld Products
- Digital Cameras

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MARKING DIAGRAM

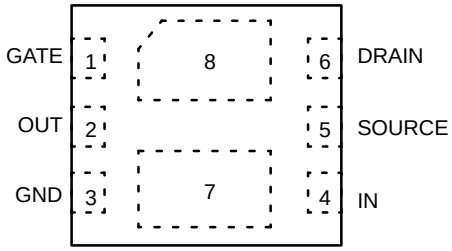


WDFN6
CASE 506AN



U2 = Specific Device Code
M = Date Code
▪ = Pb−Free Package

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

Device	Package	Shipping†
NUS1204MNT1G	WDFN6 (Pb−Free)	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Publication Order Number:
NUS1204MN/D

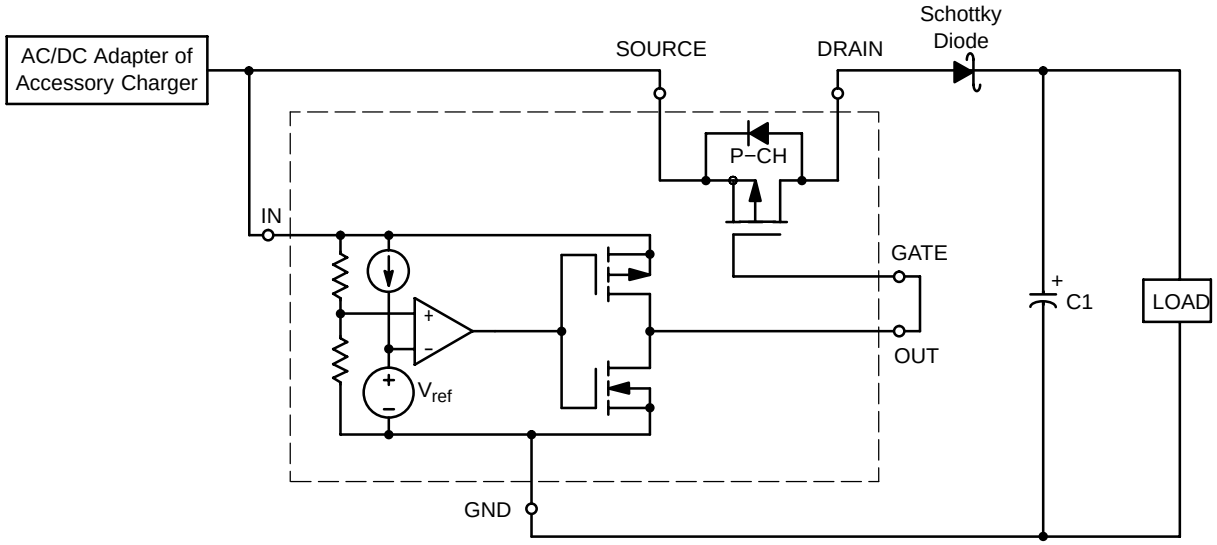


Figure 1. Simplified Schematic

PIN FUNCTION DESCRIPTIONS

Pin #	Symbol	Pin Description
1	GATE	Gate pin of the P−Channel Power MOSFET
2	OUT	This signal drives the gate of a P−channel Power MOSFET. It is controlled by the voltage level on the IN pin. When an overvoltage event is detected, the OUT pin is driven to within 1.0 V of V_{IN} in less than 20 μsec provided that gate and stray capacitance is less than 12 nF.
3, 7	GND	Circuit Ground
4	IN	This pin senses an external voltage point. If the voltage on this input rises above the overvoltage threshold (V_{TH}), the OUT pin will be driven to within 1.0 V of V_{IN}, thus disconnecting the P−Channel Power MOSFET. The nominal threshold level is 4.725 V and this threshold level can be increased with the addition of an external resistor between the IN pin and the adapter.
5	SOURCE	Source pin of the P−Channel Power MOSFET
6, 8	DRAIN	Drain pin of the P−Channel Power MOSFET

OVERVOLTAGE PROTECTION CIRCUIT TRUTH TABLE

IN	OUT
$<V_{th}$	GND
$>V_{th}$	V_{IN}

MAXIMUM RATINGS (T_A = 25°C unless otherwise stated)

Rating	Pin	Symbol	Min	Max	Unit
OUT Voltage to GND	2	V_O	−0.3	12	V
Input Pin Voltage to GND	4	V_{input}	−0.3	12	V
Maximum Power Dissipation (Note 1)	−	P_D	−	0.96	W
Thermal Resistance Junction−to−Air (Note 1) OVP IC P−Channel FET	−	$R_{\theta JA}$	−	130 130	°C/W
Junction Temperature	−	T_J	−	150	°C
Operating Ambient Temperature	−	T_A	−40	85	°C
Storage Temperature Range	−	T_{stg}	−65	150	°C
ESD Performance (HBM) (Note 2)	2,3,4	−	2.5	−	kV
Drain−to−Source Voltage		V_{DSS}		−12	V
Gate−to−Source Voltage		V_{GS}	−8	8	V
Continuous Drain Current, Steady State, T_A = 25°C (Note 1)		I_D		−0.6	A

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Surface−mounted on FR4 board using 1 inch sq pad size (Cu area = 1.127 in sq [1 oz] including traces).
2. Human body model (HBM): MIL STD 883C Method 3015−7, (R = 1500 Ω, C = 100 pF, F = 3 pulses delay 1 s).

ELECTRICAL CHARACTERISTICS (T_A= 25°C, Vcc = 6.0 V, unless otherwise specified)

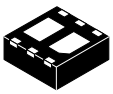
Characteristic	Symbol	Min	Typ	Max	Unit
Input Threshold (Pin 4, V_{in} Increasing)	V_{TH}	4.630	4.725	4.820	V
Input Threshold Hysteresis (Pin 4, V_{in} Decreasing)	V_{HYS}	0.135	0.225	0.315	V
Supply Current (Pin 4) (V_{in} = 4.34 V) (V_{in} = 6.5 V)	I_{in}	 − −	 − −	 3.0 3.9	μA
Minimum Operating Voltage (Pin 4) (Note 3) (T_A = 25°C) (T_A = −40°C to 85°C)	$V_{in(min)}$	 − −	 0.55 0.65	 0.70 0.80	V
Output Voltage High (V_{in} = 8.0 V; I_{Source} = 1.0 mA) Output Voltage High (V_{in} = 8.0 V; I_{Source} = 0.25 mA) Output Voltage High (V_{in} = 8.0 V; I_{Source} = 0 mA)	V_{oh}	V_{in}−1.0 V_{in}−0.25 V_{in}−0.1	−	−	V
Output Voltage Low (Input < 4.5 V; I_{Sink} = 0 mA; CNTRL = 0 V)	V_{ol}	−	−	0.1	V
Propagation Delay Input to Output Complementary Output NCP304 Series Output Transition, High to Low Output Transition, Low to High	 t_{pHL} t_{pLH}	 − −	 10 21	 − 60	μs

3. Guaranteed by design.

P−CHANNEL MOSFET (T_A= 25°C, unless otherwise specified)

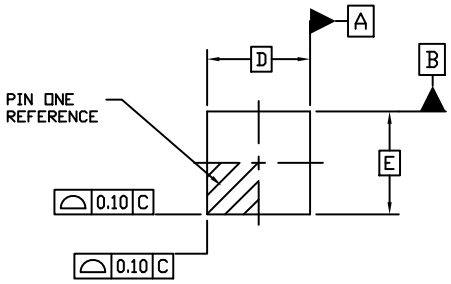
Parameter	Symbol	Min	Typ	Max	Units
Drain to Source On Resistance V_{GS} = −4.5 V, I_D = 600 mA V_{GS} = −4.5 V, I_D = 1.0 A	$R_{DS(on)}$		 75 75	 100 100	mΩ
Zero Gate Voltage Drain Current V_{GS} = −4.5 V, V_{GS} = 0 V, V_{DS} = −10 V	I_{DSS}			 −1.0	μA
Turn On Delay (Note 4) V_{GS} = −4.5 V	t_{on}		 5.5		ns
Turn Off Delay (Note 4) V_{GS} = −4.5 V	t_{off}		 20		ns
Input Capacitance V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = −10 V	C_{in}		 531		pF
Gate to Source Leakage Current V_{GS} = 8.0 V, V_{DS} = 0 V	I_{GSS}		 ±10		nA
Drain to Source Breakdown Voltage V_{GS} = 0 V, I_D = −250 μA	$V_{(BR)DSS}$	 −12			V
Gate Threshold Voltage V_{GS} = V_{DS}, I_D = −250 μA	$V_{(GS)th}$	 −0.4	 −0.7	 −1.0	V

4. Switching characteristics are independent of operating junction temperature.



WDFN6 2x2, 0.65P
CASE 506AN
ISSUE H

DATE 25 JAN 2022



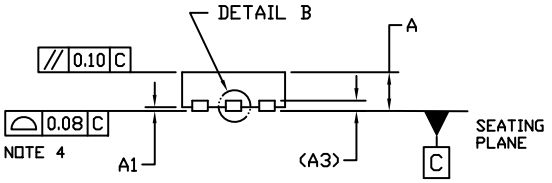
TOP VIEW



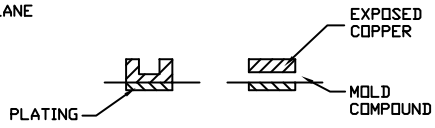
DETAIL A
OPTIONAL CONSTRUCTIONS

NOTES:

1. DIMENSIONING AND TOLERANCING PER. ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.

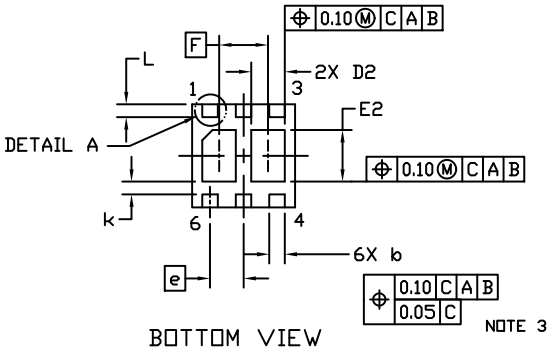


SIDE VIEW

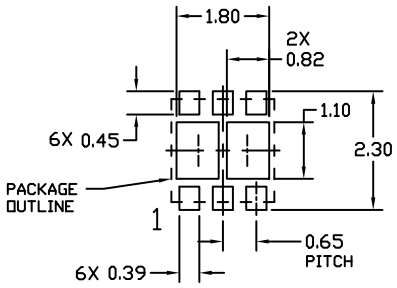


DETAIL B
OPTIONAL CONSTRUCTIONS

DIM	MILLIMETERS	
	MIN.	MAX.
A	0.70	0.80
A1	0.00	0.05
A3	0.20 REF	
b	0.25	0.35
D	2.00 BSC	
D2	0.57	0.77
E	2.00 BSC	
E2	0.90	1.10
e	0.65 BSC	
F	0.95 BSC	
k	0.25 REF	
L	0.20	0.30
L1	---	0.10



BOTTOM VIEW



RECOMMENDED
MOUNTING FOOTPRINT
SOLDERMASK DEFINED

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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