LNK562-564

LinkSwitch®-LP

Energy Efficient Off-Line Switcher IC for Linear Transformer Replacement

Product Highlights

Lowest System Cost and Advanced Safety Features

- Lowest component count switcher
- Very tight parameter tolerances using proprietary IC trimming technology and transformer construction techniques enable *Clampless*™ designs – decreases component count/system cost and increases efficiency
- Meets industry standard requirements for thermal overload protection – eliminates the thermal fuse used with linear transformers or additional components in RCC designs
- Frequency jittering greatly reduces EMI – enables low cost input filter configuration
- Meets HV creepage requirements between DRAIN and all other pins, both on the PCB and at the package
- Proprietary *E-Shield*™ transformer eliminates Y-capacitor

Superior Performance over Linear and RCC

- Hysteretic thermal shutdown protection – automatic recovery improves field reliability
- Universal input range allows worldwide operation
- Auto-restart reduces delivered power by >85% during short circuit and open loop fault conditions
- Simple ON/OFF control, no loop compensation needed
- High bandwidth provides fast turn on with no overshoot and excellent transient load response

EcoSmart® – Energy Efficiency Technology

- Easily meets all global energy efficiency regulations with no added components
- No-load consumption <150 mW at 265 VAC input
- ON/OFF control provides constant efficiency to very light loads – ideal for mandatory CEC regulations

Applications

- Chargers for cell/cordless phones, PDAs, power tools, MP3/portable audio devices, shavers etc.
- Standby and auxiliary supplies

Description

LinkSwitch-LP switcher ICs cost effectively replace all unregulated isolated linear transformer based (50/60 Hz) power supplies up to 3 W output power. For worldwide operation, a single universal input design replaces multiple linear transformer based designs. The self-biased circuit achieves an extremely low no-load consumption of under 150 mW. The internal oscillator frequency is jittered to significantly reduce both quasi-peak and average EMI, minimizing filter cost.

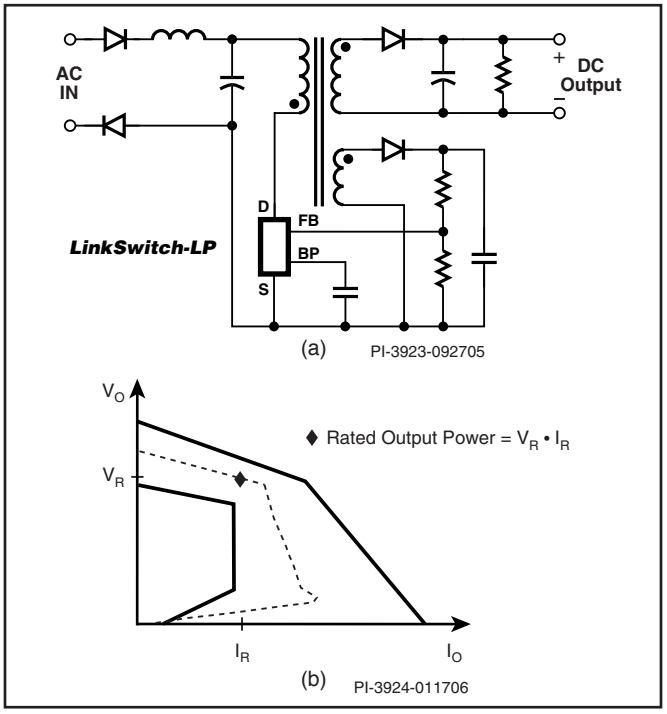


Figure 1. Typical Application – not a Simplified Circuit (a) and Output Characteristic Envelope (b).

OUTPUT POWER TABLE[1]				
PRODUCT[4]	230 VAC ±15%		85-265 VAC	
	Adapter[2]	Open Frame[3]	Adapter[2]	Open Frame[3]
LNK562P/G/D	1.9 W	1.9 W	1.9 W	1.9 W
LNK563P/G/D	2.5 W	2.5 W	2.5 W	2.5 W
LNK564P/G/D	3 W	3 W	3 W	3 W

Table 1. Output Power Table.

Notes:
1. Output power may be limited by specific application parameters including core size and Clampless operation (see Key Application Considerations).
2. Minimum continuous power in a typical non-ventilated enclosed adapter measured at 50 °C ambient.
3. Minimum practical continuous power in an open frame design with adequate heat sinking, measured at 50 °C ambient.
4. Packages: P: DIP-8B, G: SMD-8B, D: SO-8C. For lead-free package options, see Part Ordering Information.

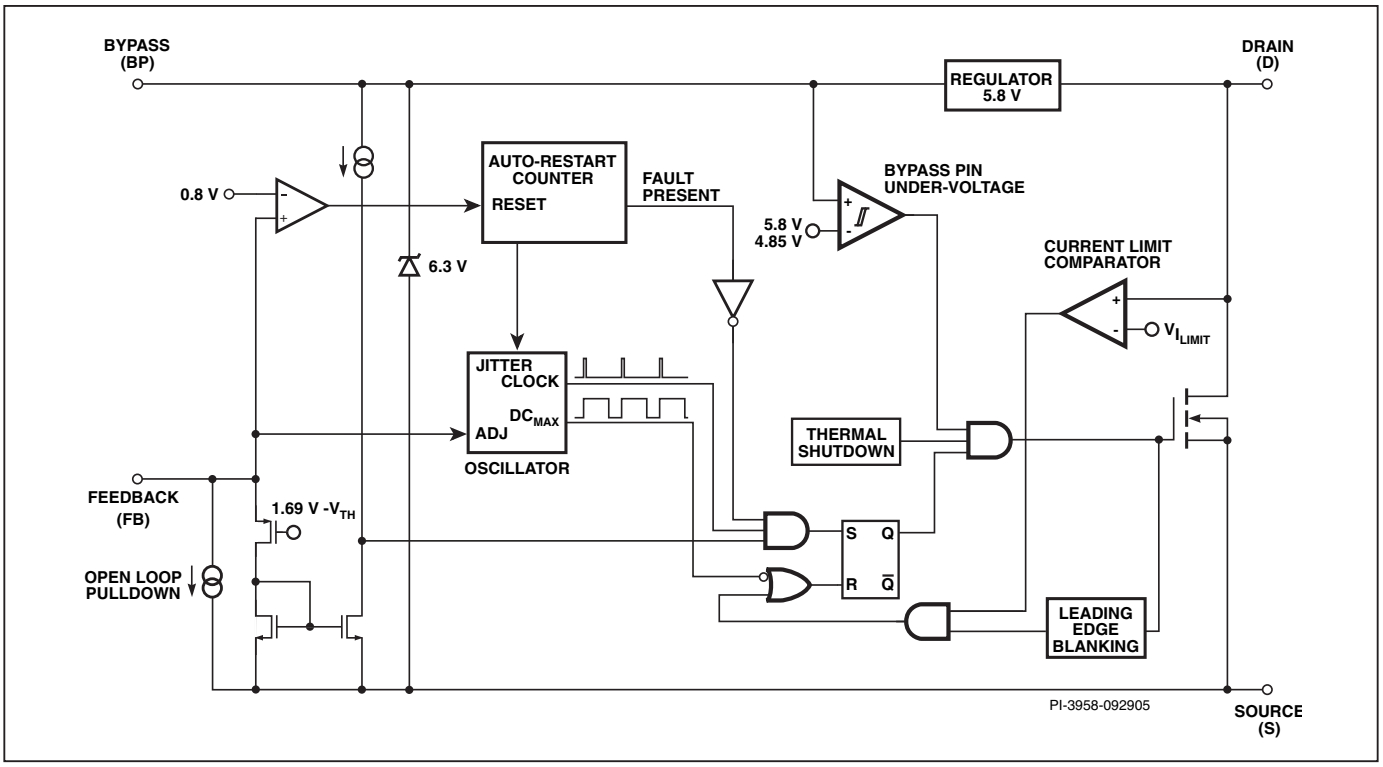


Figure 2. Functional Block Diagram.

Pin Functional Description

DRAIN (D) Pin:
The power MOSFET drain connection provides internal operating current for both startup and steady-state operation.

BYPASS (BP) Pin:
A 0.1 µF external bypass capacitor for the internally generated 5.8 V supply is connected to this pin.

FEEDBACK (FB) Pin:
During normal operation, switching of the power MOSFET is controlled by this pin. MOSFET switching is disabled when a current greater than 70 µA flows into this pin.

SOURCE (S) Pin:
This pin is the power MOSFET source connection. It is also the ground reference for the BYPASS and FEEDBACK pins.

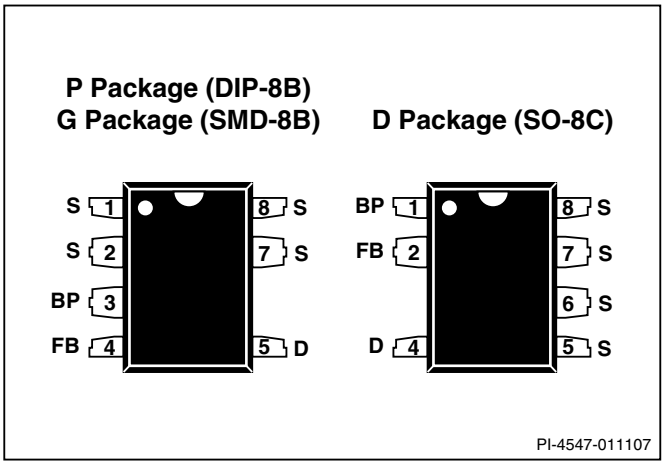


Figure 3. Pin Configuration.

LinkSwitch-LP Functional Description

LinkSwitch-LP comprises a 700 V power MOSFET switch with a power supply controller on the same die. Unlike conventional PWM (pulse width modulation) controllers, it uses a simple ON/OFF control to regulate the output voltage. The controller consists of an oscillator, feedback (sense and logic) circuit, 5.8 V regulator, BYPASS pin undervoltage circuit, over-temperature protection, frequency jittering, current limit circuit, and leading edge blanking.

Oscillator
The typical oscillator frequency is internally set to an average of 66/83/100 kHz for the LNK562, 563 & 564 respectively. Two signals are generated from the oscillator: the maximum duty cycle signal (DC_{MAX}) and the clock signal that indicates the beginning of each switching cycle.

The oscillator incorporates circuitry that introduces a small amount of frequency jitter, typically 5% of the switching frequency, to minimize EMI. The modulation rate of the frequency jitter is set to 1 kHz to optimize EMI reduction for both average and quasi-peak emissions. The frequency jitter, which is proportional to the oscillator frequency, should be measured with the oscilloscope triggered at the falling edge of the DRAIN voltage waveform. The waveform in Figure 4 illustrates the frequency jitter. The oscillator frequency is reduced when the FB pin voltage is less than 1.69 V as described below.

Feedback Input Circuit

The feedback input circuit at the FB pin consists of a low impedance source follower output set at 1.69 V. When the current delivered into this pin exceeds 70 µA, a low logic level (disable) is generated at the output of the feedback circuit. This output is sampled at the beginning of each cycle on the rising edge of the clock signal. If high, the power MOSFET is turned on for that cycle (enabled), otherwise the power MOSFET remains off (disabled). Since the sampling is done only at the beginning of each cycle, subsequent changes in the FB pin voltage or current during the remainder of the cycle are ignored. When the FB pin voltage falls below 1.69 V, the oscillator frequency linearly reduces to typically 48% at the auto-restart threshold voltage of 0.8 V. This function limits the power supply output current at output voltages below the rated voltage regulation threshold V_R (see Figure 1).

5.8 V Regulator and 6.3 V Shunt Voltage Clamp

The 5.8 V regulator charges the bypass capacitor connected to the BYPASS pin to 5.8 V by drawing a current from the voltage on the DRAIN, whenever the MOSFET is off. The BYPASS pin is the internal supply voltage node. When the MOSFET is on, the device runs off of the energy stored in the bypass capacitor. Extremely low power consumption of the internal circuitry allows *LinkSwitch-LP* to operate continuously from the current drawn from the DRAIN pin. A bypass capacitor value of 0.1 µF is sufficient for both high frequency decoupling and energy storage.

In addition, there is a 6.3 V shunt regulator clamping the BYPASS pin at 6.3 V when current is provided to the BYPASS pin externally. This facilitates powering the device externally through a resistor from the bias winding to decrease the no-load consumption.

BYPASS Pin Undervoltage

The BYPASS pin undervoltage circuitry disables the power MOSFET when the BYPASS pin voltage drops below 4.85 V. Once the BYPASS pin voltage drops below 4.85 V, it must rise back to 5.8 V to enable (turn on) the power MOSFET.

Over-Temperature Protection

The thermal shutdown circuitry senses the die temperature. The threshold is set at 142 °C typical with a 75 °C hysteresis. When the die temperature rises above this threshold (142 °C) the power MOSFET is disabled and remains disabled until the die temperature falls by 75 °C, at which point the MOSFET is re-enabled.

Current Limit

The current limit circuit senses the current in the power MOSFET. When this current exceeds the internal threshold (I_{LIMIT}), the power MOSFET is turned off for the remainder of that cycle. The leading edge blanking circuit inhibits the current limit comparator for a short time (t_{LEB}) after the power MOSFET is turned on. This leading edge blanking time has been set so that current spikes caused by capacitance and rectifier reverse recovery time will not cause premature termination of the MOSFET conduction.

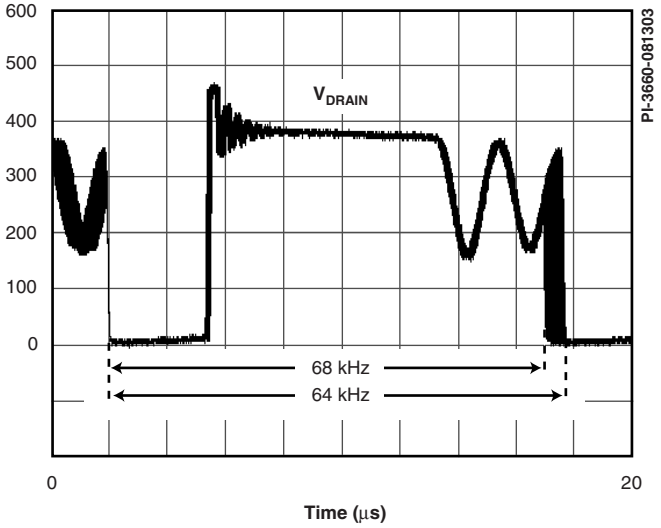


Figure 4. Frequency Jitter at f_{OSC}.

Auto Restart

In the event of a fault condition such as output short circuit or an open loop condition, *LinkSwitch-LP* enters into auto-restart operation. An internal counter clocked by the oscillator gets reset every time the FB pin voltage exceeds the FEEDBACK Pin Auto-Restart Threshold Voltage ($V_{FB(AR)}$). If the FB pin voltage drops below $V_{FB(AR)}$ for more than 100 ms, the power MOSFET switching is disabled. The auto-restart alternately enables and disables the switching of the power MOSFET at a duty cycle of typically 12% until the fault condition is removed.

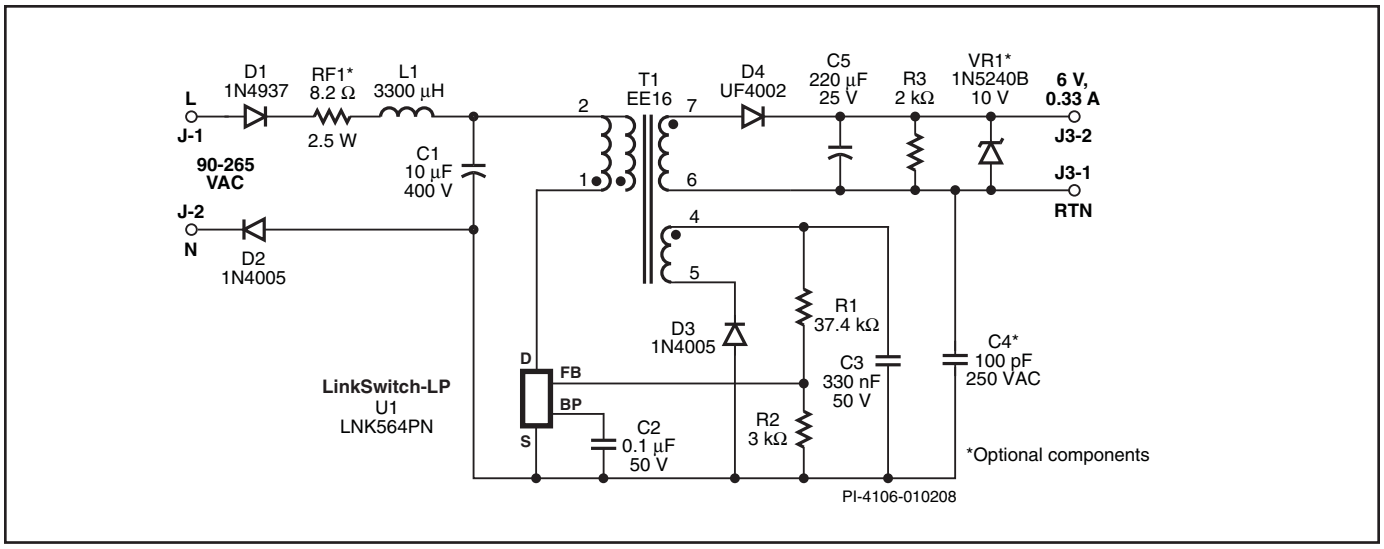


Figure 5. 6 V, 330 mA CV/CC Linear Replacement Power Supply.

Applications Example

The circuit shown in Figure 5 is a typical implementation of a 6 V, 330 mA, constant voltage, constant current (CV/CC) output power supply.

AC input differential filtering is accomplished with the very low cost input filter stage formed by C1 and L1. The proprietary frequency jitter feature of the LNK564 eliminates the need for an input pi filter, so only a single bulk capacitor is required. Adding a sleeve may allow the input inductor L1 to be used as a fuse as well as a filter component. This very simple *Filterfuse™* input stage further reduces system cost. Alternatively, a fusible resistor RF1 may be used to provide the fusing function.

Input diode D2 may be removed from the neutral phase in applications where decreased EMI margins and/or decreased input surge withstand is allowed. In such applications, D1 will need to be an 800 V diode.

The power supply utilizes simplified bias winding voltage feedback, enabled by LNK564 ON/OFF control. The resistor divider formed by R1 and R2 determine the output voltage across the transformer bias winding during the switch OFF time. In the V/I constant voltage region, the LNK564 device enables/disables switching cycles to maintain 1.69 V on the FB pin. Diode D3 and low cost ceramic capacitor C3 provide rectification and filtering of the primary feedback winding waveform. At increased loads, beyond the constant power threshold, the FB pin voltage begins to reduce as the power supply output voltage falls. The internal oscillator frequency is linearly reduced in this region until it reaches typically 50% of the starting frequency. When the FB pin voltage drops below the auto-restart threshold (typically 0.8 V on the FB pin, which is equivalent to 1 V to 1.5 V at the output of the power supply), the power supply will turn OFF for 800 ms and then turn back on for 100 ms. It will continue in this mode until the auto-restart threshold is exceeded. This function reduces the average output current during an output short circuit condition.

No-load consumption can be further reduced by increasing C3 to 0.47 µF or higher.

A *Clampless* primary circuit is achieved due to the very tight tolerance current limit trimming techniques used in manufacturing the LNK564, plus the transformer construction techniques used. Peak drain voltage is therefore limited to typically less than 550 V at 265 VAC, providing significant margin to the 700 V minimum drain voltage specification (BV_{DSS}).

Output rectification and filtering is achieved with output rectifier D4 and filter capacitor C5. Due to the auto-restart feature, the average short circuit output current is significantly less than 1 A, allowing low cost rectifier D4 to be used. Output circuitry is designed to handle a continuous short circuit on the power supply output. Diode D4 is an ultra-fast type, selected for optimum V/I output characteristics. Optional resistor R3 provides a preload, limiting the output voltage level under no-load output conditions. Despite this preload, no-load consumption is within targets at approximately 140 mW at 265 VAC. The additional margin of no-load consumption requirement can be achieved by increasing the value of R4 to 2.2 kΩ or higher while still maintaining output voltage well below the 9 V maximum specification. Placement is left on the board for an optional Zener clamp (VR1) to limit maximum output voltage under open loop conditions, if required.

Key Application Considerations

Output Power Table

The data sheet maximum output power table (Table 1) represents the maximum practical continuous output power level that can be obtained under the following assumed conditions:

1. The minimum DC input voltage is 90 V or higher for 85 VAC input, or 240 V or higher for 230 VAC input or 115 VAC with a voltage doubler. The value of the input capacitance should be large enough to meet these criteria for AC input designs.
2. Secondary output of 6 V with a Schottky rectifier diode.
3. Assumed efficiency of 70%.
4. Voltage only output (no secondary-side constant current circuit).
5. Discontinuous mode operation (K_P > 1).
6. A suitably sized core to allow a practical transformer design (see Table 2).
7. The part is board mounted with SOURCE pins soldered to a sufficient area of copper to keep the SOURCE pin temperature at or below 100 °C.
8. Ambient temperature of 50 °C for open frame designs and an internal enclosure temperature of 60 °C for adapter designs.

	LinkSwitch-LP Device		
Core Size	LNK562	LNK563	LNK564
EE13	1.1 W	1.4 W	1.7 W
EE16	1.3 W	1.7 W	2 W
EE19	1.9 W	2.5 W	3 W

Table 2. Estimate of Transformer Power Capability vs. LinkSwitch-LP Device and Core Size at a Flux Density of 1500 Gauss (150 mT).

Below a value of 1, K_P is the ratio of ripple to peak primary current. Above a value of 1, K_P is the ratio of primary MOSFET OFF time to the secondary diode conduction time. Due to the flux density requirements described below, typically a *LinkSwitch-LP* design will be discontinuous, which also has the benefit of allowing lower-cost fast (vs. ultra-fast) output diodes and reducing EMI.

***Clampless* Designs**

Clampless designs rely solely on the drain node capacitance to limit the leakage inductance induced peak drain-to-source voltage. Therefore the maximum AC input line voltage, the value of V_{OR}, the leakage inductance energy, (a function of leakage inductance and peak primary current), and the primary winding capacitance determine the peak drain voltage. With no significant dissipative element present, as is the case with an external clamp, the longer duration of the leakage inductance ringing can increase EMI.

The following requirements are recommended for a universal input or 230 VAC only *Clampless* design:

1. *Clampless* designs should only be used for $P_O \leq 2.5$ W using a V_{OR} of ≤ 90 V
2. For designs with $P_O \leq 2$ W, a two-layer primary must be used to ensure adequate primary intra-winding capacitance in the range of 25 pF to 50 pF.
3. For designs with $2 < P_O \leq 2.5$ W, a bias winding must be added to the transformer using a standard recovery rectifier diode (1N4003– 1N4007) to act as a clamp. This bias winding may also be used to externally power the device by connecting a resistor from the bias winding capacitor to the BYPASS pin. This inhibits the internal high-voltage current source, reducing device dissipation and no-load consumption.
4. For designs with $P_O > 2.5$ W, *Clampless* designs are not practical and an external RCD or Zener clamp should be used.
5. Ensure that worst-case, high line, peak drain voltage is below the BV_{DSS} specification of the internal MOSFET and ideally ≤ 650 V to allow margin for design variation.

V_{OR} (Reflected Output Voltage), is the secondary output plus output diode forward voltage drop that is reflected to the primary via the turns ratio of the transformer during the diode conduction time. The V_{OR} adds to the DC bus voltage and the leakage spike to determine the peak drain voltage.

Audible Noise

The cycle skipping mode of operation used in *LinkSwitch-LP* can generate audio frequency components in the transformer. To limit this audible noise generation, the transformer should be designed such that the peak core flux density is below 1500 Gauss (150 mT). Following this guideline and using the standard transformer production technique of dip varnishing, practically eliminates audible noise. Vacuum impregnation of the transformer is not recommended, as it does not provide any better reduction of audible noise than dip varnishing. And although vacuum impregnation has the benefit of increased transformer capacitance (which helps in *Clampless* designs), it can also upset the mechanical design of the transformer, especially if shield windings are used. Higher flux densities are possible, increasing the power capability of the transformers above what is shown in Table 2. However careful evaluation of the audible noise performance should be made using production transformer samples before approving the design.

Ceramic capacitors that use dielectrics such as Z5U, when used in clamp circuits, may also generate audio noise. If this is the case, try replacing them with a capacitor having a different dielectric or construction, for example a film type.

Bias Winding Feedback

To give the best output regulation in bias winding designs, a slow diode such as the 1N400x series should be used as the rectifier. This effectively filters the leakage inductance spike and reduces the error that this would give when using fast recovery time diodes. The use of a slow diode is a requirement in *Clampless* designs.

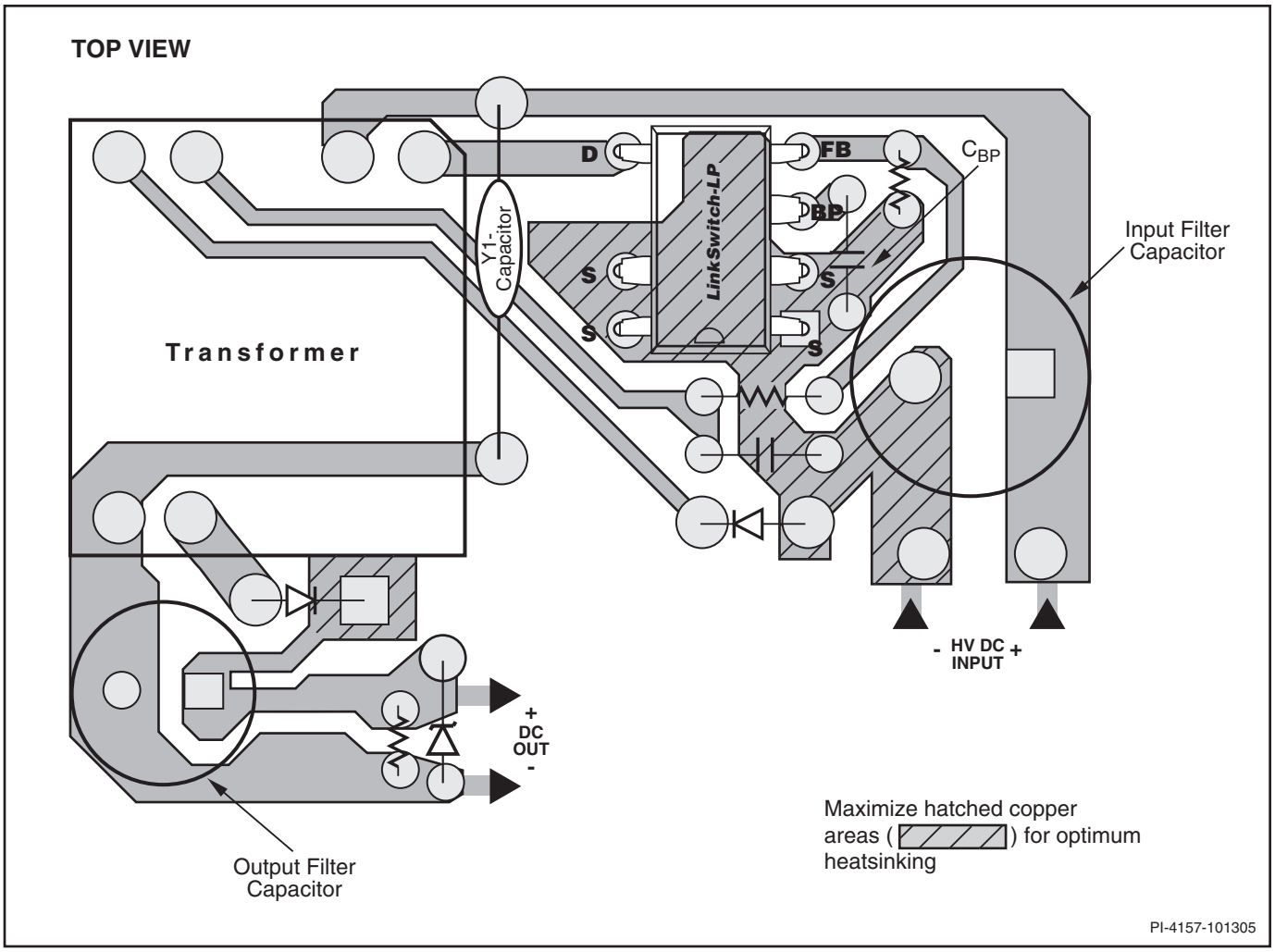


Figure 6. Recommended Circuit Board Layout for LinkSwitch-LP using P Package (Assumes a HVDC Input Stage).

LinkSwitch-LP Layout Considerations

Layout
See Figure 6 for a recommended circuit board layout for *LinkSwitch-LP* (P & G package).

Single Point Grounding
Use a single point ground connection from the input filter capacitor to the area of copper connected to the SOURCE pins.

Bypass Capacitor (C_{BP})
The BYPASS pin capacitor should be located as near as possible to the BYPASS and SOURCE pins.

Primary Loop Area
The area of the primary loop that connects the input filter capacitor, transformer primary and *LinkSwitch-LP* together should be kept as small as possible.

Primary Clamp Circuit
An external clamp may be used to limit peak voltage on the DRAIN pin at turn off. This can be achieved by using an RCD clamp or a Zener (~200 V) and diode clamp across the primary winding. In all cases, to minimize EMI, care should be taken to minimize the circuit path from the clamp components to the transformer and *LinkSwitch-LP*.

Thermal Considerations
The copper area underneath the *LinkSwitch-LP* acts not only as a single point ground, but also as a heatsink. As it is connected to the quiet source node, this area should be maximized for good heat sinking of *LinkSwitch-LP*. The same applies to the cathode of the output diode.

Y-Capacitor
The placement of the Y-type cap should be directly from the primary input filter capacitor positive terminal to the common/return terminal of the transformer secondary. Such a placement will route high magnitude common-mode surge currents away from the *LinkSwitch-LP* device. Note: If an input pi (C, L, C) EMI filter is used, then the inductor in the filter should be placed between the negative terminals on the input filter capacitors.

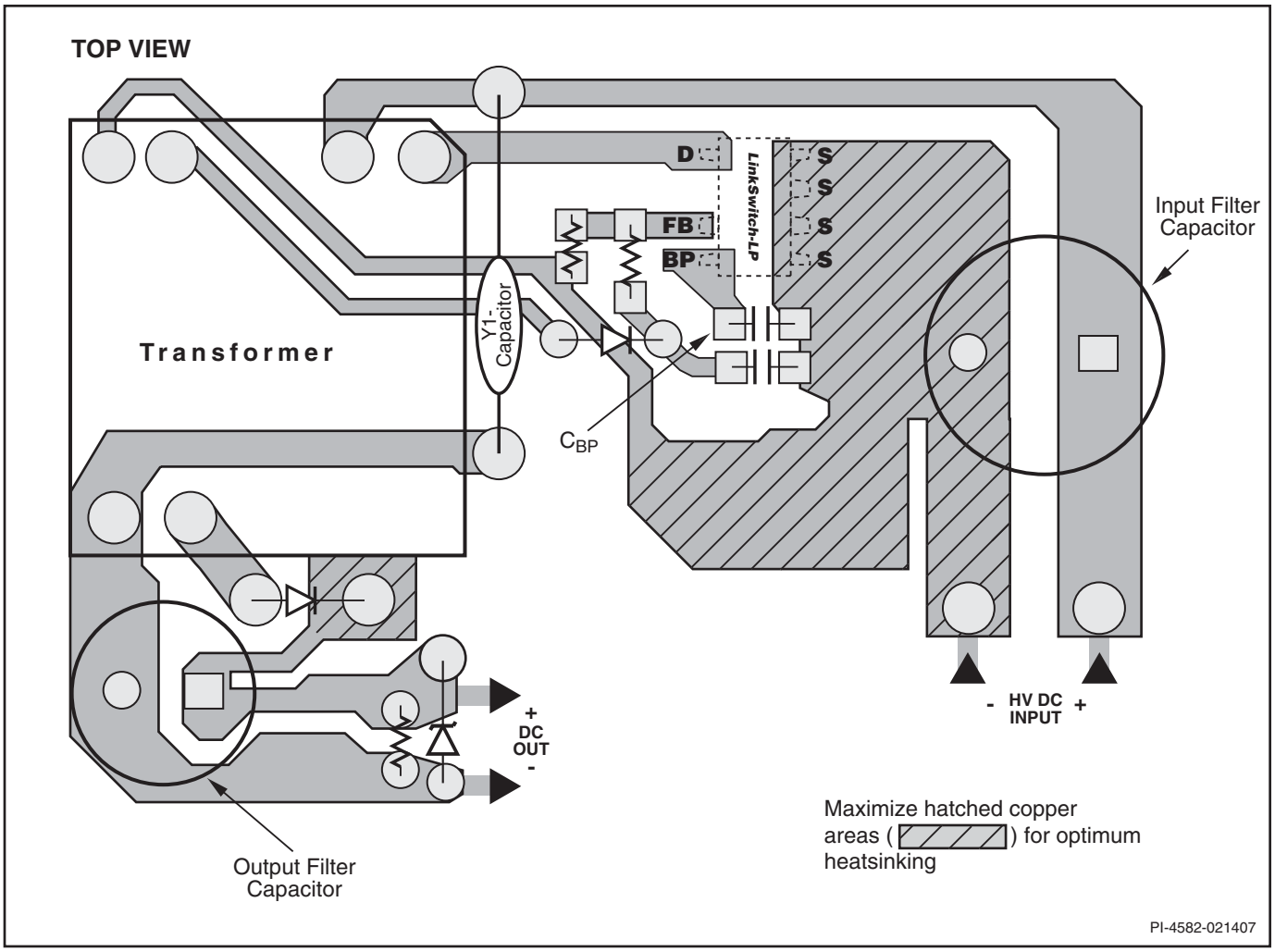


Figure 7. Recommended Circuit Board Layout for LinkSwitch-LP using D Package (Assumes a HVDC Input Stage).

Output Diode

For best performance, the area of the loop connecting the secondary winding, the output diode and the output filter capacitor should be minimized. In addition, sufficient copper area should be provided at the anode and cathode terminals of the diode for heat sinking. A larger area is preferred at the quiet cathode terminal. A large anode area can increase high-frequency radiated EMI.

Quick Design Checklist

As with any power supply design, all *LinkSwitch-LP* designs should be verified on the bench to make sure that component specifications are not exceeded under worst-case conditions. The following minimum set of tests is strongly recommended:

1. Maximum drain voltage – Verify that V_{DS} does not exceed 650 V at the highest input voltage and peak (overload) output power. A 50 V margin to the 700 V BV_{DSS} specification gives margin for design variation, especially in *Clampless* designs.
2. Maximum drain current – At maximum ambient temperature, maximum input voltage and peak output (overload) power, verify drain current waveforms for any signs of transformer saturation and excessive leading-edge current spikes at startup. Repeat under steady state conditions and verify that the leading-edge current spike event is below $I_{LIMIT(MIN)}$ at the end of the $t_{LEB(MIN)}$. Under all conditions, the maximum DRAIN current should be below the specified absolute maximum ratings.
3. Thermal Check – At specified maximum output power, minimum input voltage and maximum ambient temperature, verify that the temperature specifications are not exceeded for *LinkSwitch-LP*, transformer, output diode and output capacitors. Enough thermal margin should be allowed for part-to-part variation of the $R_{DS(ON)}$ of *LinkSwitch-LP* as specified in the data sheet. Under low line and maximum power, a maximum *LinkSwitch-LP* SOURCE pin temperature of 100 °C is recommended to allow for these variations.

Design Tools

Up-to-date information on design tools can be found at the Power Integrations web site: www.powerint.com.

ABSOLUTE MAXIMUM RATINGS[1,6]

DRAIN Voltage .....700 V
Peak DRAIN Current.....200 mA (375 mA)[2]
Peak Negative Pulsed Drain Current (see Fig. 11) ... 100 mA[3]
FEEDBACK Voltage .....-0.3 V to 9 V
FEEDBACK Current.....100 mA
BYPASS Voltage .....-0.3 V to 9 V
Storage Temperature ..... -65 °C to 150 °C
Operating Junction Temperature[4] ..... -40 °C to 150 °C
Lead Temperature[5] .....260 °C

Notes:
1. All voltages referenced to SOURCE, T_A = 25 °C.
2. The higher peak DRAIN current is allowed while the DRAIN voltage is simultaneously less than 400 V.
3. Duration not to exceed 2 µs.
4. Normally limited by internal circuitry.
5. 1/16 in. from case for 5 seconds.
6. Maximum ratings specified may be applied, one at a time, without causing permanent damage to the product. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect product reliability.

THERMAL IMPEDANCE

Thermal Impedance: P or G Package:
(θ_{JA}) ..... 70 °C/W[3]; 60 °C/W[4]
(θ_{JC})[1] ..... 11 °C/W
D Package:
(θ_{JA}) .... 100 °C/W[3]; 80 °C/W[4]
(θ_{JC})[2] ..... 30 °C/W

Notes:
1. Measured on pin 2 (SOURCE) close to plastic interface.
2. Measured on pin 8 (SOURCE) close to plastic interface.
3. Soldered to 0.36 sq. in. (232 mm^2), 2 oz. (610 g/m^2) copper clad.
4. Soldered to 1 sq. in. (645 mm^2), 2 oz. (610 g/m^2) copper clad.

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 8 (Unless Otherwise Specified)			Min	Typ	Max	Units
CONTROL FUNCTIONS								
Output Frequency	f_{OSC}	T_J = 25 °C V_{FB} = 1.69 V	Average	LNK562	61	66	71	kHz
				LNK563	77	83	89	
				LNK564	93	100	107	
Ratio of Output Frequency At Auto-Restart to f_{OSC}	$f_{OSC(AR)}$	T_J = 25 °C, V_{FB} = $V_{FB(AR)}$				48		%
Frequency Jitter		Peak-Peak Jitter, T_J = 25 °C				5		%
Maximum Duty Cycle	DC_{MAX}	S2 Open			66	70		%
FEEDBACK Pin Turnoff Threshold Current	I_{FB}	T_J = 25 °C See Note A			56	70	84	µA
FEEDBACK Pin Voltage at Turnoff Threshold	V_{FB}	T_J = 0 to 125 °C See Note A			1.60	1.69	1.78	V
DRAIN Supply Current	I_{S1}	V_{FB} ≥ 2 V (MOSFET Not Switching) See Note B				160	220	µA
	I_{S2}	FEEDBACK Open (MOSFET Switching) See Notes B, C				220	260	µA

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 8 (Unless Otherwise Specified)		Min	Typ	Max	Units
CONTROL FUNCTIONS (cont.)							
BYPASS Pin Charge Current	I_{CH1}	V_{BP} = 0 V, T_J = 25 °C, See Note D		-5.5	-3.3	-1.8	mA
	I_{CH2}	V_{BP} = 4 V, T_J = 25 °C, See Note D		-3.8	-2.3	-1.0	
BYPASS Pin Voltage	V_{BP}			5.55	5.8	6.10	V
BYPASS Pin Voltage Hysteresis	V_{BPH}			0.8	0.95	1.2	V
BYPASS Pin Supply Current	I_{BPSC}	See Note E		84			µA
CIRCUIT PROTECTION							
Current Limit	I_{LIMIT}	di/dt = 40 mA/µs T_J = 25 °C		124	136	148	mA
Power Coefficient	I^2f	di/dt = 40 mA/µs T_J = 25 °C	LNK562	1099	1221	1380	A^2Hz
			LNK563	1381	1535	1735	
			LNK564	1665	1850	2091	
Leading Edge Blanking Time	t_{LEB}	T_J = 25 °C See Note F		220	265		ns
Thermal Shutdown Temperature	T_{SD}			135	142	150	°C
Thermal Shutdown Hysteresis	T_{SHD}	See Note G			75		°C
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 13 mA	T_J = 25 °C		48	55	Ω
			T_J = 100 °C		76	88	
OFF-State Drain Leakage Current	I_{DSS}	V_{BP} = 6.2 V, V_{FB} ≥2 V, V_{DS} = 560 V, T_J = 25 °C				50	µA
Breakdown Voltage	BV_{DSS}	V_{BP} = 6.2 V, V_{FB} ≥2 V, See Note H, T_J = 25 °C		700			V
DRAIN Supply Voltage				50			V
Output Enable Delay	t_{EN}	See Figure 10				17	µs
Output Disable Setup Time	t_{DST}				0.5		µs

Parameter	Symbol	Conditions SOURCE = 0 V; T_J = -40 to 125 °C See Figure 8 (Unless Otherwise Specified)	Min	Typ	Max	Units
OUTPUT (cont.)						
FEEDBACK Pin Auto-Restart Threshold Voltage	$V_{FB(AR)}$	T_J = 25 °C		0.8		V
Auto-Restart ON-Time		V_{FB} = $V_{FB(AR)}$ T_J = 25 °C		100		ms
Auto-Restart Duty Cycle	DC_{AR}			12		%

NOTES:

A. In a scheme using a resistor divider network at the FB pin, where R_U is the resistor from the FB pin to the rectified bias voltage and R_L is the resistor from the FB pin to the SOURCE pin, the output voltage variation is influenced by V_{FB} and I_{FB} variations. To determine the contribution from the V_{FB} variation in percent, the following equation can be used:

$$x = 100 \times \left(\frac{V_{FB(MAX)}\left(\frac{R_U + R_L}{R_L}\right) + I_{FB(TYP)}R_U}{V_{FB(TYP)}\left(\frac{R_U + R_L}{R_L}\right) + I_{FB(TYP)}R_U} - 1 \right)$$

To determine the contribution from I_{FB} variation in percent, the following equation can be used:

$$y = 100 \times \left(\frac{V_{FB(TYP)}\left(\frac{R_U + R_L}{R_L}\right) + I_{FB(MAX)}R_U}{V_{FB(TYP)}\left(\frac{R_U + R_L}{R_L}\right) + I_{FB(TYP)}R_U} - 1 \right)$$

Since I_{FB} and V_{FB} are independent parameters, the composite variation in percent would be $\pm\sqrt{x^2 + y^2}$.

B. Total current consumption is the sum of I_{S1} and I_{DSS} when FEEDBACK pin voltage is ≥2 V (MOSFET not switching) and the sum of I_{S2} and I_{DSS} when FEEDBACK pin is shorted to SOURCE (MOSFET switching).

C Since the output MOSFET is switching, it is difficult to isolate the switching current from the supply current at the DRAIN. An alternative is to measure the BYPASS pin current at 6 V.

D. See Typical Performance Characteristics section Figure 16 for BYPASS pin startup charging waveform.

E. This current is only intended to supply an optional optocoupler connected between the BYPASS and FEEDBACK pins and not any other external circuitry.

F. This parameter is guaranteed by design.

G. This parameter is derived from characterization.

H. Breakdown voltage may be checked against minimum BV_{DSS} by ramping the DRAIN pin voltage up to but not exceeding minimum BV_{DSS}.

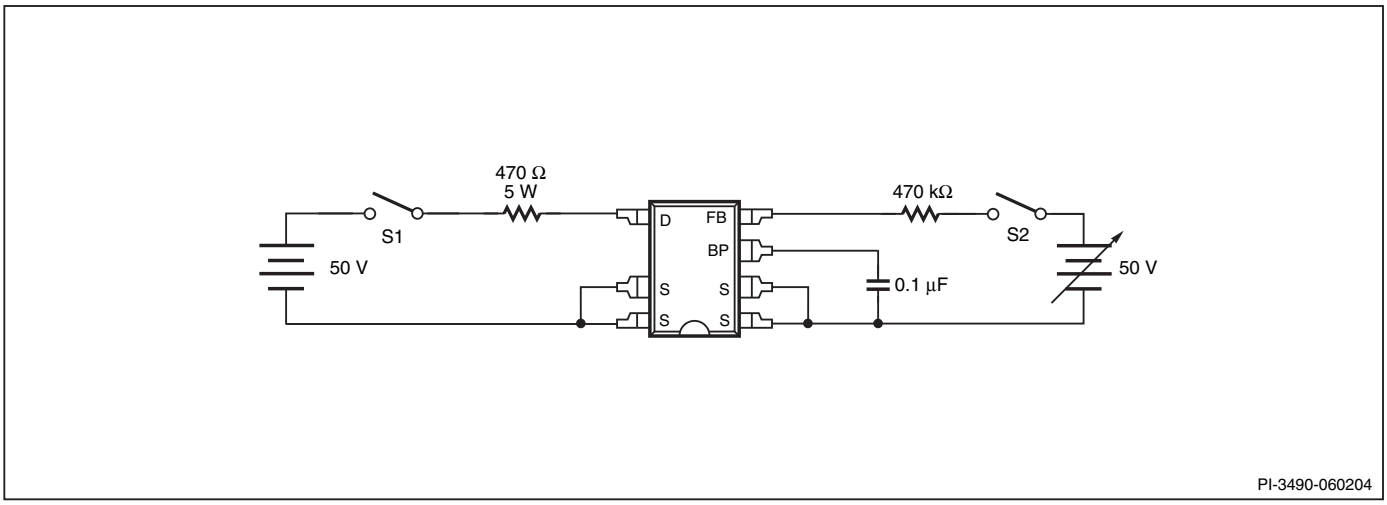


Figure 8. General Test Circuit.

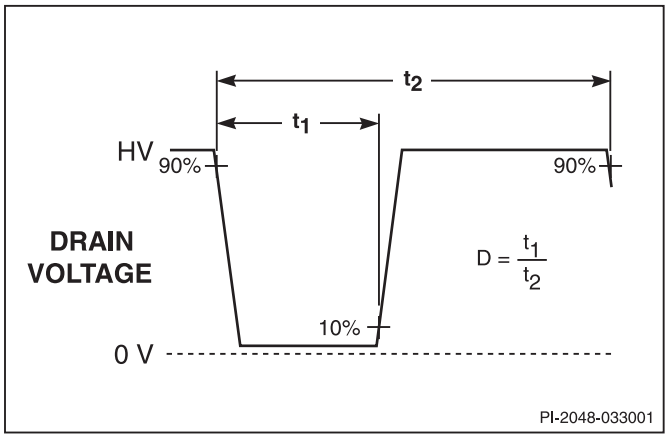


Figure 9. Duty Cycle Measurement.

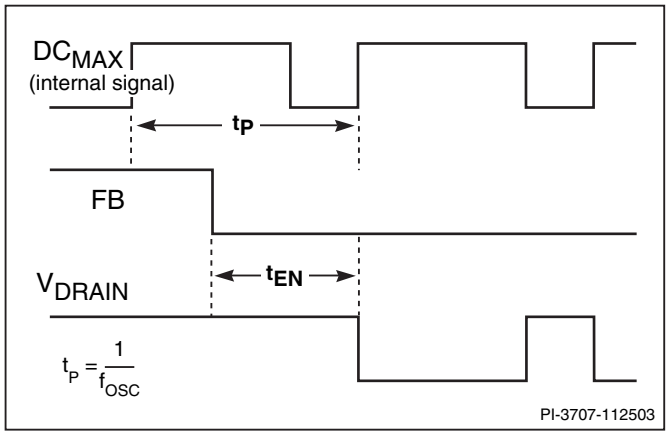


Figure 10. Output Enable Timing.

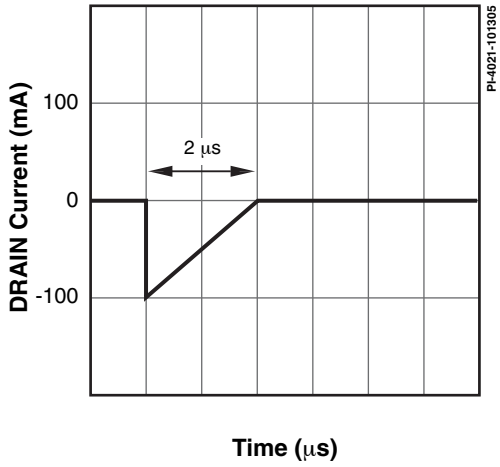


Figure 11. Peak Negative Pulsed DRAIN Current Waveform.

Typical Performance Characteristics

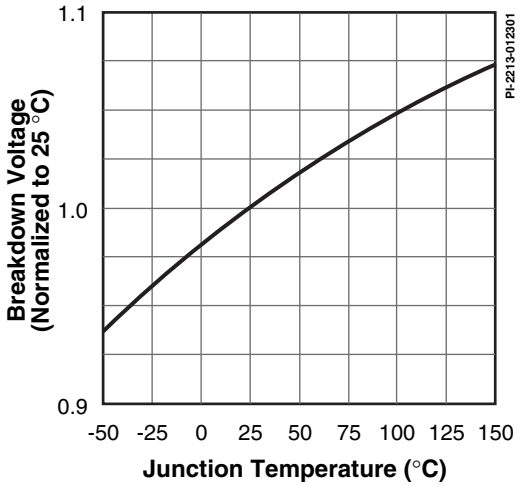


Figure 12. Breakdown vs. Temperature.

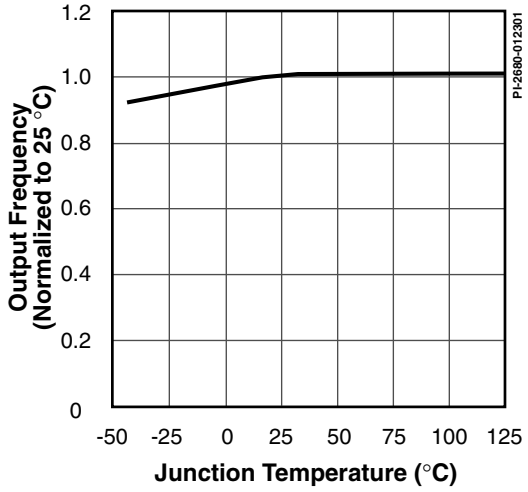


Figure 13. Frequency vs. Temperature.

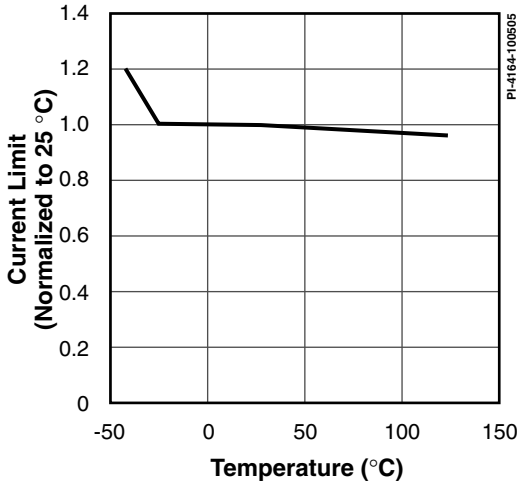


Figure 14. Current Limit vs. Temperature.

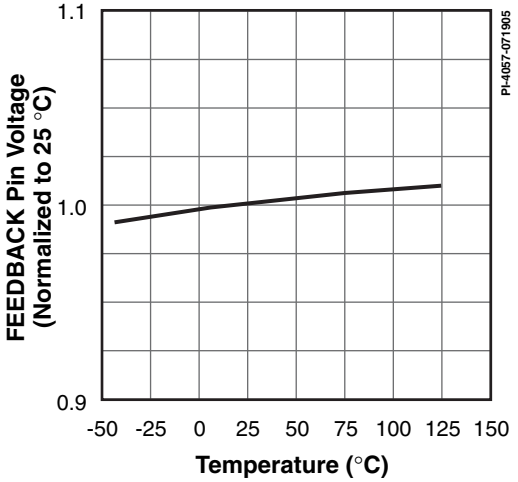


Figure 15. FEEDBACK Pin Voltage vs. Temperature.

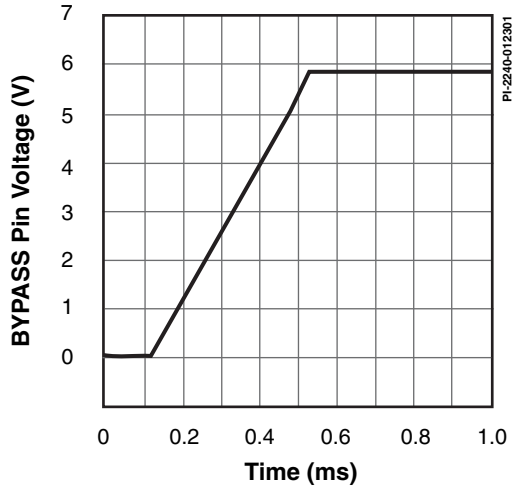


Figure 16. BYPASS Pin Startup Waveform.

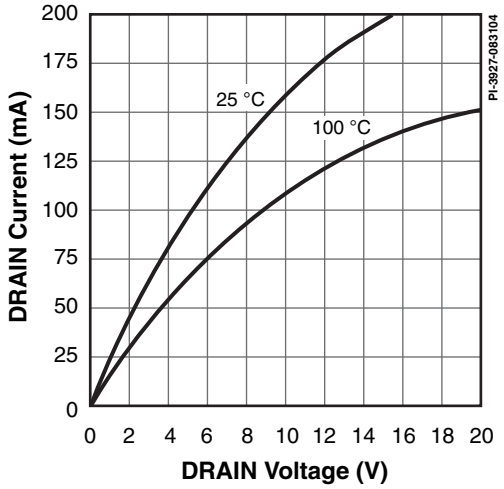


Figure 17. Output Characteristics.

Typical Performance Characteristics (cont.)

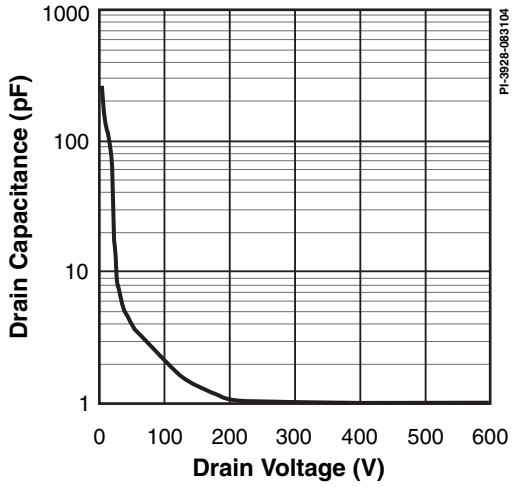


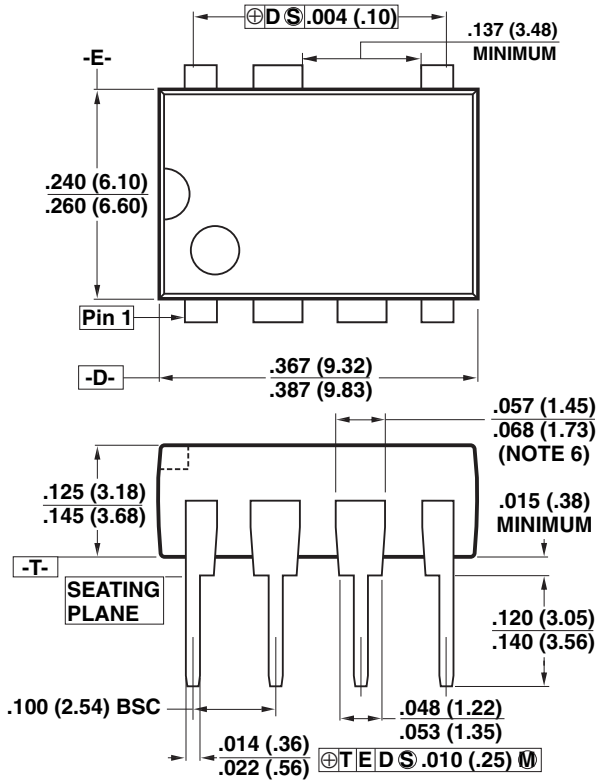
Figure 18. C_{oss} vs. Drain Voltage.

PART ORDERING INFORMATION

LNK 562 D N - TL

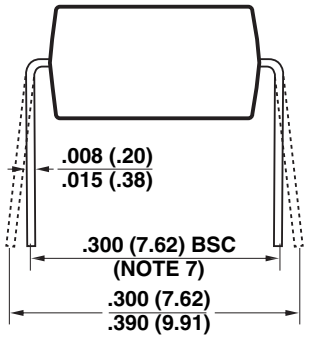
***LinkSwitch* Product Family**	
LP Series Number	
Package Identifier	
G	Plastic Surface Mount DIP
P	Plastic DIP
D	Plastic SO-8
Lead Finish	
N	Pure Matte Tin (RoHS Compliant)
G	RoHS Compliant and Halogen Free (P and D Package only)
Tape & Reel and Other Options	
Blank	Standard Configurations
TL	Tape & Reel, 1 k pcs minimum for G Package. 2.5 k pcs for D Package. Not available for P Package.

DIP-8B



Notes:

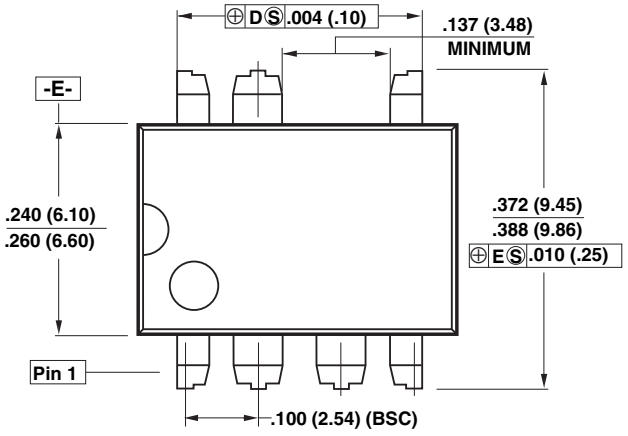
1. **Package dimensions conform to JEDEC specification MS-001-AB (Issue B 7/85) for standard dual-in-line (DIP) package with .300 inch row spacing.**
2. **Controlling dimensions are inches. Millimeter sizes are shown in parentheses.**
3. **Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.**
4. **Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. The notch and/or dimple are aids in locating Pin 1. Pin 6 is omitted.**
5. **Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).**
6. **Lead width measured at package body.**
7. **Lead spacing measured with the leads constrained to be perpendicular to plane T.**

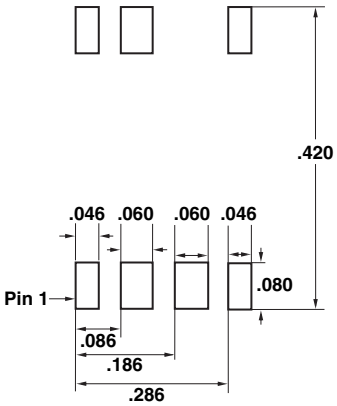


P08B

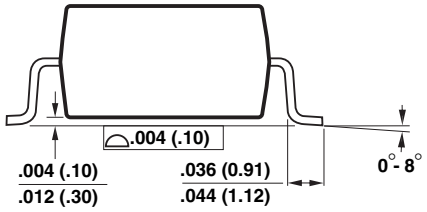
PI-2551-121504

SMD-8B





Solder Pad Dimensions



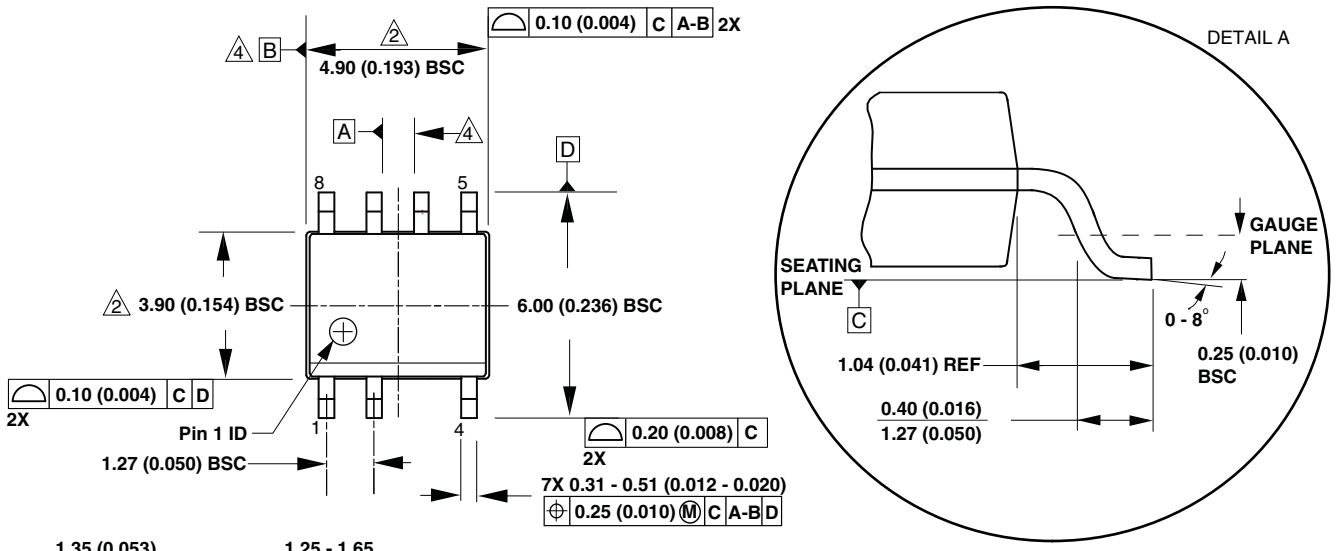
Notes:

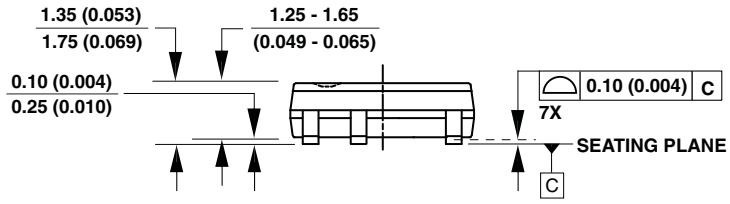
1. **Controlling dimensions are inches. Millimeter sizes are shown in parentheses.**
2. **Dimensions shown do not include mold flash or other protrusions. Mold flash or protrusions shall not exceed .006 (.15) on any side.**
3. **Pin locations start with Pin 1, and continue counter-clockwise to Pin 8 when viewed from the top. Pin 6 is omitted.**
4. **Minimum metal to metal spacing at the package body for the omitted lead location is .137 inch (3.48 mm).**
5. **Lead width measured at package body.**
6. **D and E are referenced datums on the package body.**

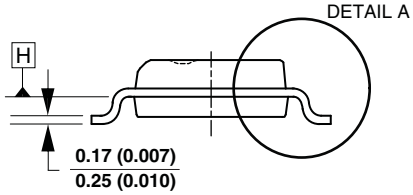
G08B

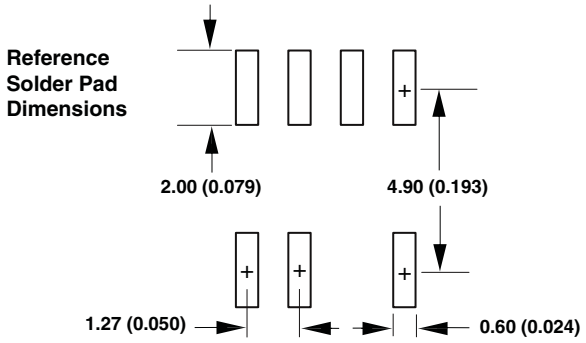
PI-2546-121504

SO-8C









Notes:

1. JEDEC reference: MS-012.
2. Package outline exclusive of mold flash and metal burr.
3. Package outline inclusive of plating thickness.
4. Datums A and B to be determined at datum plane H.
5. Controlling dimensions are in millimeters. Inch dimensions are shown in parenthesis. Angles in degrees.

D07C

PI-4526-040207

Revision	Notes	Date
E	1) Final Release Data Sheet	10/05
F	1) Revision of PI-3924	10/05
G	1) Added SO-8C Package	2/07
H	1) Updated Part Ordering Information section with Halogen Free	11/08

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