CCE4511

4-Channel IO-Link Master PHY with integrated Frame Handler

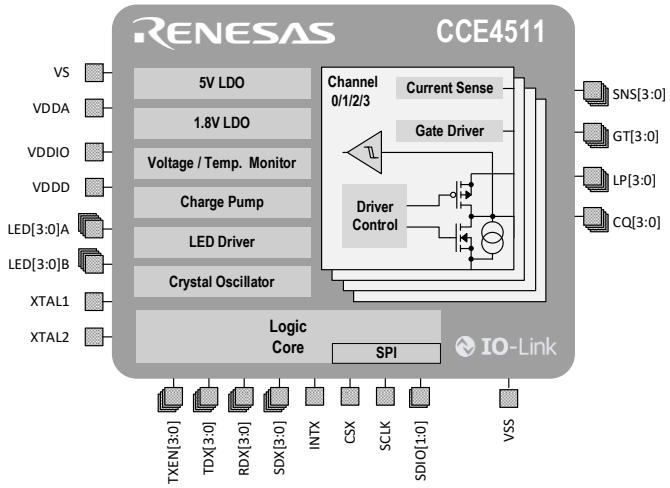
The CCE4511 is a high-voltage interface IC with overvoltage detection as well as high temperature and over-current protection, based upon a 0.18 µm HV-CMOS technology.
Typical applications are industrial IO modules, which should support the IO-Link standard. To improve the application performance, an integrated IO-Link Frame Handler is provided, which automates most of the lower layer communication tasks. This reduces the microcontroller loads significantly, thus gaining more performance for other tasks, even if slower microcontrollers are used.
A variety in fields of application is given by different configuration options.

Applications

- 4/8/12/16-port IO-Link master applications
- Factory automation
- Process automation

Available Support

Renesas provides Application Notes [3], Evaluation Board User Manual [4], and other documents for user convenience.



Features

- Ready pulse detection
- Four IO-Link compliant master channels
- Wide voltage range 8 V to 36 V
- SPI interface
- Standard IO Mode (SIO)
- Integrated UART (COM1-3)
- Hardware Frame Handler (support for all IO-Link v1.1.3 frame types)
- Fully IO-Link v1.1.3 compliant
- Automated wake-up pulse generation
- Eight status LED drivers
- Synchronization of transfers to external signals
- Integrated gate drivers for external NMOS to switch power supply of each device
- Gate driver soft start to limit device inrush current
- Integrated crystal oscillator
- Supports feed through of clock
- -40 °C to 125°C operating temperature
- Over-Temperature protection
- Supply voltage monitoring
- Overload protection for channels and connected devices
- Undervoltage detection and shutdown for each channel
- Integrated glitch filters
- Ideal fit for 4/8/12/16-port IO-Link master applications

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1. Pin Information

1.1. Pin Assignments

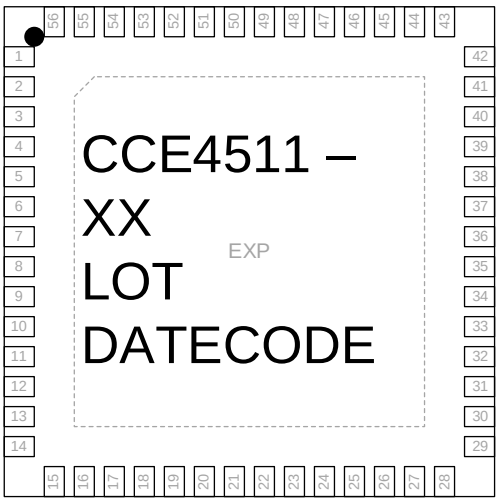


Figure 1. QFN56 Package (8x8 mm) – Top View

1.2. Pin Descriptions

Table 1: Pin Description

Pin #	Pin Name	Type (Table 2)	Drive (mA)	Reset State	Description	Power Domain
EXP	VSS	GND	-	-	Common ground at exposed pad	
1	SDX0	DO	2	LOW	Channel 0 short detected; active low	VDDIO
2	SDX1	DO	2	LOW	Channel 1 short detected; active low	VDDIO
3	SDX2	DO	2	LOW	Channel 2 short detected; active low	VDDIO
4	SDX3	DO	2	LOW	Channel 3 short detected; active low	VDDIO
5	VDDIO	PWR	-	-	1.8V - 5.0V digital IO supply	-
6	VSS	GND	-	-	Common ground, shorted to exposed pad	-
7	VDDD	PWR	-	-	1.8V digital core supply	-
8	RXD0	DO	2	LOW	CQ0 input; inverted	VDDIO
9	RXD1	DO	2	LOW	CQ1 input; inverted	VDDIO
10	RXD2	DO	2	LOW	CQ2 input; inverted	VDDIO
11	RXD3	DO	2	LOW	CQ3 input; inverted	VDDIO
12	TXD0	PD	-	-	CQ0 output, inverted	VDDIO
13	TXD1	PD	-	-	CQ1 output, inverted	VDDIO
14	TXD2	PD	-	-	CQ2 output, inverted	VDDIO
15	TXD3	PD	-	-	CQ3 output, inverted	VDDIO
16	TXEN0	PD	-	-	CQ0 driver enable, active high	VDDIO
17	TXEN1	PD	-	-	CQ1 driver enable, active high	VDDIO
18	TXEN2	PD	-	-	CQ2 driver enable, active high	VDDIO
19	TXEN3	PD	-	-	CQ3 driver enable, active high	VDDIO
20	XTAL2	DO	2	LOW	Crystal Oscillator Output	VDDD
21	XTAL1	AI	-	-	Crystal Oscillator Input; external clock source input	VDDD
22	TST	PD	-	-	Test mode enable; connect to VSS	VDDIO
23	LED3A	DOOD	20	HIGH-Z	LEDA Driver Channel 3	-
24	LED3B	DOOD	20	HIGH-Z	LEDB Driver Channel 3	-
25	GT3	AO	10	LOW	NMOS gate driver channel 3	LP3

Pin #	Pin Name	Type (Table 2)	Drive (mA)	Reset State	Description	Power Domain
26	SNS3	AI	-	-	LP current sense input channel 3	VS
27	CQ3	AIO	800	HIGH-Z	IO-Link channel 3	LP3
28	LP3	PWR	-	-	Supply channel 3	-
29	LED2A	DOOD	20	HIGH-Z	LEDA Driver Channel 2	-
30	LED2B	DOOD	20	HIGH-Z	LEDB Driver Channel 2	-
31	GT2	AO	10	LOW	NMOS gate driver channel 2	LP2
32	SNS2	AI	-	-	LP current sense input channel 2	VS
33	CQ2	AIO	800	HIGH-Z	IO-Link channel 2	LP2
34	LP2	PWR	-	-	Supply channel 2	-
35	VDDA	PWR	-	-	5.0V analog Voltage supply	-
36	VS	PWR	-	-	24V main supply	-
37	LED1A	DOOD	20	HIGH-Z	LEDA Driver Channel 1	-
38	LED1B	DOOD	20	HIGH-Z	LEDB Driver Channel 1	-
39	GT1	AO	10	LOW	NMOS gate driver channel 1	LP1
40	SNS1	AI	-	-	LP current sense input channel 1	VS
41	CQ1	AIO	800	HIGH-Z	IO-Link channel 1	LP1
42	LP1	PWR	-	-	Supply channel 1	-
43	-	-	-	-	Not connected internally	-
44	LED0A	DOOD	20	HIGH-Z	LEDA Driver Channel 0	-
45	LED0B	DOOD	20	HIGH-Z	LEDB Driver Channel 0	-
46	GT0	AO	10	LOW	NMOS gate driver channel 0	LP0
47	SNS0	AI	-	-	LP current sense input channel 0	VS
48	CQ0	AIO	800	HIGH-Z	IO-Link channel 0	LP0
49	LP0	PWR	-	-	Supply channel 0	-
50	SDIO3	DIO (PD)	2	LOW	reserved, connect to VSS	VDDIO
51	SDIO2	DIO (PD)	2	LOW	reserved, connect to VSS	VDDIO
52	SDIO1	DIO (PD)	2	LOW	SPI Master-In-Slave-Out	VDDIO
53	SDIO0	DIO (PD)	2	LOW	SPI Master-Out-Slave-In	VDDIO
54	SCLK	PD	-	LOW	SPI clock	VDDIO
55	CSX	PU	-	HIGH	SPI chip select, active low	VDDIO
56	INTX	DO	2	LOW	Interrupt signal; active low	VDDIO

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
DI	Digital input	AI	Analog input
DO	Digital output	AI	Analog input
DIO	Digital input/output	AO	Analog output
DIO	Digital input/output	AIO	Analog input/output
DOOD	Digital output open drain	PWR	Power
PU	Pull-up resistor (fixed)	GND	Ground
PD	Pull-down resistor (fixed)		

2. Block Diagram

Figure 2 shows the block diagram of the CCE4511. It consists of four identical channels containing a gate driver for switching the LP lines using external NMOS transistors as well as a CQ input logic and output driver to handle communication on the IO-Link data lines. An integrated HV charge pump generates the gate driver supply voltage. All channels share a common 5 V LDO for powering the analog part of the CCE4511 and a 1.8 V LDO that supplies the logic core. The clocks for the logic core are generated by an integrated crystal oscillator. Eight LED drivers can be used for signaling different status information. Supply voltages and die temperature are supervised by a monitor block.

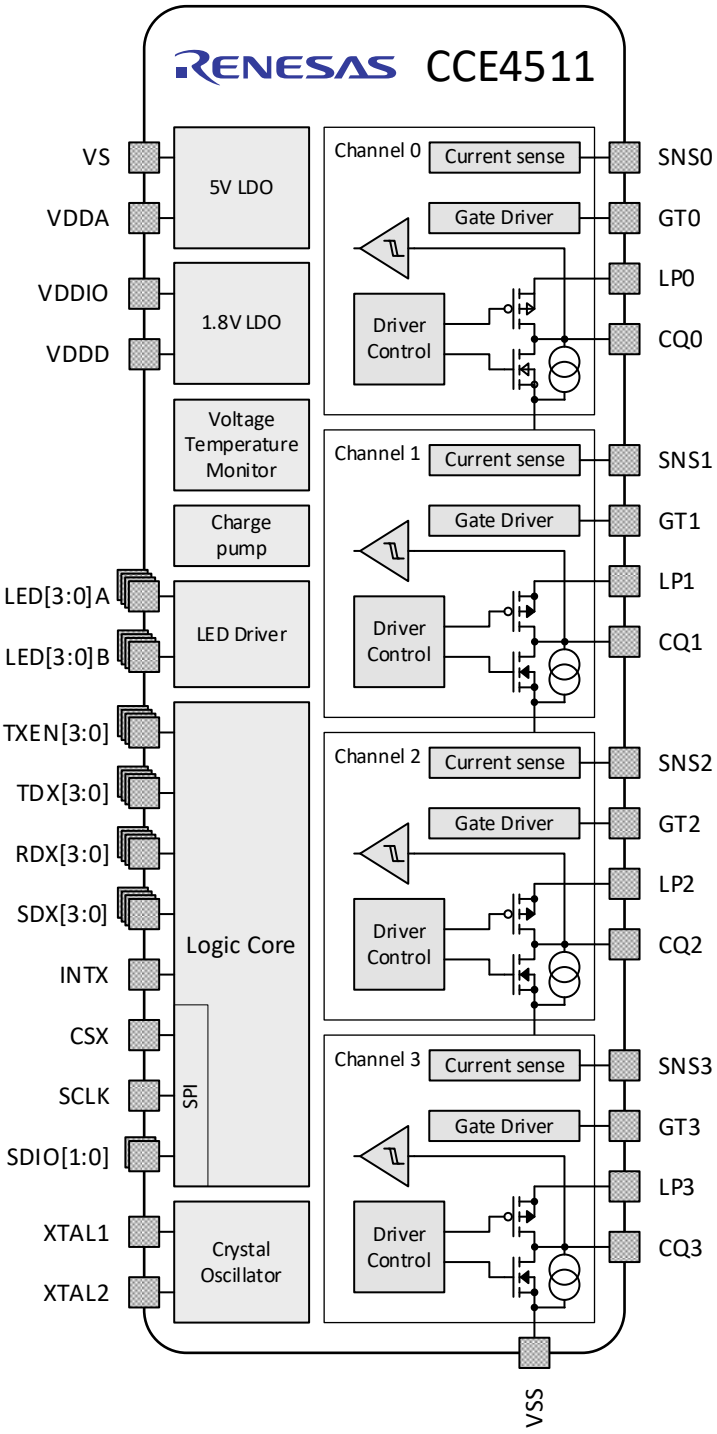


Figure 2. Block Diagram

3. Specifications

3.1. Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in section 3.2 are not implied.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
V_{VS}	HV supply voltage	-	-0.3	45	V
V_{VDDIO}	IO supply voltage	-	-0.3	5.5	V
V_{LPx}	Channel supply voltage	-	-0.3	45	V
V_{SNSx}	Current sense inputs	-	-0.3	V_{VS}+ 0.3	
V_{GTx}	Gate driver outputs	-	0.3	V_{LPx}+ 15	V
V_{CQx}	HV data IO	-	-0.3	V_{LPx}+0.3	V
V_{VDDD}	Digital core supply	-	-0.3	1.98	V
V_{VDDA}	Analog core supply	-	-0.3	5.5	V
V_{XTALx}	Crystal oscillator pins	-	-0.3	V_{VDDD}+0.3	V
V_{LEDx}	LED outputs	-	-0.3	5.5	
V_{IO}	Other IO-Pins	-	-0.3	V_{VDDIO}+0.3	V
P_{TOT_QFN48}	Power dissipation QFN56	Multilayer PCB, Exp. Pad soldered, T_{AMB} = 60°C	-	2	W
T_{JUNC}	Junction temperature	-	-	150	°C
V_{ESD}	ESD-sensitivity	Human Body Model EIA/JESD22-A114-B	-2	+2	kV
$T_{STORAGE}$	Storage temperature	-	-55	155	°C
T_{SOLDER}	Soldering temperature	12s maximum on this temperature.	-	260	°C

Note 1 Functional operation is only guaranteed within operating conditions listed under “Electrical Characteristics”. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability. Exposure to conditions beyond those ratings may cause permanent damage to the device.

3.2. Electrical Specifications

Electrical characteristics are valid for the specified temperature range and supply voltage range listed in section 3.2, unless otherwise noted.

3.2.1. General Parameters

Table 4: General Parameters

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{VS}	Main supply voltage		8	24	36	V
I_{VS}	Main supply current				6	mA
V_{LPx}	Channel supply voltage		8	24	36	V
I_{LPix}	Internal channel supply current, see Figure 18	ICQx ≤ 500 mA			2	mA
V_{VDDIO}	Pad supply voltage		1.75		5.5	V
I_{VDDIO}	Quiescent current IO supply				5	mA
T_{AMB}	Operating temperature	T_J < 150°C	-40		125	°C
ϑ_{JA_QFN56}	Thermal resistance	Junction to ambient Note 1		15		K/W

Note 1 JEDEC JESD51-2A 4-layer PCB, 70µm Cu in outer layers with 50% coverage and 35µm Cu inner layers with 90% coverage. 16 thermal vias.

3.2.2. IO-Link Channels

Table 5: IO-Link Channels

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{CQx}	CQ voltage range		-0.3		V_{LP} +0.3	V
ΔI_{CQ_LOAD}	Internal adjustable current sink at CQ accuracy vs. nominal value set by ICQ_SEL	ICQ_EN = 1	-20		20	%
V_{DROP_PMOS}	Residual voltage 'H'	Voltage drop at 500 mA			3	V
V_{DROP_NMOS}	Residual voltage 'L'	Voltage drop at 500 mA			3	V
I_{CQPEAK}	Output peak current	Duration t_{PEAK} = 1ms	0.5	1		A
t_{RISE}	Output driver rise time	▪ C_{CQ} = 5 nF, V_{VS} = 24 V ▪ 10% to 90% V_{VS} ▪ Maximum slew rate selected ▪ CQ current limit enabled		370		ns
t_{FALL}	Output driver fall time	▪ C_{CQ} = 5 nF, V_{VS} = 24 V ▪ 90% to 10% V_{VS} ▪ Maximum slew rate selected ▪ CQ current limit enabled		370		ns
t_{DLH}	CQ input delay, rising edge at CQ Note 2				450	ns
t_{DHL}	CQ input delay, falling edge at CQ Note 2				450	ns
V_{THH_IOLF}	CQ input threshold, rising edge, fixed threshold level		10.5		13	V
V_{THH_IOLR}	CQ input threshold, rising edge, ratiometric threshold level		0.525		0.65	V_{LPx}

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{THL_IOLF}	CQ input threshold, falling edge, fixed threshold level		8		11.5	V
V_{THL_IOLR}	CQ input threshold, falling edge, ratiometric threshold level		0.40		0.575	V_{LPx}
V_{HYS_IOLF}	CQ fixed input threshold hysteresis			2		V
V_{HYS_IOLR}	CQ ratiometric input threshold hysteresis			0.10		V_{LPx}
I_{CQ_OVC}	CQ driver overload detection threshold		500		800	mA
I_{CQ_LIM}	CQ driver current limit		500	650	1000	mA
$\Delta I_{CQ_LIM_OVC}$	I_{CQ_LIM} - I_{CQ_OVC}		1 Note 1			mA

Note 1 This ensures that an overload condition is always flagged if the output current is limited.

Note 2 Parameter verified by design, not fully tested in production.

3.2.3. NMOS Gate Drivers

Table 6: NMOS Gate Drivers

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{GATE_ON}	On switching time	C_{GATE} = 1 nF		1		ms
t_{GATE_OFF}	Off switching time	C_{GATE} = 1 nF		10		µs
V_{GATE_ON}	Output voltage		V_{VS}+8		V_{VS}+12	V
C_{GATE}	External capacitance			1		nF
I_{TGSL}	External gate-source leakage current	External NMOS	-1		1	µA
I_{GATE_CHG}	Gate charge current		15		30	µA
R_{GATE_DIS}	Gate discharge resistor			1.5		kΩ
V_{SENSE_OVC}	Overcurrent detection threshold: V_{VS}-V_{SNSx}		215	240	265	mV
V_{SENSE_LIM}	Current limit threshold: V_{VS}-V_{SNSx}		350		500	mV
V_{GT_LIM}	Gate voltage clamp V_{GTx} - V_{LPx}				17	V

3.2.4. Oscillator

Table 7: Crystal Oscillator

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{OSC}	Frequency			14.7456		MHz
$t_{STARTUP}$	Power up to Oscillator running delay Note 1	ESR_{XTAL} <= 100 Ω			2	ms

Note 1 Parameter verified by design, not fully tested in production

3.2.5. Digital Pads

Table 8: Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{INH}	Input voltage 'H'		0.7			V_{VDDIO}
V_{INL}	Input voltage 'L'				0.3	V_{VDDIO}
C_{IN}	Input capacitance			5		pF
I_{ILEAK}	Input leakage current	No pull-up/pull-down	-1		1	µA
V_{OUTH}	Output voltage 'H'	I_{OUT} = 2 mA Note 1	0.8			V_{VDDIO}
V_{OUTL}	Output voltage 'L'	I_{OUT} = -2 mA Note 1			0.2	V_{VDDIO}
I_{IH}	Weak pull-up current	V_{PIN} = 0 V, VDDIO = 5 V		40		µA
I_{IL}	Weak pull-down current	V_{PIN} = VDDIO, VDDIO = 5 V		40		µA

Note 1 For VDDIO < 2.25 V, CFG.PAD_DRV_STRENGTH high assumed.

3.2.6. Serial Peripheral Interface

Table 9: Serial Peripheral Interface

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{spi_1V8}	SCLK frequency (1 / t_{SPI_c}) Note 1	VDDIO < 2.25 V			15	MHz
f_{spi_2V5}		VDDIO ≥ 2.25 V			22	MHz
f_{spi_3V3}		VDDIO ≥ 3.0 V			27	MHz
f_{spi_5V0}		VDDIO ≥ 4.5 V			32	MHz
t_{spi_ch}	SCLK high pulse width Note 2		5			ns
t_{spi_cl}	SCLK low pulse width Note 2		5			ns
t_{spi_s}	SCLK start after select Note 2		0			ns
t_{spi_h}	CSX falling to SCLK rising Note 2		0			ns
t_{spi_e}	SCLK falling to CSX falling Note 2		0			ns
t_{spi_k}	CSX rising to SCLK rising Note 2		0			ns
t_{spi_i}	CSX high pulse width Note 2		5			ns
$t_{spi_o_s_1V8}$	▪ MISO enable delay ▪ Falling CS to MISO stable ▪ C_{load} ≤ 20 pF	VDDIO < 2.25 V			28	ns
$t_{spi_o_s_2V5}$		VDDIO ≥ 2.25 V			17	ns
$t_{spi_o_s_3V3}$		VDDIO ≥ 3.0 V			13	ns
$t_{spi_o_s_5V0}$		VDDIO ≥ 4.5 V			11	ns

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Note 2					
$t_{spi_o_1V8}$	▪ MISO output delay ▪ Falling SCLK to MISO stable ▪ C_{load} ≤ 20 pF Note 2	VDDIO < 2.25 V			28	ns
$t_{spi_o_2V5}$		VDDIO ≥ 2.25 V			17	ns
$t_{spi_o_3V3}$		VDDIO ≥ 3.0 V			13	ns
$t_{spi_o_5V0}$		VDDIO ≥ 4.5 V			11	ns
$t_{spi_o_e_1V8}$	▪ MISO disable delay ▪ Rising CS to MISO disable ▪ C_{load} ≤ 20 pF Note 2	VDDIO < 2.25 V			16	ns
$t_{spi_o_e_2V5}$		VDDIO ≥ 2.25 V			11	ns
$t_{spi_o_e_3V3}$		VDDIO ≥ 3.0 V			9	ns
$t_{spi_o_e_5V0}$		VDDIO ≥ 4.5V			8	ns
$t_{spi_i_s}$	MOSI setup time Note 2				3	ns
$t_{spi_i_h}$	MOSI hold time Note 2				1	ns

Note 1 The maximum achievable SCLK frequency depends on the external delay at the SCLK and SDIO1 (MISO) signals. This delay depends on the SPI master (IOs of the driving MCU) and delays at the PCB. A total external round-trip delay for SCLK and MISO of 8n is assumed for this calculation. A 20pF capacitive load at SDIO1 is assumed for this scenario. PAD_DRV_STRENGTH = 1 is assumed.

Note 2 Parameter verified by design, not fully tested in production.

3.2.7. Monitoring

Table 10: Voltage monitors

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
$V_{THR_UV_1V8_OH}$	VDDD and VDDIO undervoltage detection rising edge threshold		1.66	1.7	1.74	V
$V_{THR_UV_1V8_OL}$	VDDD and VDDIO undervoltage detection falling edge threshold		1.55	1.62	1.7	V
$V_{THR_UV_5V_OH}$	5 V undervoltage detection rising edge threshold		4.56	4.68	4.8	V
$V_{THR_UV_5V_OL}$	5 V undervoltage detection falling edge threshold		4.45	4.56	4.7	V
$V_{THR_UV_24V_OH}$	VS and LPx undervoltage detection rising edge threshold		7.6	7.8	8	V
$V_{THR_OV_24V_OL}$	VS and LPx overvoltage detection rising edge threshold		36.2	37	38.1	V
$V_{THR_OV_24V_OH}$	VS and LPx overvoltage detection falling edge threshold		36	36.8	37.9	V
$V_{THR_UV_24V_OL}$	VS and LPx undervoltage detection falling edge threshold		7.4	7.6	7.8	V

Table 11: Temperature Monitor

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_{WARN_FALL}	Warning temperature falling edge Note 1			140		°C
T_{WARN_RISE}	Warning temperature rising edge Note 1			150		°C

Note 1 Parameter verified by design, not fully tested in production.

3.2.8. LEDs

Table 12: LED Driver

Parameter	Description	Conditions	Min	Typ	Max	Unit
f_{PWM}	PWM frequency	f_{OSC} = 14.7456 MHz		225		Hz
D	Output duty cycle Note 1		1		100	%
I_{OUT}	Typical value of LED output current	Set via LDRV_A and LDRV_B registers	2		20	mA
I_{OUT_ACC}	LED current accuracy	LED pin voltage 0.5 V ~ 3 V	-25		30	%

Note 1 Parameter verified by design, not fully tested in production.

4. Functional Description

4.1. Clocking

The IC is clocked by connecting an external 14.7456MHz crystal at the XTAL1 and XTAL2 pins.

A single crystal can be used to provide reference clock signals to multiple CCE4511. All CCE4511 must share the same VS and VDDIO supply for this feature. Figure 3 shows the recommended connection to share the same clock for multiple, maximum four CCE4511 devices.

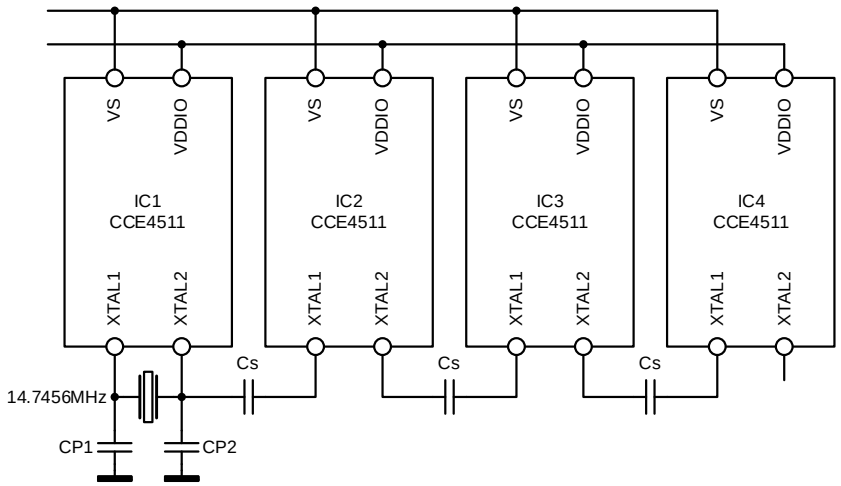


Figure 3. Daisy-Chaining Clock for Multiple CCE4511

Select C_S as 100 pF. C_{P1} and C_{P2} are there to provide the required load capacitance (C_L) for the crystal to resonate the target frequency, see the manufacturer's datasheet for the crystal for details. If the clock of the CCE4511 devices is not shared (C_S = 0), C_{P1} and C_{P2} can be calculated as:

$$C_{P1} = C_{P2} = 2C_L - 3C_{PX}$$

C_{PX} represents the parasitic capacitance to ground or supplies introduced by the PCB traces for the XTAL1 and XTAL2 signals and XTAL1 and XTAL2 pins of the CCE4511 respectively. If the crystal is placed close to the CCE4511 a value of $C_{PX} \approx$ 2 - 3pF can be assumed.

If the signals from XTAL2 is used to provide a clock to another CCE4511 via C_S, C_{P2} is calculated as:

$$C_{P2} = 2C_L - 4C_{PX}$$

The oscillators output frequency accuracy is constrained by the IO-Link timing requirements. Deviation from the nominal value must not exceed ±0.1%.

4.2. Power Supply

Two external supplies are required for the CCE4511.

The VS (24V) supply powers the internal voltage and current reference which is required for all other regulators (VDDD, VDDA) and analog circuitry (voltage monitors, temperature monitor, channels, charge pump).

A 5V voltage regulator with high-voltage input generates VDDA from VS. An external 1µF capacitor is required at VDDA to ensure stability of the voltage regulator, Renesas recommends an X5R or X7R MLCC capacitor.
Note: Do not connect external loads to VDDA!

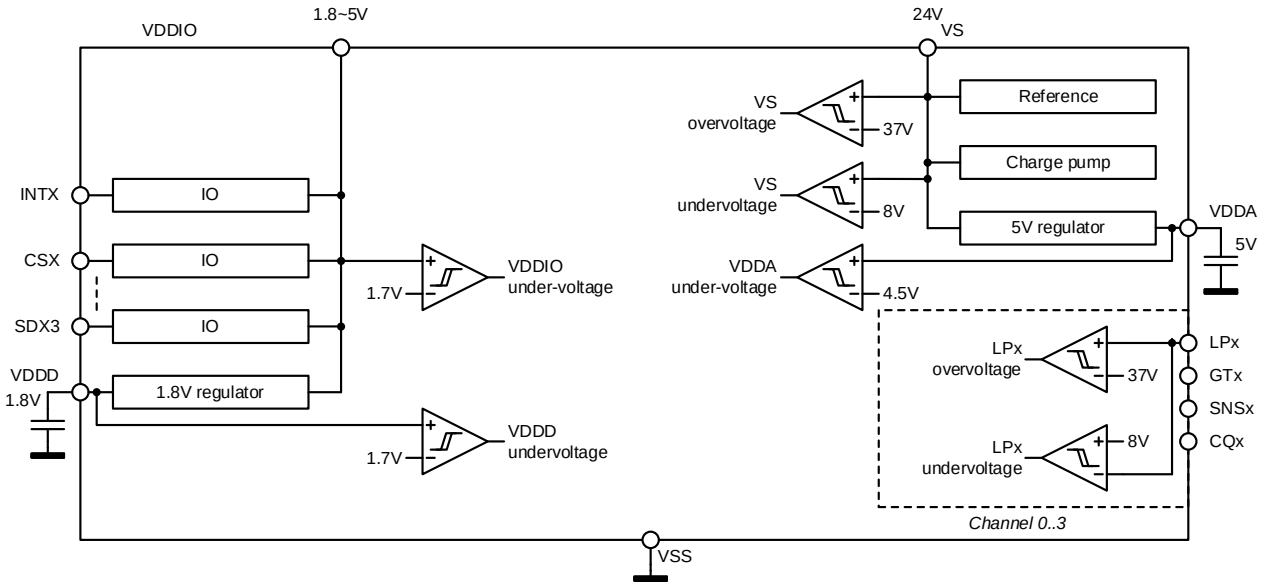


Figure 4. Power Supply and Monitor Diagram

VDDIO powers all digital IOs (INTX, CSX, SCLK, SDIO, TXEN, TXD, RXD, SDX) and the 1.8 V voltage regulator. If VDDIO is between 2.25 V and 5.5 V, the on-chip 1.8 V voltage regulator generates the VDDD supply for the internal logic. An external 4.7µF capacitor is required at VDDD to ensure stability of the voltage regulator, Renesas recommends an X5R or X7R MLCC regulator.
Note: Do not connect external loads to VDDD!

If VDDIO is supplied with 1.8 V, VDDIO and VDDD must be shorted externally, thus bypassing the 1.8V voltage regulator. VDDIO must then be between 1.75 V and 1.98 V. After power-up the 1.8 voltage regulator must be disabled by setting the VDDD_LDO_DIS bit in the CFG register. Configure the IO-cells by setting the PAD_DRV_STRENGTH bit in the CFG register to use high drive strength to guarantee the timings given in section 3.2.

VS and VDDIO can be powered-up in any order.

4.3. Temperature and Voltage Monitoring

Each supply is connected to an under-voltage monitor. The high-voltage supplies (VS, VLPx) are also connected to over-voltage monitors.

By default, the chip is configured to automatically disable all channels if the chip temperature is too high (see Table 11 for over-temperature settings) or the VS supply voltage is out of range.

If any LP voltage is below the under-voltage threshold, the corresponding CQ driver is disabled.

The corresponding interrupt flags can be read back from the INT_SRC_ENV and INT_SRC_STAT register. The automatic protection feature is controlled via the PROT register.

An on-chip temperature sensor signals if the CCE4511 temperature exceeds safe limits.

The internal logic is held in reset until VDDD and VDDA are above their under-voltage thresholds. If CHIP_RESET is written as 1, the internal logic is reset.

After a reset (power-on or CHIP_RESET), check that the CHIP_READY flag is set before using any channel. This ensures that all internal circuitry is up and running.

Be aware that the CCE4511 disables all external FET drivers by default after start-up. The Channel Registers contains non-deterministic values for some of their read-only fields if the corresponding channel is not supplied!

4.4. Operational Modes

There are three possible operational modes for each of the CCE4511 IO-Link Channels: Standard I/O (see section 4.4.1), UART (see section 4.4.2), and Frame Handler Mode (see section 4.4.3). Each channel's mode can be configured in the MODE field at any time.
The Automated Wake-up procedure can be used to wake-up an IO-Link device and to transition to the Frame Handler mode.

4.4.1. Standard I/O (SIO) Mode

If a channel is configured in the Standard I/O Mode, the state of the output stage is freely configurable. The DRV bits in the CFG1 register allows the user to choose between N-mode (PMOS always off), P-mode (NMOS always off), Push-Pull driving mode and CQ output disable. Depending on the status of the CSS bit, either TXD and TXEN pins or the CQ_OUT bit is used to control the CQ output stage. The SIO_RXD bit in the MISO status nibble (see section 4.12.4) and CQ_IN register bit always reflect the output of the CQ input buffer, see Figure 5.

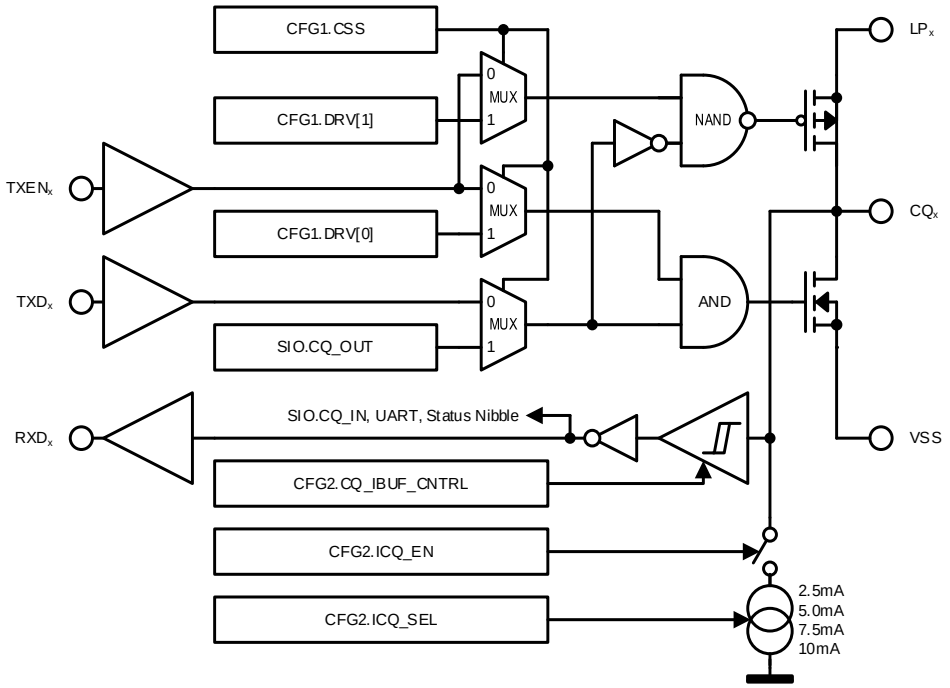


Figure 5. SIO Mode – CQ Driving Logic

In SIO mode an Automated Wake-up (see section 4.7.1) or Ready pulse detection (see section 4.7.2) can be started. These features ignore the status of the CSS bit and the DRV bits of the CFG1 register and control the CQ output directly.

4.4.2. UART Mode

If a channel is configured in UART Mode, the output stage is configured according to the DRV field in the CFG1 register. Its COM speed must be set in the CFG1 register.

By default, the channel listens for incoming UART transactions at the CQ pin. If a character is received, an interrupt is triggered, and the data can be read back from the UART register. A transmission is started by writing the data to the UART register.

The received UART data is not buffered. Receiving multiple characters while not reading them back, causes data loss that is indicated by the ERR bit in the MISO status nibble.

Use the IS_RX_REC and IS_RX_REC interrupt sources and the RXRDY status flag to identify if data was received or can be transmitted by the UART and to reduce the chance of data collisions.

4.4.3. Frame Handler Mode

The Frame Handler mode extends the UART mode. Like in UART mode, the output stage is configured according to the DRV field in the CFG1 register. The Frame Handler mode can be entered by using the Automated Wake-up procedure or by setting the MODE and COM field of the channels CFG1 register.

It automates the exchange of messages (M-sequences), defined by the IO-Link Interface and System Specification [1]. The checksum and parity information for Master Messages can be automatically calculated. Checksum and parity information of Device Messages are automatically verified. The Frame Handler will also monitor the specified timing constraints and takes care to comply with them as well, see section 4.5 for details.

4.5. Frame Handler

4.5.1. Message Sequence Configuration

In general, each IO-Link Message-Sequence (M-sequence) consists of a Master and a Device Message, the latter is also called Device Response. The Master Message starts with the M-sequence control (MC) octet followed by the checksum/M-sequence type (CKT) octet. Depending on the M-Sequence type defined in the CKT octet, the communication channel and the R/W bit (write direction) defined in the MC octet, process data is sent by the master. Depending on the R/W bit in the MC octet, the master or the device sends On-request Data (OD). Depending on the M-Sequence type defined in the CKT octet, the communication channel and the R/W bit defined in the MC octet, process data is sent by the device.

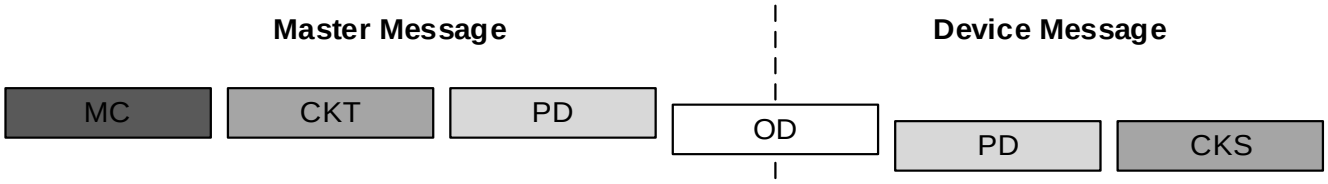


Figure 6. General M-Sequence Structure

The IO-Link Interface and System Specification [1] defines three valid M-sequence types (Type 0, Type 1 and Type 2).

The Frame Handler analyzes the MC and CKT octets sent to the Frame buffer (see section 4.5.2) to identify the M-sequence type, communication channel and write direction. Additional information is required for the Frame Handler to calculate how many octets need to be sent in the Master Message and how many octets to expect in the Device Message. This information needs to be stored in the MPD (master process data length), OD (On-request data length) and DPD (device process data length) registers.

M-sequences of Type 0 always transfer a single octet of On-demand data in the Master or the Device Message. Based on the data flow direction, the Frame Handle knows the number of octets to send in the Master Message and to receive in the Device Message.
The content of the MPD, OD, DPD registers is ignored if a Type 0 M-sequence is detected.

M-sequences of Type 1 always transfer either two octets of process data or two or more octets of On-request data. If a Type 1 message is to be sent or received, either MPD (master write) or DPD (master read) must be set to two if the process data communication channel is selected in the MC octet of the Master Message otherwise a non-standard compliant Master Message is sent, or a non-standard compliant Device Message is expected by the Frame Handler. If the process data Communication channel is not selected in the MC octet, the number of On-request data octets to be sent or received must be present in the OD register.

M-sequences of Type 2 contain process and On-request data. The Frame Handler reads the MPD, OD, and DPD registers to determine the number of process data octets to send in the Master Message (MPD), the number of On-request data octets to send or receive (OD, write direction) and the number of process data octets to receive with the Device Message.

If the M-sequence type in the CKT is set to 3, the Frame Handler expects one octet of On-request data to be sent or received [1]. This corresponds to the behavior for Type 0 M-sequences.

Note: The frame-subtypes for Type 1 and Type 2 M-sequences mentioned in A.2 of the IO-Link Interface and System Specification [1] are not explicitly set by the user and then evaluated by the Frame Handler. They are rather implicitly defined via the Communication channel field of the MC octet and the contents of the OD, MPD and DPD registers.

Examples:

- To initiate a master write M-sequence of TYPE_1_1, MPD has to be set to 2, the Communication channel field of the MC octet has to be set to 0 and the M-sequence type field of the CKT octet has to be set to 1. DPD and OD are ignored by the Frame Handler.
- To initiate a master read M-sequence of TYPE_1_2, OD has to be set to 2, the R/W bit of the MC octet to 1 and the Communication channel field of the MC octet to 1, 2, or 3. The M-sequence type field of the CKT octet has to be set to 1. The MPD and DPD registers are ignored by the Frame Handler.
- To initiate a master write M-sequence of TYPE_2_3, MPD and OD have to be set to 1, DPD has to be set to 0, the R/W bit of the MC octet to 0 and the M-sequence type field of the CKT octet to 2.
  The Communication channel field of the MC octet is ignored by the Frame Handler!
- To initiate a master read M-sequence TYPE_2_5, MPD, DPD and OD have to be set to 1, the R/W bit of the MC octet to 1, and the M-sequence type field of the CKT octet to 2.
  The Communication channel field of the MC octet is ignored by the Frame Handler!

4.5.2. Frame Buffer

Each channel has its own 66 Byte frame buffer to store master or Device Messages in a First-In-First-Out fashion. This eases the real-time requirements at the SPI interface. Data can be added to the frame buffer by writing the FHD register. Data can be fetched from the frame buffer by reading FHD.

The frame buffer is active if the IC is in Frame handler mode only. If the IC is not in Frame Handler mode or an Automated Wake-up procedure is running, data written to the FHD register is ignored and a read from the FHD register returns an undefined value.

The frame buffer can only contain a single Master Message which is sent by the Frame Handler via CQ or a single Device Message received via CQ, but not both at the same time. A write to FHD appends bytes to the Master Message in the frame buffer. Once a full Master Message is stored at the frame buffer, successive writes to the frame buffer are ignored until the Device Message was received and read via the SPI. If a full Device Message could not be received (for example, due to timeout), a Frame Handler SKIP or RESET is required to force the frame buffer into the idle state. If the frame buffer was set to the idle state, it is considered empty and new Master Message data is accepted by writing to FHD.

A read from FHD returns one byte of the Device Message stored in the frame buffer. Bulk read or write accesses to the FHD register can be used to transfer message data with minimal communication overhead at the SPI interface. If the FHD register is read and no Device Message data is available in the frame buffer, the returned value is undefined and must be ignored.

All Device Message data must be read via the SPI from the frame buffer before the next Master Message can be stored in the frame buffer.

The frame buffer can be reset to its idle state by a Frame Handler RESET or SKIP; see section 4.5.6.

4.5.3. Checksum

If the automatic checksum calculation is enabled, the Frame Handler calculates the 6-bit checksum of the Master Message in the frame buffer and overwrites the checksum value previously stored in the frame buffer. As the

[1] According to the IO-Link Interface and System Specification [1], Type 3 messages are reserved and shall not be used.

checksum is calculated over all bytes of the Master Message stored in the frame buffer, the full Master Message must be transferred to the frame buffer before it can be sent to the IO-Link device. The Master Message sent to the frame buffer does not need to have a valid checksum, the Frame Handler calculates and overwrites the checksum bits when sending the message.

The Frame Handler will always calculate the 6-bit checksum of the Device Message after the reception of the final UART frame of the Device Message and signals a checksum error if the calculated and the received checksum do not match.

4.5.4. Transceiver Modes

The Frame Handler decides upon the following criteria when an M-sequence can be started:

- Automatic Checksum enabled (CRC bit in the FHC register)
  - If enabled, a full Master Message must be available in the frame buffer before a transmission starts.
  - If disabled, a transmission can start as soon as at least one byte of the Master Message is available in the frame buffer.
- Synchronization enabled (SYNC_INT_EN or SYNC_EXT_EN bits in the FHC register)
  - If enabled, a synchronization event starts the Offset Timer. After the Offset Timer elapsed, a Master Message is sent if available in the frame buffer. If no adequate data is available in the frame buffer when the Offset Timer elapsed, no transmission is started.
- Cycle Timer enabled (CYCT register)
  - If enabled (CYCT register not zero), the Cycle Timer starts if a Master Message is available in the frame buffer or, if synchronization is enabled, a synchronization request is received.
  - If the Cycle Timer elapsed the next Master Message can be sent.

If an M-sequence is to be started (Cycle Timer elapsed or Offset Timer elapsed) and no Master Message data is available in the frame buffer, the Frame Handler ignores this event without triggering an error.

Figures in the following sections use the graphical representation shown in Figure 7. It illustrates the sequences of writing to and reading from the frame buffer as well as sending and receiving master and Device Messages via CQ and shows the frame buffer status.

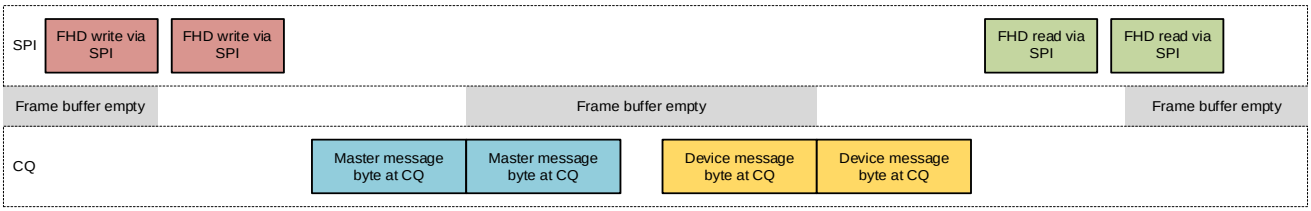
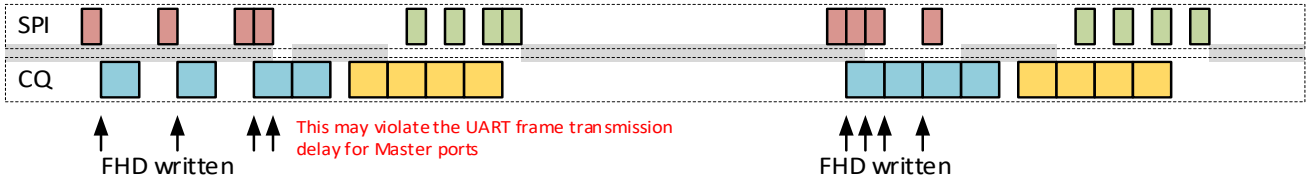


Figure 7. Accessing Framebuffer and CQ

4.5.4.1. Automatic Checksum Off, Synchronization Off, Cycle Timer Off

A byte written to the FHD register is immediately sent at the CQ pin. After the last byte of the Master Message was sent, the Frame Handler waits for the Device Message. A new Master Message can be sent after the Device Message was read from the frame buffer.



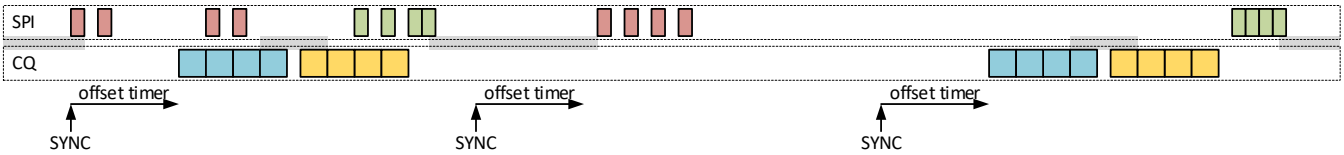
Legend: see Figure 7 for colors

Figure 8. Automatic Checksum Off, Synchronization Off, Cycle Timer Off

Note: The IO-Link specification requires a UART *"frame transmission delay for master ports"* (IO-Link Interface and System Specification [1], A.3.3) of maximum 1 T_{bit}. After a byte was transmitted at the CQ pin, the next byte must be available in the frame buffer at least 1 T_{bit} later or the sent Master Message is not compliant to the IO-Link standard.

4.5.4.2. Automatic Checksum Off, Synchronization On, Cycle Timer Off

If a synchronization request was received, the Offset Timer is started. When the Offset Timer elapsed, the Master Message in the frame buffer is sent via the CQ pin. If no data is available in the frame buffer when the Offset Timer elapsed, no data is sent.



Legend: see Figure 7 for colors

Figure 9. Automatic Checksum Off, Synchronization On, Cycle Timer Off

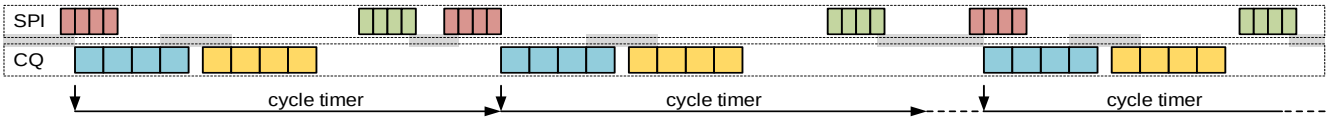
If a subsequent synchronization request is received and the offset time has not elapsed, this synchronization request is ignored. If the transmission of a Master Message started, synchronization requests are ignored until the Device Message was fetched from the frame buffer completely.

4.5.4.3. Automatic Checksum Off, Synchronization Off, Cycle Timer On

A byte written to the FHD register is immediately sent at the CQ pin. At the same time the Cycle Timer is started. After the last byte of the Master Message was sent, the Frame Handler waits for the Device Message.

If the Cycle Timer elapsed and at least one byte of the next Master Message is available in the frame buffer, the Cycle Timer is restarted and the data available in the frame buffer is sent at the CQ pin.

If the Cycle Timer elapsed and no Master Message data is available in the frame buffer, the Cycle Timer is stopped until a new byte was written to the frame buffer via the FHD register. Then the Cycle Timer is restarted and the Master Message bytes are sent via the CQ pin.



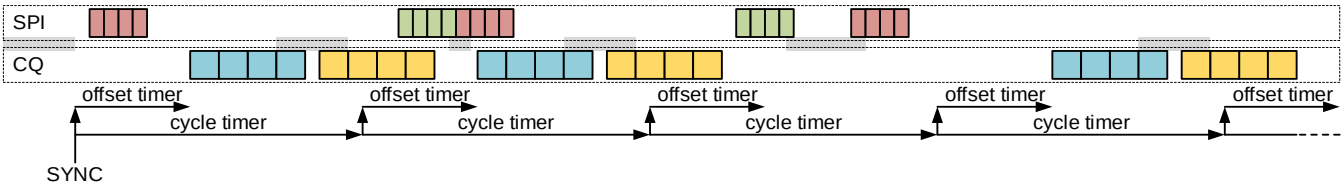
Legend: see Figure 7 for colors

Figure 10. Automatic Checksum Off, Synchronization Off, Cycle Timer On

4.5.4.4. Automatic Checksum Off, Synchronization On, Cycle Timer On

After an initial synchronization request was received, the Offset and Cycle Timers are initially started. When the Offset Timer elapsed, an available Master Message in the frame buffer is sent via the CQ pin. Transmission starts if at least one byte of a Master Message is available in the frame buffer. It is up to the user to write the remaining bytes of the Master Message fast enough to the frame buffer to not violate the UART frame transmission delay for master ports. If no Master Message data is available in the frame buffer when the Offset Timer elapsed, no UART frames are sent during this cycle. After the last byte of the Master Message was sent, the Frame Handler waits for the Device Message.

After the Cycle Timer elapsed, the process starts over by starting the Offset Timer and restarting the Cycle Timer.
Note: the Offset Timer timeout must not exceed the Cycle Timer timeout, otherwise the behavior of the Frame Handler is undefined.



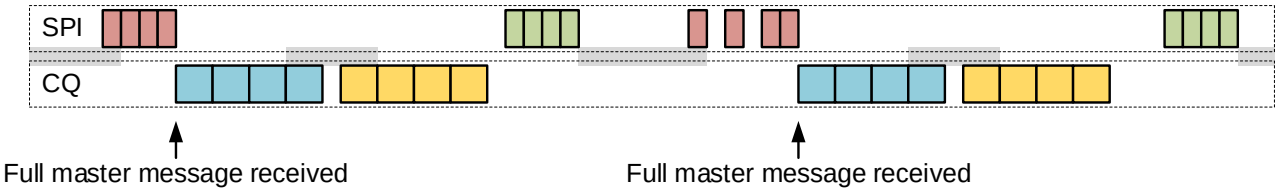
Legend: see Figure 7 for colors

Figure 11. Automatic Checksum Off, Synchronization On, Cycle Timer On

While the Cycle Timer is running, additional synchronization events are ignored. The Cycle Timer keeps running until the Frame Handler is reset or the Cycle Timer gets disabled. A Frame Handler SKIP does not disable or reset the Cycle Timer.

4.5.4.5. Automatic Checksum On, Synchronization Off, Cycle Timer Off

Once a full Master Message is written to the frame buffer via the FHD register, the message is sent via the CQ pin. After the last byte of the Master Message was sent, the Frame Handler waits for the Device Message. A new Master Message can be sent after the Device Message was read from the frame buffer.

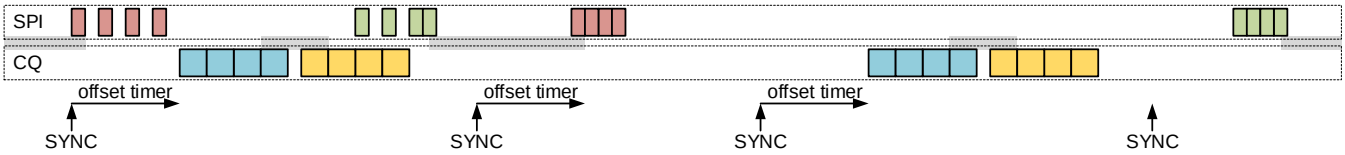


Legend: see Figure 7 for colors

Figure 12. Automatic Checksum On, Synchronization Off, Cycle Timer Off

4.5.4.6. Automatic Checksum On, Synchronization On, Cycle Timer Off

If a synchronization request was received, the Offset Timer is started. When the Offset Timer elapsed, the Master Message in the frame buffer is sent via the CQ pin. If no full Master Message is available in the frame buffer when the Offset Timer elapsed, no data is sent.



Legend: see Figure 7 for colors

Figure 13. Automatic Checksum On, Synchronization On, Cycle Timer Off

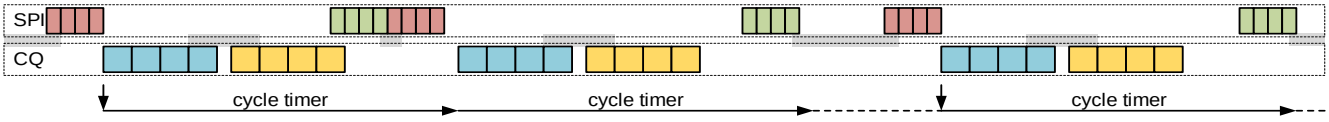
If a subsequent synchronization request is received and the offset time has not elapsed, this synchronization request is ignored. If the transmission of a Master Message started, synchronization requests are ignored until the Device Message was fetched from the frame buffer completely.

4.5.4.7. Automatic Checksum On, Synchronization Off, Cycle Timer On

After a full Master Message was written to the frame buffer via the FHD register, the message is immediately sent at the CQ pin and the Cycle Timer is started. After the last byte of the Master Message was sent, the Frame Handler waits for the Device Message.

If the Cycle Timer elapsed and a full Master Message is available in the frame buffer, the Cycle Timer is restarted, and the Master Message is sent at the CQ pin.

If the Cycle Timer elapsed and no full Master Message is available at the frame buffer, the Cycle Timer is stopped until a full Master Message was written to the frame buffer. Thereupon the Cycle Timer is restarted, and the Master Message is sent via the CQ pin.

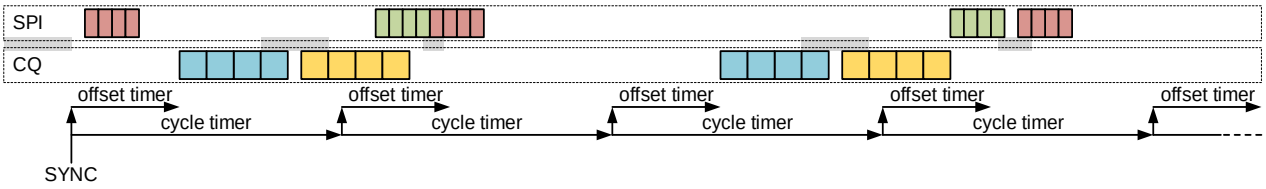


Legend: see Figure 7 for colors

Figure 14. Automatic Checksum On, Synchronization Off, Cycle Timer On

4.5.4.8. Automatic Checksum On, Synchronization On, Cycle Timer On

After an initial synchronization request was received, the Offset and Cycle Timers are initially started. When the Offset Timer elapsed, the Master Message available in the frame buffer is sent via the CQ pin. If no full Master Message is available in the frame buffer when the Offset Timer elapsed, no data is sent during this cycle. After the last byte of the Master Message was sent, the Frame Handler waits for the Device Message.
After the Cycle Timer elapsed, the process starts over by starting the Offset Timer and restarting the Cycle Timer. Note: the Offset Timer timeout must not exceed the Cycle Timer timeout, otherwise the behavior of the Frame Handler is undefined.



Legend: see Figure 7 for colors

Figure 15. Automatic checksum on, synchronization on, cycle timer on

While the Cycle Timer is running, additional synchronization events are ignored. The Cycle Timer keeps running until the Frame Handler is reset or the Cycle Timer gets disabled. A Frame Handler SKIP does not disable or reset the Cycle Timer.

4.5.5. M-Sequence Handling

Interrupts can be configured to trigger after parts of or the complete Device Message are received. The interrupt behavior can be modified using the INT_* and TLVL register, see section 4.6.

Parity or checksum errors in the received Device Message are indicated by the Status Nibble error flag and the STATUS_MODE_FH.STATE register. The erroneous Device Message is stored in the frame buffer.

The Frame Handler checks the following timing constraints of the IO-Link Interface and System Specification [1]:

- UART frame transmission delay of Master ports (Annex A.3.3 in [1]), t1
- UART frame transmission delay of Devices (Annex A.3.4 in [1]), t2
- Response time of Devices (Annex A.3.5 in [1]), tA

If any of these timing constraints are violated by the M-sequence (Master and/or the Device Message), a timeout is flagged.

According to the IO-Link Interface and System Specification [1] (Annex A.3.5, Response time of Devices) the device is expected to respond within 1 $T_{BIT} \leq t_A \leq 10\ T_{BIT}$ after the Master Message was sent. However, some IO-Link busses in the field violate this constraint. To be able to support such devices, the TOUT_RESPONSE_RLX bits in the CFG3 register can be used to extend the timeout.

To allow support for devices which violate the UART frame transmission delay (t_2), the threshold used by the Frame Handler to check for this timeout can be relaxed using the TOUT_GAP_RLX bits in the CFG2 register.

4.5.6. States, Skip, and Reset Function

The Frame Handler is implemented as a finite-state-machine (FSM) which is either idle, transmitting a Master Message, or receiving a Device Message (see Figure 16).

In IDLE mode the Frame Handler waits for Master Message Data to be available in the frame buffer, the expiry of the offset or Cycle Timer depending on the transceiver modes (see section 4.5.4). The Frame Handler is sending data at CQ only TRANSMIT mode. The Frame Handler is waiting for or receiving and storing Device Message data to the frame buffer only in RECEIVE mode.

Setting the RST or the SKIP bit of the FHC register immediately resets the FSM to the idle state by aborting the transmission of a Master Message or reception of the Device Message. . Data present in the frame buffer is rejected but the Frame Handler configuration (FHC, MPD, OD, DPD) is retained. If the RST bit is set, the SKIP bit is ignored. If RST is set to one, the Cycle Timer is also reset. If only the SKIP bit is set, the Cycle Timer is left untouched, see Table 13.

The Frame Handler is also reset while it is not in the idle state and:

- the FHC register is written and the SKIP bit is not set,
- or the Cycle Timer is enabled or disabled,
- or any of the OD, MPD and DPD registers are written.

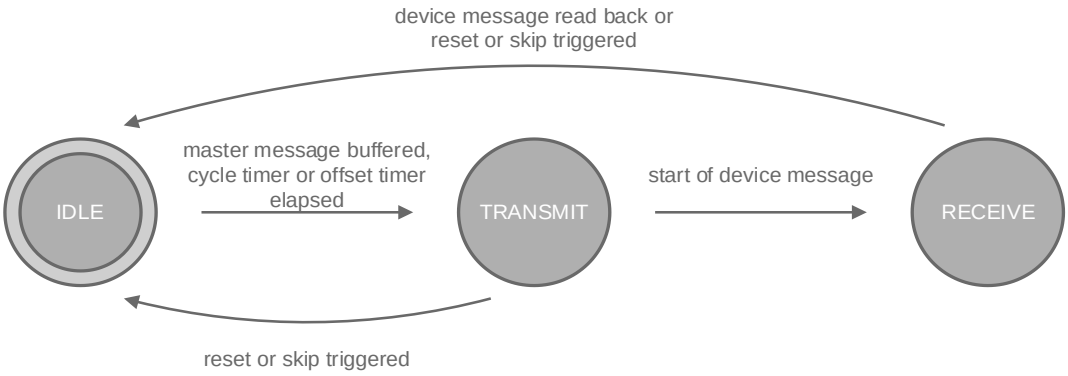


Figure 16. Frame Handler State Machine Diagram

Table 13: States Influenced by Frame Handler SKIP or RST

State	FH SKIP	FH RST
Communication speed (COM)	Retained	Retained
Framebuffer	Data invalidated, ready to receive new Master Message via SPI	Data invalidated, ready to receive new Master Message via SPI
MPD, OD, DPD registers	Retained	Retained
Cycle Timer	Keeps running	Reset, timer needs to be restarted
CYCT register	Retained	Retained
Offset Timer	Reset	Reset
Offset Timer register	Retained	Retained

4.5.7. Cycle Timer

A Cycle Timer is available for channels configured in Frame Handler mode. It enables the user to comply with the configured IO-Link cycle times without further effort. The cycle time is set up in the CYCT register. The format of this register resembles the defined structure in the IO-Link Interface and System Specification [1].

Renesas does not recommend to configure cycle times that are shorter than 400µs which is the minimum cycle time stated by the standard (IO-Link Interface and System Specification [1], A.3.7). To disable the Cycle Timer, set the register to zero.

By setting the SKIP bit in the FHC register, the Frame Handler can be reset without affecting the Cycle Timer: the Cycle Timer is stopped and internal counter resets to zero (see section 4.5.6). The CYCT register content does not change due to a Frame Handler reset.

If the Cycle Timer is disabled (CYCT set to 0), a write to the CYCT register does not start the Cycle Timer. A trigger to start the transmission of a Master Message is required to start the Cycle Timer (see section 4.5.4).

If the Cycle Timer is already running and a new value is written to the CYCT register, the Cycle Timer uses the new value after the current timeout period elapsed.

If the Cycle Timer started, a new Master Message is not sent until the configured cycle time (and the Offset Timer if enabled) has elapsed.

4.5.8. Synchronization

The start of transmission can be triggered by an external signal or by writing to the STx bits of the SYNC register.

Synchronization to an external signal can be enabled by setting the SYNC_EXT_EN bit in the FHC register. Each channel can select one of the TXD [3:0] pins as synchronization source via the SYNC_SRC_SEL bits. If enabled, a rising or falling edge initiates the start of transmission. The SYNC_EDGE bit selects the active edge of the synchronization signal. The synchronization pulse must be at least 150ns wide to be properly detected.

If the SYNC_INT_EN bit in the FHC register is set, the start of transmission can be triggered by writing the STx bit of the SYNC register. Writing ’1’ to the STx bit, channel x starts the transmission of a message as described in section 4.5.4.

4.5.9. Offset Timer

To delay the start of transmission of a Master Message, the Offset Timer (SOTO_TIMER) can be used. This allows to align the start of a Device Message across multiple channels. This requires knowing the delay between the start of the Master Message and the start of the Device Message.
Note: this is an experimental feature and the mentioned delay is device dependent and not part of the IO-Link IODD specification.

The Offset Timer timeout can be set by the SOTO_PRESCALER field and WRP_SOTO_TIMER register.

4.6. Interrupt Handling

There are four interrupt source registers for each channel and one global interrupt source register: INT_SRC_STAT, INT_SRC_SIO, INT_SRC_UART, INT_SRC_FH, and INT_SRC_ENV. They can be individually enabled by configuring their corresponding interrupt enable registers. All enabled interrupt flags from the four channels are logically “or”ed and the inverted result is connected to the pin INTX. By default, all interrupt sources are disabled at startup and there is no global interrupt enable. If the CSS bit is set, the SDX pins output the interrupt information of the corresponding channel and can be used by the microcontroller to quickly identify the interrupt-source.

The interrupt source bits are always set when a transition to the active state is observed at the related signals. The interrupt source bits are set even if the interrupt sources are disabled by the enable bits. To clear an interrupt, the MCU must read the related interrupt source register. Note: that all bits of this interrupt source register are cleared by the read of the register.

See Table 14, Table 15, and Table 16 for the interrupt sources for the each available channel modes. See Figure 17 for the interrupt sources that are available in Frame Handler mode.

Table 14: SIO Interrupt Sources

Interrupt	Name	Condition
IS_RP_ERR	Ready-pulse error interrupt	Error during ready-pulse detection
IS_READY_DET	Ready-pulse Interrupt	Valid ready-pulse detected

Interrupt	Name	Condition
IS_CQ_FALL	CQ-Fall Interrupt	Falling edge at Pin CQ is detected
IS_CQ_RISE	CQ-Rise Interrupt	Rising edge at Pin CQ is detected

Table 15: UART Interrupt Sources

Interrupt	Name	Condition
IS_RX_OFLW	UART overflow interrupt	UART byte received but previously received byte nat read via SPI from the UART register
IS_RX_REC	UART receive interrupt	UART has received one byte
IS_TX_RDY	UART TX-ready interrupt	UART is ready to send data

Table 16: Frame Handler Interrupt Sources

Interrupt	Name	Condition
IS_ERR	Error interrupt	Checksum or parity error received
IS_EOC	End of cycle interrupt	The Cycle Timer has elapsed
IS_WURQ	Wake-up-request interrupt	Wake-up procedure has finished
IS_TOUT	Timeout interrupt	Timeout has been detected, see section 4.5.5.
IS_SOT	Start of transaction interrupt	Transmitting of a Master Message started
IS_SOR	Start of reception interrupt	Receiving a Device Message started (received start bit of the UART frame).
IS_LVL	Message level interrupt	Number of Device response bytes received reaches the threshold in CFG4.TLVL
IS_MSG	End of message interrupt	Last octet of a valid Device Message received

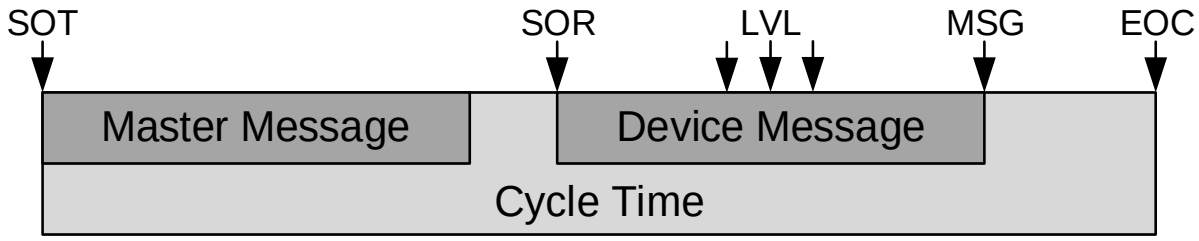


Figure 17. Interrupt Trigger Positions

The IS_LVL interrupt source is triggered if the number of Device Message octets received reached the value given in CFG4.TLVL. The current number of octets in the frame buffer can be queried in the BLVL register of the channel.

4.7. Additional IO-Link Related Features

4.7.1. Automated Wake-up

The automated wake-up procedure is started if the channel is configured in SIO mode and 2'b01 is written to the STARTUP_SEQ bits in the SIO register. The CSS bit in the CFG1 register is ignored during the automated wake-up procedure and the TXEN and TXD pins do no longer control the CQ pin of the channel running the procedure. If the procedure is active, the STARTUP_SEQ bits read 2'b01. An active wake-up procedure can be aborted by writing a non-zero value to the STARTUP_SEQ bit.

During the procedure, the channel is set into Frame Handler mode and runs the wake-up procedure which complies to the IO-Link standard (IO-Link Interface and System Specification [1], section 7.3.2.2). After the procedure is finished, a WURQ interrupt is set, the CQ pin is automatically configured as push-pull output and the channel stays in Frame Handler mode. During the wake-up procedure the master sends data to the device and waits for a Device Message starting at the highest communication speed (COM3). If the device does not

reply, the same message is sent again at the next lower communication speeds (COM2, COM1) until the device answers. Timing constraints are ignored by the wake-up procedure and considered invalid if the Device responses with an invalid checksum, a wrong parity bit, or violation of the Response time of Devices or UART frame transmission delay of Devices [2],. If no valid Device response was received during the wake-up procedure, the corresponding error flags of the Frame Handler and the ERR flag in the MISO status nibble are set. The channel stays in Frame Handler mode even if the wake-up procedure finished with an error condition. The COM setting of the Frame Handler is altered by the wake-up procedure.

If the wake-up procedure succeeds, the FH_RXD flag in the MISO status nibble (see section 4.12.4) is set and the Frame Handler uses the detected COM mode which can be read back from the CFG1 register. Note that the FH_RXD flag of the MISO status nibble is cleared if the Frame Handler is reset, for example, by the AUTO_SKIP feature. For this reason, the use of the AUTO_SKIP feature is discouraged.

Note: if the AUTO_SKIP feature after wake-up is disabled, the data received from the device during Wake-Up has to be read from the frame buffer before writing new data to the FHD register. The first Master Message written to the frame buffer after the Automated Wake-Up succeeded is sent to the device after a sync-event happens. To comply to the minimum recovery time (see IO-Link Interface and System Specification [1], section A.3.9), the message is not sent before the 100TBIT have elapsed if the sync-feature is disabled. If a cycle time is configured, its timer starts 100TBIT after the Automated Wake-Up succeeded.

Table 17: MISO Status Nibble Bits, STARTUP_SEQ Set to 2'b01 (Wake-Up Procedure)

FH_RXD	ERR	S_MODE	Status
0	0	0	Wake-up current pulse is sent
0	0	1	Wake-up procedure running.
1	0	1	Wake-up procedure succeeded
0	1	1	Wake-up procedure failed due to timeout

4.7.2. Ready Pulse Detection

The IO-Link Safety System Extensions with SMI Specification [2] specifies a ready pulse which is sent by a functional safety IO-Link Device after power-up to indicate that it successfully passed internal safety related checks. If the STARTUP_SEQ bits in the SIO register are set to 2'b10, the CCE4511 runs the ready pulse detection. This enables the channel's gate driver (for the external NMOS LP switch), waits for the under-voltage at LP to disappear and is then ready to detect the Ready pulse.

The timeout for waiting for a Ready pulse can be set via the WRP_SOTO_TIMER register.

If the Ready pulse detection fails (that is, timeout waiting for the Ready pulse), the ERR bit of the MISO status nibble is set. If the Startup Sequencer was able to detect a Ready pulse, the FH_RXD bit of the MISO status nibble is set.

If both bits of STARTUP_SEQ are set in the SIO register in a single register write, the CCE4511 starts the Ready pulse detection and, if this finished successfully, starts the Automated Wake-up sequence after the maximum "End of Ready pulse to ready for Wake-up"-time tRW.

Table 18: MISO Status Nibble Bits, STARTUP_SEQ Set to 2'b10 (Ready Pulse Detection)

FH_RXD	ERR	S_MODE	Status
0	0	0	Ready pulse detection running
1	0	0	Ready pulse detection succeeded
0	1	0	Ready pulse detection failed

Table 19: MISO Status Nibble Bits, STARTUP_SEQ Set to 2'b11 (Wake-up + Ready Pulse Detection)

FH_RXD	ERR	S_MODE	Status
0	0	0	Ready pulse detection running

[2]See IO-Link Interface and System Specification [1], Annex A.3

0	1	0	Ready pulse detection failed; no wake-up procedure is done
1	0	0	Ready pulse detection succeeded, and wake-up current pulse is sent
0	0	1	Ready pulse detection succeeded and wake-up procedure running
1	0	1	Ready pulse detection and wake-up succeeded
0	1	1	Ready pulse detection succeeded and wake-up failed with timeout

4.8. Overcurrent Protection

The LPx supply current (ILPX) can be monitored by an external shunt resistor to shut down the LPx supply and power down the device if safe limits are exceeded, see section 4.8 and Figure 18.

The currents of the CQ output transistors (ICQxP, ICQxN) of each channel are monitored to signal excessive current through these devices, see section 4.10.2.

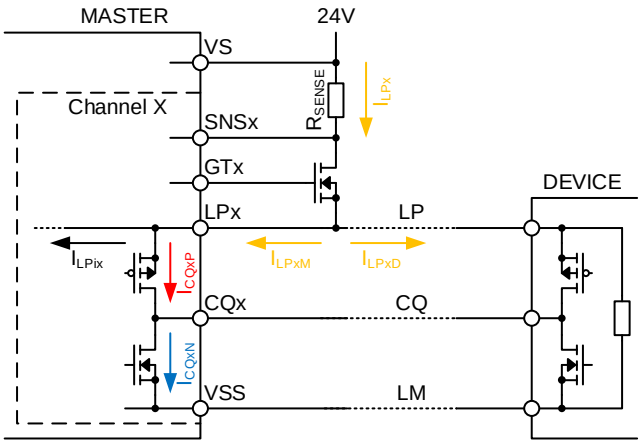


Figure 18. Over-Current Detection

4.9. LPx Switch and Current Sense

An external NMOS can be used to switch the LP voltage of each channel individually. GTEN controls whether the external switch is turned on or off.

4.9.1. Without Current Limit

When the external NMOS is to be switched on, the GTx pin of the channel sources I_{GATE_CHG} (20 µA) to charge the gate of the external NMOS to V_{VS} + 10 V.

4.9.2. Current Limits

If LPX_CLA_EN is set, the external NMOS gate voltage is regulated, so that the voltage drop across the external sense resistor (R_{SNS}) never exceeds V_{SENSE_LIM}. This limits the current through the sense resistor to V_{SENSE_LIM}/R_{SNS}. The current used to regulate the gate charge of the external NMOS does not exceed $\pm I_{GATE_CHG}$.
Note: limit the thermal stress to the external NMOS in this case.

If the external NMOS is to be switched off by clearing GTEN, the GTx pin is connected to LPx internally by a resistor (R_{GATE_DIS}).

On-chip protection limits the GTx pin voltage to V_{GT_LIM}.

To ensure stability of the current limit feature for a wide range of applications, an external compensation network (100 kΩ resistor and 470 pF cap in series) at GTx is required.

4.9.3. LPx Overcurrent Detection

The LPx current sensing can detect high supply currents to the connected IO-Link device and the associated channels IO-Link stage. The following two separate mechanisms are implemented:

- LPx overcurrent function (controlled via LPX_OVC_EN)
- LPx current limit function (controlled via LPX_CLA_EN).

Both functions are enabled by default and require an external shunt to sense the LPx current. If LPX_OVC_EN is enabled, an over-current (I_{SENSE_OVC}) is flagged if the voltage across this resistor exceeds V_{SENSE_OVC} (240 mV). After a time of $t_{LPXOVCDET}$, GTEN is set to '0' and the GTx pin is forced to LPx and shutting off the external NMOS for a time of $t_{LPXOVCDIS}$. After that time, the external NMOS is automatically switched on again. This feature can be disabled via LPX_OVC_POWER_ON. Register LPX_OVC_TIME defines the two timeout values.

If LPX_CLA_EN is enabled, a current limit is flagged if the voltage across the resistor exceeds V_{SENSE_LIM}. After a time of $t_{LPXCLADET}$, GTEN is set to '0' and the GTx pin is forced to LPx and shutting off the external NMOS for a time of $t_{LPXCLADIS}$. After that time, the external NMOS is automatically switched on again. This feature can be disabled via LPX_CLA_POWER_ON. Register LPX_CLA_TIME defines the two timeout values.

If an over-current was detected, the IS_LPX_OVC interrupt source is set. If the channel was disabled due to over-current, the IS_CH_DIS_LPX_OVC interrupt source is set.

If the LPx current limit is active, the IS_LPX_CLA interrupt source is set. If the channel was disabled due to an active current limit, the IS_CH_DIS_LPX_CLA interrupt source is set.

The value of the shunt resistor must be selected to provide the current limits required by the application:

$$R_{SENSE} = \frac{V_{SENSE_OVC}}{I_{SENSE_OVC}} = \frac{240mV}{I_{SENSE_OVC}}$$

For example, for an over-current detection threshold of 1 A, a 240 mΩ shunt is required.

4.10. CQ Input and Output Stage

4.10.1. Input Buffer

The input buffer converts the voltage at the CQ pin to a logic value (0 or 1). As the supply voltage range of the CCE4511 exceeds the range required by IO-Link specification, the input buffer not only implements a comparator for the CQ pin voltage using fixed thresholds (V_{THH_IOLF}, V_{THL_IOLF}, as required by the IO-Link Interface and System Specification [1]) but also a comparator with thresholds ratiometric to the LP voltage of the corresponding channel (V_{THH_IOLR}, V_{THL_IOLR}), see Figure 19.

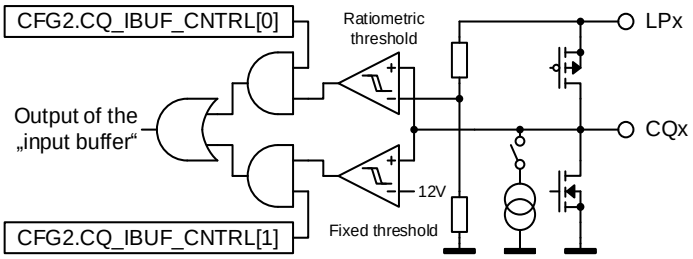


Figure 19: CQ Input Buffer

If both comparators are enabled by the CFG2.CQ_IBUF_CNTRL register, the ratiometric input buffers thresholds is used at supply voltages below ~20V. At supply voltages above ~20V, the fixed thresholds are active as required by the IO-Link Interface and System Specification [1]. This allows to use the input buffer at the full supply voltage range. Figure 20 shows the input buffer thresholds vs. supply voltage if both comparators are enabled.

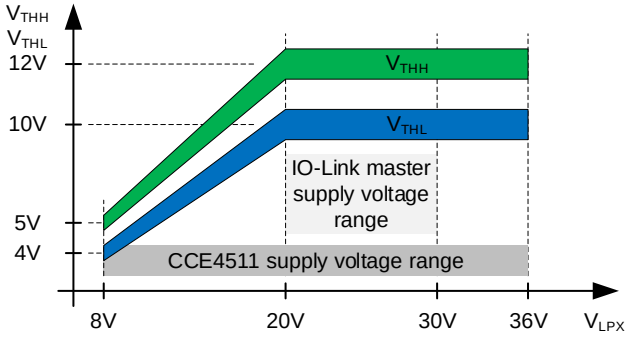


Figure 20: CQ Input Buffer Thresholds vs. Supply Voltage

The CFG2 CQ_IBUF_CNTRL in Register CFG2 allows to enable the fixed threshold CQ input buffer and ratiometric CQ input buffer individually.

Note: If both thresholds are disabled (CQ_IBUF_CNTRL=0), the input function at the CQ pin is disabled. The CQ pins are low internally. Reception of UART frame or the detection of the logic state of the CQ pin in SIO mode is no longer possible until any of the input thresholds is enabled again.

4.10.2. Current Limit and Overcurrent Detection

The forward current through the CQ output PMOS (I_{CQxP}) and NMOS (I_{CQxN}) transistors is monitored. This current is internally limited to I_{CQ_LIM}. The current limit can be disabled via CQ_CLA_EN.

If I_{CQx} exceeds I_{CQ_OVC} while the corresponding transistor is switched on, an over-current is flagged and the IS_CQ_OVC interrupt source is set. If the channel was disabled due to an over-current, the IS_CH_DIS_CQ_OVC interrupt source is set. The over-current detection can be disabled via CQ_OVC_EN.

If CSS is zero, the SDX pin of a channel is pulled low if an over-current or current limit event is detected at CQ or at the SNS pin. Note that if CSS is set, the SDX pins carry the interrupt information of the corresponding channel and can be used to quickly identify the interrupt-source.

The output transistor of a channel is automatically disabled if the transistor's currents exceed the over-current threshold for a time greater than $t_{CQOVCDET}$. The channel stays disabled and gets re-enabled after a time $t_{CQOVCDIS}$. If the over-current condition at CQ still persists, the channel is disabled again. This high current polling reduces the power dissipation of the chip and reduces the risk of overheating. Timing is configured in the CQ_OVC_TIME register.

4.10.3. Current Sink

The IO-Link Interface and System Specification [1] mandates a current sink (ILL_M) at the CQ output of master ports. In the CCE4511 this current sink can be activated using the ICQ_EN register. The sink current can be selected via ICQ_SEL. If the CCE4511 drives the CQ line high, the current sink is deactivated, else it is activated if ICQ_EN is set.

4.11. LED Drivers

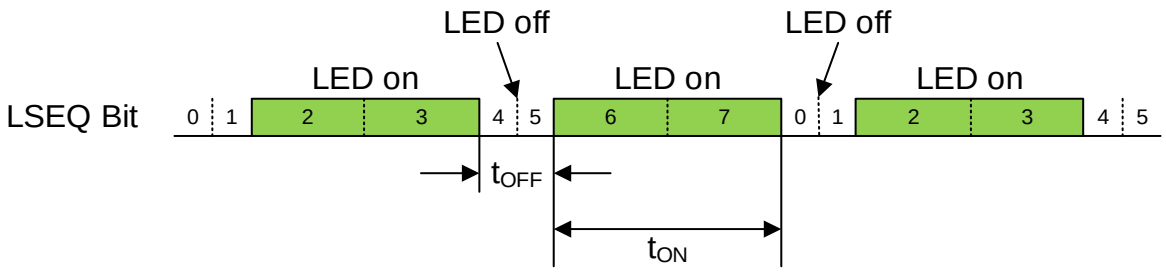
The chip integrates two LED drivers for each of the channels (labeled as *A and *B). Each LED output is controlled by three registers (LSEQ_A, LSEQ_B, LHLD_A, LHLD_B, LDRV_A, LDRV_B).

The LED forward current can be adjusted, and the output can use a PWM to be dimmed via LDRV_A and LDRV_B registers.

An 8-bit pattern can be programmed for each LED by the registers LSEQ_A and LSEQ_B. Each LSEQ_* register is read from LSB to MSB starting at bit 0 (1: LED is on, 0: LED is off). After bit 7 was read, the pattern starts over at bit 0.

The LHLD_A and LHLD_B registers define the time the LED is turned on or off for each bit in the LSEQ_* registers. As an example, writing LSEQ=0xCC and LHLD=0x80 resemble the specified blinking sequence for

channels that operate in IO-Link mode, starting with the “LED off” state (IO-Link Interface and System Specification [1], 10.10.3).



Calculation of the LED sequence timing:

t_{LO} = 50ms + 50ms × HLDL = 50ms

t_{OFF} = 2 × t_{LO} = 100ms

t_{HI} = 50ms + 50ms × HLDH = 450ms

t_{ON} = 2 × t_{HI} = 900ms

Figure 21: IO-Link LED Timing

By writing the LED_SYNC register, the pattern of an LED output restarts at index 0 if the corresponding bit is set. This allows to synchronize the LED ‘blink’-sequences across the LED outputs.

4.12. Serial Peripheral Interface

To read and write registers of this device, a synchronous serial interface (SPI) is provided. Traditionally, an SPI interface consists of an active-low ChipSelect (CSX), SerialClock (SCLK), MasterOutSlaveIn (MOSI) and MasterInSlaveOut (MISO) line, which allows to send and receive a single bit during each clock period.

The CCE4511 acts as an SPI slave, an SPI master is required to provide the ChipSelect and SerialClock signal.

4.12.1. SPI Transaction Format

The CCE4511 is designed as SPI slave and uses the CPOL=0, CPHA=0 configuration. During each transaction, a minimum number of two bytes should be transferred. For bulk access to the registers (for example Frame Handler buffers via the FHD), multiple bytes can be transferred in a single SPI frame.

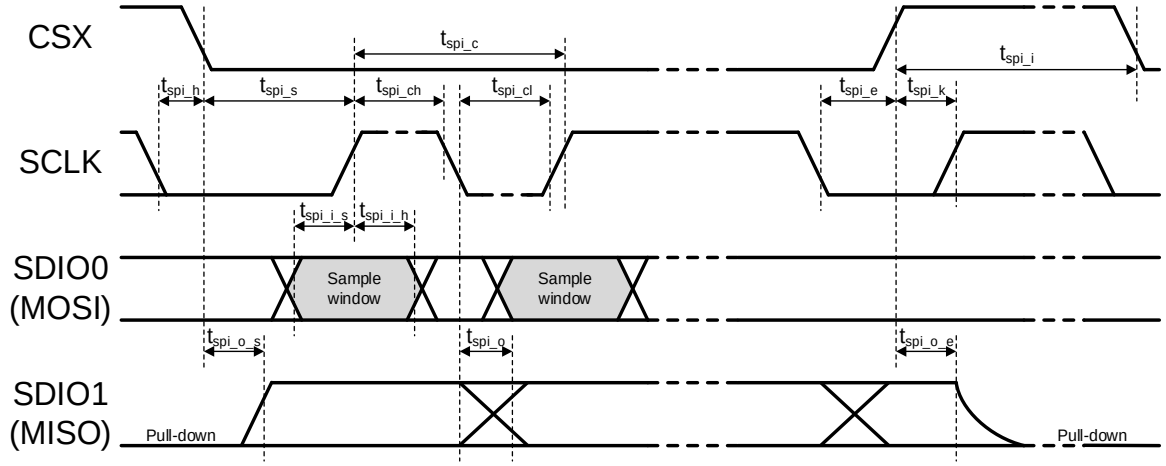


Figure 22: SPI Timing Diagram

4.12.2. SPI Frame

The first SPI frame starts with a falling edge of the CSX pin. The SPI interface then reads an 8-bit address-byte, followed by an 8-bit command-byte. Each bit is sampled at SDIO0 (MOSI) at the rising edge of the SCLK pin. MSB is transmitted first (see Figure 24 and Figure 25). The LSB of the command-byte defines if registers are

read (high) or written (low) with this SPI frame. The remaining bits of the command-byte define the address-mode and the number of data bytes that follow the command-byte. See Table 22 and Table 23 for a detailed description.

An SPI frame ends either with a rising edge of the CSX-pin or after the number of data-bytes that are specified in the command-byte have been transmitted. If the CSX-pin stays low, a new SPI frame starts immediately and the address-byte, followed by the command byte, is transmitted.

Address-byte	Command-byte	Data-byte 1	…	Data-byte n

Figure 23: Basic SPI Frame Structure

If registers are read by an SPI frame, the MSB of this register is present at SDIO1 (MISO) after the first falling edge at SCLK after the last bit of the command-byte was latched. Multiple registers can be read in the same SPI read frame depending on the number of data bytes configured via the command-byte. Depending on the configured address-mode, the address is incremented before the next register is present at SDIO1.

On SDIO1 (MISO), the first 2 bytes of a frame always reflect the current state of all four channels.

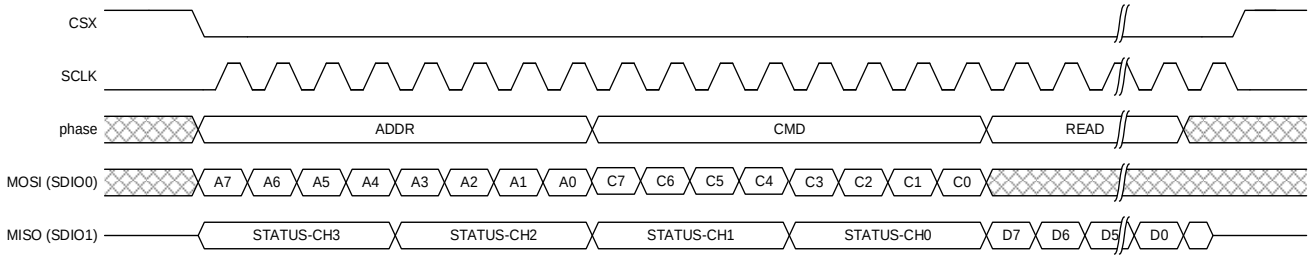


Figure 24: SPI Read Frame

If registers are to be written by an SPI frame, the MSB of the data to write follows the LSB of the Command-byte. The register is written after the LSB of the write data was received. Multiple registers can be written in the same SPI write frame depending on the number of data bytes configured via the command-byte. Depending on the configured address-mode, the address is incremented after the LSB of the write data was received. The MISO line returns the STATUS nibble bits during the first 16 clock cycles and is driven to undefined values during the remaining clock cycles of a frame.

An SPI frame can be aborted by pulling the CSX pin high while SCLK is in the idle state (low).

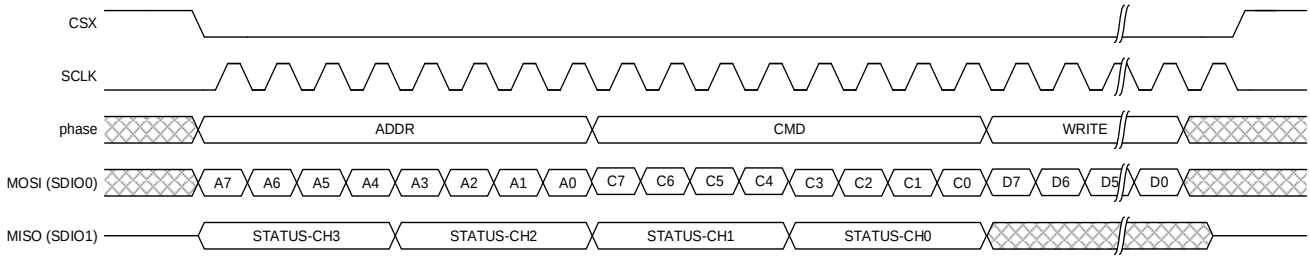


Figure 25: SPI Write Frame

Table 20: Address Byte Structure

Description	REG_ADDR							
Address-byte	A7	A6	A5	A4	A3	A2	A1	A0

Table 21: Command Byte Structure

Function	DATA_NO					ADDR_MODE		DIR
Command-byte	C7	C6	C5	C4	C3	C2	C1	C0

Table 22: Command Byte

Bit	Name	Description
C7:C3	DATA_NO	Number of Databytes per SPI-frame. If set to 31, an unlimited number of data bytes can be read&written. Pin CSX must be set high to finish this frame.
C2:C1	ADDR_MODE	Defines address increment for consecutive register reads&writes, see Table 23.
C0	DIR	● 0: Write data to CCE4511 registers ● 1: Read data from CCE4511 registers

Table 23: ADDR_MODE Encoding

ADDR_MODE[1:0]	Description
0	Address is not changed after register read/write
1	Address is incremented by 1 after each register read/write
2	Address is incremented by 32 after each register read/write
3	Do not use.

4.12.3. MISO Format in SPI Mode

Table 24: MISO Format

Bit	7	6	5	4	3	2	1	0
1st Byte	STATUS-CH3 Note 1				STATUS-CH2			
2nd Byte	STATUS-CH1 Note 1				STATUS-CH0			
3rd Byte	DATA Note 2							
	…							
nth Byte	DATA Note 2							

Note 1 Status code for channel n
0x0-0xF, format is dependent on configured mode, see section 4.12.4

Note 2 Current value on read access to register
0x00-0xFF, 4th -nth byte is optional; not valid on write access

4.12.4. MISO Status Nibble

The MISO status nibbles allow to receive status of each channel early during an SPI communication without reading any register.

Table 25: MISO Status Nibble

Bit position	STAT Bit 3	STAT Bit 2	STAT Bit 1	STAT Bit 0
Description	SIO_RXD Note 1	FH_RXD Note 2	ERR Note 3	S_MODE Note 4

Note 1 Current CQ value (only in SIO-Mode)
0b0: High level detected at CQ
0b1: Low level detected at CQ
If the CCE4511 is not in SIO mode this bit is undefined and should be ignored.

Note 2 Reflects the current Frame Handler state.
0b0: No data available for read in frame buffer
0b1: Data available for read in frame buffer or the Startup Sequencer detected a Ready Pulse at CQ

Note 3 Error flag
0b0: No error detected
0b1: Error detected (parity error, invalid checksum, timeout, buffer overflow, Startup Sequencer error)

Note 4 Channel Mode
0b0: Channel is in SIO or UART mode
0b1: Channel is in Frame Handler mode
The status nibble bits change their meaning if the automated wake-up (see section 4.7.1) and/or the ready pulse detection (see section 4.7.2) features are used.

4.13. Register Description

256 8-bit registers can be read or written via the SPI interface. Registers marked as reserved must never be written to a value other than zero. Consider registers not listed in this section as *reserved*. Each register bit has a dedicated access mode

Table 26: Register Bit Access Modes

Mode	Mnemonic	Description
-	reserved	A read returns an undefined value. This bit must always be written to 0.
R	read-only	Write access to this bit has no effect on the registers content or behavior of the chip.
R/W	read-write	Register can be read or written.
RC	clear-on-read	Read returns the current value of this bit and resets its value to 0. Write to this bit has no effect on the register-content or behavior of the chip
W	write-only	A read will always return 0 for this bit. If written as 1 an internal action will be triggered.

4.13.1. Memory Map

Table 27: Memory Map

Address	Name	Description
0x00-0x1F	Chip_control	Chip control registers
0x20-0x7F	-	Reserved. Factory use only.
0x80-0x9F	Channel0	Channel 0 registers
0xA0-0xBF	Channel1	Channel 1 registers
0xC0-0xDF	Channel2	Channel 2 registers
0xE0-0xFF	Channel3	Channel 3 registers

4.13.2. Chip Control Registers

Table 28: Register map chip_control

Address	Register	Description
0x00	REV	CCE4511 revision code
0x01	PROT	Controls if the channels should become disabled by on chip high temperature or VS overvoltage protection.
0x02	INT_SRC_ENV	Environment interrupt-source-register. Contains information about high temperature and high voltage in the chip
0x03	INT_EN_ENV	Interrupt enable register for INT_SRC_ENV
0x04	LED_SYNC	LED sequence synchronization
0x05	SYNC	Synchronization configuration
0x06	MONITOR_EN	Enable signals for voltage and temperature monitors
0x07	CFG	Global configuration register
0x18	FLAG_ENV	Environment-flag-register. Contains information about high temperature, over- and undervoltage in the chip

Table 29: REV (0x00)

Bit	Mode	Symbol	Description	Reset
7:4	R	MAJ	Major revision code	0x3
3:0	R	MIN	Minor revision code	0x1

Table 30: PROT (0x01)

Bit	Mode	Symbol	Description	Reset
7	R/W	PTEMP3	Channel 3 disable on over-temperature **0b0** : Channel 3 is not disabled if over-temperature was flagged **0b1** : Channel 3 is disabled if over-temperature was flagged	0x1
6	R/W	P_OV3	Channel 3 disable on over-voltage at VS **0b0** : Channel 3 is not disabled if over-voltage was flagged **0b1** : Channel 3 is disabled if over-voltage was flagged	0x1
5	R/W	PTEMP2	Channel 2 disable on over-temperature **0b0** : Channel 2 is not disabled if over-temperature was flagged **0b1** : Channel 2 is disabled if over-temperature was flagged	0x1
4	R/W	P_OV2	Channel 2 disable on over-voltage at VS **0b0** : Channel 2 is not disabled if over-voltage was flagged **0b1** : Channel 2 is disabled if over-voltage was flagged	0x1
3	R/W	PTEMP1	Channel 1 disable on over-temperature **0b0** : Channel 1 is not disabled if over-temperature was flagged **0b1** : Channel 1 is disabled if over-temperature was flagged	0x1
2	R/W	P_OV1	Channel 1 disable on over-voltage at VS	0x1

Bit	Mode	Symbol	Description	Reset
			0b0 : Channel 1 is not disabled if over-voltage was flagged **0b1** : Channel 1 is disabled if over-voltage was flagged	
1	R/W	PTEMP0	Channel 0 disable on over-temperature **0b0** : Channel 0 is not disabled if over-temperature was flagged **0b1** : Channel 0 is disabled if over-temperature was flagged	0x1
0	R/W	P_OV0	Channel 0 disable on over-voltage at VS **0b0** : Channel 0 is not disabled if over-voltage was flagged **0b1** : Channel 0 is disabled if over-voltage was flagged	0x1

Table 31: INT_SRC_ENV (0x02)

Bit	Mode	Symbol	Description	Reset
7:6	-	-	Reserved	0x0
5	RC	IS_VS_OV	VS overvoltage **1b1** : overvoltage detected **1b0** : no overvoltage detected	0x0
4	RC	IS_VS_UV	VS undervoltage **1b1** : undervoltage detected **1b0** : no undervoltage detected	0x0
3	RC	IS_VDDA_UV	VDDA undervoltage **1b1** : undervoltage detected **1b0** : no undervoltage detected	0x0
2	RC	IS_VDDIO_UV	VDDIO undervoltage **1b1** : undervoltage detected **1b0** : no undervoltage detected	0x0
1	-	-	Reserved	0x0
0	RC	IS_T_HIGH	High temperature **1b1** : high temperature detected **1b0** : no high temperature detected	0x0

Table 32: INT_EN_ENV (0x03)

Bit	Mode	Symbol	Description	Reset
7:6	-	-	Reserved	0x0
5	R/W	IE_VS_OV	Enables the interrupt source VS_OV **1b1** : enabled **1b0** : disabled	0x0
4	R/W	IE_VS_UV	Enables the interrupt source VS_UV **1b1** : enabled	0x0

Bit	Mode	Symbol	Description	Reset
			1b0 : disabled	
3	R/W	IE_VDDA_UV	Enables the interrupt source VDDA_UV **1b1** : enabled **1b0** : disabled	0x0
2	R/W	IE_VDDIO_UV	Enables the interrupt source VDDIO_UV **1b1** : enabled **1b0** : disabled	0x0
1	-	-	Reserved	0x0
0	R/W	IE_T_HIGH	Enables the interrupt source T_HIGH **1b1** : enabled **1b0** : disabled	0x0

Table 33: LED_SYNC (0x04)

Bit	Mode	Symbol	Description	Reset
7	W	SYNC_LED3B	**1** : sequence for LED3B output restarts from bit 0	0x0
6	W	SYNC_LED2B	**1** : sequence for LED2B output restarts from bit 0	0x0
5	W	SYNC_LED1B	**1** : sequence for LED1B output restarts from bit 0	0x0
4	W	SYNC_LED0B	**1** : sequence for LED0B output restarts from bit 0	0x0
3	W	SYNC_LED3A	**1** : sequence for LED3A output restarts from bit 0	0x0
2	W	SYNC_LED2A	**1** : sequence for LED2A output restarts from bit 0	0x0
1	W	SYNC_LED1A	**1** : sequence for LED1A output restarts from bit 0	0x0
0	W	SYNC_LED0A	**1** : sequence for LED0A output restarts from bit 0	0x0

Table 34: SYNC (0x05)

Bit	Mode	Symbol	Description	Reset
7:4	-	-	Reserved	0x0
3	W	ST3	Synchronous start of transmission trigger 3 **0b1** : write 0b1 to trigger start of transmission in channel 3	0x0
2	W	ST2	Synchronous start of transmission trigger 2 **0b1** : write 0b1 to trigger start of transmission in channel 2	0x0
1	W	ST1	Synchronous start of transmission trigger 1 **0b1** : write 0b1 to trigger start of transmission in channel 1	0x0
0	W	ST0	Synchronous start of transmission trigger 0 **0b1** : write 0b1 to trigger start of transmission in channel 0	0x0

Table 35: MONITOR_EN (0x06)

Bit	Mode	Symbol	Description	Reset
7	R/W	MON_TSD	**1b0** temperature monitoring block disabled. Overtemperature will not be flagged!	0x1

Bit	Mode	Symbol	Description	Reset
			1b1 temperature monitoring block enabled.	
6:3	R/W	VMON_LP	LP voltage monitors enable **0b0000** : all LP voltage monitors are disabled **0bxxx1** : LP voltage monitor for channel0 is enabled **0bxx1x** : LP voltage monitor for channel1 is enabled **0bx1xx** : LP voltage monitor for channel2 is enabled **0b1xxx** : LP voltage monitor for channel3 is enabled	0xF
2	R/W	VMON_VS	VS voltage monitor enable	0x1
1	R/W	VMON_VDDIO	VDDIO voltage monitor enable	0x1
0	R/W	VMON_VDDD	VDDD voltage monitor enable - for factory use only! Can only be written if TST-pin is above or equal 5V!	0x1

Table 36: CFG (0x07)

Bit	Mode	Symbol	Description	Reset
7	R	CHIP_READY	The Chip-ready signal will be set to 1 when the internal initialization of CCE4511's digital core has finished. **1b0** : internal initialization is ongoing **1b1** : internal initialization has finished Note: bit is typically 1b1 30µs after reset, see section 4.3.	0x0
6	W	CHIP_RESET	If this bit is written as 1, the internal logic is reset.	0x0
5	R/W	TEST_FACTORY_RESET	This Bit can be set to '1' via SPI and will be reset to '0' after a hardware reset. It has no affect on the functionality of the chip but can be used to check if the digital core has gone through a reset.	0x0
4:3	-	-	Reserved	0x0
2	R/W	VDDD_LDO_DIS	1.8V voltage regulator control **1b0** : 1.8V voltage regulator is enabled **1b1** : 1.8V voltage regulator is disabled **Note:** The 1.8V VDDD must be supplied externally if this bit is set to 1'b1!	0x0
1	R/W	PAD_DRV_STRENGTH	IO-Pad Drive Strength Configuration **1'b0** : digital IO-pads use low drive strength **1'b1** : digital IO-pads use high drive strenth	0x1
0	R/W	TSD_HYST_EN	Temperature monitor hysteresis enable **1'b0** : Temperature monitor hysteres is disabled **1'b1** : Temperature monitor hysteres is enabled	0x1

Table 37: FLAG_ENV (0x18)

Bit	Mode	Symbol	Description	Reset
7:6	-	-	Reserved	0x0
5	R	FLAG_VS_OV	VS is currently above its allowed max malue	0x0

Bit	Mode	Symbol	Description	Reset
4	R	FLAG_VS_UV	VS is currently below its allowed min malue	0x0
3	R	FLAG_VDDA_UV	VDDA is currently below its allowed min malue	0x0
2	R	FLAG_VDDIO_UV	VDDIO is currently below its allowed min malue	0x0
1	-	-	Reserved	0x0
0	R	FLAG_T_HIGH	The chip temperature is currently above its allowed maximum value!	0x0

4.13.3. Channel Registers

Each channel has 32 identical registers to control its function and to report its status. This section lists the register and register addresses for Channel 0. Refer to the Memory map, section 4.13.1, for the register addresses for channels 1, 2 and 3.

Table 38: Register map Channel0

Address	Register	Description
0x80	CFG1	Configuration 1
0x81	CFG2	Configuration 2
0x82	CFG3	Configuration 3
0x83	SIO	SIO Control
0x84	UART	UART Data
0x85	FHC	Frame Handler Control
0x86	OD	On-Request Data Length
0x87	MPD	Master Process Data Length
0x88	DPD	Device Process Data Length
0x89	CYCT	Cycle Time
0x8A	FHD	Frame Handler Data
0x8B	BLVL	Frame Handler Buffer Level
0x8C	LSEQ_A	LED A Sequence
0x8D	LHLD_A	LED A Hold Times
0x8E	LSEQ_B	LED B Sequence
0x8F	LHLD_B	LED B Hold Times
0x90	CFG4	Configuration 4
0x91	WRP_SOTO_TIMER	Wakeup-Ready-Pulse and Start-Of-Transmission-Offset Timer
0x92	STATUS_MODE_FH	Status (when channel is in mode FH)
0x92	STATUS_MODE_UART	Status (when channel is in mode UART)
0x92	STATUS_MODE_SIO	Status (when channel is in mode SIO)
0x93	INT_SRC_STAT	Status interrupt sources
0x94	INT_EN_STAT	Status interrupt enables
0x95	INT_SRC_SIO	SIO interrupt sources
0x96	INT_EN_SIO	SIO interrupt enables
0x97	INT_SRC_UART	UART interrupt sources
0x98	INT_EN_UART	UART interrupt enables
0x99	INT_SRC_FH	Frame Handler interrupt sources
0x9A	INT_EN_FH	Frame Handler interrupt enables
0x9B	LDRV_A	LED A driver configuration
0x9C	LDRV_B	LED B driver configuration
0x9D	LPX_CLA_TIME	LPx Current Limit Active Timer
0x9E	LPX_OVC_TIME	LPx Overcurrent Timer
0x9F	CQ_OVC_TIME	CQ Overcurrent Timer

Table 39: CFG1 (0x80)

Bit	Mode	Symbol	Description	Reset
7	R/W	GTEN	Gate driver enable **0b0** : Gate driver is disabled **0b1** : Gate driver is enabled **Note:** This bit is read-only while the channel is disabled due to current limit ($t_{LPXCLADIS}$) or overcurrent ($t_{LPXOVCDIS}$). Write accesses will be ignored during that time!	0x0
6:5	R/W	DRV	Ouput stage configuration **00b** : CQ output disabled **01b** : N-mode **10b** : P-mode **11b** : Push-Pull **Note:** In SIO mode these bits only affect the output stage configuration if bit CFG1.CSS is set to 1.If CFG1.CSS is set to 0, the TXEN and TXD pins control the output stage. During ready-pulse-detection and wake-up-request these bits are ignored and the output stage is controlled directly by these features.	0x0
4	R/W	CSS	Channel Source Select in SIO-mode (ignored when sending wake-up request) **0b0** : Pin-mode CQ is controlled by the TXD and TXEN pins in SIO-mode SDX pin low if the CQ output transistors current exceeds the overcurrent threshold or transitor current is actively limited by the output driver **0b1** : Logic mode CQ is controlled by the SIO.CQ_OUT and the CFG1.DRV bits in SIO-mode. SDX pin outputs interrupt status of this channel	0x1
3:2	R/W	COM	Selects the UART communication speed **0b00** : Disabled **0b01** : COM1 - 4.8 kBd **0b10** : COM2 - 38.4 kBd **0b11** : COM3 - 230.4 kBd	0x0
1:0	R/W	MODE	Selects the channel operation mode **0b00** : Standard I/O (SIO) **0b01** : UART **0b10** : Frame Handler **0b11** : reserved	0x0

Table 40: CFG2 (0x81)

Bit	Mode	Symbol	Description	Reset
7	R/W	TOUT_GAP_RLX	UART frame transmission delay of Devices (t_2) timeout check	0x0

Bit	Mode	Symbol	Description	Reset
			0b0 : strict timeout detection (≤3 t_{Bit}) **0b1** : relaxed timeout detection (≤6 t_{Bit})	
6	R/W	CQ_OVC_EN	CQ driver overcurrent detection enable **Note: Disabling this feature may cause damage to master and/or device** **0b0** : disabled **0b1** : enabled	0x1
5	R/W	CQ_CLA_EN	CQ driver current limit enable **Note: Disabling this feature may cause damage to master and/or device** **0b0** : disabled **0b1** : enabled	0x1
4:3	R/W	CQ_IBUF_CNTRL	CQ input buffer control **0b00** : input buffer is disabled. Input buffer signals CQ low. **0b01** : input buffer is enabled with ratiometric thresholds **0b10** : input buffer is enabled with fixed thresholds **0b11** : input buffer is enabled with combined thresholds	0x3
2:1	R/W	ICQ_SEL	Current sink value (I_{CQ}) **0b00** : I_{CQ} = 2.5 mA **0b01** : I_{CQ} = 5 mA **0b10** : I_{CQ} = 7.5 mA **0b11** : I_{CQ} = 10 mA	0x0
0	R/W	ICQ_EN	Current sink configuration for CQ **0b0** : current sink disabled (I_{CQ} = 0mA) **0b1** : current sink enabled (see ICQ_SEL for value of I_{CQ})	0x0

Table 41: CFG3 (0x82)

Bit	Mode	Symbol	Description	Reset
7	R/W	LPX_CLA_EN	External NMOS current limit (gate regulation) enable **Note: Disabling this feature may cause damage to master and/or device** **0b0** : disabled **0b1** : enabled	0x1
6	R/W	LPX_CLA_POWER_ON	Defines if the external NMOS is automatically switched-on, after it was disabled due to an active current limit. **0b0** : external NMOS is not automatically switched-on after $t_{LPXCLADIS}$ **0b1** : external NMOS is automatically switched-on after $t_{LPXCLADIS}$	0x1
5	R/W	LPX_OVC_EN	External NMOS overcurrent detection enable	0x1

Bit	Mode	Symbol	Description	Reset
			Note: Disabling this feature may cause damage to master and/or device **0b0** : disabled **0b1** : enabled	
4	R/W	LPX_OVC_POWER_ON	Defines if the external NMOS is automatically switched-on, after it was disabled due to an overcurrent event. **0b0** : external NMOS is not automatically switched-on after $t_{LPXOVCDIS}$ **0b1** : external NMOS is automatically switched-on after $t_{LPXOVCDIS}$	0x1
3:2	R/W	SLEW	CQ Output slew rate **0x0** : Slew rate: 15V/µs **0x1** : Slew rate: 30V/µs **0x2** : Slew rate: 45V/µs **0x3** : Slew rate: 55V/µs	0x0
1:0	R/W	TOUT_RESPONSE_RLX	Response time of Devices (t_A) timeout **0b00** : 10 t_{Bit} **0b01** : 20 t_{Bit} **0b10** : 30 t_{Bit} **0b11** : 40 t_{Bit} Note that the IO-Link standard demands a 10 t_{BIT} timeout. The WURQ procedure may violate the T_{DMT} (Bit time of subsequent data transmission rate) requirement of the IO-Link specification if the t_A timeout is et to 40 t_{BIT}.	0x0

Table 42: SIO (0x83)

Bit	Mode	Symbol	Description	Reset
7:6	R/W	STARTUP_SEQ	Startup sequencer, controls the automatic procedure for ready pulse detection and wake-up pulse generation *read values:* **0b00** : no automatic startup procedure is running at the moment **0b01** : automated wake-up pulse is running **0b10** : automated ready-pulse detection is running **0b11** : N/A *when STARTUP_SEQ reads 0b00, write as:* **0b00** : ignored **0b01** : Start automated wake-up procedure (no ready pulse detection) **0b10** : Start automated ready-pulse detection (no wake-up pulse generation) **0b11** : Start automated ready-pulse detection followed by an automated wake-up pulse	0x0

Bit	Mode	Symbol	Description	Reset
			When STARTUP_SEQ doen not read 0b00, write as: **0b00** : ignored **0b01 - 0b11**: Aborts startup procedure **Please note:** The remaining bits of this registers are not changed if STARTUP_SEQ is != 2'b00 during write	
5:3	-	-	Reserved	0x0
2	R/W	AUTO_SKIP	Controls a feature that initiates an automatic SKIP of the Framehandler after a successful wake-up request **1b0** : Framehandler is not skipped **1b1** : Framehandler is skipped **Please note:** This bit is only changed if the bits SIO[7:6] are 2'b00 during the write access!	0x0
1	R	CQ_IN	Status of CQ pin (Note the inverted logic!) **0b0** : High level detected at CQ **0b1** : Low level detected at CQ Note: Only valid if the channel is powered! See section 4.3.	0x1
0	R/W	CQ_OUT	Driver output value (Note the inverted logic!) **0b0** : Drive CQ high **0b1** : Drive CQ low **Please note:** This bit is only changed if the bits SIO[7:6] are 2'b00 during the write access!	0x1

Table 43: UART (0x84)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	DATA	Received/Transmitted value over UART **0 .. 255** : read returns received value, write transmits value	0x0

Table 44: FHC (0x85)

Bit	Mode	Symbol	Description	Reset
7	W	RST	Reset frame handler **0b0** : ignored **0b1** : resets frame handler and cycle time counter **Note:** If this bit is written as one, bits 5:0 are ignored!	0x0
6	W	SKIP	Skip a frame **0b0** : ignored **0b1** : resets frame handler without resetting cycle timer counter **Note:** If this bit is written as one, bits 5:0 are ignored!	0x0

Bit	Mode	Symbol	Description	Reset
			Note: If this bit is written as zwero and the Frame Handler is not in the idle state, a Frame Handler reset is triggered!	
5	R/W	CRC	Automatic CRC calculation mode enable **0b0** : CRC-mode disabled **0b1** : CRC-mode enabled	0x0
4	R/W	SYNC_INT_EN	Internal SYNC enable **0b0** : internal synchronization is disabled **0b1** : internal synchronization is enabled	0x0
3	R/W	SYNC_EXT_EN	External SYNC enable **0b0** : external synchronization is disabled **0b1** : external synchronization is enabled	0x0
2:1	R/W	SYNC_SRC_SEL	Select signal that defines the external SYNC source **0b00** : TXD[0] is used as external SYNC signal **0b01** : TXD[1] is used as external SYNC signal **0b10** : TXD[2] is used as external SYNC signal **0b11** : TXD[3] is used as external SYNC signal	0x0
0	R/W	SYNC_SRC_EDGE	Select signal that defines the external SYNC source edge **0b0** : falling edge of the source signal starts the SYNC offset timer **0b1** : rising edge of the source signal starts the SYNC offset timer	0x0

Table 45: OD (0x86)

Bit	Mode	Symbol	Description	Reset
7:6	-	-	Reserved	0x0
5:0	R/W	OD_LEN	On-Request Data length **0..32** : Number of OD bytes in M-sequence. **Note:** M-sequences compliant to the IO-Link Spec rev. 1.1.3 containing On-demand data may only contain 1, 2, 8 or 32 bytes of On-Demand data. **33..63** : If values in this range are written to this register, the write is ignored. **Note:** If this register is written whiile the Frame Handler is not in the idle state will, a Framehandler reset is triggered.	0x1

Table 46: MPD (0x87)

Bit	Mode	Symbol	Description	Reset
7:6	-	-	Reserved	0x0
5:0	R/W	MPD_LEN	Master Process Data length **0..32** : Number of Process Data bytes in the master message.	0x0

Bit	Mode	Symbol	Description	Reset
			33..63 : If values in this range are written to this register, the write is ignored. **Note:** If this register is written while the Frame Handler is not in the idle state will, a Framehandler reset is triggered.	

Table 47: DPD (0x88)

Bit	Mode	Symbol	Description	Reset
7:6	-	-	Reserved	0x0
5:0	R/W	DPD_LEN	Device Process Data length **0..32** : Number of Process Data bytes in the device message. **33..63** : If values in this range are written to this register, the write is ignored. **Note:** If this register is written while the Frame Handler is not in the idle state will, a Framehandler reset is triggered.	0x0

Table 48: CYCT (0x89)

Bit	Mode	Symbol	Description	Reset
7:6	R/W	BASE	Base/offset for cycle time **0b00** : BASE is 100µs; no OFFSET; disabled if MULT is 0 **0b01** : BASE is 400µs; OFFSET is 6.4 ms **0b10** : BASE is 1.6ms; OFFSET is 32 ms **0b11** : reserved. **Note:** A write to the CYCT register is ignored if BASE=0b11!	0x0
5:0	R/W	MULT	Multiplier for cycle timer **0 .. 63** : Multiplier value t_{CYC} = OFFSET + BASE * MULT	0x0

Table 49: FHD (0x8A)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	DATA	Read returns data from the frame buffer Write stores data to the frame buffer **Note:** If the IC is not in Frame Handler mode or an Automated Wake-Up procedure is active, writes are ignored and reads return undefined data.The frame buffer may contain only a single Master Message or a single Device Message.	0x0

Table 50: BLVL (0x8B)

Bit	Mode	Symbol	Description	Reset
7:0	R	FCNT	Read returns current number of unread received bytes in the frame buffer.	0x0

Table 51: LSEQ_A (0x8C)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	SEQ	LED blinking sequence **0x00** : always off **0x01 .. 0xFE** : blinking; 0b0 represents off-state; 0b1 represents on-state; LSB processed first **0xFF** : always on	0x0

Table 52: LHLD_A (0x8D)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	HLDH	LED hold time configuration for on-state **0 .. 15** : Base time multiplier t_{HI} = 50 ms + 50 ms * HLDH	0x0
3:0	R/W	HLDL	LED hold time configuration for off-state **0 .. 15** : Base time multiplier t_{LO} = 50 ms + 50 ms * HLDL	0x0

Table 53: LSEQ_B (0x8E)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	SEQ	LED blinking sequence **0x00** : always off **0x01 .. 0xFE** : blinking; 0b0 represents off-state; 0b1 represents on-state; LSB processed first **0xFF** : always on	0x0

Table 54: LHLD_B (0x8F)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	HLDH	LED hold time configuration for on-state **0 .. 15** : Base time multiplier t_{HI} = 50 ms + 50 ms * HLDH	0x0
3:0	R/W	HLDL	LED hold time configuration for off-state **0 .. 15** : Base time multiplier t_{LO} = 50 ms + 50 ms * HLDL	0x0

Table 55: CFG4 (0x90)

Bit	Mode	Symbol	Description	Reset
7:2	R/W	TLVL	Frame buffer receive threshold level **n :** LVL interrupt triggered after n received UART frames of the Device Message. If it is set to **0**, no LVL interrupt is triggered.	0x0

Bit	Mode	Symbol	Description	Reset
1:0	R/W	SOTO_PRESCALER	Prescaler for SOTO_TIMER (see WRP_SOTO_TIMER register) **2'b00** : time unit = 1µs **2'b01** : time unit = T_clk_xtal*64 = 1TBIT@COM3 = 4.34µs **2'b10** : time unit = 10µs **2'b11** : time unit = T_clk_xtal*(64*11)) = 11TBIT@COM3 = 47.743µs	0x0

Table 56: WRP_SOTO_TIMER (0x91)

Bit	Mode	Symbol	Description	Reset
7:0	R/W	COUNT	Counter value for Ready-pulse-detection-timer and Start-of-transmission-offset-timer (SOTO timer) During Ready pulse detection this value is interpreted like this: **Timeout for Ready pulse = (COUNT+1) * 250ms** After startup sequence has finished, this value will be used for the start-of-transmission-offset-timer in the following way: **offset-time = COUNT * time unit (defined by CFG4.SOTO_PRESCALER)**	0x0

Table 57: STATUS_MODE_SIO (0x92)

Bit	Mode	Symbol	Description	Reset
7	R	LP_OV	Status of overvoltage detection at LP **0b1 :** overvoltage is currently detected **0b0 :** no overvoltage is currently detected	0x0
6	R	LP_UV	Status of undervoltage detection at LP **0b1 :** undervoltage is currently detected **0b0 :** no undervoltage is currently detected	0x0
5	R	LP_OVC_OR_CLA	Status of overcurrent- or current-limit-detection at LP **0b1 :** overcurrent or current-limit is currently detected **0b0 :** neither overcurrent nor current-limit is currently detected	0x0
4	R	CQ_OVC	Status of overcurrent-detection at CQ **0b1 :** overcurrent is currently detected **0b0 :** no overcurrent is currently detected Note: Only valid if the channel is powered! See section 4.3.	0x0
3	R	WURQ	Wake-up pulse indicator	0x0

Bit	Mode	Symbol	Description	Reset
			0b0 : No automatic Wake-up pulse is being sent **0b1** : Automatic Wake-up pulse is being sent	
2	R	RXD	input state **0b0** : High level detected at CQ pin **0b1** : Low level detected at CQ pin	0x1
1	R	TXEN	output enable state **0b0** : Channel driver is disabled **0b1** : Channel driver is enabled	0x0
0	R	TXD	output value **0b0** : CQ is driven high **0b1** : CQ is driven low	0x1

Table 58: STATUS_MODE_FH (0x92)

Bit	Mode	Symbol	Description	Reset
7	R	LP_OV	Status of overvoltage detection at LP **0b1 :** overvoltage is currently detected **0b0 :** no overvoltage is currently detected	0x0
6	R	LP_UV	Status of undervoltage detection at LP **0b1 :** undervoltage is currently detected **0b0 :** no undervoltage is currently detected	0x0
5	R	LP_OVC_OR_CLA	Status of overcurrent- or current-limit-detection at LP **0b1 :** overcurrent or current-limit is currently detected **0b0 :** neither overcurrent nor current-limit is currently detected	0x0
4	R	CQ_OVC	Status of overcurrent-detection at CQ **0b1 :** overcurrent is currently detected **0b0 :** no overcurrent is currently detected Note: Only valid if the channel is powered! See section 4.3.	0x0
3	R	TOUT_STAT	Frame handler timeout **0b0** : No timeout detected / cycle time not passed **0b1** : Timeout detected / cycle time passed	0x0
2:0	R	STATE	Frame handler state **0b000** : IDLE(*) **0b001** : Transmission output required; frame handler waits for data at register FHD **0b010** : Transmission active; no further output required **0b011** : Transmission active; further output required **0b100** : Receiving active **0b101** : Receiving active; new input available, read register FHD	0x0

Bit	Mode	Symbol	Description	Reset
			0b110 : Receiving active; received message is erroneous **0b111** : Receiving active; received message is erroneous; new input available, read register FHD (*) IDLE here means that either the transmission has not yet been initiated by a write to FHD, or that it has been initiated, no further output is required, and no data has yet been sent. This could be due to a) a wait for a sync_event or b) a wait for the offset timer to finish or c) a wait for the cycle timer to finish.	

Table 59: STATUS_MODE_UART (0x92)

Bit	Mode	Symbol	Description	Reset
7	R	LP_OV	Status of overvoltage detection at LP **0b1 :** overvoltage is currently detected **0b0 :** no overvoltage is currently detected	0x0
6	R	LP_UV	Status of undervoltage detection at LP **0b1 :** undervoltage is currently detected **0b0 :** no undervoltage is currently detected	0x0
5	R	LP_OVC_OR_CLA	Status of overcurrent- or current-limit-detection at LP **0b1 :** overcurrent or current-limit is currently detected **0b0 :** neither overcurrent nor current-limit is currently detected	0x0
4	R	CQ_OVC	Status of overcurrent-detection at CQ **0b1 :** overcurrent is currently detected **0b0 :** no overcurrent is currently detected Note: Only valid if the channel is powered! See section 4.3.	0x0
3	R	OFLW	UART receive buffer overflow **0b0** : no data overflow detected **0b1** : data overflow is detected, unread byte in the UART register was overridden	0x0
2	R	RXERR	UART parity error flag **0b0** : Last byte was received without parity error **0b1** : Last byte was received with parity error	0x0
1	R	RXRDY	UART receive state indicator **0b0** : UART is receiving data **0b1** : UART is idle and ready for receiving	0x0
0	-	-	Reserved	0x0

Table 60: INT_SRC_STAT (0x93)

Bit	Mode	Symbol	Description	Reset
7	RC	IS_LP_OV	LP overvoltage **1b1** : overvoltage detected **1b0** : no overvoltage detected	0x0
6	RC	IS_LP_UV	LP undervoltage **1b1** : undervoltage detected **1b0** : no undervoltage detectedd	0x0
5	RC	IS_CH_DIS_LPX_CLA	Channel disabled due to a detected current limit active on LPx **1b1** : channel disabled **1b0** : channel not disabled	0x0
4	RC	IS_CH_DIS_LPX_OVC	Channel disabled due to a detected overcurrent on LPx **1b1** : channel disabled **1b0** : channel not disabled	0x0
3	RC	IS_CH_DIS_CQ_OVC	Channel disabled due to a detected overcurrent on CQ **1b1** : channel disabled **1b0** : channel not disabled Note: Only valid if the channel is powered!	0x0
2	RC	IS_LPX_CLA	Current limit active detected at LPx **1b1** : detected **1b0** : not detected	0x0
1	RC	IS_LPX_OVC	Overcurrent detected at LPx **1b1** : overcurrent detected **1b0** : overcurrent not detected	0x0
0	RC	IS_CQ_OVC	Overcurrent detected at CQ **1b1** : overcurrent detected **1b0** : overcurrent not detected Note: Only valid if the channel is powered!	0x0

Table 61: INT_EN_STAT (0x94)

Bit	Mode	Symbol	Description	Reset
7	R/W	IE_LP_OV	Enables the interrupt source LP_OV **1b1** : enabled **1b0** : disabled	0x0
6	R/W	IE_LP_UV	Enables the interrupt source LP_UV **1b1** : enabled **1b0** : disabled	0x0
5	R/W	IE_CH_DIS_LPX_CLA	Enables the interrupt source CH_DIS_LPX_CLA	0x0

Bit	Mode	Symbol	Description	Reset
			1b1 : enabled **1b0** : disabled	
4	R/W	IE_CH_DIS_LPX_OVC	Enables the interrupt source CH_DIS_LPX_OVC **1b1** : enabled **1b0** : disabled	0x0
3	R/W	IE_CH_DIS_CQ_OVC	Enables the interrupt source CH_DIS_CQ_OVC **1b1** : enabled **1b0** : disabled	0x0
2	R/W	IE_LPX_CLA	Enables the interrupt source LPX_CLA **1b1** : enabled **1b0** : disabled	0x0
1	R/W	IE_LPX_OVC	Enables the interrupt source LPX_OVC **1b1** : enabled **1b0** : disabled	0x0
0	R/W	IE_CQ_OVC	Enables the interrupt source CQ_OVC **1b1** : enabled **1b0** : disabled	0x0

Table 62: INT_SRC_SIO (0x95)

Bit	Mode	Symbol	Description	Reset
7:4	-	-	Reserved	0x0
3	RC	IS_RP_ERR	Error during ready-pulse detection due to ready-pulse with wrong length or timeout while waiting for ready-pulse **1b1** : error **1b0** : no error	0x0
2	RC	IS_READY_DET	Valid ready-pulse detected **1b1** : detected **1b0** : not detected	0x0
1	RC	IS_CQ_FALL	Falling edge at Pin CQ (voltage changed from VS to 0V) **1b1** : falling edge **1b0** : no falling edge Note: Only valid if the channel is powered! See section 4.3.	0x0
0	RC	IS_CQ_RISE	Rising edge at Pin CQ (voltage changed from 0V to VS) **1b1** : rising edge **1b0** : no rising edge Note: Only valid if the channel is powered! See section 4.3.	0x0

Table 63: INT_EN_SIO (0x96)

Bit	Mode	Symbol	Description	Reset
7:4	-	-	Reserved	0x0
3	R/W	IE_RP_ERR	Enables the interrupt source RP_ERR **1b1** : enabled **1b0** : disabled	0x0
2	R/W	IE_READY_DET	Enables the interrupt source READY_DET **1b1** : enabled **1b0** : disabled	0x0
1	R/W	IE_CQ_FALL	Enables the interrupt source CQ_FALL **1b1** : enabled **1b0** : disabled	0x0
0	R/W	IE_CQ_RISE	Enables the interrupt source CQ_RISE **1b1** : enabled **1b0** : disabled	0x0

Table 64: INT_SRC_UART (0x97)

Bit	Mode	Symbol	Description	Reset
7:3	-	-	Reserved	0x0
2	RC	IS_RX_OFLW	UART receive overflow **1b1** : overflow detected **1b0** : no overflow detected	0x0
1	RC	IS_RX_REC	UART received one byte. Received data can be read from the UART register. **1b1** : one byte received **1b0** : no byte received	0x0
0	RC	IS_TX_RDY	UART is ready to send data. Send data can be written to the UART register. **1b1** : UART ready **1b0** : UART not ready	0x0

Table 65: INT_EN_UART (0x98)

Bit	Mode	Symbol	Description	Reset
7:3	-	-	Reserved	0x0
2	R/W	IE_RX_OFLW	Enables the interrupt source RX_OFLW **1b1** : enabled **1b0** : disabled	0x0
1	R/W	IE_RX_REC	Enables the interrupt source RX_REC **1b1** : enabled **1b0** : disabled	0x0
0	R/W	IE_TX_RDY	Enables the interrupt source TX_RDY	0x0

Bit	Mode	Symbol	Description	Reset
			1b1 : enabled **1b0** : disabled	

Table 66: INT_SRC_FH (0x99)

Bit	Mode	Symbol	Description	Reset
7	RC	IS_ERR	Error received (Triggers when a checksum or parity error was received within the device message) **1b1** : error received **1b0** : no error received	0x0
6	RC	IS_EOC	End of Cycle time (Triggers when the cycle timer has elapsed) **1b1** : timer has elapsed **1b0** : timer has not yet elapsed	0x0
5	RC	IS_WURQ	Wake-up procedure finished **1b1** : wake-up finished **1b0** : wake-up not yet finished	0x0
4	RC	IS_TOUT	Timeout detected **1b1** : detected **1b0** : not detected	0x0
3	RC	IS_SOT	Master Message transmission started **1b1** : started **1b0** : not started	0x0
2	RC	IS_SOR	Start bit of the device response received **1b1** : bit received **1b0** : bit not yet received	0x0
1	RC	IS_LVL	Specified number of device message bytes received. See CFG4.TLVL! **1b1** : received **1b0** : not yet received	0x0
0	RC	IS_MSG	The last character of a message was received. **1b1** : received **1b0** : not yet received	0x0

Table 67: INT_EN_FH (0x9A)

Bit	Mode	Symbol	Description	Reset
7	R/W	IE_ERR	Enables the interrupt source ERR **1b1** : enabled **1b0** : disabled	0x0
6	R/W	IE_EOC	Enables the interrupt source EOC **1b1** : enabled **1b0** : disabled	0x0

Bit	Mode	Symbol	Description	Reset
5	R/W	IE_WURQ	Enables the interrupt source WURQ **1b1** : enabled **1b0** : disabled	0x0
4	R/W	IE_TOUT	Enables the interrupt source TOUT **1b1** : enabled **1b0** : disabled	0x0
3	R/W	IE_SOT	Enables the interrupt source SOT **1b1** : enabled **1b0** : disabled	0x0
2	R/W	IE_SOR	Enables the interrupt source SOR **1b1** : enabled **1b0** : disabled	0x0
1	R/W	IE_LVL	Enables the interrupt source LVL **1b1** : enabled **1b0** : disabled	0x0
0	R/W	IE_MSG	Enables the interrupt source MSG **1b1** : enabled **1b0** : disabled	0x0

Table 68: LDRV_A (0x9B)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	I_LED	LEDA driving current **0 .. 10** : LED current multiplier **11 .. 15** : I_LED = 10 I_{OUT_A} = I_LED * 2mA	0x0
3:0	R/W	PWM	LEDA PWM duty cycle **0 :** 1.0% **1 :** 1.4% **2 :** 1.8% **3 :** 2.5% **4 :** 3.4% **5 :** 4.6% **6 :** 6.3% **7 :** 8.6% **8 :** 11% **9 :** 16% **10 :** 22% **11 :** 29% **12 :** 40% **13 :** 54% **14 :** 74% **15 :** PWM disabled, output on	0xF

Table 69: LDRV_B (0x9C)

Bit	Mode	Symbol	Description	Reset
7:4	R/W	I_LED	LEDB driving current **0 .. 10** : LED current multiplier **11 .. 15** : I_LED = 10 I_{OUT_B} = I_LED * 2mA	0x0
3:0	R/W	PWM	LEDB PWM duty cycle **0 :** 1.0% **1 :** 1.4% **2 :** 1.8% **3 :** 2.5% **4 :** 3.4% **5 :** 4.6% **6 :** 6.3% **7 :** 8.6% **8 :** 11% **9 :** 16% **10 :** 22% **11 :** 29% **12 :** 40% **13 :** 54% **14 :** 74% **15 :** PWM disabled, output on	0xF

Table 70: LPX_CLA_TIME (0x9D)

Bit	Mode	Symbol	Description	Reset
7	R/W	FACTOR	FACTOR for LPx current-limit-active disable time **0b0** : FACTOR=10 **0b1** : FACTOR=100	0x0
6:5	R/W	BASE	Time base for LPx current-limit-active detection time **0b00** : BASE=20µs **0b01** : BASE=100µs **0b10** : BASE=1ms **0b11** : BASE=10ms	0x1
4:0	R/W	MULT	Multiplier for LPx current-limit-active detection time **0 :** automatic channel shutdown after time $t_{LPXCLADET}$ is disabled **1 ... 31 :** Multiplier value $t_{LPXCLADET}$ = BASE * MULT $t_{LPXCLADIS}$ = $t_{LPXCLADET}$ * FACTOR	0x1

Table 71: LPX_OVC_TIME (0x9E)

Bit	Mode	Symbol	Description	Reset
7	R/W	FACTOR	FACTOR for LPx overcurrent disable time **0b0** : FACTOR=10 **0b1** : FACTOR=100	0x0
6:5	R/W	BASE	Time base for LPx overcurrent detection time **0b00** : BASE=20µs **0b01** : BASE=100µs **0b10** : BASE=1ms **0b11** : BASE=10ms	0x1
4:0	R/W	MULT	Multiplier for LPx overcurrent detection time **0 :** automatic channel shutdown after time $t_{LPXOVCDET}$ is disabled **1 ... 31 :** Multiplier value $t_{LPXOVCDET}$ = BASE * MULT $t_{LPXOVCDIS}$ = $t_{LPXOVCDET}$ * FACTOR	0x1

Table 72: CQ_OVC_TIME (0x9F)

Bit	Mode	Symbol	Description	Reset
7	R/W	FACTOR	FACTOR for CQ overcurrent disable time **0b0** : FACTOR=10 **0b1** : FACTOR=100	0x0
6:5	R/W	BASE	Time base for CQ overcurrent detection time **0b00** : BASE=20µs **0b01** : BASE=100µs **0b10** : BASE=1ms **0b11** : BASE=10ms	0x1
4:0	R/W	MULT	Multiplier for CQ overcurrent detection time **0 :** automatic channel shutdown after time $t_{CQOVCDET}$ is disabled **1 ... 31 :** Multiplier value $t_{CQOVCDET}$ = BASE * MULT $t_{CQOVCDIS}$ = $t_{CQOVCDET}$ * FACTOR	0x1

5. Package Outline

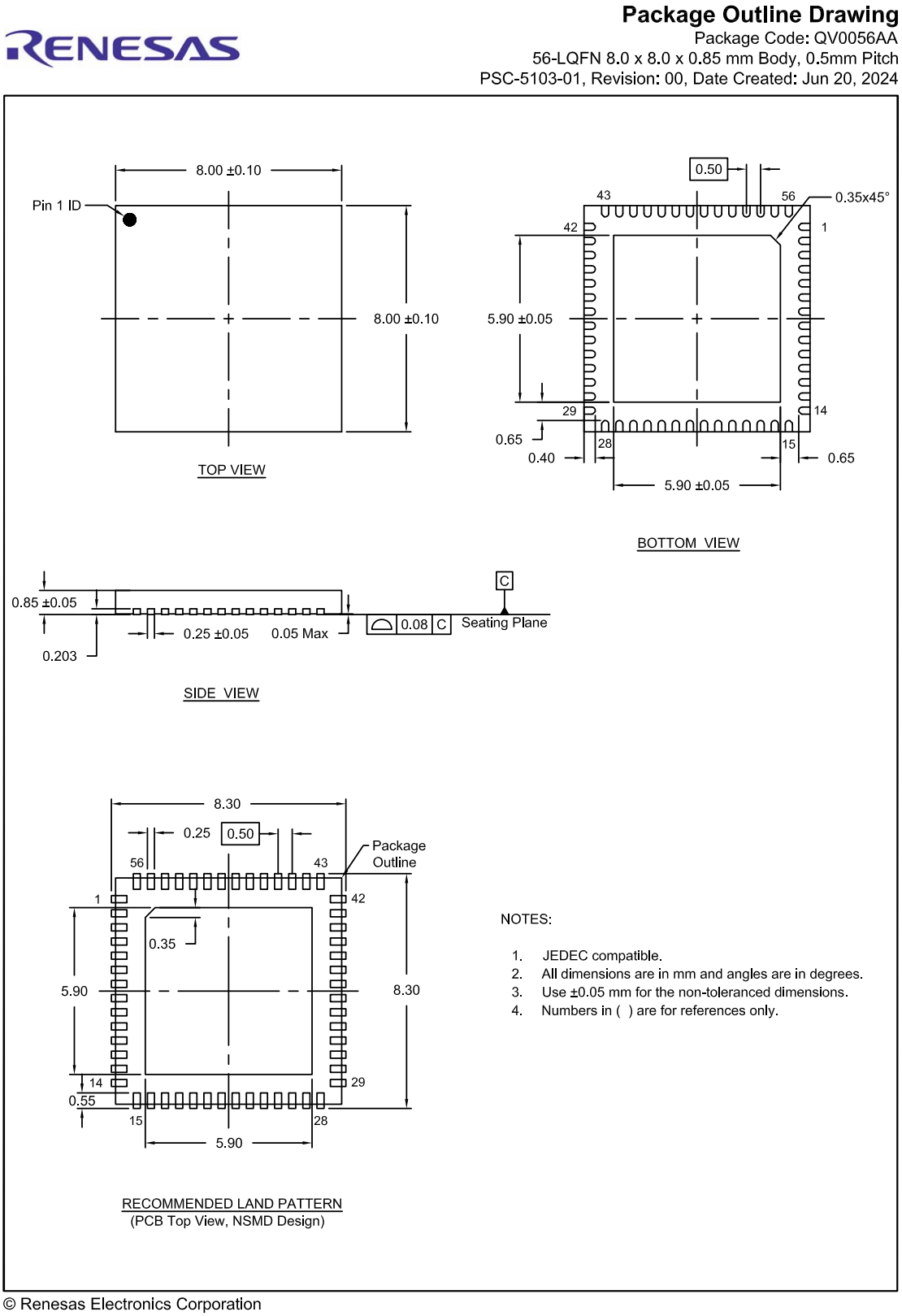
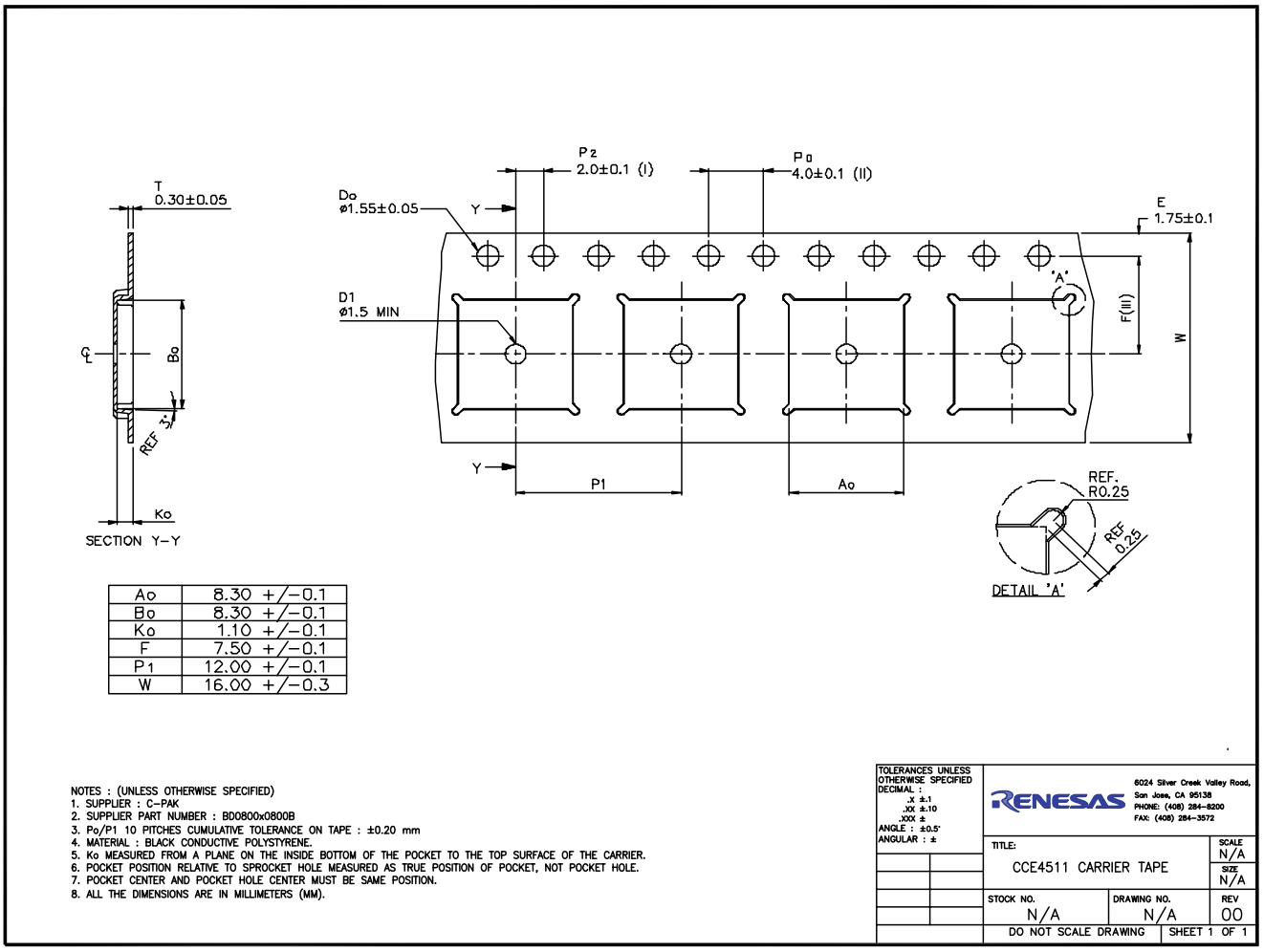


Figure 26. Package Outline Drawing

6. Tape and Reel information

6.1. Tape Information



Ao	8.30 +/−0.1
Bo	8.30 +/−0.1
Ko	1.10 +/−0.1
F	7.50 +/−0.1
P1	12.00 +/−0.1
W	16.00 +/−0.3

Figure 27. Carrier Tape Drawing

6.2. Reel Information

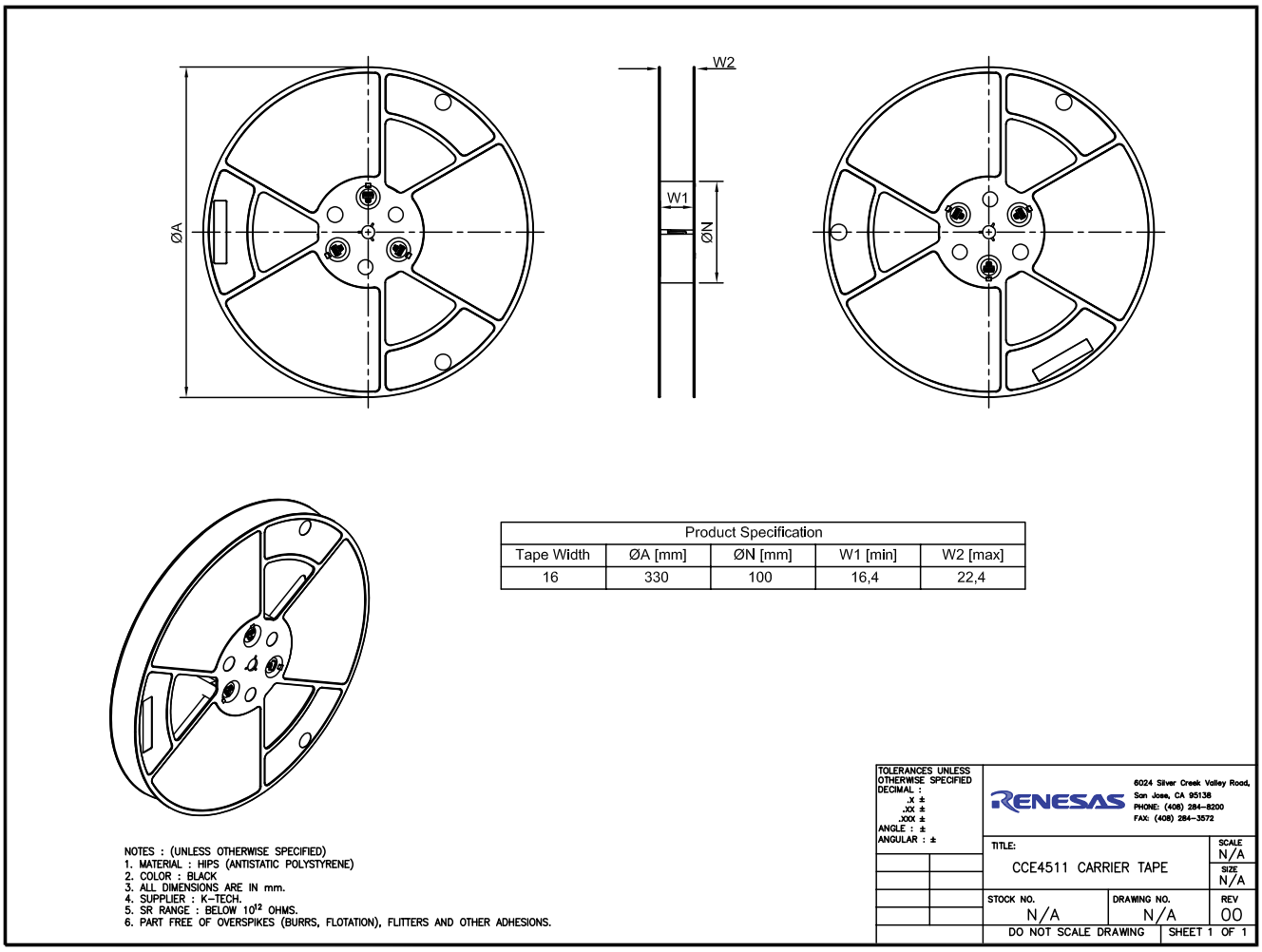


Figure 28. Reel Drawing

7. Ordering Information

Please take the corresponding order number from Table 73 and consult your Renesas Electronics local sales representative.

Table 73: Ordering Information

Part	Order No.	Package	Delivery	Quantity
CCE4511	CCE4511CA	QFN56	Tape & Reel	4500 parts per reel

8. References

[1] IO-Link Community, IO-Link Interface and System Specification, version 1.1.3, June 2019

[2] IO-Link Community, IO-Link Safety System Extensions with SMI Specification, V1.1.3, March 2022

[3] CCE4511 Typical Application Circuitry AN

[4] CCE4511 Evaluation Board V1 User Manual

Note 1 References are for the latest published version, unless otherwise indicated.

9. Revision History

Revision	Date	Description
1.00	Sep 16, 2024	Initial release.