HC55185

VoIP Ringing SLIC Family

FN4831
Rev 15.00
February 9, 2012

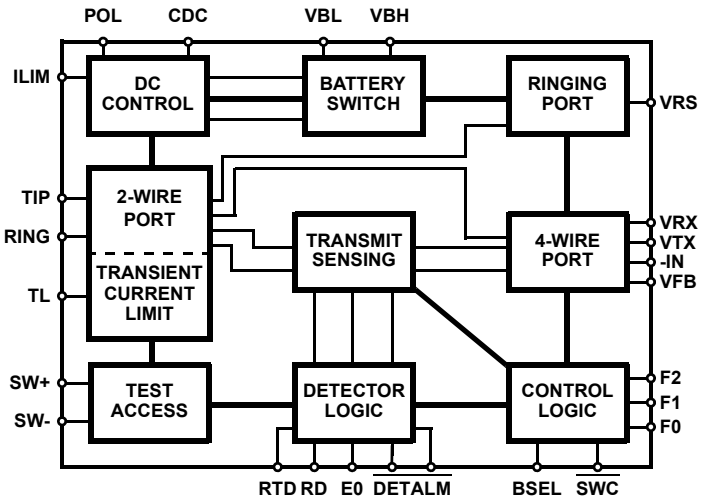
The RSLIC-VoIP family of ringing subscriber line interface circuits (RSLIC) supports analog Plain Old Telephone Service (POTS) in short and medium loop length, wireless and wireline applications. Ideally suited for remote subscriber units, this family of products offers flexibility to designers with high ringing voltage and low power consumption system requirements.

The RSLIC-VoIP family operates to 100V, which translates directly to the amount of ringing voltage supplied to the end subscriber. With the high operating voltage, subscriber loop lengths can be extended to 500Ω (i.e., 5,000 feet) and beyond.

Other key features across the product family include: low power consumption, ringing using sinusoidal or trapezoidal waveforms, robust auto-detection mechanisms for when subscribers go on or off hook, and minimal external discrete application components. Integrated test access features are also offered on selected products to support loopback testing as well as line measurement tests.

There are five product offerings of the HC55185 with each version providing voltage grades of high battery voltage and longitudinal balance. The voltage feed amplifier design uses low fixed loop gains to achieve high analog performance with low susceptibility to system induced noise.

Block Diagram



Features

- Onboard Ringing Generation
- Compatible with Existing HC5518x Devices
- Low Standby Power Consumption (75V, 65mW)
- Reduced Idle Channel Noise
- Programmable Transient Current Limit
- Improved Off Hook Software Interface
- Integrated MTU DC Characteristics
- Low External Component Count
- Silent Polarity Reversal
- Pulse Metering and On Hook Transmission
- Tip Open Ground Start Operation
- Balanced and Unbalanced Ringing
- Thermal Shutdown with Alarm Indicator
- 28 Lead Surface Mount Packaging
- Reduced Footprint Micro Leadframe Packaging
- Dielectric Isolated (DI) High Voltage Design
- QFN Package Option
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Product Outline
  - Near Chip Scale Package Footprint; Improves PCB Efficiency and has a Thinner Profile
- Pb-free (RoHS compliant)

Applications

- Voice Over Internet Protocol (VoIP)
- Cable Modems
- Voice Over DSL (VoDSL)
- Short Loop Access Platforms
- Remote Subscriber Units
- Terminal Adapters

Related Literature

- AN9814, “HC5518XEVAL Evaluation Board User’s Guide”
- AN9824, “SPICE Model Tutorial of the RSLIC18™ AC Loop”
- Interfacing to DSP CODECs (Contact Factory)
- TB379 “Thermal Characterization of Packaged Semiconductor Devices”
- AN9922, “Thermal Characterization and Board Level Modeling of the RSLIC18 in the MLFP Package”

Ordering Information

PART NUMBER (Notes 2, 3)	PART MARKING	HIGH BATTERY (VBH)			LONGITUDINAL BALANCE		FULL TEST	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
		100V	85V	75V	58dB	53dB				
HC55185AIMZ (Note 1)	HC55185 AIMZ	•			•		•	-40 to +85	28 Ld PLCC	N28.45
HC55185BIMZ (Note 1)	HC55185 BIMZ		•		•		•	-40 to +85	28 Ld PLCC	N28.45
HC55185CIMZ (Note 1)	HC55185 CIMZ	•				•	•	-40 to +85	28 Ld PLCC	N28.45
HC55185DIMZ (Note 1)	HC55185 DIMZ		•			•	•	-40 to +85	28 Ld PLCC	N28.45
HC55185ECMZ (Note 1)	HC55185 ECMZ			•		•		0 to +75	28 Ld PLCC	N28.45
HC55185ECRZ (Note 1)	HC55185 ECRZ			•		•		0 to +75	32 Ld QFN	L32.7x7 (Note 4)
HC55185FCMZ (Note 1)	HC55185 FCMZ			•		•	•	0 to +85	28 Ld PLCC	N28.45
HC55185FCRZ (Note 1)	HC55185 FCRZ			•		•	•	0 to +85	32 Ld QFN	L32.7x7 (Note 4)
HC55185GIMZ	HC55185 GIMZ	•				•		-40 to +85	28 Ld PLCC	N28.45
HC55185GCMZ	HC55185 GCMZ	•				•	•	0 to +85	28 Ld PLCC	N28.45
HC55185GCRZ (Note 1)	HC55185 GCRZ	•				•	•	0 to +85	32 Ld QFN	L32.7x7 (Note 4)

NOTES:

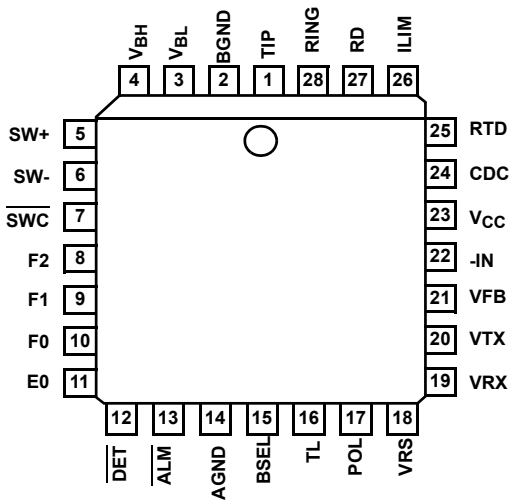
1. Add "96" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for HC55185. For more information on MSL please see tech brief TB363.
4. Reference “Special Considerations for the QFN Package” on page 8.

Device Operating Modes

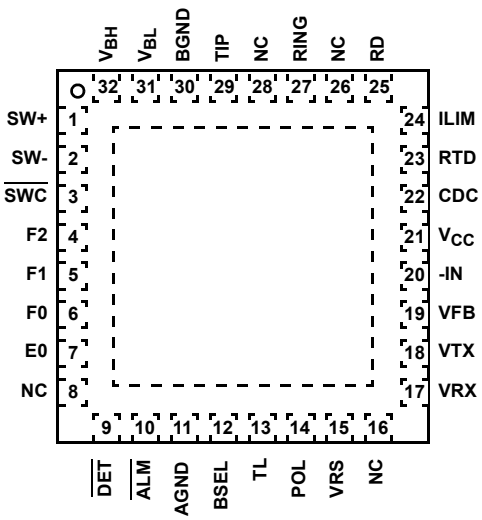
MODE	F2	F1	F0	E0 = 1	E0 = 0	Uncommitted Switch Logic	HC55185A	HC55185B	HC55185C	HC55185D	HC55185E	HC55185F	HC55185G
Low Power Standby	0	0	0	SHD	GKD	Enabled	•	•	•	•	•	•	•
Forward Active	0	0	1	SHD	GKD	Enabled	•	•	•	•	•	•	•
Unbalanced Ringing	0	1	0	RTD	RTD	Enabled							•
Reverse Active	0	1	1	SHD	GKD	Enabled	•	•	•	•	•	•	•
Ringing	1	0	0	RTD	RTD	Enabled	•	•	•	•	•	•	•
Forward Loop Back	1	0	1	SHD	GKD	Enabled	•	•	•	•		•	•
Tip Open	1	1	0	SHD	GKD	Enabled	•	•	•	•		•	•
Power Denial	1	1	1	n/a	n/a	Disabled - off	•	•	•	•	•	•	•

Pinouts

HC55185
(28 LD PLCC)
TOP VIEW



HC55185
(32 LD QFN)
TOP VIEW



Absolute Maximum Ratings T_A = +25°C

Maximum Supply Voltages
- V_{CC} . . . . . -0.5V to +7V
- V_{CC} - V_{BH} 110V
- Uncommitted Switch Voltage . . . . . -110V

Maximum Tip/Ring Negative Voltage Pulse (Note 5) . . . . . VBH -15V
Maximum Tip/Ring Positive Voltage Pulse (Note 5) . . . . . +8V
ESD (Human Body Model). 500V

Operating Conditions

Temperature Range
Commercial (C suffix) . . . . . 0°C to +85°C
Industrial (I suffix). . . . . -40°C to +85°C
Positive Power Supply (V_{CC}). . . . . +5V, ±5%
Low Battery Power Supply (V_{BL}). . . . . -16V to -52V, ±5%
High Battery Power Supply (V_{BH})
AIM, CIM . . . . . V_{BL} to 100V, ±5%
BIM, DIM . . . . . V_{BL} to -85V, ±10%
EIM. . . . . V_{BL} to -75V, ±10%
Uncommitted Switch (loop back or relay driver) . . . . . +5V to -100V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PLCC (Note 6)	53	N/A
QFN (Notes 7, 8)	25	0.5

Maximum Junction Temperature Plastic . . . . . +150°C
Maximum Storage Temperature Range. . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp
For Recommended soldering conditions see Tech Brief TB389

Die Characteristics

Substrate Potential . . . . . V_{BH}
Process . . . . . Bipolar-DI

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. Characterized with 2 x 10µs, and 10 x 1000µs first level lightning surge waveforms (GR-1089-CORE).
6. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
7. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
8. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Unless Otherwise Specified, T_A = -40°C to +85°C for industrial (I) grade and T_A = 0°C to +85°C for commercial (C) grade, V_{BL} = -24V, V_{BH} = -100V, -85V or -75V, V_{CC} = +5V, AGND = BGND = 0V, loop current limit = 25mA. All AC parameters are specified at 600Ω 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0Ω. **Boldface limits apply over the operating temperature range.**

PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNITS
RINGING PARAMETERS					
VRS Input Impedance (Note 9)		**450**	-	-	kΩ
Differential Ringing Gain (Note 10)	Balanced Ringing, VRS to 2-Wire, R_{LOAD} = ∞	**78**	80	**82**	V/V
	Unbalanced Ringing, VRS to 2-Wire, R_{LOAD} = ∞		40		V/V
Centering Voltage Accuracy	Tip, Referenced to V_{BH}/2 + 0.5 (Note 13)	-	± 2.5	-	V
	Ring, Referenced to V_{BH}/2 + 0.5	-	± 2.5	-	V
Open Circuit Ringing Voltage	Balanced Ringing, VRS Input = 0.840V_{RMS}	-	67	-	V_{RMS}
	Unbalanced Ringing, VRS Input = 0.840V_{RMS}		33.5		V_{RMS}
Ringing Voltage Total Distortion	R_L = 1.3 kΩ, V_{T-R} = |V_{BH}| -5	-	-	**4.0**	%
4-Wire to 2-Wire Ringing Off Isolation	Active Mode, Referenced to VRS Input	-	90	-	dB
2-Wire to 4-Wire Transmit Isolation	Ringing Mode Referenced to the Differential Ringing Amplitude	-	80	-	dB
AC TRANSMISSION PARAMETERS					
Receive Input Impedance (Note 9)		**160**	-	-	kΩ
Transmit Output Impedance (Note 9)		-	-	**1**	Ω
4-Wire Port Overload Level (Note 9)	THD = 1%	**3.1**	3.5	-	V_{PEAK}

Electrical Specifications

Unless Otherwise Specified, T_A = -40°C to +85°C for industrial (I) grade and T_A = 0°C to +85°C for commercial (C) grade, V_{BL} = -24V, V_{BH} = -100V, -85V or -75V, V_{CC} = +5V, AGND = BGND = 0V, loop current limit = 25mA. All AC parameters are specified at 600Ω 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0Ω. **Boldface limits apply over the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNITS
2-Wire Port Overload Level (Note 9)	THD = 1%	**3.1**	3.5	-	V_{PEAK}
2-Wire Return Loss	300Hz	-	24	-	dB
	1kHz	-	40	-	dB
	3.4kHz	-	21	-	dB
2-Wire Longitudinal Balance (Note 11)	Forward Active, Grade A and B	**58**	62	-	dB
	Forward Active, Grade C, D and E	**53**	59	-	dB
4-Wire Longitudinal Balance (Note 11)	Forward Active, Grade A and B	**58**	67	-	dB
	Forward Active, Grade C, D and E	**53**	64	-	dB
2-Wire to 4-Wire Level Linearity 4-Wire to 2-Wire Level Linearity Referenced to -10dBm	+3 to -40dBm, 1kHz	-	±0.025	-	dB
	-40 to -50dBm, 1kHz	-	±0.050	-	dB
	-50 to -55dBm, 1kHz	-	±0.100	-	dB
Longitudinal Current Capability Per Wire (Note 9)	Test for False Detect	**20**	-	-	mA_{RMS}
	Test for False Detect, Low Power Standby	**10**	-	-	mA_{RMS}
4-Wire to 2-Wire Insertion Loss		**-0.20**	0.00	**+0.20**	dB
2-Wire to 4-Wire Insertion Loss		**-6.22**	-6.02	**-5.82**	dB
4-Wire to 4-Wire Insertion Loss		**-6.22**	-6.02	**-5.82**	dB
Forward Active Idle Channel Noise	2-Wire C-Message, T = +25°C	-	10	13	dBrnC
	4-Wire C-Message, T = +25°C	-	4	7	dBrnC
Reverse Active Idle Channel Noise	2-Wire C-Message, T = +25°C	-	11	14	dBrnC
	4-Wire C-Message, T = +25°C	-	5	8	dBrnC
DC PARAMETERS					
Off Hook Loop Current Limit	Programming Accuracy	**-8.5**	-	**+8.5**	%
	Programming Range	**15**	-	**45**	mA
Off Hook Transient Current Limit	Programming Accuracy	**-10**	-	**+10**	%
	Programming Range	**40**	-	**100**	mA
Loop Current During Low Power Standby	Forward Polarity Only	**18**	-	**26**	mA
Open Circuit Voltage (|Tip - Ring|)	V_{BL} = -16V	-	8.0	-	V_{DC}
	V_{BL} = -24V	**14**	15.5	**17**	V_{DC}
	V_{BH} > -60V	**43**	49	-	V_{DC}
Low Power Standby, Open Circuit Voltage (Tip - Ring)	V_{BL} = -48V	-	44.5	-	V_{DC}
	V_{BH} > -60V	**43**	51.5	-	V_{DC}
Absolute Open Circuit Voltage	V_{RG} in LPS and FA; V_{TG} in RA; V_{BH} > -60V	-	-53	**-56**	V_{DC}
TEST ACCESS FUNCTIONS					
Switch On Voltage	I_{OL} = 45mA; All modes except Power Denial	-	0.30	**0.60**	V
Loopback Max Battery		-	-	**52**	V
LOOP DETECTORS AND SUPERVISORY FUNCTIONS					
Switch Hook Programming Range		**5**	-	**15**	mA

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PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNITS
Switch Hook Programming Accuracy	Assumes 1% External Programming Resistor	**-10**	-	**+10**	%
Dial Pulse Distortion		-	1.0	-	%
Ring Trip Comparator Threshold		**2.3**	2.5	**2.9**	V
Ring Trip Programming Current Accuracy		**-10**	-	**+10**	%
Ground Key Threshold		-	12	-	mA
E0 Transition, DET Output Delay		-	20	-	µs
Thermal Alarm Output	IC Junction Temperature	-	175	-	°C
LOGIC INPUTS (F0, F1, F2, E0, $\overline{SWC}$, BSEL)					
Input Low Voltage		-	-	**0.8**	V
Input High Voltage		**2.0**	-	-	V
Input Low Current	V_{IL} = 0.4V	**-20**	-10	-	µA
Input High Current	V_{IH} = 2.4V	-	-	**1**	µA
LOGIC OUTPUTS ($\overline{DET}$, $\overline{ALM}$)					
Output Low Voltage	I_{OL} = 5mA	-	0.15	**0.4**	V
Output High Voltage	I_{OH} = 100µA	**2.4**	3.5	-	V
SUPPLY CURRENTS					
Low Power Standby, BSEL = 1	I_{CC}	-	3.9	**6.0**	mA
	I_{BH}	-	0.66	**0.90**	mA
Forward or Reverse Active, BSEL = 0	I_{CC}	-	4.9	**6.5**	mA
	I_{BL}	-	1.2	**2.5**	mA
Forward Active, BSEL = 1	I_{CC}	-	7.0	**9.5**	mA
	I_{BL}	-	0.9	**2.0**	mA
	I_{BH}	-	2.2	**3.0**	mA
Ringing, BSEL = 1 (Balanced Ringing, 100)	I_{CC}	-	6.4	**9.0**	mA
	I_{BL}	-	0.3	**1.0**	mA
	I_{BH}	-	2.0	**3.0**	mA
Ringing, BSEL = 1 (Unbalanced Ringing, 010)	I_{CC}	-	9.3	-	mA
	I_{BL}	-	0.3	-	mA
	I_{BH}	-	2.4	-	mA
Forward Loopback, BSEL = 0	I_{CC}	-	10.3	**13.5**	mA
	I_{BL}	-	23.5	**32**	mA
Tip Open, BSEL = 0	I_{CC}	-	3.8	**5.5**	mA
	I_{BL}	-	0.3	**1.0**	mA
Power Denial, BSEL = 0 or 1	I_{CC}	-	4.0	**6.0**	mA
	I_{BL}	-	0.22	**0.5**	mA

Electrical Specifications Unless Otherwise Specified, T_A = -40°C to +85°C for industrial (I) grade and T_A = 0°C to +85°C for commercial (C) grade, V_{BL} = -24V, V_{BH} = -100V, -85V or -75V, V_{CC} = +5V, AGND = BGND = 0V, loop current limit = 25mA. All AC parameters are specified at 600Ω 2-wire terminating impedance over the frequency band of 300Hz to 3.4kHz. Protection resistors = 0Ω. **Boldface limits apply over the operating temperature range. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNITS
ON HOOK POWER DISSIPATION (Note 12)					
Forward or Reverse	V_{BL} = -24V	-	55	-	mW
Low Power Standby	V_{BH} = -100V	-	85	-	mW
	V_{BH} = -85V	-	75	-	mW
	V_{BH} = -75V	-	65	-	mW
Ringing	V_{BH} = -100V	-	250	-	mW
	V_{BH} = -85V	-	230	-	mW
	V_{BH} = -75V	-	225	-	mW
OFF HOOK POWER DISSIPATION (Note 12)					
Forward or Reverse	V_{BL} = -24V	-	305	-	mW
POWER SUPPLY REJECTION RATIO					
V_{CC} to 2-Wire	f = 300Hz	-	40	-	dB
	f = 1kHz	-	35	-	dB
	f = 3.4kHz	-	28	-	dB
V_{CC} to 4-Wire	f = 300Hz	-	45	-	dB
	f = 1kHz	-	43	-	dB
	f = 3.4kHz	-	33	-	dB
V_{BL} to 2-Wire	300Hz ≤ f ≤ 3.4kHz	-	30	-	dB
V_{BL} to 4-Wire	300Hz ≤ f ≤ 3.4kHz	-	35	-	dB
V_{BH} to 2-Wire	300Hz ≤ f ≤ 3.4kHz	-	33	-	dB
V_{BH} to 4-Wire	300Hz ≤ f ≤ 1kHz	-	40	-	dB
	1kHz < f ≤ 3.4kHz	-	45	-	dB

NOTES:

9. These parameters are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
10. Differential Ringing Gain is measured with VRS = 0.795V_{RMS} for -100V devices, VRS = 0.663 V_{RMS} for -85V devices and VRS = 0.575V_{RMS} for -75V devices.
11. Longitudinal Balance is tested per IEEE455-1985, with 368Ω per Tip and Ring terminal.
12. The power dissipation is based on actual device measurements and will be less than worst case calculations based on data sheet supply current limits.
13. For Unbalanced Ringing the Tip terminal is offset to 0V and the Ring terminal is centered at Vbh/2 + 0.5V.
14. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Special Considerations for the QFN Package

The new QFN package offers a significant footprint reduction (65%) and improved thermal performance with respect to the 28 lead PLCC. To realize the thermal enhancements and maintain the high voltage (-100V) performance, the exposed leadframe should be soldered to a power/heat sink plane that is electrically connected to the high battery supply (V_{BH}) within the application board. This approach distributes the heat evenly across the board and is accomplished by using conductive thermal vias. Reference technical brief TB379 and AN9922 for additional information on thermal characterization and board layout considerations.

Product Family Cross Reference

The following table provides an ordering and functional cross reference for the existing HC55180 through HC55184 products and the new and improved HC55185 product.

TABLE 1. PRODUCT CROSS REFERENCE

EXISTING DEVICES	FUNCTIONAL EQUIVALENT
HC55180CIM, HC55180DIM	None Offered
HC55181AIM, HC55182AIM	HC55185AIM
HC55181BIM, HC55182BIM	HC55185BIM
HC55181CIM, HC55182CIM	HC55185CIM
HC55181DIM, HC55182DIM	HC55185DIM
HC55183ECM, HC55184ECM	HC55185ECM

Any of the HC55185 products may be used without the battery switch function by shorting the supply pins VBL and VBH together. This provides compatibility with HC55180 type applications, which do not require the battery switch.

Application Circuit Modifications

The HC55185 basic application circuit is nearly identical to that of the HC55180 through HC55184. The HC55185 requires an additional resistor to program the transient current limit feature. This programming resistor is connected from pin 16 (TL) to ground. In addition, some component values have been changed to improve overall device performance. Table 2 lists the component value changes required for the HC55185 application circuit.

TABLE 2. COMPONENT VALUE CHANGES

REFERENCE	HC55180 - 184	HC55185
RS	210kΩ	66.5kΩ
RP1	≥ 35Ω	≥ 49Ω
RP2	≥ 35Ω	≥ 49Ω
CFB	0.47µ	4.7µ

The value of RS is based on a 600Ω termination impedance and RP1 = RP2 = 49.9Ω. Design equations are provided to calculate RS for other combinations of termination and protection resistance.

The CFB capacitor must be non-polarized for proper device operation in Reverse Active. Ceramic surface mount capacitors (1206 body style) are available from Panasonic with a 6.3V voltage rating. These can be used for CFB since it is internally limited to approximately ±3V. The CDC capacitor may be either polarized or non polarized.

Parametric Improvements

The most significant parametric improvement of the HC55185 is reduction in Idle Channel Noise. This improvement was accomplished by redistributing gains in the impedance matching loop. The impact to the application circuit is the change in the impedance programming resistor RS. The redistribution of gains also improves AC performance at the upper end of the voice band.

Functional Improvements

In addition to parametric improvements, internal circuit changes and application circuit changes have been made to improve the overall device functionality.

Off Hook Interface

The transient behavior of the device in response to mode changes has been significantly improved. The benefit to the application is reduction or more likely elimination of $\overline{DET}$ glitches when off hook events occur. In addition to internal circuit modifications, the change of CFB value contributes to this functional improvement.

Transient Current Limit

The drive current capability of the output amplifiers is determined by an externally programmable output current limit circuit, which is separate from the DC loop current limit function and programmed at the pin TL. The current limit circuit works in both the source and sink direction, with an internally fixed offset to prevent the current limit functions from turning on simultaneously. The current limit function is provided by sensing line current and reducing the voltage drive to the load when the externally set threshold is exceeded, hence forcing a constant source or sink current.

SOURCE CURRENT PROGRAMMING

The source current is externally programmed as shown in Equation 1.

$$R_{TL} = \frac{1780}{I_{SRC}} \quad \text{(EQ. 1)}$$

For example, a source current limit setting of 50mA is programmed with a 35.6kΩ resistor connected from pin 16 of the device to ground. This setting determines the maximum amount of current that flows from Tip to Ring during an off hook event until the DC loop current limit responds. In addition, this setting also determines the amount of current

that will flow from Tip or Ring when external battery faults occur.

SINK CURRENT PROGRAMMING

The sink current limit is internally offset 20% higher than the externally programmed source current limit setting.

$$I_{SNK} = 1.20 \times I_{SRC} \quad \text{(EQ. 2)}$$

If the source current limit is set to 50mA, the sink current limit will be 60mA. This setting will determine the maximum current that flows into Tip or Ring when external ground faults occur.

FUNCTIONAL DESCRIPTION

Each amplifier is designed to limit source current and sink current. Figure 1 shows the functionality of the circuit for the case of limiting the source current. A similar diagram applies to the sink current limit with current polarity changed accordingly.

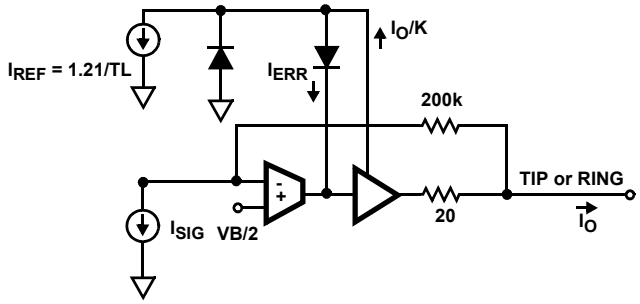


FIGURE 1. CURRENT LIMIT FUNCTIONAL DIAGRAM

During normal operation, the error current (I_{ERR}) is zero and the output voltage is determined by the signal current (I_{SIG}) multiplied by the 200k feedback resistor. With the current polarity as shown for I_{SIG}, the output voltage moves positive with respect to half battery. Assuming the amplifier output is driving a load at a more negative potential, the amplifier output will source current.

During excessive output source current flow, the scaled output current (I_O/K) exceeds the reference current (I_{REF}) forcing an error current (I_{ERR}). With the polarity as shown, the error current subtracts from the signal current, which reduces the amplifier output voltage. By reducing the output voltage, the source current to the load is decreased and the output current is limited.

DETERMINING THE PROPER SETTING

Since this feature programs the maximum output current of the device, the setting must be high enough to allow for detection of ring trip or programmed off hook loop current, whichever is greater.

To allow for proper ring trip operation, the transient current limit setting should be set at least 25% higher than the peak ring trip current setting. Setting the transient current 25% higher should account for programming tolerances of both the ring trip threshold and the transient current limit.

If loop current is larger than ring trip current (low REN applications) then the transient current limit should be set at least 35% higher than the loop current setting. The slightly higher offset accounts for the slope of the loop current limit function.

Attention to detail should be exercised when programming the transient current limit setting. If ring trip detect does not occur while ringing, then re-examine the transient current limit and ring trip threshold settings.

Design Equations

Loop Supervision Thresholds

SWITCH HOOK DETECT

The switch hook detect threshold is set by a single external resistor, R_{SH}. Equation 3 is used to calculate the value of R_{SH}.

$$R_{SH} = 600/I_{SH} \quad \text{(EQ. 3)}$$

The term I_{SH} is the desired DC loop current threshold. The loop current threshold programming range is from 5mA to 15mA.

GROUND KEY DETECT

The ground key detector senses a DC current imbalance between the Tip and Ring terminals when the ring terminal is connected to ground. The ground key detect threshold is not externally programmable and is internally fixed to 12mA regardless of the switch hook threshold.

RING TRIP DETECT

The ring trip detect threshold is set by a single external resistor, R_{RT}. I_{RT} should be set between the peak ringing current and the peak off hook current while still ringing.

$$R_{RT} = 1800/I_{RT} \quad \text{(EQ. 4)}$$

In addition, the ring trip current must be set below the transient current limit, including tolerances. The capacitor C_{RT}, in parallel with R_{RT}, will set the ring trip response time.

Loop Current Limit

The loop current limit of the device is programmed by the external resistor R_{IL}. The value of R_{IL} can be calculated using Equation 5:

$$R_{IL} = \frac{1760}{I_{LIM}} \quad \text{(EQ. 5)}$$

The term I_{LIM} is the desired loop current limit. The loop current limit programming range is from 15mA to 45mA.

Impedance Matching

The impedance of the device is programmed with the external component R_S. R_S is the gain setting resistor for the feedback amplifier that provides impedance matching. If complex impedance matching is required, then a complex network can be substituted for R_S.

RESISTIVE IMPEDANCE SYNTHESIS

The source impedance of the device, Z_O, can be calculated in Equation 6.

$$R_S = 133.3(Z_O) \quad \text{(EQ. 6)}$$

The required impedance is defined by the terminating impedance and protection resistors, as shown in Equation 7.

$$Z_O = Z_L - 2R_P \quad \text{(EQ. 7)}$$

4-WIRE TO 2-WIRE GAIN

The 4-wire to 2-wire gain is defined as the receive gain. It is a function of the terminating impedance, synthesized impedance and protection resistors. Equation 8 calculates the receive gain, G_{42}.

$$G_{42} = -2\left(\frac{Z_L}{Z_O + 2R_P + Z_L}\right) \quad \text{(EQ. 8)}$$

When the device source impedance and protection resistors equals the terminating impedance, the receive gain equals unity.

2-WIRE TO 4-WIRE GAIN

The 2-wire to 4-wire gain (G_{24}) is the gain from tip and ring to the VTX output. The transmit gain is calculated in Equation 9.

$$G_{24} = -\left(\frac{Z_O}{Z_O + 2R_P + Z_L}\right) \quad \text{(EQ. 9)}$$

When the protection resistors are set to zero, the transmit gain is -6dB.

TRANSHYBRID GAIN

The transhybrid gain is defined as the 4-wire to 4-wire gain (G_{44}).

$$G_{44} = -\left(\frac{Z_O}{Z_O + 2R_P + Z_L}\right) \quad \text{(EQ. 10)}$$

When the protection resistors are set to zero, the transhybrid gain is -6dB.

COMPLEX IMPEDANCE SYNTHESIS

Substituting the impedance programming resistor, R_S, with a complex programming network provides complex impedance synthesis.

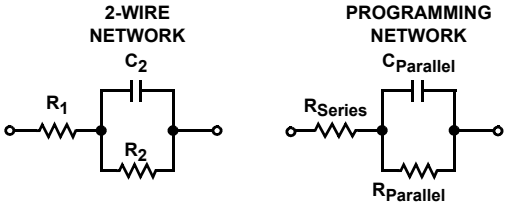


FIGURE 2. COMPLEX PROGRAMMING NETWORK

The reference designators in the programming network match the evaluation board. The component R_S has a different design equation than the R_S used for resistive impedance synthesis. The design equations for each component are provided in the following equations.

$$R_{Series} = 133.3 \times (R_1 - 2(R_P)) \quad \text{(EQ. 11)}$$

$$R_{Parallel} = 133.3 \times R_2 \quad \text{(EQ. 12)}$$

$$C_{Parallel} = C_2 / 133.3 \quad \text{(EQ. 13)}$$

Low Power Standby

Overview

The low power standby mode (LPS, 000) should be used during idle line conditions. The device is designed to operate from the high battery during this mode. Most of the internal circuitry is powered down, resulting in low power dissipation. If the 2-wire (tip/ring) DC voltage requirements are not critical during idle line conditions, the device may be operated from the low battery. Operation from the low battery will decrease the standby power dissipation.

TABLE 3. DEVICE INTERFACES DURING LPS

INTERFACE	ON	OFF	NOTES
Receive		x	AC transmission, impedance matching and ringing are disabled during this mode.
Ringing		x	
Transmit		x	
2-Wire	x		Amplifiers disabled.
Loop Detect	x		Switch hook or ground key.

2-Wire Interface

During LPS, the 2-wire interface is maintained with internal switches and voltage references. The Tip and Ring amplifiers are turned off to conserve power. The device will provide MTU compliance, loop current and loop supervision. Figure 3 represents the internal circuitry providing the 2-wire interface during low power standby.

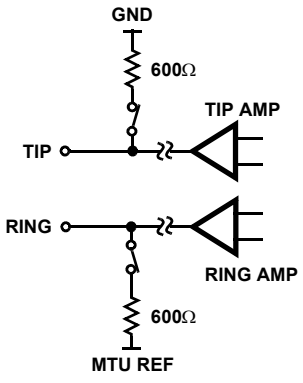


FIGURE 3. LPS 2-WIRE INTERFACE CIRCUIT DIAGRAM

MTU Compliance

Maintenance Termination Unit or MTU compliance places DC voltage requirements on the 2-wire terminals during idle

line conditions. The minimum idle voltage is 42.75V. The high side of the MTU range is 56V. The voltage is expressed as the difference between Tip and Ring.

The Tip voltage is held near ground through a 600Ω resistor and switch. The Ring voltage is limited to a maximum of -56V (by MTU REF) when operating from either the high or low battery. A switch and 600Ω resistor connect the MTU reference to the Ring terminal. When the high battery voltage exceeds the MTU reference of -56V, the Ring terminal will be clamped by the internal reference (typically -54V). The same Ring relationships apply when operating from the low battery voltage. For high battery voltages (V_{BH}) less than or equal to the internal MTU reference threshold:

$$V_{RING} = V_{BH} + 4 \quad \text{(EQ. 14)}$$

Loop Current

During LPS, the device will provide current to a load. The current path is through resistors and switches, and will be a function of the off hook loop resistance (R_{LOOP}). This includes the off hook phone resistance and copper loop resistance. The current available during LPS is determined by Equation 15.

$$I_{LOOP} = (-1-(-49))/(600+600+R_{LOOP}) \quad \text{(EQ. 15)}$$

Internal current limiting of the standby switches will limit the maximum current to 20mA.

Another loop current related parameter is longitudinal current capability. The longitudinal current capability is reduced to $10mA_{RMS}$ per pin. The reduction in longitudinal current capability is a result of turning off the Tip and Ring amplifiers.

On Hook Power Dissipation

The on hook power dissipation of the device during LPS is determined by the operating voltages and quiescent currents and is calculated using Equation 16.

$$P_{LPS} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \quad \text{(EQ. 16)}$$

The quiescent current terms are specified in the electrical tables for each operating mode. Load power dissipation is not a factor since this is an on hook mode. Some applications may specify a standby current. The standby current may be a charging current required for modern telephone electronics.

Standby Current Power Dissipation

Any standby line current, I_{SLC}, introduces an additional power dissipation term P_{SLC}. Equation 17 illustrates the power contribution is zero when the standby line current is zero.

$$P_{SLC} = I_{SLC} \times (|V_{BH}| - 49 + 1 + I_{SLC} x1200) \quad \text{(EQ. 17)}$$

If the battery voltage is less than -49V (the MTU clamp is off), the standby line current power contribution reduces to Equation 18.

$$P_{SLC} = I_{SLC} \times (|V_{BH}| + 1 + I_{SLC} x1200) \quad \text{(EQ. 18)}$$

Most applications do not specify charging current requirements during standby. When specified, the typical charging current may be as high as 5mA.

Forward Active

Overview

The forward active mode (FA, 001) is the primary AC transmission mode of the device. On hook transmission, DC loop feed and voice transmission are supported during forward active. Loop supervision is provided by either the switch hook detector (E0 = 1) or the ground key detector (E0 = 0). The device may be operated from either high or low battery for on-hook transmission and low battery for loop feed.

On-Hook Transmission

The primary purpose of on hook transmission will be to support caller ID and other advanced signalling features. The transmission over load level while on hook is $3.5V_{PEAK}$.

When operating from the high battery, the DC voltages at Tip and Ring are MTU compliant. The typical Tip voltage is -4V and the Ring voltage is a function of the battery voltage for battery voltages less than -60V as shown in Equation 19.

$$V_{RING} = V_{BH} + 4 \quad \text{(EQ. 19)}$$

Loop supervision is provided by the switch hook detector at the $\overline{DET}$ output. When $\overline{DET}$ goes low, the low battery should be selected for DC loop feed and voice transmission.

Feed Architecture

The design implements a voltage feed current sense architecture. The device controls the voltage across Tip and Ring based on the sensing of load current. Resistors are placed in series with Tip and Ring outputs to provide the current sensing. Figure 4 illustrates the concept.

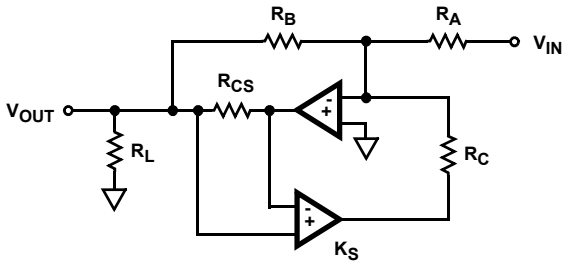


FIGURE 4. VOLTAGE FEED CURRENT SENSE DIAGRAM

By monitoring the current at the amplifier output, a negative feedback mechanism sets the output voltage for a defined load. The amplifier gains are set by resistor ratios (R_A, R_B, R_C) providing all the performance benefits of matched

resistors. The internal sense resistor, R_{CS}, is much smaller than the gain resistors and is typically 20Ω for this device. The feedback mechanism, K_S, represents the amplifier configuration providing the negative feedback.

DC Loop Feed

The feedback mechanism for monitoring the DC portion of the loop current is the loop detector. A low pass filter is used in the feedback to block voice band signals from interfering with the loop current limit function. The pole of the low pass filter is set by the external capacitor C_{DC}. The value of the external capacitor should be 4.7µF.

Most applications will operate the device from low battery while off hook. The DC feed characteristic of the device will drive Tip and Ring towards half battery to regulate the DC loop current. For light loads, Tip will be near -4V and Ring will be near V_{VBL} + 4V. The following diagram shows the DC feed characteristic.

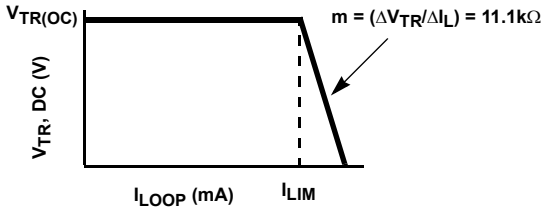


FIGURE 5. DC FEED CHARACTERISTIC

The point on the y-axis labeled $V_{TR(OC)}$ is the open circuit Tip to Ring voltage and is defined by the feed battery voltage.

$$V_{TR(OC)} = |V_{BL}| - 8 \quad \text{(EQ. 20)}$$

The curve of Figure 5 determines the actual loop current for a given set of loop conditions. The loop conditions are determined by the low battery voltage and the DC loop impedance. The DC loop impedance is the sum of the protection resistance, copper resistance (Ω/foot) and the telephone off hook DC resistance.

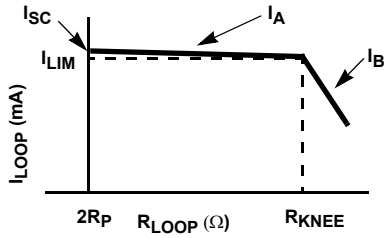


FIGURE 6. I_{LOOP} vs R_{LOOP} LOAD CHARACTERISTIC

The slope of the feed characteristic and the battery voltage define the maximum loop current on the shortest possible loop as the short circuit current I_{SC}.

$$I_{SC} = I_{LIM} + \frac{V_{TR(OC)} - 2R_P I_{LIM}}{1.1e4} \quad \text{(EQ. 21)}$$

The term I_{LIM} is the programmed current limit, $1760/R_{IL}$. The line segment I_A represents the constant current region of the loop current limit function.

$$I_A = I_{LIM} + \frac{V_{TR(OC)} - R_{LOOP} I_{LIM}}{1.1e4} \quad \text{(EQ. 22)}$$

The maximum loop impedance for a programmed loop current is defined as R_{KNEE}.

$$R_{KNEE} = \frac{V_{TR(OC)}}{I_{LIM}} \quad \text{(EQ. 23)}$$

When R_{KNEE} is exceeded, the device will transition from constant current feed to constant voltage, resistive feed. The line segment I_B represents the resistive feed portion of the load characteristic.

$$I_B = \frac{V_{TR(OC)}}{R_{LOOP}} \quad \text{(EQ. 24)}$$

Voice Transmission

The feedback mechanism for monitoring the AC portion of the loop current consists of two amplifiers, the sense amplifier (SA) and the transmit amplifier (TA). The AC feedback signal is used for impedance synthesis. A detailed model of the AC feed back loop is provided below.

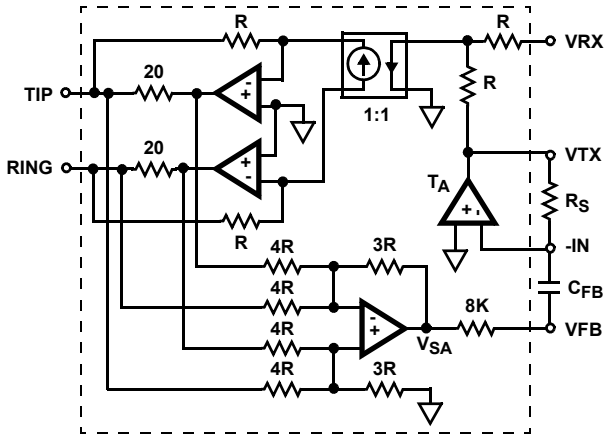


FIGURE 7. AC SIGNAL TRANSMISSION MODEL

The gain of the transmit amplifier, set by R_S, determines the programmed impedance of the device. The capacitor C_{FB} blocks the DC component of the loop current. The ground symbols in the model represent AC grounds, not actual DC potentials.

The sense amp output voltage, V_{SA}, as a function of Tip and Ring voltage and load is calculated using Equation 25.

$$V_{SA} = -(V_T - V_R)\frac{30}{Z_L} \quad \text{(EQ. 25)}$$

The transmit amplifier provides the programmable gain required for impedance synthesis. In addition, the output of

this amplifier interfaces to the CODEC transmit input. The output voltage is calculated using Equation 26.

$$V_{VTX} = -V_{SA}\left(\frac{R_S}{8e3}\right) \quad \text{(EQ. 26)}$$

Once the impedance matching components have been selected using the design equations, the above equations provide additional insight as to the expected AC node voltages for a specific Tip and Ring load.

Transhybrid Balance

The final step in completing the impedance synthesis design is calculating the necessary gains for transhybrid balance. The AC feed back loop produces an echo at the V_{TX} output of the signal injected at V_{RX}. The echo must be cancelled to maintain voice quality. Most applications will use a summing amplifier in the CODEC front end as shown below to cancel the echo signal.

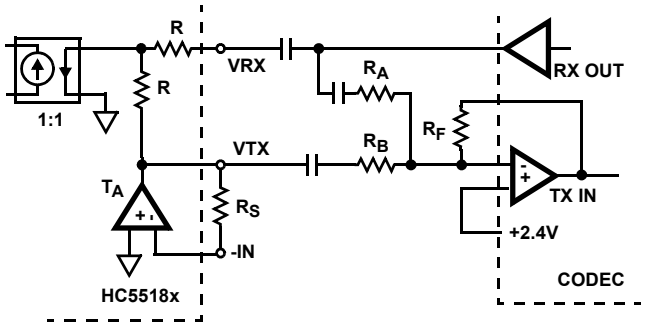


FIGURE 8. TRANSHYBRID BALANCE INTERFACE

The resistor ratio, R_F/R_B, provides the final adjustment for the transmit gain, G_{TX}. The transmit gain is calculated using Equation 27.

$$G_{TX} = -G_{24}\left(\frac{R_F}{R_B}\right) \quad \text{(EQ. 27)}$$

Most applications set $R_F = R_B$, hence the device 2-wire to 4-wire equals the transmit gain. Typically R_B is greater than 20kΩ to prevent loading of the device transmit output.

The resistor ratio, R_F/R_A, is determined by the transhybrid gain of the device, G_{44}. R_F is previously defined by the transmit gain requirement and R_A is calculated using Equation 28.

$$R_A = \frac{R_B}{G_{44}} \quad \text{(EQ. 28)}$$

Power Dissipation

The power dissipated by the device during on hook transmission is strictly a function of the quiescent currents for each supply voltage during Forward Active operation.

$$P_{FAQ} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \quad \text{(EQ. 29)}$$

Off hook power dissipation is increased above the quiescent power dissipation by the DC load. If the loop length is less than or equal to R_{KNEE}, the device is providing constant current, I_A, and the power dissipation is calculated using Equation 30.

$$P_{FA(IA)} = P_{FA(Q)} + (V_{BL} x I_A) - (R_{LOOP} x I^2_A) \quad \text{(EQ. 30)}$$

If the loop length is greater than R_{KNEE}, the device is operating in the constant voltage, resistive feed region. The power dissipated in this region is calculated using Equation 31.

$$P_{FA(IB)} = P_{FA(Q)} + (V_{BL} x I_B) - (R_{LOOP} x I^2_B) \quad \text{(EQ. 31)}$$

Since the current relationships are different for constant current versus constant voltage, the region of device operation is critical to valid power dissipation calculations.

Reverse Active

Overview

The reverse active mode (RA, 011) provides the same functionality as the forward active mode. On hook transmission, DC loop feed and voice transmission are supported. Loop supervision is provided by either the switch hook detector (E0 = 1) or the ground key detector (E0 = 0). The device may be operated from either high or low battery.

During reverse active the Tip and Ring DC voltage characteristics exchange roles. That is, Ring is typically 4V below ground and Tip is typically 4V more positive than battery. Otherwise, all feed and voice transmission characteristics are identical to forward active.

Silent Polarity Reversal

Changing from forward active to reverse active or vice versa is referred to as polarity reversal. Many applications require slew rate control of the polarity reversal event. Requirements range from minimizing cross talk to protocol signalling.

The device uses an external low voltage capacitor, C_{POL}, to set the reversal time. Once programmed, the reversal time will remain nearly constant over various load conditions. In addition, the reversal timing capacitor is isolated from the AC loop, therefore loop stability is not impacted.

The internal circuitry used to set the polarity reversal time is shown in Figure 9.

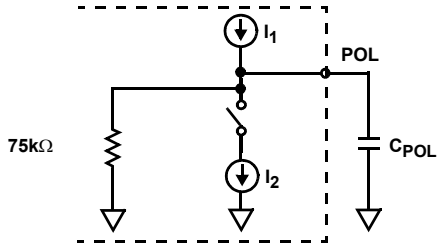


FIGURE 9. REVERSAL TIMING CONTROL

During forward active, the current from source I1 charges the external timing capacitor C_{POL} and the switch is open.

The internal resistor provides a clamping function for voltages on the POL node. During reverse active, the switch closes and I2 (roughly twice I1) pulls current from I1 and the timing capacitor. The current at the POL node provides the drive to a differential pair, which controls the reversal time of the Tip and Ring DC voltages.

$$C_{POL} = \frac{\Delta time}{75000} \quad \text{(EQ. 32)}$$

Where Δtime is the required reversal time. Polarized capacitors may be used for C_{POL}. The low voltage at the POL pin and minimal voltage excursion $\pm$0.75V, are well suited to polarized capacitors.

Power Dissipation

The power dissipation equations for forward active operation also apply to the reverse active mode.

Ringing

Overview

The ringing mode (RNG,100) provides linear amplification to support a variety of ringing waveforms. A programmable ring trip function provides loop supervision and auto disconnect upon ring trip. The device is designed to operate from the high battery during this mode.

Architecture

The device provides linear amplification to the signal applied to the ringing input, V_{RS}. The differential ringing gain of the device is 80V/V. The circuit model for the ringing path is shown in Figure 10.

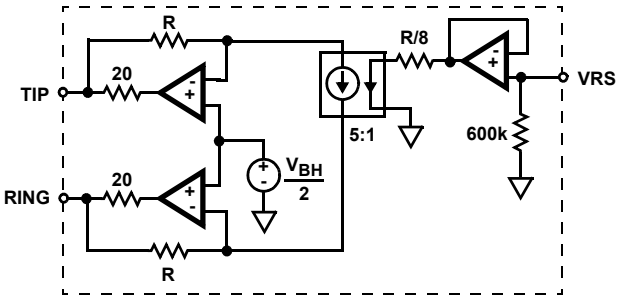


FIGURE 10. LINEAR RINGING MODEL

The voltage gain from the VRS input to the Tip output is 40V/V. The resistor ratio provides a gain of 8 and the current mirror provides a gain of 5. The voltage gain from the VRS input to the Ring output is -40V/V. The equations for the Tip and Ring outputs during ringing are provided in the following equations.

$$V_T = \frac{V_{BH}}{2} + (40 \times VRS) \quad \text{(EQ. 33)}$$

$$V_R = \frac{V_{BH}}{2} - (40 \times VRS) \quad \text{(EQ. 34)}$$

When the input signal at VRS is zero, the Tip and Ring amplifier outputs are centered at half battery. The device provides auto centering for easy implementation of sinusoidal ringing waveforms. Both AC and DC control of the Tip and Ring outputs is available during ringing. This feature allows for DC offsets as part of the ringing waveform.

Ringing Input

The ringing input, V_{RS}, is a high impedance input. The high impedance allows the use of low value capacitors for AC coupling the ring signal. The V_{RS} input is enabled only during the ringing mode, therefore a free running oscillator may be connected to VRS at all times.

When operating from a battery of -100V, each amplifier, Tip and Ring, will swing a maximum of $95V_{P-P}$. Hence, the maximum signal swing at VRS to achieve full scale ringing is approximately $2.4V_{P-P}$. The low signal levels are compatible with the output voltage range of the CODEC. The digital nature of the CODEC ideally suits it for the function of programmable ringing generator. See Applications Section.

Logic Control

Ringing patterns consist of silent intervals. The ringing to silent pattern is called the ringing cadence. During the silent portion of ringing, the device can be programmed to any other operating mode. The most likely candidates are low power standby or forward active. Depending on system requirements, the low or high battery may be selected.

Loop supervision is provided with the ring trip detector. The ring trip detector senses the change in loop current when the phone is taken off hook. The loop detector full wave rectifies the ringing current, which is then filtered with external components R_{RT} and C_{RT}. The resistor R_{RT} sets the trip threshold and the capacitor C_{RT} sets the trip response time. Most applications will require a trip response time less than 150ms.

Three very distinct actions occur when the devices detects a ring trip. First, the $\overline{DET}$ output is latched low. The latching mechanism eliminates the need for software filtering of the detector output. The latch is cleared when the operating mode is changed externally. Second, the VRS input is disabled, removing the ring signal from the line. Third, the device is internally forced to the forward active mode.

Power Dissipation

The power dissipation during ringing is dictated by the load driving requirements and the ringing waveform. The key to valid power calculations is the correct definition of average and RMS currents. The average current defines the high battery supply current. The RMS current defines the load current.

The cadence provides a time averaging reduction in the peak power. The total power dissipation consists of ringing power, P_r, and the silent interval power, P_s.

$$P_{RNG} = P_r \times \frac{t_r}{t_r + t_s} + P_s \times \frac{t_s}{t_r + t_s} \quad \text{(EQ. 35)}$$

The terms t_R and t_S represent the cadence. The ringing interval is t_R and the silent interval is t_S. The typical cadence ratio t_R:t_S is 1:2.

The quiescent power of the device in the ringing mode is defined in Equation 36.

$$P_{r(Q)} = V_{BH} \times I_{BHQ} + V_{BL} \times I_{BLQ} + V_{CC} \times I_{CCQ} \quad \text{(EQ. 36)}$$

The total power during the ringing interval is the sum of the quiescent power and loading power:

$$P_r = P_{r(Q)} + V_{BH} \times I_{AVG} - \frac{V_{RMS}^2}{Z_{REN} + R_{LOOP}} \quad \text{(EQ. 37)}$$

For sinusoidal waveforms, the average current, I_{AVG}, is defined in Equation 38.

$$I_{AVG} = \left(\frac{2}{\pi}\right) \frac{V_{RMS} \times \sqrt{2}}{Z_{REN} + R_{LOOP}} \quad \text{(EQ. 38)}$$

The silent interval power dissipation will be determined by the quiescent power of the selected operating mode.

Unbalanced Ringing

The HC55185GCM offers a new Unbalanced Ringing mode (010). This feature has been added to accommodate some Analog PBX Trunk Lines that require the Tip terminal to be held near ground for the duration of the ringing bursts. The Tip terminal is offset to 0V's with an internal current source that is applied to the inverting input of the Tip amplifier. This reduces the differential ringing gain to 40V/V. The Ring terminal will center at Vbh/2 and swing from -Vbh to ground. As in Balanced Ringing, off hook detection is accomplished by sensing the peak current and comparing it to a preset threshold. This allows the same sensing, comparing and threshold circuitry to be used in both Ringing modes. This mode of operation does not require any additional external components.

Forward Loop Back

Overview

The Forward Loop Back mode (FLB, 101) provides test capability for the device. An internal signal path is enabled allowing for both DC and AC verification. The internal 600Ω terminating resistor has a tolerance of ±20%. The device is intended to operate from only the low battery during this mode.

Architecture

When the forward loop back mode is initiated internal switches connect a 600Ω load across the outputs of the Tip and Ring amplifiers.

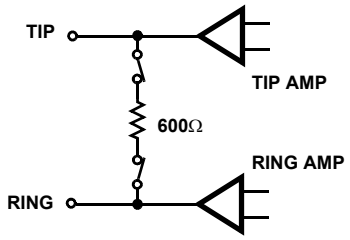


FIGURE 11. FORWARD LOOP BACK INTERNAL TERMINATION

DC Verification

When the internal signal path is provided, DC current will flow from Tip to Ring. The DC current will force $\overline{DET}$ low, indicating the presence of loop current. In addition, the $\overline{ALM}$ output will also go low. This does not indicate a thermal alarm condition. Rather, proper logic operation is verified in the event of a thermal shutdown. In addition to verifying device functionality, toggling the logic outputs verifies the interface to the system controller.

AC Verification

The entire AC loop of the device is active during the forward loop back mode. Therefore a 4-wire to 4-wire level test capability is provided. Depending on the transhybrid balance implementation, test coverage is provided by a one or two step process.

System architectures which cannot disable the transhybrid function would require a two step process. The first step would be to send a test tone to the device while on hook and not in forward loop back mode. The return signal would be the test level times the gain R_F/R_A of the transhybrid amplifier. Since the device would not be terminated, cancellation would not occur. The second step would be to program the device to FLB and resend the test tone. The return signal would be much lower in amplitude than the first step, indicating the device was active and the internal termination attenuated the return signal.

System architectures which disable the transhybrid function would achieve test coverage with a signal step. Once the transhybrid function is disable, program the device for FLB and send the test tone. The return signal level is determined by the 4-wire to 4-wire gain of the device.

Tip Open

Overview

The tip open mode (110) is intended for compatibility for PBX type interfaces. Used during idle line conditions, the device does not provide transmission. Loop supervision is provided by either the switch hook detector (E0 = 1) or the ground key detector (E0 = 0). The ground key detector will be used in most applications. The device may be operated from either high or low battery.

Functionality

During tip open operation, the Tip switch is disabled and the Ring switch is enabled. The minimum Tip impedance is 30kΩ. The only active path through the device will be the Ring switch.

In keeping with the MTU characteristics of the device, Ring will not exceed -56V when operating from the high battery. Though MTU does not apply to tip open, safety requirements are satisfied.

Power Denial

Overview

The power denial mode (111) will shutdown the entire device except for the logic interface. Loop supervision is not provided. This mode may be used as a sleep mode or to shut down in the presence of a persistent thermal alarm. Switching between high and low battery will have no effect during power denial.

Functionality

During power denial, both the Tip and Ring amplifiers are disabled, representing high impedances. The voltages at both outputs are near ground. The logic control to the uncommitted switch is disabled during power denial forcing the switch to the open state.

Thermal Shutdown

In the event the safe die temperature is exceeded, the $\overline{ALM}$ output will go low and $\overline{DET}$ will go high and the part will automatically shutdown. When the device cools, $\overline{ALM}$ will go high and $\overline{DET}$ will reflect the loop status. If the thermal fault persists, $\overline{ALM}$ will go low again and the part will shutdown. Programming power denial will permanently shutdown the device and stop the self cooling cycling.

Battery Switching

Overview

The integrated battery switch selects between the high battery and low battery. The battery switch is controlled with the logic input BSEL. When BSEL is a logic high, the high battery is selected and when a logic low, the low battery is selected. All operating modes of the device will operate from high or low battery except forward loop back.

Functionality

The logic control is independent of the operating mode decode. Independent logic control provides the most flexibility and will support all application configurations.

When changing device operating states, battery switching should occur simultaneously with or prior to changing the operating mode. In most cases, this will minimize overall power dissipation and prevent glitches on the $\overline{DET}$ output.

The only external component required to support the battery switch is a diode in series with the V_{BH} supply lead. In the event that high battery is removed, the diode allows the device to transition to low battery operation.

Low Battery Operation

All off hook operating conditions should use the low battery. The prime benefit will be reduced power dissipation. The typical low battery for the device is -24V. However this may be increased to support longer loop lengths or high loop current requirements. Standby conditions may also operate from the low battery if MTU compliance is not required, further reducing standby power dissipation.

High Battery Operation

Other than ringing, the high battery should be used for standby conditions which must provide MTU compliance. During standby operation the power consumption is typically 85mW with -100V battery. If ringing requirements do not require full 100V operation, then a lower battery will result in lower standby power.

High Voltage Decoupling

The 100V rating of the device will require a capacitor of higher voltage rating for decoupling. Suggested decoupling values for all device pins are 0.1µF. Standard surface mount ceramic capacitors are rated at 100V. For applications driven at low cost and small size, the decoupling scheme shown below could be implemented.

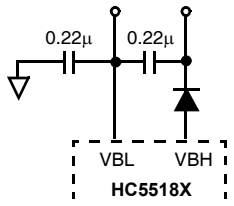


FIGURE 12. ALTERNATE DECOUPLING SCHEME

It is important to place the external diode between the VBH pin and the decoupling capacitor. Attaching the decoupling capacitor directly to the VBH pin will degrade the reliability of the device. Refer to Figure 12 for the proper arrangement. This applies to both single and stacked and decoupling arrangements.

If VBL and VBH are tied together to override the battery switch function, then the external diode is not needed and the decoupling may be attached directly to VBH.

Uncommitted Switch

Overview

The uncommitted switch is a three terminal device designed for flexibility. The logic control input, $\overline{SWC}$, allows switch operation during all states except Power Denial. The switch is activated by a logic low. The positive and negative terminals of the device are labeled SW+ and SW- respectively.

Relay Driver

The uncommitted switch may be used as a relay driver by connecting SW+ to the relay coil and SW- to ground. The switch is designed to have a maximum on voltage of 0.6V with a load current of 45mA.

Since the device provides the ringing waveform, the relay functions which may be supported include subscriber disconnect, test access or line interface bypass. An external snubber diode is not required when using the uncommitted switch as a relay driver.

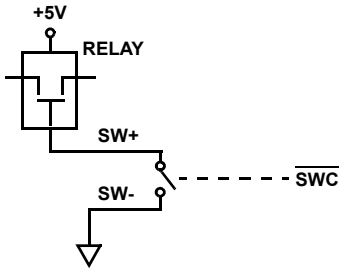


FIGURE 13. EXTERNAL RELAY SWITCHING

Test Load

The switch may be used to connect test loads across Tip and Ring. The test loads can provide external test termination for the device. Proper connection of the uncommitted switch to Tip and Ring is shown in Figure 14.

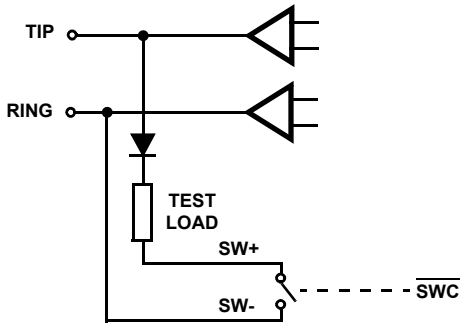


FIGURE 14. TEST LOAD SWITCHING

The diode in series with the test load blocks current from flowing through the uncommitted switch when the polarity of the Tip and Ring terminals are reversed. In addition to the reverse active state, the polarity of Tip and Ring are reversed for half of the ringing cycle. With independent logic control and the blocking diode, the uncommitted switch may be continuously connected to the Tip and Ring terminals.

Basic Application Circuit

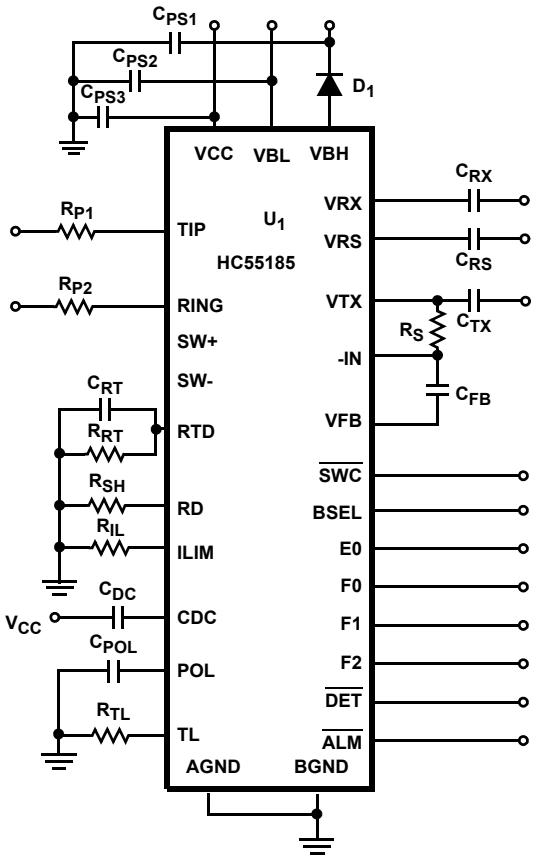


FIGURE 15. HC55185 BASIC APPLICATION CIRCUIT

TABLE 4. BASIC APPLICATION CIRCUIT COMPONENT LIST

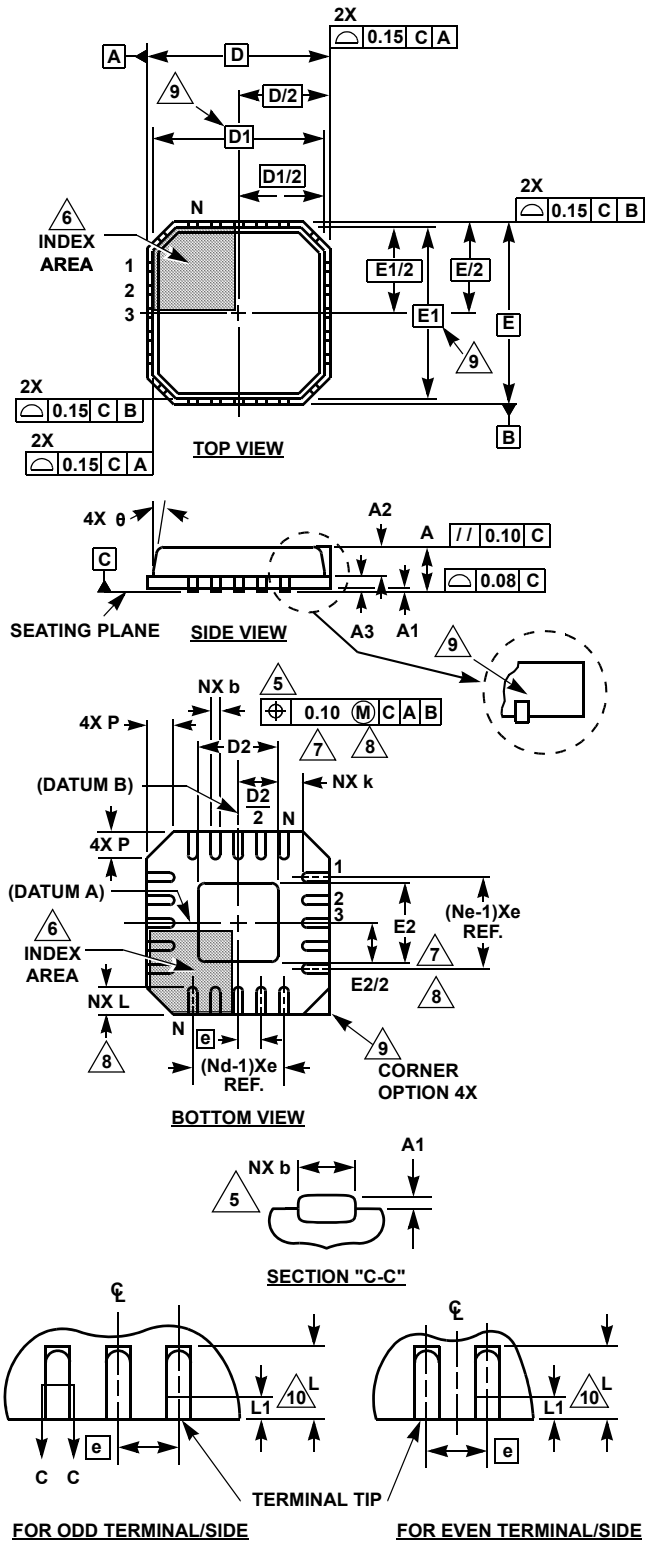
COMPONENT	VALUE	TOL	RATING
U1 - Ringing SLIC	HC55185	N/A	N/A
R_{TL}	18.7kΩ	1%	0.1W
R_{RT}	23.7kΩ	1%	0.1W
R_{SH}	49.9kΩ	1%	0.1W
R_{IL}	71.5kΩ	1%	0.1W
R_S	66.5kΩ	1%	0.1W
C_{RX}, C_{RS}, C_{TX}, C_{RT}, C_{POL}	0.47µF	20%	10V
C_{DC}, C_{FB}	4.7µF	20%	10V
C_{PS1}	0.1µF	20%	>100V
C_{PS2}, C_{PS3}	0.1µF	20%	100V
D_1	1N400X type with breakdown > 100V.		
R_{P1}, R_{P2} Standard applications will use ≥ 49Ω per side. Protection resistor values are application dependent and will be determined by protection requirements.			

Design Parameters: Ring Trip Threshold = $76mA_{PEAK}$, Switch Hook Threshold = 12mA, Loop Current Limit = 24.6mA, Synthesize Device Impedance = (3*66.5kΩ)/400 = 498.8Ω, with 49.9Ω protection resistors, impedance across Tip and Ring terminals = 599Ω. Transient current limit = 95mA.

Pin Descriptions

PLCC	QFN	SYMBOL	DESCRIPTION
1	29	TIP	TIP power amplifier output.
2	30	BGND	Battery Ground - To be connected to zero potential. All loop current and longitudinal current flow from this ground. Internally separate from AGND but it is recommended that it is connected to the same potential as AGND.
3	31	VBL	Low battery supply connection.
4	32	VBH	High battery supply connection for the most negative battery.
5	1	SW+	Uncommitted switch positive terminal.
6	2	SW-	Uncommitted switch negative terminal.
7	3	$\overline{SWC}$	Switch control input. This TTL compatible input controls the uncommitted switch, with a logic “0” enabling the switch and logic “1” disabling the switch. The logic control is disabled in the Power Denial state, forcing the switch to the open state
8	4	F2	Mode Control Input - MSB. F2-F0 for the TTL compatible parallel control interface for controlling the various modes of operation of the device.
9	5	F1	Mode control input.
10	6	F0	Mode control input.
11	7	E0	Detector Output Selection Input. This TTL input controls the multiplexing of the SHD (E0 = 1) and GKD (E0 = 0) comparator outputs to the $\overline{DET}$ output based upon the state at the F2-F0 pins (see the Device Operating Modes table shown on page 2).
12	9	DET	Detector Output - This TTL output provides on-hook/off-hook status of the loop based upon the selected operating mode. The detected output will either be switch hook, ground key or ring trip (see the Device Operating Modes table shown on page 2).
13	10	ALM	Thermal Shutdown Alarm. This pin signals the internal die temperature has exceeded safe operating temperature (approximately 175°C) and the device has been powered down automatically.
14	11	AGND	Analog ground reference. This pin should be externally connected to BGND.
15	12	BSEL	Selects between high and low battery, with a logic “1” selecting the high battery and logic “0” the low battery.
16	13	TL	Programming pin for the transient current limit feature, set by an external resistor to ground.
17	14	POL	External capacitor on this pin sets the polarity reversal time.
18	15	VRS	Ringing Signal Input - Analog input for driving 2-wire interface while in Ring Mode.
19	17	VRX	Analog Receive Voltage - 4-wire analog audio input voltage. AC couples to CODEC.
20	18	VTX	Transmit Output Voltage - Output of impedance matching amplifier, AC couples to CODEC.
21	19	VFB	Feedback voltage for impedance matching. This voltage is scaled to accomplish impedance matching.
22	20	-IN	Impedance matching amplifier summing node.
23	21	VCC	Positive voltage power supply, usually +5V.
24	22	CDC	DC Biasing Filter Capacitor - Connects between this pin and V_{CC}.
25	23	RTD	Ring trip filter network.
26	24	ILIM	Loop Current Limit programming resistor.
27	25	RD	Switch hook detection threshold programming resistor.
28	27	RING	RING power amplifier output.

Quad Flat No-Lead Plastic Package (QFN)



L32.7x7

32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VKKC ISSUE C)

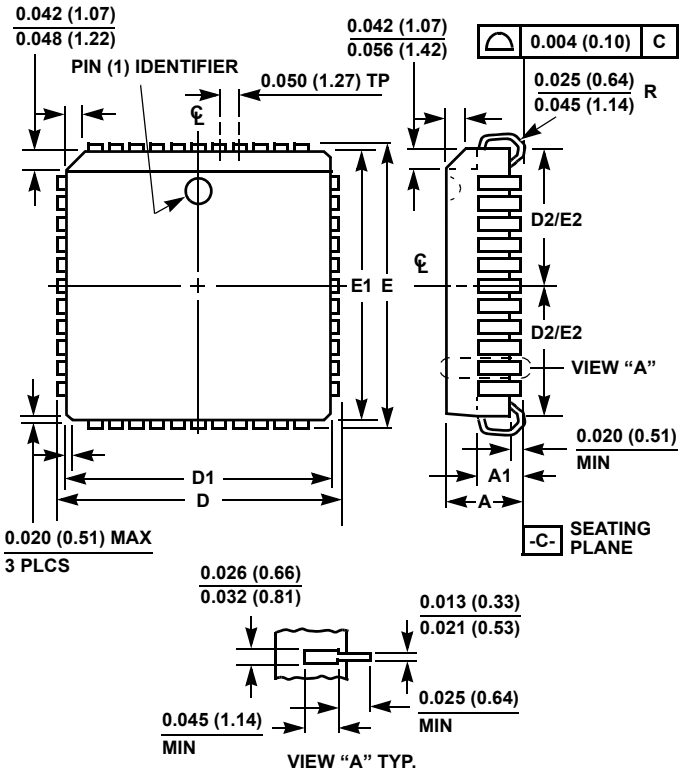
SYMBOL	MILLIMETERS			NOTES
	MIN	TYP	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.38	5, 8
D		7.00 BSC		-
D1		6.75 BSC		9
D2	4.55	4.70	4.85	7, 8
E		7.00 BSC		-
E1		6.75 BSC		9
E2	4.55	4.70	4.85	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		32		2
Nd		8		3
Ne		8		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 4 8/03

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Plastic Leaded Chip Carrier Packages (PLCC)



N28.45 (JEDEC MS-018AB ISSUE A)
28 LEAD PLASTIC LEADED CHIP CARRIER PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.165	0.180	4.20	4.57	-
A1	0.090	0.120	2.29	3.04	-
D	0.485	0.495	12.32	12.57	-
D1	0.450	0.456	11.43	11.58	3
D2	0.191	0.219	4.86	5.56	4, 5
E	0.485	0.495	12.32	12.57	-
E1	0.450	0.456	11.43	11.58	3
E2	0.191	0.219	4.86	5.56	4, 5
N	28		28		6

Rev. 2 11/97

NOTES:

1. Controlling dimension: INCH. Converted millimeter dimensions are not necessarily exact.
2. Dimensions and tolerancing per ANSI Y14.5M-1982.
3. Dimensions D1 and E1 do not include mold protrusions. Allowable mold protrusion is 0.010 inch (0.25mm) per side. Dimensions D1 and E1 include mold mismatch and are measured at the extreme material condition at the body parting line.
4. To be measured at seating plane -C- contact point.
5. Centerline to be determined where center leads exit plastic body.
6. "N" is the number of terminal positions.

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