LVDS Interface ICs

35bit LVDS Receiver 5:35 DeSerializer

BU8255KVT

●Description

LVDS Interface IC of ROHM "Serializer" "Deserializer" operate from 8MHz to 150MHz wide clock range, and number of bits range is from 35 to 70. Data is transmitted seven times (7X) stream and reduce cable number by 3(1/3) or less. The ROHM's LVDS has low swing mode to be able to expect further low EMI.

●Features

- ■Five channels of LVDS data stream are converted to 35bits data of parallel LVCMOS level outputs.
- ■30bits of RGB output data, 5bits of timing and control output data(HSYNC, VSYNC, DE, CTL1 and CTL2) are transmitted available.
- ■Support clock frequency from 8MHz up to 112MHz.
- ■Support consumer video format including 480i, 480P, 720P and 1080i as well.
- ■Support many kinds of PC video formats such as VGA, SVGA, XGA and SXGA.
- ■Provide 784Mbps per 1ch or 3.92Gbps per device throughput rate using 112MHz clock rate.
- ■User programmable LVCMOS data output triggering timing by using either rising or falling edge of clock.
- ■30bit LVDS transmitter is recommended to use BU8254KVT.

●Applications

Flat Panel Display

◇Precaution

- ・This chip is not designed to protect from radioactivity.
- ・The chip is made strictly for the specific application or equipment.
  Then it is necessary that the unit is measured as need.
- ・This document may be used as strategic technical data which subjects to COCOM regulations.

Status of this document

The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

Jun.2008

●Block Diagram

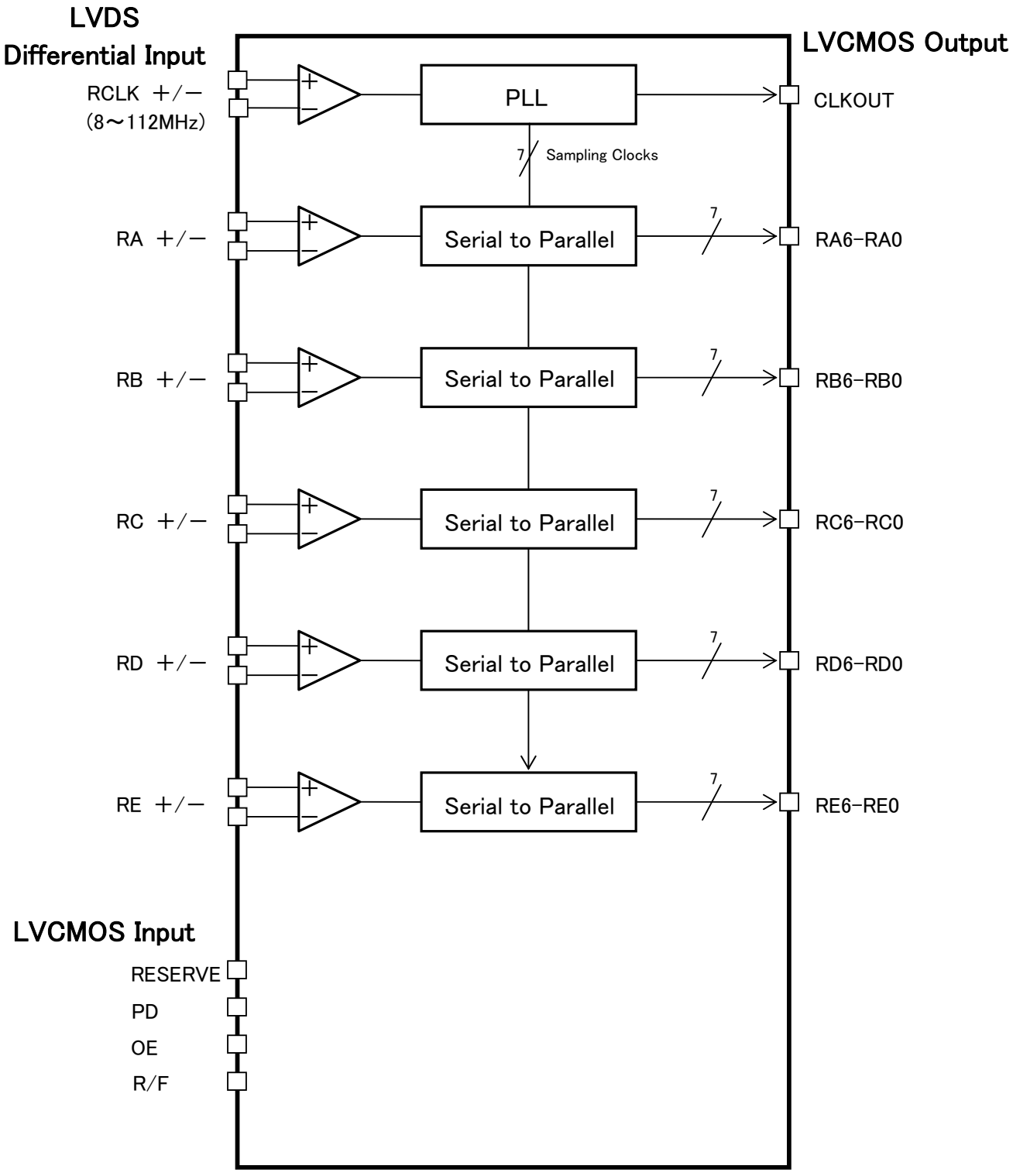


Figure-1 Block Diagram

●TQFP64V Package Specification

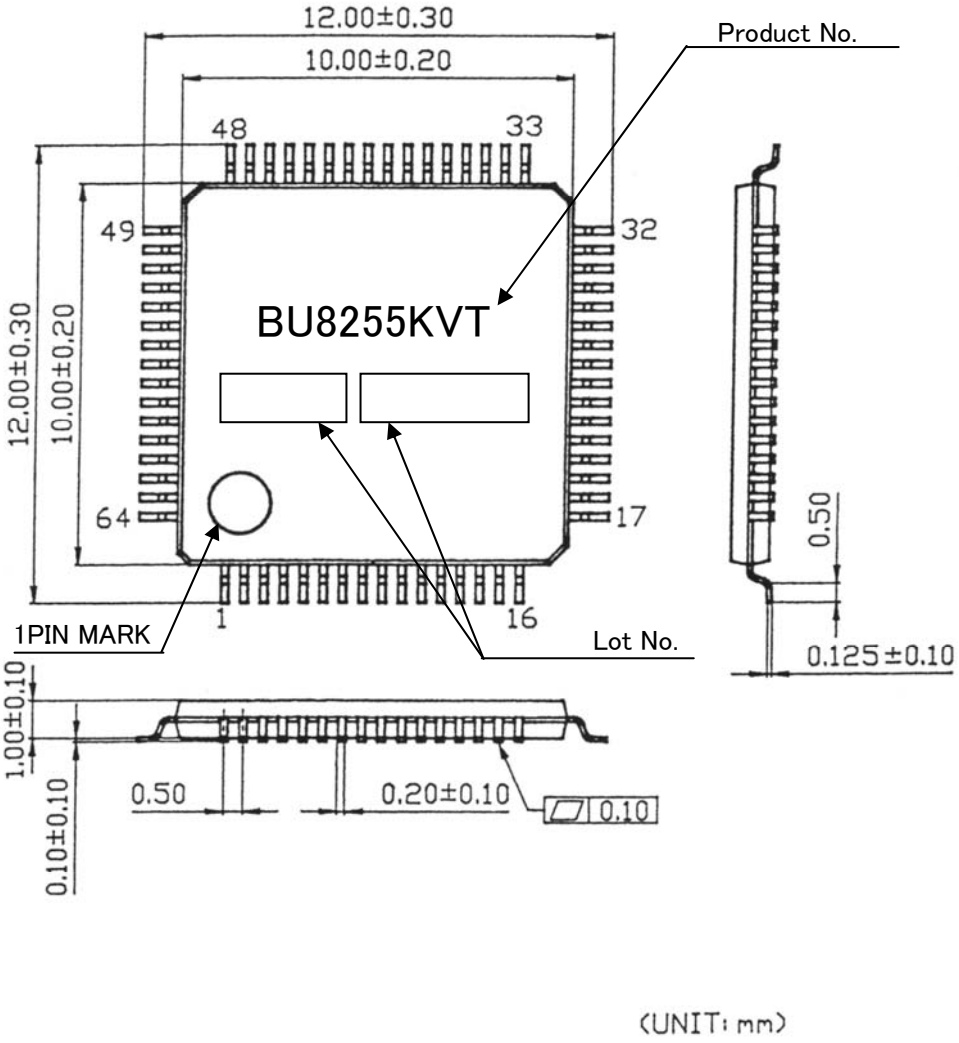


Figure-2　TQFP64V Package

●Pin Diagram

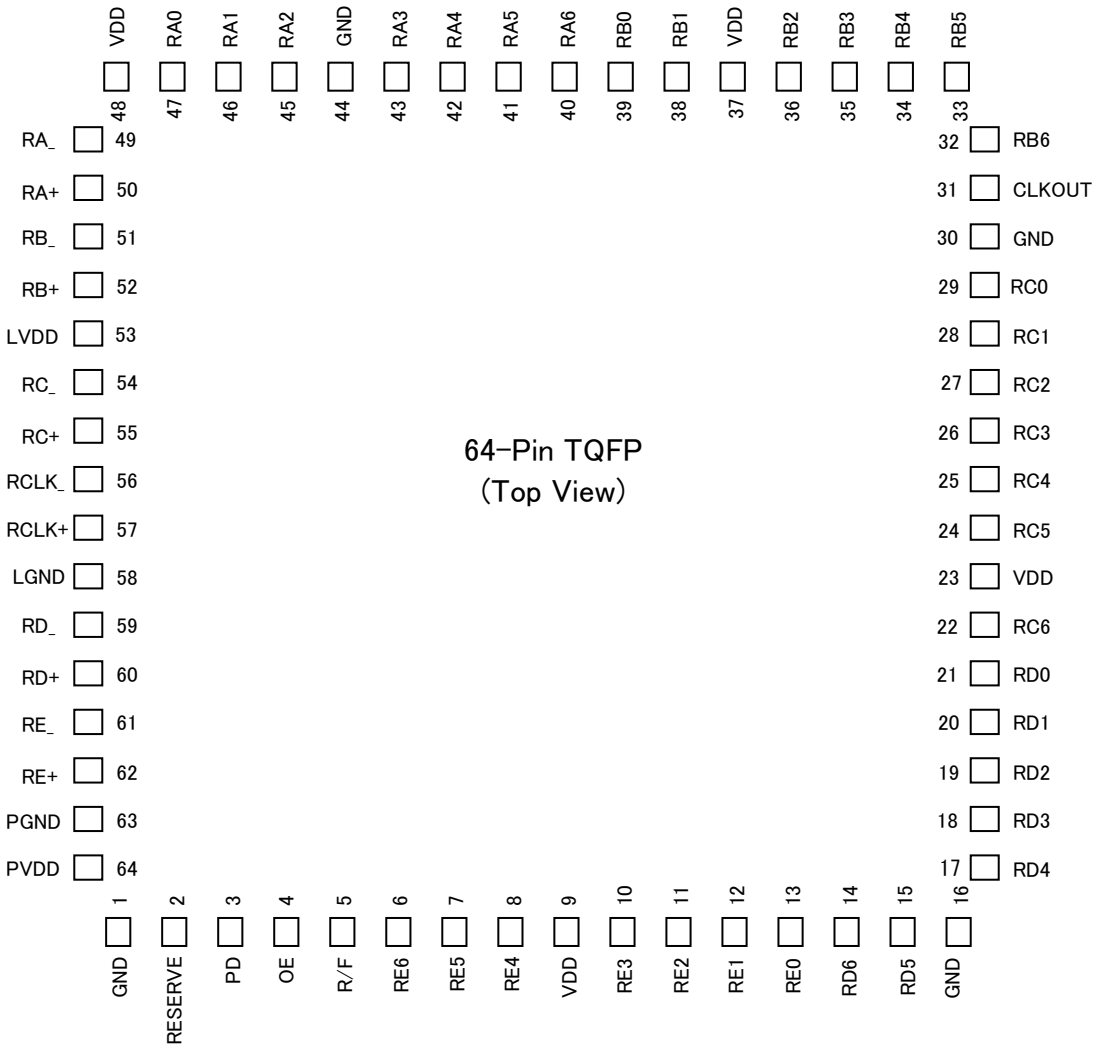


Figure-3　Pin diagram (Top view)

●Pin Description

Table .1: Pin description

Pin Name	Pin No.	I/O	Description
RA+, RA−	50,49	LVDS Input	LVDS data input + : Positive input of LVDS data differential pair. − : Negative input of LVDS data differential pair.
RB+, RB−	52,51	LVDS Input	
RC+, RC−	55,54	LVDS Input	
RD+, RD−	60,59	LVDS Input	
RE+, RE−	62,61	LVDS Input	
RCLK+, RCLK−	57,56	LVDS Input	LVDS clock input
RA6～RA0	40,41,42,43, 45,46,47	Output	LVCMOS data outputs.
RB6～RB0	32,33,34,35, 36,38,39	Output	
RC6～RC0	22,24,25,26, 27,28,29	Output	
RD6～RD0	14,15,17,18, 19,20,21	Output	
RE6～RE0	6,7,8,10,11,1 2,13	Output	
RESERVE	2	Input	Reserved input, must be “Low” for normal operation.
PD	3	Input	Power down input for the internal system. H: Normal operation. L: Power down (All output are “Low”).
OE	4	Input	Power down input for the data output driver. H: Output enable (Normal operation). L: Output disable(All outputs are “Hi-Z”).
R/F	5	Input	Select input pin for data output clock triggering edge. H: Output data is latched on rising edge. L: Output data is latched on falling edge.
VDD	9,23,37,48	Power	3.3V output driver and digital core power supply pin.
CLKOUT	31	Output	LVCMOS level clock output.
GND	1,16,30,44	Ground	GND pin for both data output driver cells and the digital cores.
LVDD	53	Power	Power supply pin for LVDS inputs.
LGND	58	Ground	Ground pin for LVDS inputs.
PVDD	64	Power	Power supply pin for PLL core.
PGND	63	Ground	Ground pin for PLL core.

●Function Description

Table .2: Function explanation list

PD	R/F	OE	Data output (Rxn) *1	Clock output
0	0	0	Hi-Z	Hi-Z
0	0	1	All fixed low	Fixed Low
0	1	0	Hi-Z	Hi-Z
0	1	1	All fixed low	Fixed Low
1	0	0	Hi-Z	Hi-Z
1	0	1	Data output	Output data is latched by falling edge of clock.
1	1	0	Hi-Z	Hi-Z
1	1	1	Data output	Output data is latched by rising edge of clock

*1 : Rxn

x = A,B,C,D,E

n = 0,1,2,3,4,5,6

●Electrical Characteristics

■Rating

Table .3: Absolute maximum rating

Item	Symbol	Value		Unit
		Min.	Max.	
Supply voltage	V_{DD}	−0.3	4.0	V
Input voltage	V_{IN}	−0.3	V_{DD}+0.3	V
Output voltage	V_{OUT}	−0.3	V_{DD}+0.3	V
Storage temperature range	Tstg	−55	125	℃

Table .4: Package power

Package	PD(mW)	DERATING(mW/℃) *1
TQFP64V	700	7.0
	1000*2	10.0*2

∗1 At temperature Ta > 25℃

∗2 Package power when mounting on the PCB board.

The size of PCB board :70 × 70 × 1.6 (mm^3)

The material of PCB board :The FR4 glass epoxy board.(3% or less copper foil area)

Table .5: Recommended operating conditions

Item	Symbol	Value			Unit	Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	3.0	3.3	3.6	V	VDD, LVDD, PVDD
Supply Noise Voltage	V_{NOZ}	−	−	0.1	V	
Operating temperature range	Topr	−20	−	85	℃	Clock frequency from 8MHz up to 90MHz
		0	−	70	℃	Clock frequency from 90MHz up to 112MHz

■DC Characteristics

Table .6: LVCMOS DC character (V_{DD}=3.0V～3.6V, Ta=−20℃～85℃)

Symbol	Item	Value			Unit	Condition
		Min.	Typ.	Max.		
V_{IH}	High Input voltage	V_{DD}×0.8	−	V_{DD}	V	
V_{IL}	Low Input voltage	0.0	−	V_{DD}×0.2	V	
V_{OH}	High Output voltage	V_{DD}−0.5	−	V_{DD}	V	I_{OH}=−4mA (data) I_{OH}=−8mA (clock)
V_{OL}	Low Output voltage	0.0	−	0.4	V	I_{OL}=4mA (data) I_{OL}=8mA (clock)
I_{INC}	Input current	−	−	±10	μA	0V≤V_{IN}≤V_{DD}

Table .7: LVDS Receiver DC character (V_{DD}=3.0V～3.6V, Ta=−20℃～85℃)

Symbol	Item	Value			Unit	Condition
		Min.	Typ.	Max.		
V_{TH}	Differential input High threshold	−	−	100	mV	V_{OC}*1=1.2V
V_{TL}	Differential input Low threshold	−100	−	−	mV	V_{OC}*1=1.2V
I_{INL}	Input current	−	−	±25	μA	V_{IN}=2.4V / 0V V_{DD}=3.6V

*1Common Mode Voltage

■Supply Current

Table .8: Supply current

Symbol	Item	Value		Unit	Condition	
		Min.	Max.			
I_{RCCG}	Receiver supply current (Gray Scale Pattern)	52	–	mA	fCLKOUT=90MHz	C_L=8pF, V_{DD}=3.3V
I_{RCCW}	Receiver supply current (Worst Case Pattern)	95	–	mA	fCLKOUT=90MHz	C_L=8pF, V_{DD}=3.3V
I_{RCCS}	Receiver power down supply current	–	10	μA	PD=L, OE=L	

Gray Scale Pattern

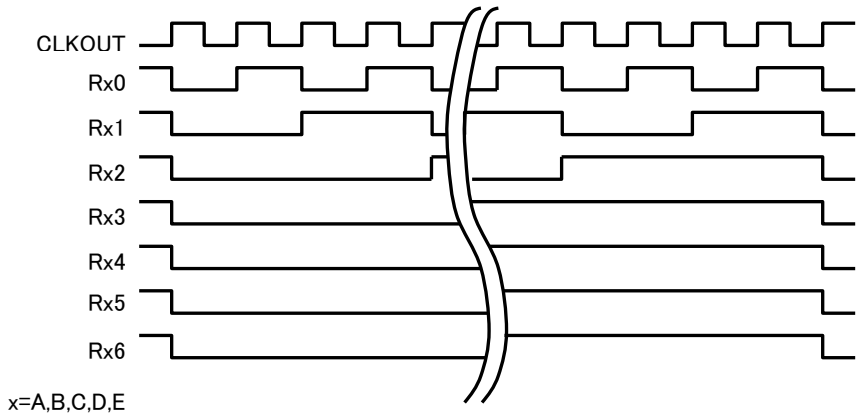


Figure-4 Gray Scale Pattern

Worst Case Pattern (Maximum power condition)

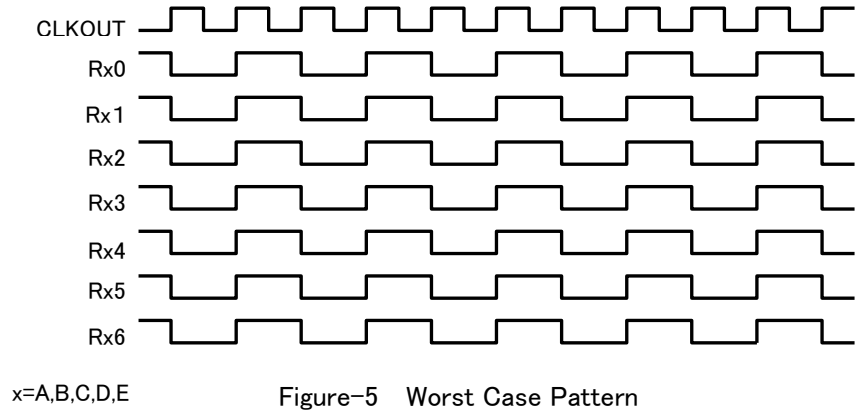


Figure-5 Worst Case Pattern

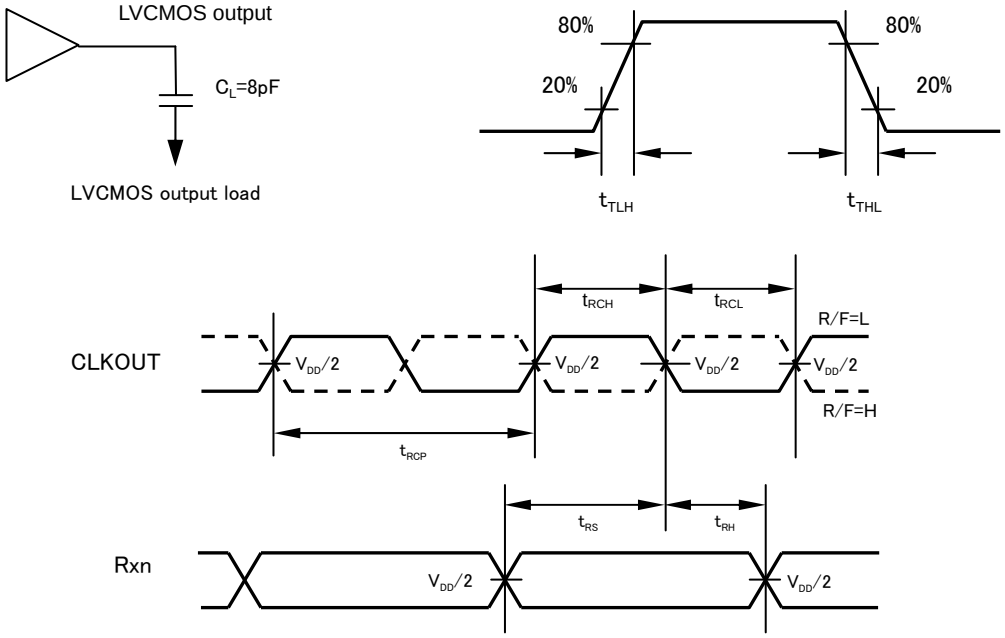
■AC Characteristics

Table .9 : Switching characteristics

Symbol	Item	Value			Unit
		Min.	Typ.	Max.	
t_{RCP}	CLKOUT period	8.93	–	125	ns
t_{RCH}	CLKOUT "H" time	–	$0.5t_{RCP}-1.0$	–	ns
t_{RCL}	CLKOUT "L" time	–	$0.5t_{RCP}-1.0$	–	ns
t_{RS}	LVCMOS data setup to CLKOUT	$0.5t_{RCP}-1.4$	–	–	ns
t_{RH}	LVCMOS data hold from CLKOUT	$0.23t_{RCP}-1.0$	–	–	ns
t_{TLH}	LVCMOS data rise time	–	1.0	2.0	ns
t_{THL}	LVCMOS data fall time	–	1.0	2.0	ns
t_{RIP1}	Input data position0	−0.25	0.0	+0.25	ns
t_{RIP0}	Input data position1	$\frac{t_{RCIP}}{7}-0.25$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7}+0.25$	ns
t_{RIP6}	Input data position2	$2\frac{t_{RCIP}}{7}-0.25$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7}+0.25$	ns
t_{RIP5}	Input data position3	$3\frac{t_{RCIP}}{7}-0.25$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7}+0.25$	ns
t_{RIP4}	Input data position4	$4\frac{t_{RCIP}}{7}-0.25$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7}+0.25$	ns
t_{RIP3}	Input data position5	$5\frac{t_{RCIP}}{7}-0.25$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7}+0.25$	ns
t_{RIP2}	Input data position6	$6\frac{t_{RCIP}}{7}-0.25$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7}+0.25$	ns
t_{RPLL}	Phase Locked Loop set time	–	–	10.0	ms
t_{RCIP}	Clock input period	8.93	–	125	ns

●AC Timing Diagrams

■LVCMOS



x=A,B,C,D,E
n=0,1,2,3,4,5,6

Figure-6　LVCMOS output timing

■Phase-Locked Loop set time

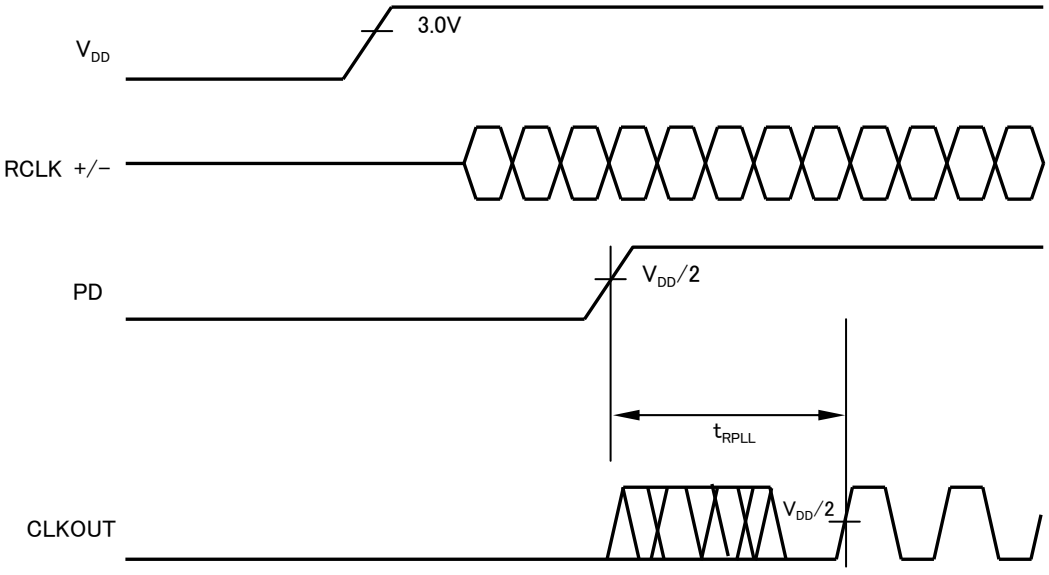
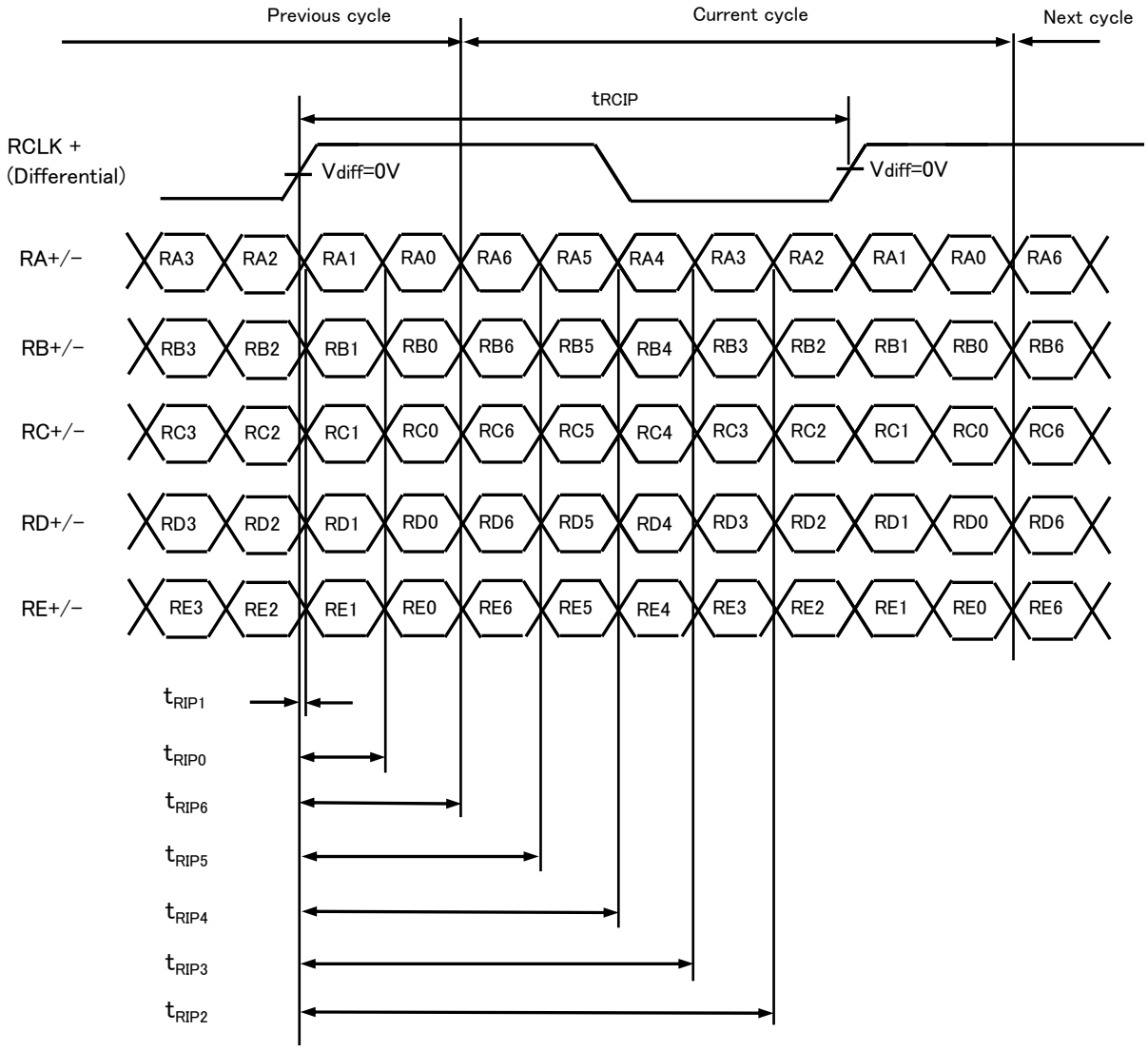


Figure-7　Phase-Locked Loop set time

●LVDS　Data, Clock Input Timing



Figure−8　LVDS data and clock input timing

●LVDS Data, Clock Input and LVSMOS Output Timing

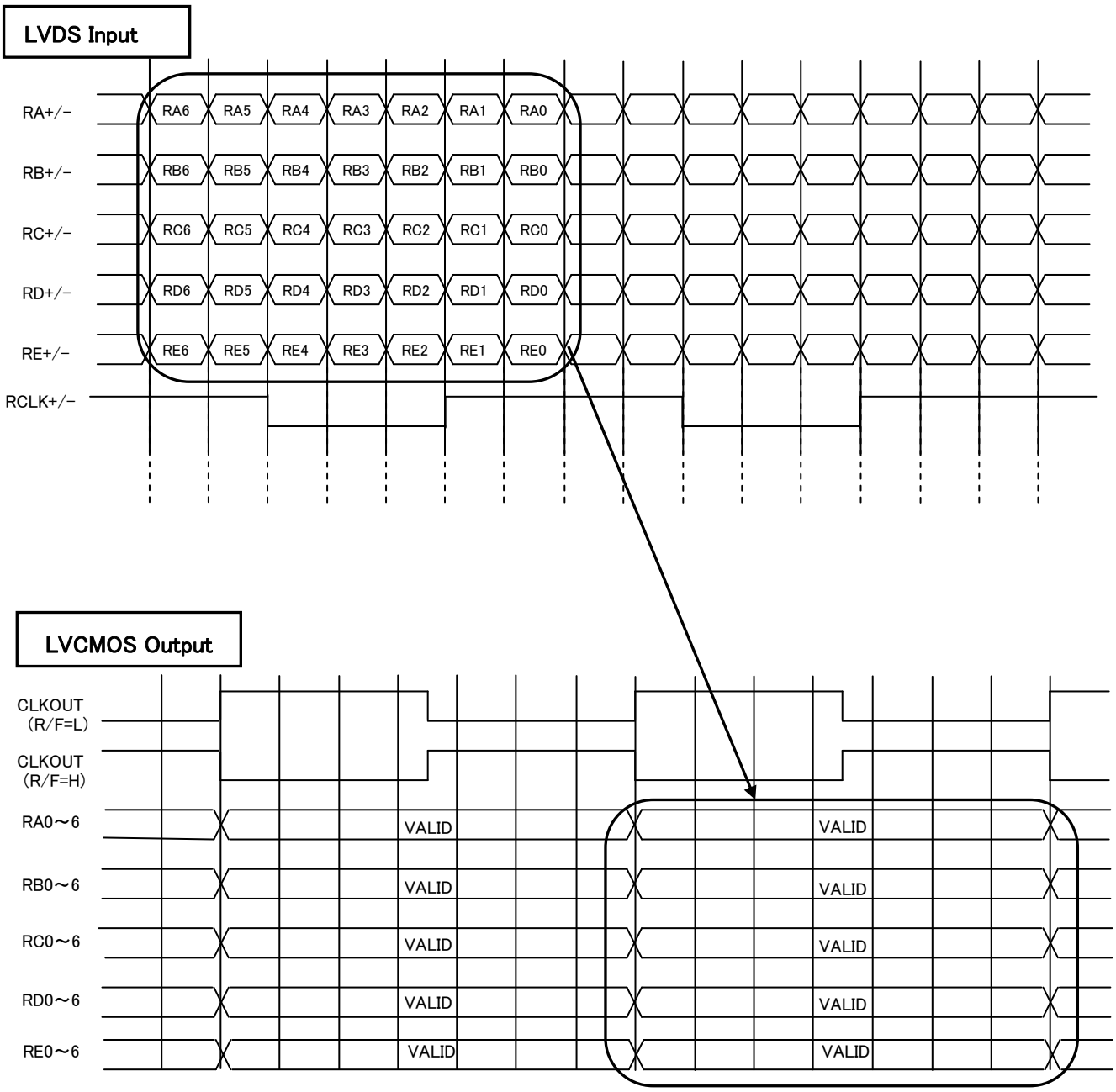


Figure-9　LVDS Data, Clock Input and LVCMOS Output Timing

●About the Power On Reset

Power on reset is not mandatory for this device.
(The PD pin should be set to high level when power on reset procedure is not used.)

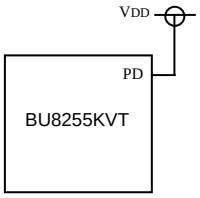


Figure-10　Terminal connection when power on reset is not used.

However, Power on reset procedure is strongly recommend for internal logic initialization by following two methods.

① The method of using CR circuit.
② The method of using external specific IC.

It is recommend to do enough examination for target application.

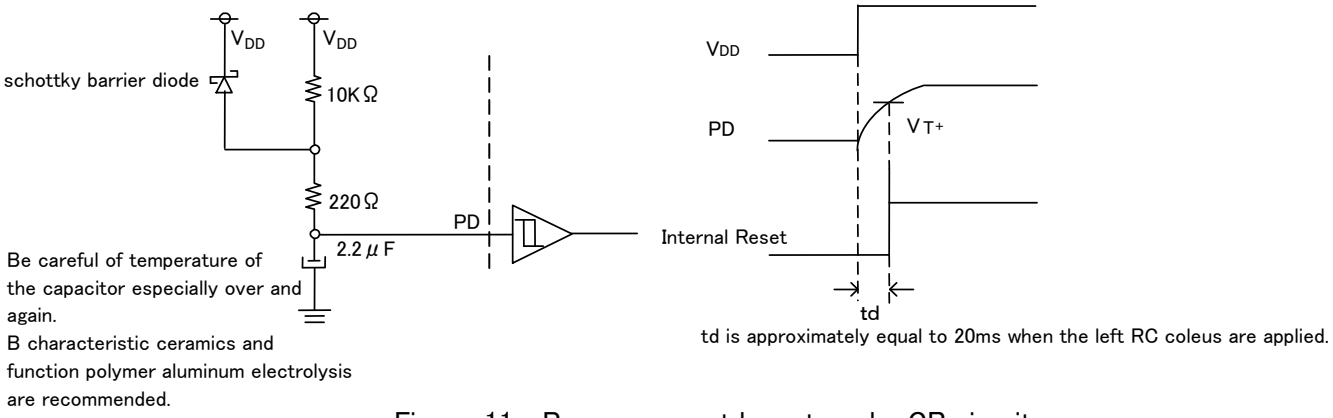


Figure-11　Power on reset by external a CR circuit

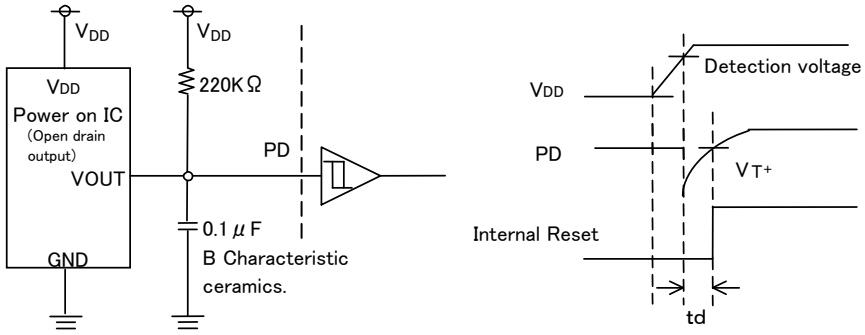
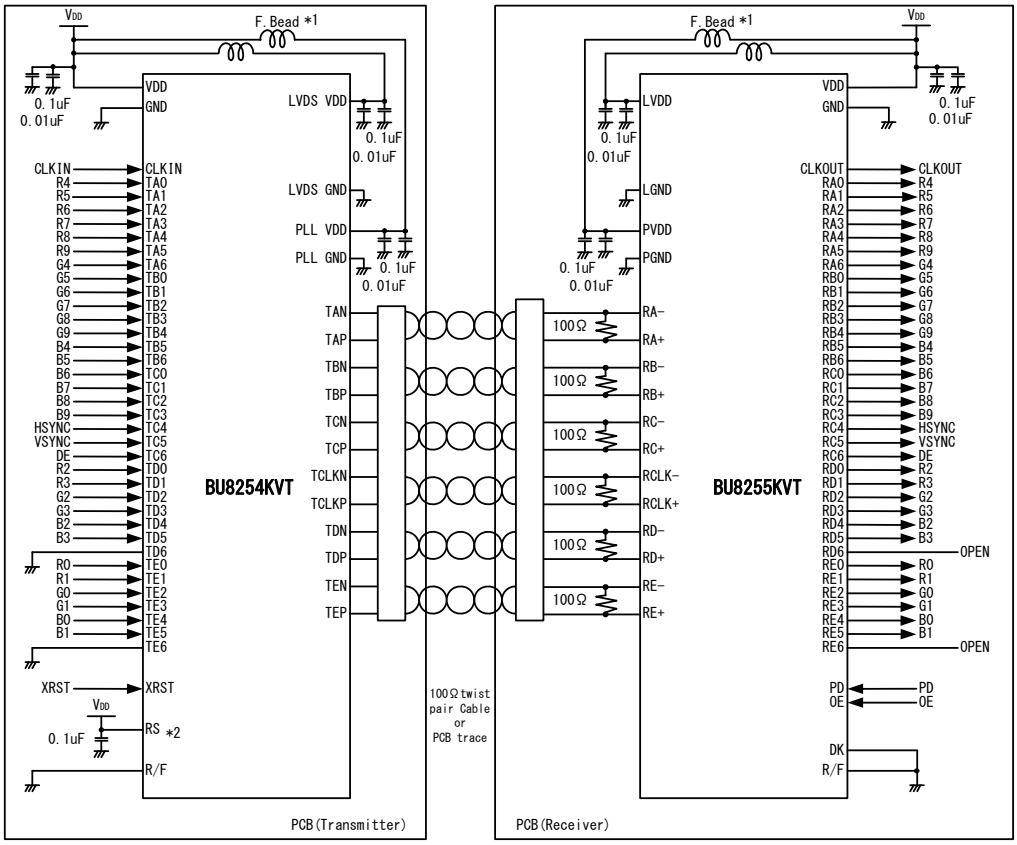


Figure-12　Power on reset by specific IC

●10 LVDS Level Input & Output

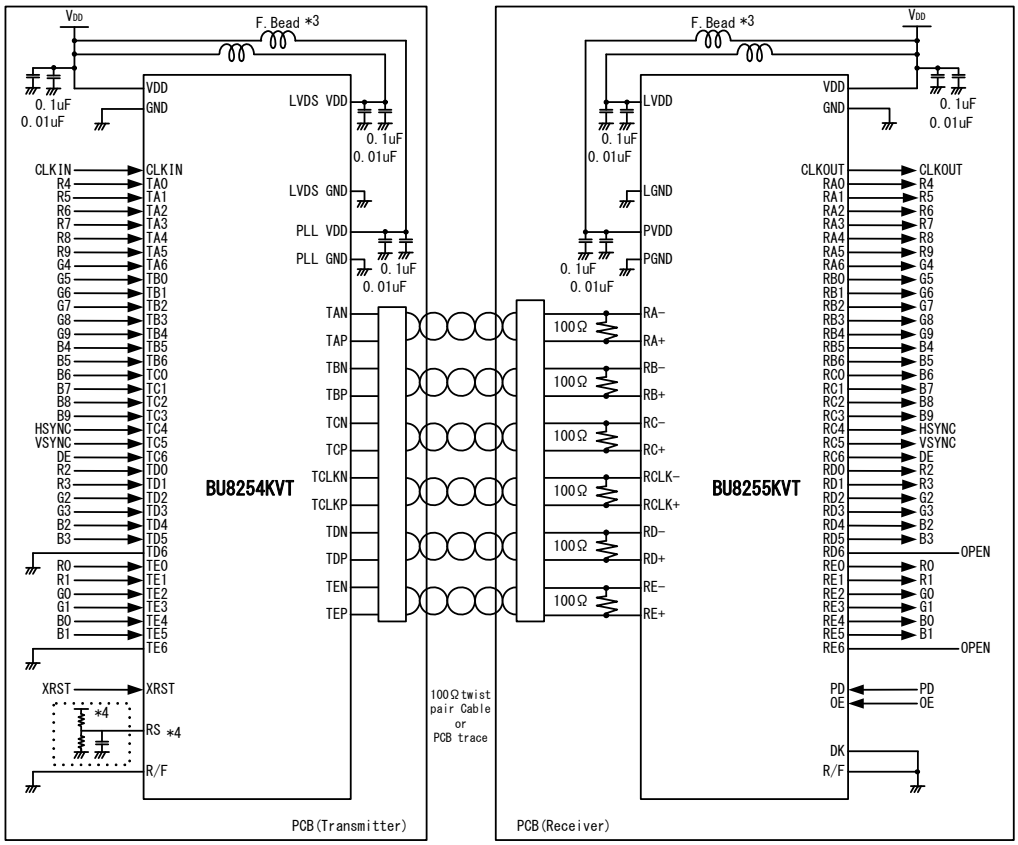
Example:
BU8254KVT : LVCMOS level input/Falling edge/LVDS normal(350mV) swing output
BU8255KVT : LVCMOS level output/Falling edge



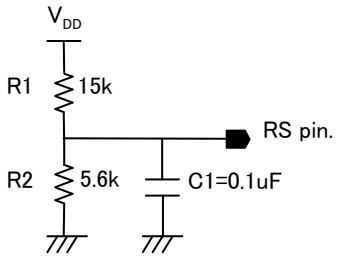
＊1 Recommended Parts:
F.Bead : BLM18A-Series (Murata Manufacturing Co.)
＊2 :If RS pin is tied to V_{DD},LVDS swing is 350m V.
If RS pin is tied to GND,LVDS swing is 200m V.

●10bit Small Swing Input & LVCMOS Level Output

Example:
BU8254KVT : LVCMOS level input/Falling edge/LVDS normal(350mV) swing output
BU8255KVT : LVCMOS level output/Falling edge



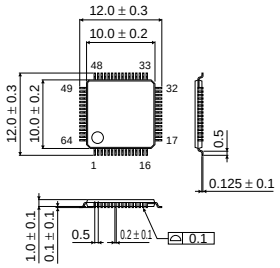
＊3 Recommended Parts:
F.Bead : BLM18A-Series (Murata Manufacturing Co.)
＊4 :RS pin acts as VREF input pin when input voltage is set to half of high level signal input.
We recommend to locate by-pass condenser near the RS pin.



Example for LVTTL(1.8V input):(R1,R2)=(15kΩ,5.6kΩ)

TQFP64V

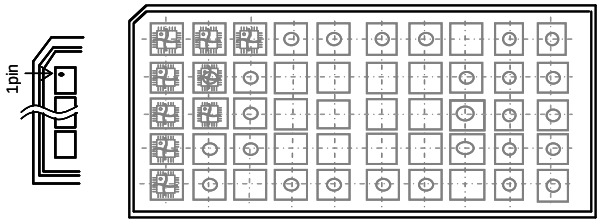
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(Unit:mm)

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Container	Tray(with dry pack)
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray.



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Denmark	TEL: +45-3694-4739	FAX: +45-3694-4789	**Hong Kong**	TEL: +852-2-740-6262	FAX: +852-2-375-8971
Barcelona	TEL: +34-9375-24320	FAX: +34-9375-24410	**Taipei**	TEL: +886-2-2500-6956	FAX: +886-2-2503-2869
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Poland	TEL: +48-22-5757213	FAX: +48-22-5757001	**Singapore**	TEL: +65-6332-2322	FAX: +65-6332-5662
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