Structure Silicon monolithic integrated circuit

Product Name PCM CODEC IC

Product No. **BU8925MUV**

Physical dimentions Figure1 (VQFN032V5050)

Features
- 16bit Linear ・μ/A-Law codec
- Built-in PLL circuit for system clock generation
- Support for below frequency about PCM data transmission clock.
  - μ/A-Law 64kHz - 2048 kHz
  - Linear 128 kHz - 2048 kHz
- Built-in Output amplifier for line drives (600Ω)
- Power down control using NRST pin

○ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Digital supply voltage	DVDD	−0.3～4.5	V
Analog supply voltage	AVDD	−0.3～4.5	V
Input voltage for digital terminal	V_{TD}	DVSS−0.3～4.5	V
Input voltage for analog terminal	V_{TA}	AVSS−0.3～AVDD+0.3	V
Input current	I_{IN}	−10～+10	mA
Power dissipation *1	P_d	300	mW
Storage temperature range	T_{stg}	−55～125	℃

(*1) Note: Reduce to 3 mW/℃ when Ta = 25℃ or above

○ Recommended Operating Power Supply Voltage and temperature Range

Parameter	Symbol	Rating			Unit
		Min	Typ	Max	
Digital supply voltage	DVDD	1.65	1.80	1.95	V
Analog supply voltage	AVDD	2.700	2.800	3.465	V
Operating temperature range	T_{opr}	−30	-	85	℃

This product is not designed to protect itself against radioactive rays.

Status of this document

The Japanese version of this document is the formal specification. A customer may use this translation version only for a reference to help reading the formal version. If there are any differences in translation version of this document, formal version takes priority.

○ Electrical Characteristics

Unless otherwise noted, Ta = 25℃, AVDD=2.8, DVDD=1.8V, FSYNC=8kHz, DCLK=256kHz.

Parameter	Symbol	Specified Value			Unit	Condition
		Min	Typ	Max		
Current consumption						
Standby current consumption	IDD1	-	0.1	3.0	uA	NRST=DVSS and FSYNC,DCLK=DVSS
Full Operation	IDD2	-	2.5	3.8	mA	NRST,BST=DVDD and No input signal
DC Characteristics						
Digital H level input voltage	VIH	DVDDx0.75	-	4.5	V	
Digital L level input voltage	VIL	-0.3	-	DVDDx0.25	V	
Digital H level input current	IIH	-	-	1	uA	VIH=DVDD
Digital L level input current	IIL	-	-	-1	uA	VIL=DVSS
Digital H level output voltage	VOH	DVDDx0.8	-	DVDD	V	IOH= -1mA
Digital L level output voltage	VOL	0	-	DVDDx0.2	V	IOL= 1mA

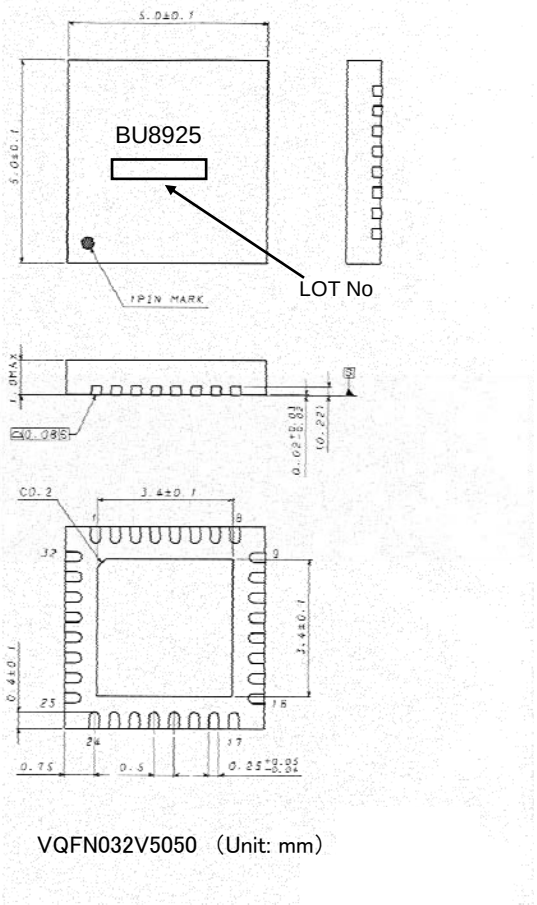
Unless otherwise noted, Ta=25°C, AVDD=2.8V, DVDD＝1.8V, FSYNC=8kHz, DCLK=256kHz and linear mode.

Parameter	symbol	Condition		Specified Value			Unit
				Min	Typ	Max	
Transmit signal-to-distortion ratio (AUX1IN→PCMOUT)	S_{DT}	1020Hz ＊2, ＊3	0dBm0	45	-	-	dB
			-30dBm0	35	-	-	
			-40dBm0	29	-	-	
			-45dBm0	24	-	-	
Receive signal-to-distortion ratio (PCMIN→AUDOUT)	S_{DR}	1020Hz ＊2	0dBm0	45	-	-	dB
			-30dBm0	35	-	-	
			-40dBm0	29	-	-	
			-45dBm0	24	-	-	
Transmit Gain Tracking (AUX1IN→PCMOUT)	G_{TX}	1020Hz, Reference level=-10dBm0 ＊3	+3.0～0.5dBm0	-3.0	-	3.0	dB
			+0.5～-40dBm0	-1.0	-	1.0	
			-40～-50dBm0	-2.0	-	2.0	
			-50～-55dBm0	-2.0	-	2.0	
Receive Gain Tracking (PCMIN→AUDOUT)	G_{RX}	1020Hz, Reference level=-10dBm0	+3.0～-40dBm0	-1.0	-	1.0	dB
			-40～-50dBm0	-2.0	-	2.0	
			-50～-55dBm0	-2.0	-	2.0	
Transmit reference level	V_{ITX1}	1020Hz, 0dBm0	AUX1IN→PCMOUT	0.375	0.500	0.667	Vrms
Receive reference level	V_{ORX}	1020Hz, 0dBm0	PCMIN→AUDOUT	0.400	0.475	0.564	Vrms
Transmit Gain Loss relative to Frequency (AUX1IN→PCMOUT)	G_{RTX}	1020Hz	0.06kHz	24	-	-	dB
			0.2kHz	0	-	2.5	
			0.3～0.4kHz	-0.3	-	0.5	
			0.4～3.0kHz	-0.3	-	0.3	
			3.4kHz	-0.3	-	0.9	
			3.6kHz	0	-	-	
			3.78kHz	6.5	-	-	
Receive Gain Loss relative to Frequency (PCMIN→AUDOUT)	G_{RRX}	1020Hz	0.06kHz	24	-	-	dB
			0.2kHz	0	-	2.5	
			0.3～2.8kHz	-0.3	-	0.3	
			2.8～3.0kHz	-0.3	-	0.5	
			3.4kHz	-0.3	-	0.9	
			3.6kHz	0	-	-	
			3.78kHz	6.5	-	-	
Transmit noise level	V_{NTX}	AUX1IN= AGND level. ＊2		-	-	-76	dBV
Receive noise level	V_{NRX}	PCMIN="L", Using A-Weight filter.		-	-	-85	dBV

＊2 Using C-MESSAGE filter

＊3 Specified that 0dBm0 is 0.5Vrms.

○ Physical dimentions (Figure1)



VQFN032V5050 （Unit: mm）

○Pin assignment

Pin No	Pin name	Pin No	Pin name
1	NC	17	AUX1IN
2	DVSS	18	AVSS
3	DVDD	19	AVDD
4	BST	20	AUDOUT
5	NRST	21	AVDD
6	DSEL	22	AVSS
7	FRM2	23	BGFLT
8	TEST	24	NC
9	FRM1	25	AGND
10	NC	26	VREF
11	NC	27	PLLCAP
12	NC	28	PCMSEL
13	NC	29	FSYNC
14	NC	30	DCLK
15	NC	31	PCMIN
16	NC	32	PCMOUT

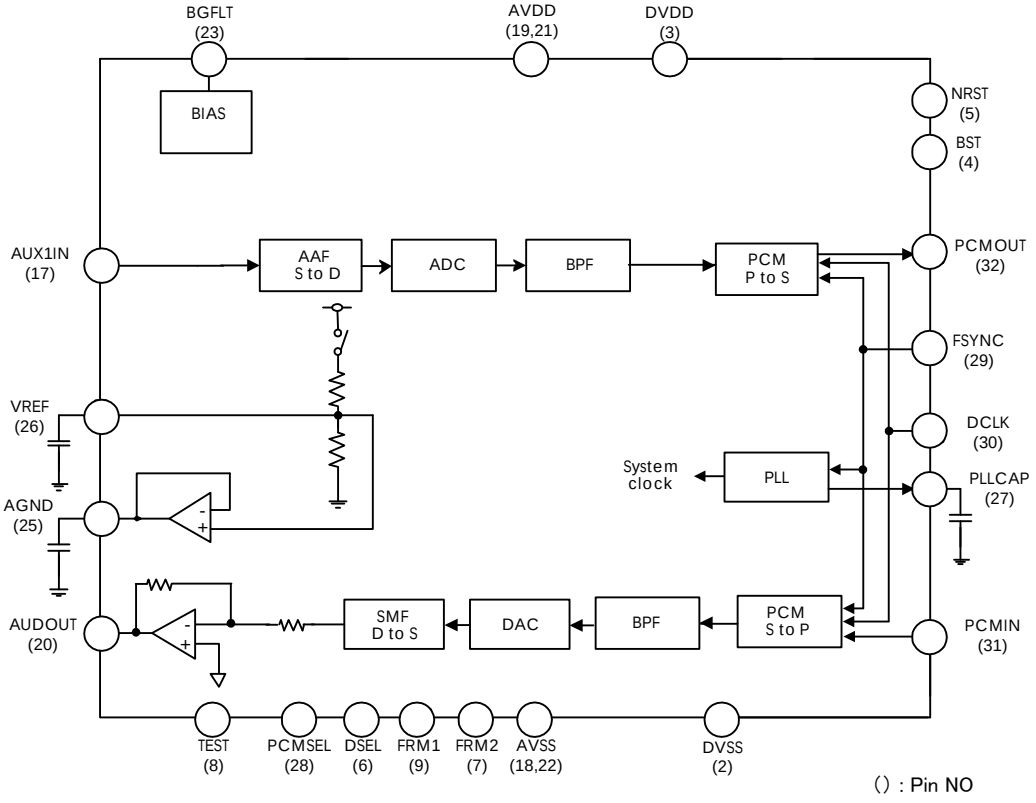
Power down control using only NRST pin.

NRST = L : Power down mode

NRST = H : Active mode

NC : This pin is not connected with internal.

○ Block diagram (Figure2)



() : Pin NO

○ Cautions on use

(1) Absolute Maximum Ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions

These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector

The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line

Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines.In this regard, for the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.

Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage

Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting

In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field

Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB

On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9)Input terminals

In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern

If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor

In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) Others

In case of use this LSI, please peruse some other detail documents, we called ,Technical note, Functinal description, Application note.

Notes

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