Dear customer

ROHM Co., Ltd. ("ROHM"), on the 1st day of April, 2024,
has absorbed into merger with 100%-owned subsidiary of LAPIS Technology Co., Ltd.

Therefore, all references to "LAPIS Technology Co., Ltd.", "LAPIS Technology"
and/or "LAPIS" in this document shall be replaced with "ROHM Co., Ltd."
Furthermore, there are no changes to the documents relating to our products other than
the company name, the company trademark, logo, etc.

Thank you for your understanding.

ROHM Co., Ltd.
April 1, 2024

Dear customer

LAPIS Semiconductor Co., Ltd. ("LAPIS Semiconductor"), on the 1st day of October, 2020, implemented the incorporation-type company split (shinsetsu-bunkatsu) in which LAPIS established a new company, LAPIS Technology Co., Ltd. (“LAPIS Technology”) and LAPIS Technology succeeded LAPIS Semiconductor’s LSI business.

Therefore, all references to "LAPIS Semiconductor Co., Ltd.", "LAPIS Semiconductor" and/or "LAPIS" in this document shall be replaced with "LAPIS Technology Co., Ltd."

Furthermore, there are no changes to the documents relating to our products other than the company name, the company trademark, logo, etc.

Thank you for your understanding.

LAPIS Technology Co., Ltd.
October 1, 2020

ROHM GROUP
LAPIS SEMICONDUCTOR

FEDL620Q150A-01
Issue Date: May 7, 2015

ML620Q151A/2A/3A/4A/5A/6A/7A/8A/9A

16-bit micro controller

GENERAL DESCRIPTION

This LSI is a high-performance 16-bit CMOS microcontroller into which rich peripheral circuits, such as 10-bit A/D converter, timer, PWM, synchronous serial port, UART, I2C bus interface (master), Low level detect circuit, are incorporated around 16-bit CPU nX-U16/100.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel procesing. and, this LSI has a data flash-memory fill area by a software which can be written in. In addition, it has an on-chip debugging function, which allows software debugging/rewriting with the LSI mounted on the board.

FEATURES

- CPU
  - 16-bit RISC CPU (CPU name: nX-U16/100)
  - Instruction system:16-bit instructions
  - Instruction set:Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - On-Chip debug function
  - Minimum instruction execution time
    Approx 30.5 μs (at 32.768kHz system clock)
    Approx 0.122 μs (at 8.192MHz system clock)

- Internal memory
  - Flash-memory

Product	Program area	Rewrite cycle
ML620Q151A/ML620Q154A/ML620Q157A	32-Kbyte* (16K × 16-bit)	100
ML620Q152A/ML620Q155A/ML620Q158A	48-Kbyte* (24K × 16-bit)	
ML620Q153A/ML620Q156A/ML620Q159A	64-Kbyte* (32K × 16-bit)	

  * including unusable 1KByte TEST area
    Internal 2-Kbyte Data Flash (1-Kbyte × 2) Rewrite cycle: 10,000 times
  - SRAM: Internal 2-Kbyte RAM (2-Kbyte × 8 -bits)

- Interrupt controller
  - 2 non-maskable interrupt sources (Internal source: BACK-UP CLOCK, WDT)
  - maskable interrupt

Product	Interrupt source
ML620Q151A/ML620Q154A/ML620Q157A	27 (Internal source: 20, External source: 7)
ML620Q152A/ML620Q155A/ML620Q158A	28 (Internal source: 20, External source: 8)
ML620Q153A/ML620Q156A/ML620Q159A	28 (Internal source: 20, External source: 8)

  - 4 steps of interrupt level, and a mask function

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- Time base counter

– Low-speed time base counter × 1 channel

- Watchdog timer
  – Generates a non-maskable interrupt upon the first overflow and a system reset occurs upon the second
  – Free running
  – Overflow period: 4 types selectable (125ms, 500ms, 2s, 8s @32.768kHz)

- Timers
  – 8 bits × 2ch (16-bits configuration available × 1ch)
  – 16 bits × 4ch

- PWM
  – 16bits × 4ch
  – The auto reload timer mode / PWM mode
  – Timer start-stop function by the software and an external trigger.
  – A pulse width can be measured using an external-trigger input.
  – An external event can be selected as the counter clock.
  – Complement synchronous PWM

- Synchronous serial port
  – 1ch
  – Master/slave selectable
  – LSB first/MSB first selectable
  – 8-bit length/16-bit length selectable

- UART
  – Full-duplex × 1ch (Half-duplex × 2ch)
  – Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  – Positive logic/negative logic selectable
  – Built-in baud rate generator

- I^2C bus interface
  – Master function only
  – Fast mode (400kbit/s), Standard mode (100kbit/s)

- Successive approximation type A/D converter
  – 10-bit A/D converter
  – Input: 12ch（Maximum）
  – Conversion time: 43us, 13.5μs per channel (conversion-time is selectable)

- Analog Comparator
  – 1ch
  – Edge for the interrupt and sampling function is selectable.

- General-purpose ports (including secondary functions)
  - Input-only ports

Product	Input-only ports (including multiple functions)	
	When not using the crystal resonator	When using the crystal resonator
ML620Q151A/ML620Q152A/ML620Q153A	6ch	5ch
ML620Q154A/ML620Q155A/ML620Q156A	7ch	6ch
ML620Q157A/ML620Q158A/ML620Q159A	7ch	6ch

  - Output-only ports : 4ch
  - Input/output ports

Product	Input/output ports (including multiple functions)	
	When not using the crystal resonator	When using the crystal resonator
ML620Q151A/ML620Q152A/ML620Q153A	31ch	30ch
ML620Q154A/ML620Q155A/ML620Q156A	34ch	33ch
ML620Q157A/ML620Q158A/ML620Q159A	46ch	45ch

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset by the watchdog timer (WDT) overflow
  - Reset by the Low Level Detector (LLD)

- Low Level detect function
  - Threshold voltages: 4values (1.9V/2.55V/3.7V/4.2V)
    A threshold voltage is selected as Code-Option.
  - LLD is a ready as a supply-voltage supervisory reset.
    Reset or an interrupt output is selectable as Code-Option.

- Clock
  - Low-speed clock (This LSI can not guarantee the operation without low-speed clock)
    Crystal oscillation (32.768 kHz) or Built-in RC oscillation (32.768kHz)
    Crystal oscillation or Built-in RC oscillation is selectable as Code-Option.
  - High-speed clock
    Built-in RC oscillation (2.097MHz) or Built-in PLL oscillation (8.192MHz)

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block control function: Operation of an intact functional block circuit is powerd down. (register reset and clock stop)

- Package

Product	Package
ML620Q151A/ML620Q152A/ML620Q153A	48pinTQFP (P-TQFP48-0707-0.50-QK)
ML620Q154A/ML620Q155A/ML620Q156A	52pinTQFP (P-TQFP52-1010-0.65-TK)
ML620Q157A/ML620Q158A/ML620Q159A	64pinQFP (P-QFP64-1414-0.80-UK)

- Guaranteed operating range
  - Operating temperature: –40°C to +105°C
  - Operating voltage: V_{DD} = 1.8V to 5.5V

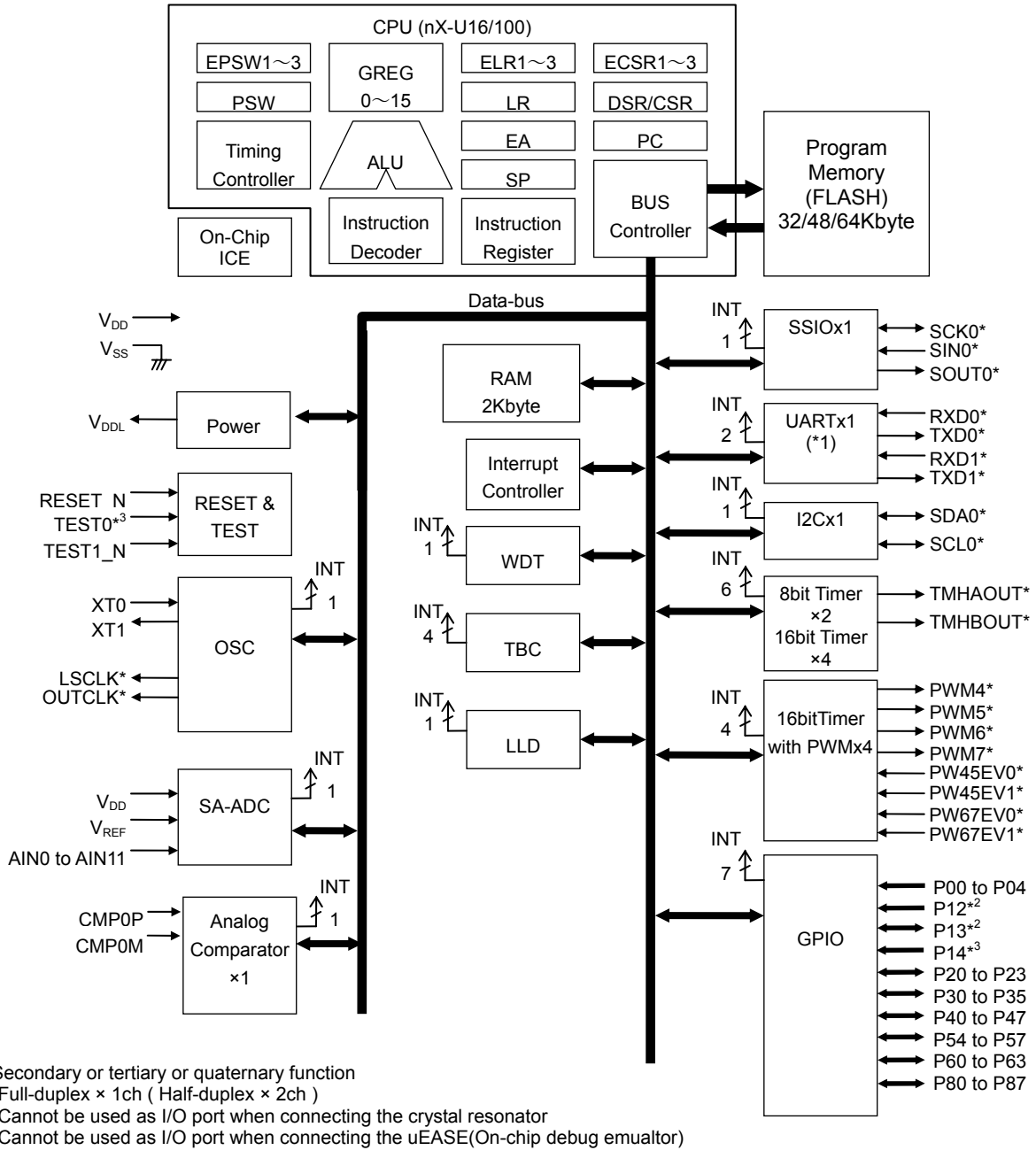
The difference point of this LSI is shown below.

function		ML620Q151A/152A/153A	ML620Q154A/155A/156A	ML620Q157A/158A/159A
Shipment		48pinTQFP	52pinTQFP	64pinQFP
flash capacity (program area)		32Kbyte(ML620Q151A) 48Kbyte(ML620Q152A) 52Kbyte(ML620Q153A)	32Kbyte(ML620Q154A) 48Kbyte(ML620Q155A) 52Kbyte(ML620Q156A)	32Kbyte(ML620Q157A) 48Kbyte(ML620Q158A) 52Kbyte(ML620Q159A)
maskable interrupt		27	28	28
Input-only port (At the case of crystal unused)		6	7	7
	P05 port	–	Available	Available
Input/output port (At the case of crystal unused)		31	34	46
	P36,P53,P64 ports	–	Available	Available
	P37 port	–	–	Available
	P50～P52 ports	–	–	Available
	P65～P67 ports	–	–	Available
	P70～P74 ports	–	–	Available

—:none

BLOCK DIAGRAM

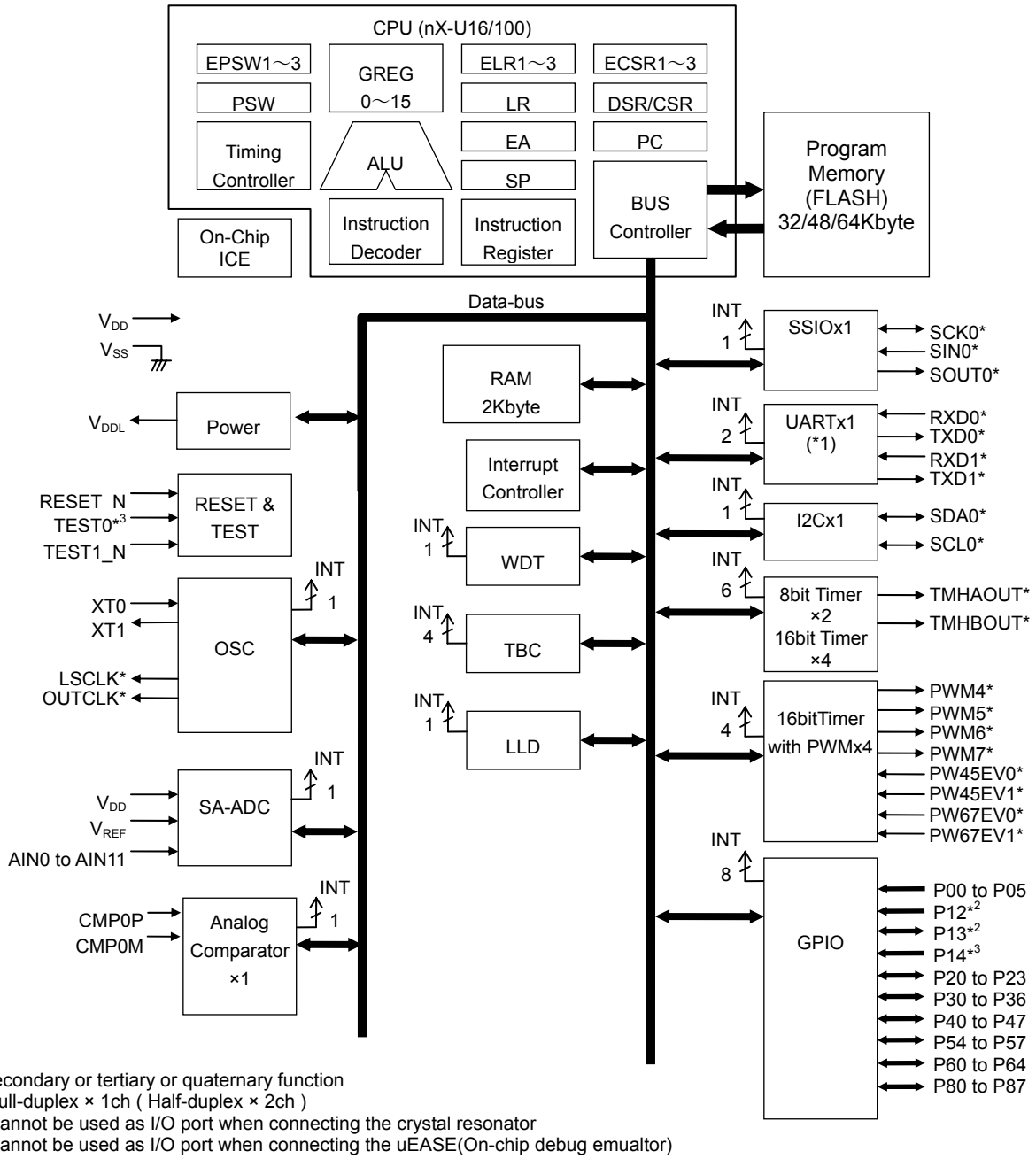
Block Diagram of ML620Q151A/ML620Q152A/ML620Q153A(TQFP48)



* Secondary or tertiary or quaternary function
*1 Full-duplex × 1ch (Half-duplex × 2ch)
*2 Cannot be used as I/O port when connecting the crystal resonator
*3 Cannot be used as I/O port when connecting the uEASE(On-chip debug emualtor)

Figure 1-1 Block Diagram of ML620Q151A/ML620Q152A/ML620Q153A(TQFP48)

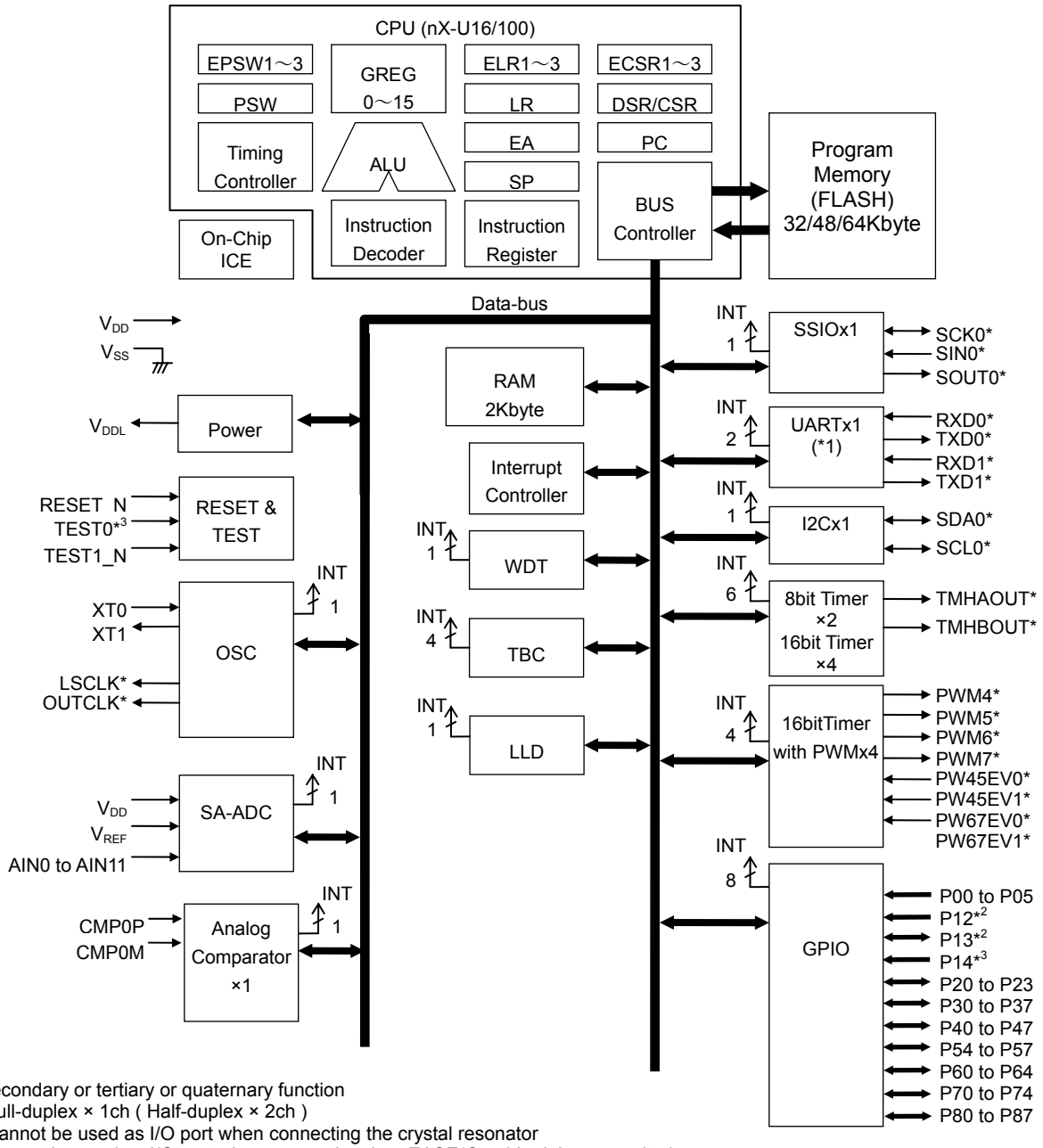
Block Diagram of ML620Q154A/ML620Q155A/ML620Q156A(TQFP52)



* Secondary or tertiary or quaternary function
*1 Full-duplex × 1ch (Half-duplex × 2ch)
*2 Cannot be used as I/O port when connecting the crystal resonator
*3 Cannot be used as I/O port when connecting the uEASE(On-chip debug emualtor)

Figure 1-2 Block Diagram of ML620Q154A/ML620Q155A/ML620Q156A(TQFP52)

Block Diagram of ML620Q157A/ML620Q158A/ML620Q159A(QFP64)



* Secondary or tertiary or quaternary function
*1 Full-duplex × 1ch (Half-duplex × 2ch)
*2 Cannot be used as I/O port when connecting the crystal resonator
*3 Cannot be used as I/O port when connecting the uEASE(On-chip debug emualtor)

Figure 1-3 Block Diagram of ML620Q157A/ML620Q158A/ML620Q159A(QFP64)

PIN CONFIGURATION

ML620Q151A/ML620Q152A/ML620Q153A TQFP48 package product

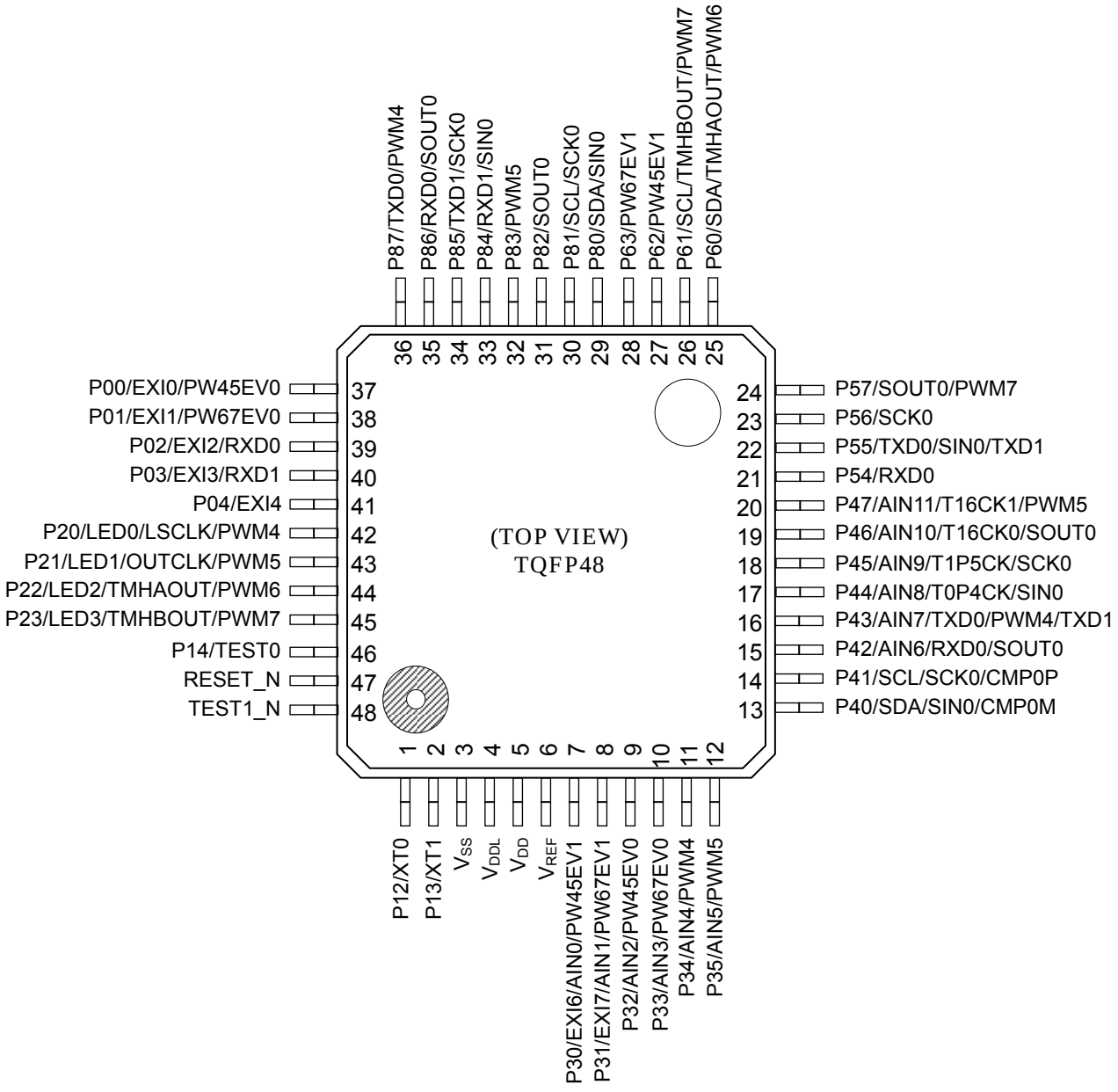


Figure 1-4 Pin Layout of ML620Q151A/ML620Q152A/ML620Q153A TQFP48 Package

ML620Q154A/ML620Q155A/ML620Q156A TQFP52 package product

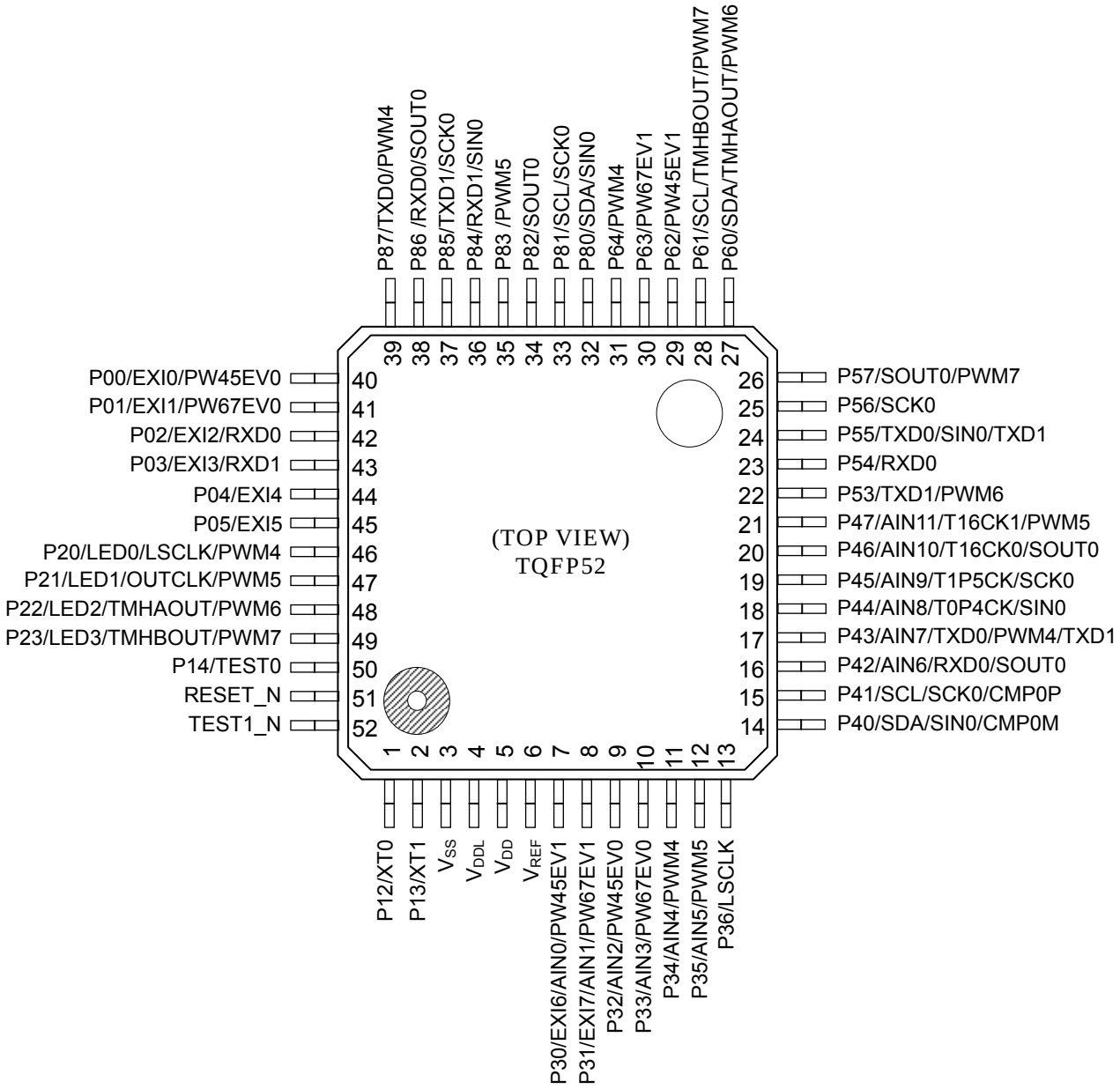


Figure 1-5 Pin Layout of ML620Q154A/ML620Q155A/ML620Q156A TQFP52 Package

ML620Q157A/ML620Q158A/ML620Q159A QFP64 package product

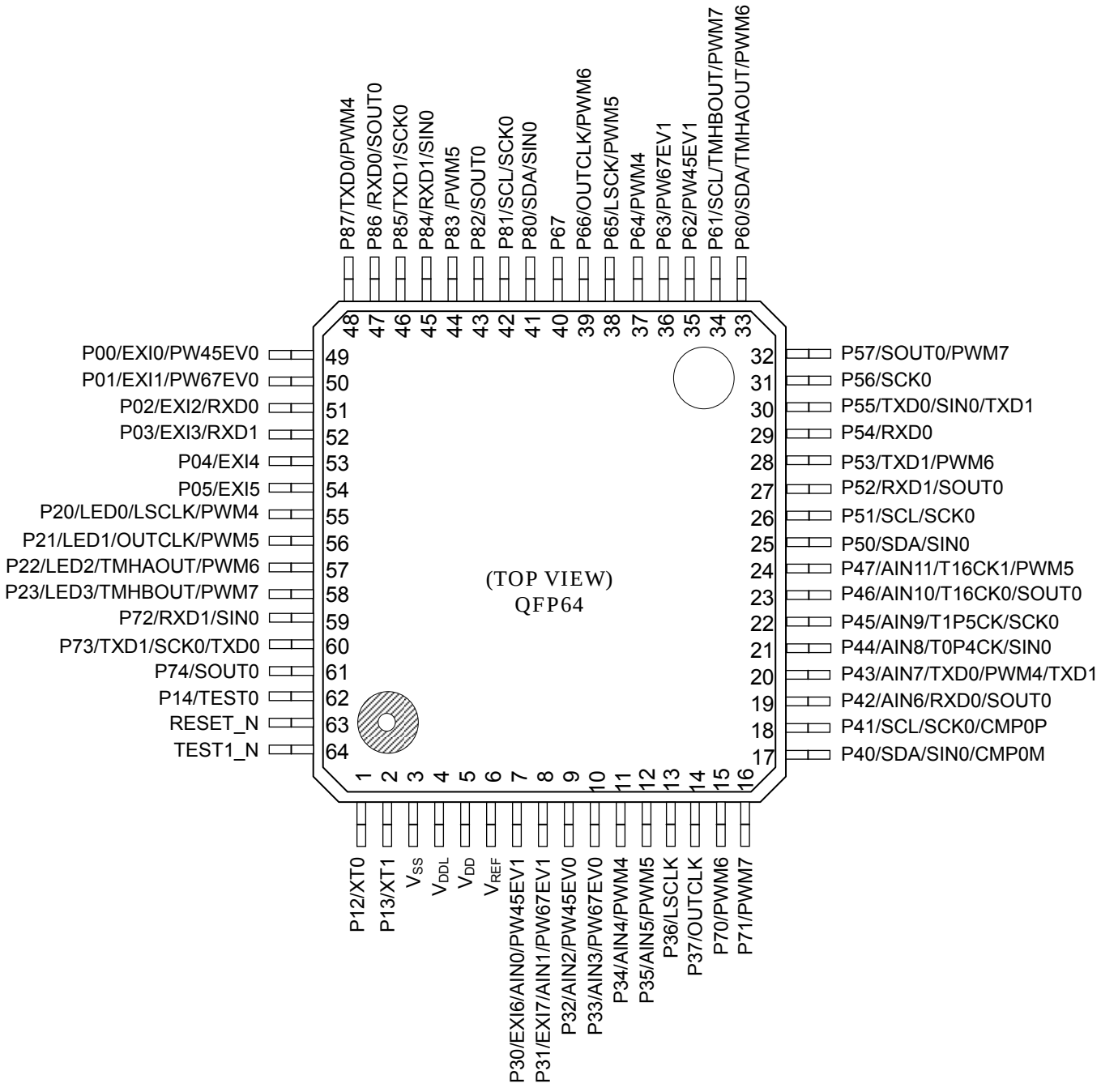


Figure 1-6 Pin Layout of ML620Q157A/ML620Q158A/ML620Q159A QFP64 Package

List of Pins

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	De-scription	Pin name	I/O	De-scription	Pin name	I/O	De-scription
3	3	3	Vss	—	Negative power supply pin	—	—	—	—	—	—	—	—	—
5	5	5	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—	—	—	—
4	4	4	V_{DDL}	—	Power supply for internal logic (internally generated)	—	—	—	—	—	—	—	—	—
46	50	62	P14/ TEST0	I	Input port/ Input pin for testing	—	—	—	—	—	—	—	—	—
47	51	63	RESET_N	I	Reset input pin	—	—	—	—	—	—	—	—	—
48	52	64	TEST1_N	I	Input pin for testing	—	—	—	—	—	—	—	—	—
1	1	1	P12/ XT0	I	Input port/ Low-speed clock oscillation pin	—	—	—	—	—	—	—	—	—
2	2	2	P13/ XT1	I/O	Input/output port/ Low-speed clock oscillation pin	—	—	—	—	—	—	—	—	—
6	6	6	V_{REF}	—	Reference power supply pin of Successive-approximation type ADC	—	—	—	—	—	—	—	—	—
37	40	49	P00/EXI0/ PW45EV0	I	Input port / External interrupt / PW45EV0 input	—	—	—	—	—	—	—	—	—
38	41	50	P01/EXI1/ PW67EV0	I	Input port / External interrupt / PW67EV0 input	—	—	—	—	—	—	—	—	—
39	42	51	P02/EXI2/ RXD0	I	Input port / External interrupt UART0 data input	—	—	—	—	—	—	—	—	—
40	43	52	P03/EXI3/ RXD1	I	Input port / External interrupt UART1 data input	—	—	—	—	—	—	—	—	—
41	44	53	P04/EXI4	I	Input port / External interrupt	—	—	—	—	—	—	—	—	—
—	45	54	P05/EXI5	I	Input port / External interrupt	—	—	—	—	—	—	—	—	—
42	46	55	P20/ LED0/	O	Output port / LED drive	LSCLK	O	Low-speed clock output	PWM4	O	PWM4 output	—	—	—
43	47	56	P21/ LED1/	O	Output port / LED drive	OUTCLK	O	Low-speed clock output	PWM5	O	PWM5 output	—	—	—
44	48	57	P22/ LED2/	O	Output port / LED drive	—	—	—	TMHAOUT	O	TimerA output	PWM6	O	PWM6 output
45	49	58	P23/ LED3/	O	Output port / LED drive	—	—	—	TMHBOUT	O	TimerB output	PWM7	O	PWM7 output
7	7	7	P30/EXI6 PW45EV1/ AIN0	I/O	Input/output port / PW45EV1 input / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
8	8	8	P31/EXI7 PW67EV1/ AIN1	I/O	Input/output port / PW67EV1 input / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
9	9	9	P32/ PW45EV0/ AIN2	I/O	Input/output port / PW45EV0 input / Successive approximation type ADC input	—	—	—	—	—	—	—	—	—
10	10	10	P33/ PW67EV0/ AIN3	I/O	Input/output port / PW67EV0 input / Successive approximation type	—	—	—	—	—	—	—	—	—

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	De-scription	Pin name	I/O	De-scription	Pin name	I/O	De-scription
					ADC input									
11	11	11	P34/ AIN4/	I/O	Input/output port / Successive approximation type ADC input	—	—	—	PWM4	O	PWM4 output	—	—	—
12	12	12	P35/ AIN5/	I/O	Input/output port / Successive approximation type ADC input	—	—	—	PWM5	O	PWM5 output	—	—	—
—	13	13	P36	I/O	Input/output port	LSCLK	O	Low-speed clock output	—	—	—	—	—	—
—	—	14	P37	I/O	Input/output port	OUTCLK	O	Low-speed clock output	—	—	—	—	—	—
13	14	17	P40/ CMP0M	I/O	Input/output port / Comparator0 inverting input	SDA	I/O	I^2C data input/output	SIN0	I	SSIO0 data input	—	—	—
14	15	18	P41/ CMP0P	I/O	Input/output port / Comparator0 non-inverting input	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—
15	16	19	P42/ AIN6	I/O	Input/output port / Successive approximation type ADC input	RXD0	I	UART0 data input	SOUT0	O	SSIO0 data output	—	—	—
16	17	20	P43/ AIN7	I/O	Input/output port / Successive approximation type ADC input	TXD0	O	UART0 data output	PWM4	O	PWM4 output	TXD1	O	UART1 data output
17	18	21	P44/ T0P4CK/ AIN8	I/O	Input/output port / PWM4 external clock input/ Successive approximation type ADC input	—	—	—	SIN0	I	SSIO0 data input	—	—	—
18	19	22	P45/ T1P5CK/ AIN9	I/O	Input/output port / PWM5 external clock input/ Successive approximation type ADC input	—	—	—	SCK0	I/O	SSIO0 synchronous clock input/output	—	—	—
19	20	23	P46/ T16CK0/ AIN10	I/O	Input/output port / Timer8,A / PWM6 external clock input / Successive approximation type ADC input	—	—	—	SOUT0	O	SSIO0 data output	—	—	—
20	21	24	P47/ T16CK1/ AIN11	I/O	Input/output port / Timer9,B / PWM7 external clock input / Successive approximation type ADC input	—	—	—	PWM5	O	PWM5 output	—	—	—
—	—	25	P50	I/O	Input/output port	SDA	I/O	I^2C data input/output	SIN0	I	SSIO0 data input			
—	—	26	P51	I/O	Input/output port	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO0 synchronous clock input/output			
—	—	27	P52	I/O	Input/output port	RXD1	I	UART1 data input	SOUT0	O	SSIO0 data output			

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	De-scription	Pin name	I/O	De-scription	Pin name	I/O	De-scription
—	22	28	P53	I/O	Input/output port	TXD1	O	UART1 data output	PWM6	O	PWM6 output	—	—	—
21	23	29	P54	I/O	Input/output port	RXD0	I	UART0 data input	—	—	—	—	—	—
22	24	30	P55	I/O	Input/output port	TXD0	O	UART0 data output	SIN0	I	SSIO0 data input	TXD1	O	UART1 data output
23	25	31	P56	I/O	Input/output port	—	—	—	SCK0	I/O	SSIO0 synchron ous clock input/out put	—	—	—
24	26	32	P57	I/O	Input/output port	—	—	—	SOUT0	O	SSIO0 data output	PWM7	O	PWM7 output
25	27	33	P60	I/O	Input/output port	SDA	I/O	I^2C data input/ou tput	TMHAO UT	O	TimerA output	PWM6	O	PWM6 output
26	28	34	P61	I/O	Input/output port	SCL	I/O	I^2C clock input/ou tput	TMHBO UT	O	TimerB output	PWM7	O	PWM7 output
27	29	35	P62/ PW45EV1	I/O	Input/output port / PW45EV1 input	—	—	—	—	—	—	—	—	—
28	30	36	P63/ PW67EV1	I/O	Input/output port / PW67EV1 input	—	—	—	—	—	—	—	—	—
—	31	37	P64	I/O	Input/output port	—	—	—	PWM4	O	PWM4 output	—	—	—
—	—	38	P65	I/O	Input/output port	LSCLK	O	Low-spe ed clock output	PWM5	O	PWM5 output	—	—	—
—	—	39	P66	I/O	Input/output port	OUTCLK	O	Low-spe ed clock output	PWM6	O	PWM6 output	—	—	—
—	—	40	P67	I/O	Input/output port	—	—	—	—	—	—	—	—	—
—	—	15	P70	I/O	Input/output port	—	—	—	PWM6	O	PWM6 output	—	—	—
—	—	16	P71	I/O	Input/output port	—	—	—	PWM7	O	PWM7 output	—	—	—
—	—	59	P72	I/O	Input/output port	RXD1	I	UART1 data input	SIN0	I	SSIO0 data input	—	—	—
—	—	60	P73	I/O	Input/output port	TXD1	O	UART1 data output	SCK0	I/O	SSIO0 synchron ous clock input/out put	TXD0	O	UART0 data output
—	—	61	P74	I/O	Input/output port	—	—	—	SOUT0	O	SSIO0 data output	—	—	—
29	32	41	P80	I/O	Input/output port	SDA	I/O	I^2C data input/ou tput	SIN0	I	SSIO0 data input	—	—	—
30	33	42	P81	I/O	Input/output port	SCL	I/O	I^2C clock input/ou tput	SCK0	I/O	SSIO0 synchron ous clock input/out put	—	—	—
31	34	43	P82	I/O	Input/output port	—	—	—	SOUT0	O	SSIO0 data output	—	—	—
32	35	44	P83	I/O	Input/output port	—	—	—	PWM5	O	PWM5 output	—	—	—
33	36	45	P84	I/O	Input/output port	RXD1	I	UART1 data	SIN0	I	SSIO0 data	—	—	—

48 Pin No.	52 Pin No.	64 Pin No.	Primary function			Secondary function			Tertiary function			Quaternary function		
			Pin name	I/O	Description	Pin name	I/O	De-scription	Pin name	I/O	De-scription	Pin name	I/O	De-scription
								input			input			
34	37	46	P85	I/O	Input/output port	TXD1	O	UART1 data output	SCK0	I/O	SSIO0 synchron ous clock input/out put	—	—	—
35	38	47	P86	I/O	Input/output port	RXD0	I	UART0 data input	SOUT0	O	SSIO0 data output	—	—	—
36	39	48	P87	I/O	Input/output port	TXD0	O	UART0 data output	PWM4	O	PWM4 output	—	—	—

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/ Quaternary	Logic
Power supply				
V_{SS}	—	Negative power supply pin	—	—
V_{DD}	—	Positive power supply pin	—	—
V_{DDL}	—	Positive power supply pin for internal logic (internally generated). Connect capacitors (C_L) (see Measuring Circuit 1) between this pin and V_{SS} .	—	—
Test				
TEST0	I	Input/output pin for testing.	—	Positive
TEST1_N	I	Input/output pin for testing. This pin has a pull-up resistor built in.	—	Negative
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, the device is placed in system reset mode and the internal circuit is initialized. If after that this pin is set to a “H” level, program execution starts. This pin has a pull-up resistor built in.	—	Negative
XT0	I	Crystal connection pin for low-speed clock. A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and VSS as required.	—	—
XT1	O		—	—
LSCLK*	O	Low-speed clock output. This function is allocated to the secondary function of the P20/P36/P65 pin.	Secondary	—
OUTCLK*	O	High-speed clock output. This function is allocated to the secondary function of the P21/P37/P66 pin.	Secondary	—
General-purpose input port				
P00 to P05*	I	General-purpose input or output ports.	Primary	Positive
P12	I			
P13	I/O			
P14	I			
General-purpose output port				
P20 to P23	O	General-purpose output ports. Provided with a secondary or tertiary or quaternary function for each port. Cannot be used as ports if their secondary functions or tertiary or quaternary are used.	Secondary/ Tertiary/ Quaternary	Positive
General-purpose input/output port				
P30 to P37*	I/O	General-purpose output ports. Provided with a secondary or tertiary or quaternary function for each port. Cannot be used as ports if their secondary functions or tertiary or quaternary are used.	Secondary/ Tertiary/ Quaternary	Positive
P40 to P47				
P50 to P57*				
P60 to P67*				
P70 to P74*				
P80 to P87				

*: ML620Q15XA have a different pin configuration for each package. See “LIST OF PINS” for more details.

Pin name	I/O	Description	Primary/ Secondary/ Tertiary/	Logic

			Quaternary	
UART				
TXD0*	O	UART0 data output pin. Allocated to the secondary function of the P43, P55 , P87 and the fourthly function of the P73.	Secondary Quaternary	Positive
RXD0*	I	UART0 data input pin. Allocated to the secondary function of the P02, P42, P54 and P86.	Secondary	Positive
TXD1*	O	UART1 data output pin. Allocated to the secondary function of the P53, P73, P85, and the fourthly function of the P43, P55.	Secondary Quaternary	Positive
RXD1*	I	UART1 data input pin. Allocated to the secondary function of the P03, P52, P72 and P84.	Secondary	Positive
I^2C bus interface				
SDA*	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P40, P50, P60 and P80. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL*	I/O	I^2C clock output pin. This pin is used as the secondary function of the P41, P51, P61 and P81. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SIN0*	I	Synchronous serial data input pin. Allocated to the tertiary function of the P40, P44, P50, P55, P72, P80 and P84.	Tertiary	Positive
SCK0*	I/O	Synchronous serial clock input/output pin. Allocated to the tertiary function of the P41, P45, P51, P56, P73, P81 and P85.	Tertiary	—
SOUT0*	O	Synchronous serial data output pin. Allocated to the tertiary function of the P42, P46, P52, P57, P74, P82 and P86.	Tertiary	Positive
PWM				
PWM4*	O	PWM4 output pin. Allocated to the tertiary function of the P34, P43, P64 and P87.	Tertiary	Positive
PWM5*	O	PWM5 output pin. Allocated to the tertiary function of the P35, P47, P65 and P83.	Tertiary	Positive
PWM6*	O	PWM6 output pin. Allocated to the tertiary function of the P53, P66, P70 and fourthly function of the P22 and P60.	Tertiary Quaternary	Positive
PWM7*	O	PWM7 output pin. Allocated to the tertiary function of the P71 and fourthly function of the P23, P57, and P61.	Tertiary Quaternary	Positive
PW45EV0 PW45EV1	I	Control start /stop/clear for PWM4 and PWM5. Allocated to the primary function of the P00, P30, P32 and P62.	Primary	—
PW67EV0 PW67EV1	I	Control start /stop/clear pin for PWM6 and PWM7. Allocated to the primary function of the P01, P31, P33, and P63.	Primary	—
T0P4CK	I	External clock input pin for timer 0 and PWM4. Allocated to the primary function of the P44 pin.	Primary	—
T1P5CK	I	External clock input pin for timer 1 and PWM5. Allocated to the primary function of the P45 pin.	Primary	—

*: ML620Q15XA have a different pin configuration for each package. See “LIST OF PINS” for more details.

Pin name	I/O	Description	Primary/ Secondary	Logic
External interrupt				
EXI0～7*	I	External maskable interrupt input pins. The interrupt is enabled and interrupt edge is selectable by the software for each bit. Allocated to the primary function of the P00 to P05 and P30 to P31.	Primary	Positive/ Negative
Timer				
T16CK0	I	External clock input pin for 16bit timer 8, timer A and PWM6. Allocated to the primary function of the P46 pin.	Primary	—
T16CK1	I	External clock input pin for 16bit timer 9, timer B and PWM7. Allocated to the primary function of the P47 pin.	Primary	—
TMHAOUT	O	16bit timer A output pin. Allocated to the tertiary function of the P22 andn P60.	Tertiary	Positive
TMHBOUT	O	16bit timer B output pin. Allocated to the tertiary function of the P23 and P61.	Tertiary	Positive
LED drive				
LED0 to LED3	O	Pins for LED driving. Allocated to the primary function of the P20 to P23 pins.	Primary	Positive/ Negative
Successive-approximation type A/D converter				
V_{REF}	I	Reference power supply pin for successive approximation type A/D converter.	—	—
AIN0 to AIN11	I	Analog inputs to Ch0–Ch11 of the successive-approximation type A/D converter. Allocated to the secondary function of the P30 to P35 and P42 to P47 pins.	—	—
Analog Comparator				
CMP0P	I	Non-inverting input for comparator0. This pin is used as the primary function of the P41 pin.	—	—
CMP0M	I	Inverting input for comparator0. This pin is used as the primary function of the P40 pin.	—	—

*: ML620Q15XA have a different pin configuration for each package. See “LIST OF PINS” for more details.

TERMINATION OF UNUSED PINS

How to Terminate Unused Pins

Pin	Recommended pin termination
RESET_N	open
P14/TEST0	open
TEST1_N	open
V_{REF}	Connect to V_{DD}
P00 to P05*	Connect V_{DD} or V_{SS}
P12	Connect V_{DD} or V_{SS}
P13	open
P20 to P23	open
P30 to P37*	open
P40 to P47	open
P50 to P57*	open
P60 to P67*	open
P70 to P74*	open
P80 to P87	open

*: ML620Q15XA have a different pin configuration for each package. See “LIST OF PINS” for more details.

Note:
For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	−0.3 to +6.5	V
Power supply voltage 2	V_{DDL}	Ta = 25°C	−0.3 to +2.0	V
Reference voltage	V_{REF}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Analog input voltage	V_{AI}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Input voltage	V_{IN}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	−0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3,4,5,6,7,8 Ta = 25°C	−12 to +11	mA
Output current 2	I_{OUT2}	Port2 Ta = 25°C	−12 to +20	mA
Power dissipation	PD	Ta = 25°C	1	W
Storage temperature	T_{STG}	—	−55 to +150	°C

Recommended Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	−40 to +105	°C
Operating voltage	V_{DD}	—	1.8 to 5.5	V
Reference voltage	V_{REF}	—	1.8 to V_{DD}	V
Analog input voltage	V_{AI}	—	V_{SS} to V_{REF}	V
Operating frequency (CPU)	f_{OP}	—	30k to 8.4M	Hz
Low-speed crystal oscillation frequency	f_{XTL}	—	32.768k	Hz
Low-speed crystal oscillation external capacitor	C_{DL}	Use 32.768KHz Crystal Oscillator DT-26 (DAISHINKU CORP.)	12 to 25	pF
	C_{GL}		12 to 25	
Capacitor externally connected to V_{DDL} pin	C_L	—	2.2±30%	μF

Flash Memory Operating Conditions

(V_{SS} = 0V)

Parameter	Symbol	Condition		Range	Unit
Operating temperature	T_{OP}	Data flash memory, At write/erase		-40 to +105	°C
		Flash ROM, At write/erase		0 to +40	
Operating voltage	V_{DD}	At write/erase		1.8 to 5.5	V
Maximum rewrite count	C_{EPD}	Data Flash		10,000	times
	C_{EPP}	Program Flash		100	
Erase unit	—	Chip erase		All area	—
	—	Block erase	Program Flash	8	KB
			Data Flash	2	KB
	—	Sector erase (Data Flash only)		1	KB
Erase time	—	Chip erase, Block erase, Sector erase		100	ms
Write unit	—	—		1 word (2 Bytes)	—
Write time (Max.)	—	1 word (2 Bytes)		40	μs
Data retention period	Y_{DR}	—		15	years

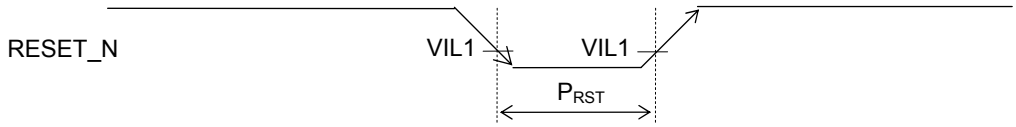
DC Characteristics (Oscillation, Reset)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

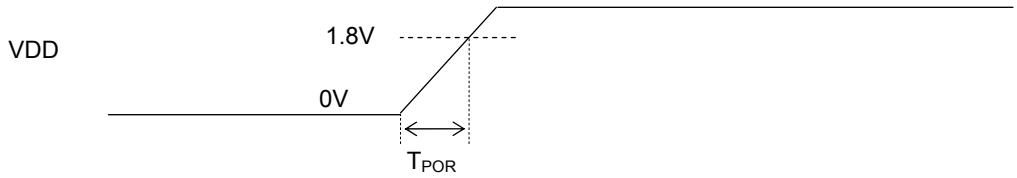
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Low-speed crystal oscillation start time*1	T_{XTL}	—	—	0.6	2	s	1
Low-speed RC oscillator frequency	f_{LCR}	Ta= +25°C	Typ -1%	32.768k	Typ +1%	Hz	
		Ta= -40 to 85°C	Typ -2.5%	32.768k	Typ +2.5%	Hz	
		Ta= -40 to 105°C	Typ -3%	32.768k	Typ +3%	Hz	
High-speed RC oscillator ferequency	f_{HCR}	Ta= +25°C	Typ -5%	2.097	Typ +5%	MHz	
		Ta= -40°C to +105°C	Typ -15%	2.097	Typ +15%	MHz	
PLL oscillation frequency	f_{PLL}	LSCLK=32.768kHz 2,048 clock average	Typ -1%	8.192	Typ +1%	MHz	
Reset pulse width	P_{RST}	—	100	—	—	μs	
Reset noise rejection pulse width	P_{NRST}	—	—	—	0.4		
Power On Reset rising time	T_{POR}	—	—	—	10	ms	

*1: Use 32.768KHz Crystal Oscillator DT-26 (Daishinku) with capacitance C_{GL}/C_{DL}＝12pF.

Reset



Reset pulse width (P_{RST})



Power On Reset VDD Rising Time (T_{POR})

DC Characteristics (LLD)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
LLD threshold voltage	V_{D-}	When power falling	LD1 to 0 = 0H	1.8	1.9	2	V	1
			LD1 to 0 = 1H	2.45	2.55	2.65		
			LD1 to 0 = 2H	3.6	3.7	3.8		
			LD1 to 0 = 3H	4.1	4.2	4.3		
	V_{D+}	When power rising	LD1 to 0 = 0H	1.85	1.98	2.1		
			LD1 to 0 = 1H	2.5	2.63	2.75		
			LD1 to 0 = 2H	3.65	3.78	3.9		
			LD1 to 0 = 3H	4.15	4.28	4.4		
Hysterisis	V_{hys}	—	—	—	80	—	mV	mA

DC Characteristics (Analog Comparator)

(V_{DD}=2.2 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Common mode Input voltage	CMPnM V_{IN}	—	0	—	V_{DD} -1.4	V	1
	CMPnP V_{IN}	—	0	—	V_{DD}		
Input offset voltage	V_{CMPOF}	—	—	5	100	mV	
Response time	T_{CMP}	CMPnP = CMPnM ± 100mV	—	—	1	μS	

DC Characteristics (IDD)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Supply current 1	IDD1	CPU is in STOP state. Low-speed/high-speed oscillation is stopped. V_{DD}=3.0V	-40 to +35℃	—	1.0	6	μA	1
			-40 to +105℃	—	1.0	22		
Supply current 2	IDD2	Crystal Oscillating. CPU is in HALT state (LTBC,WBC: Operating*2). High-speed oscillation is stopped. V_{DD}=3.0V	-40 to +35℃	—	2.5	7		
			-40 to +105℃	—	2.5	24		
		Internal RC Oscillating. CPU is in HALT state (LTBC,WBC: Operating*2). High-speed oscillation is stopped. V_{DD}=3.0V	-40 to +35℃	—	3.5	9		
			-40 to +105℃	—	3.5	26		
Supply current 3	IDD3	CPU: Running at 32kHz*1 High-speed oscillation is stopped. V_{DD}=3.0V	-40 to +35℃	—	13	20		
			-40 to +105℃	—	13	42		
Supply current 4	IDD4	CPU: Running at 2MHz RC oscillating mode*2 V_{DD}=5.0V		—	0.64	2.0	mA	
Supply current 5	IDD5	CPU: Running at 8.192MHz PLL oscillating mode*2 V_{DD}=5.0V		—	5	8		

*1: Case when the CPU operating rate is 100% (with no HALT state)

*2 : Significant bits of BLKCON0 to BLKCON4 registers are all “1”.

DC Characteristics (VOHL, IOHL)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit	Measuring circuit
Output voltage 1 (P20 to P23) (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	VOH1	IOH1 = –0.5mA		V_{DD} –0.5	—	—	V	2
	VOL1	IOL1 = +0.5mA		—	—	0.5		
Output voltage 2 (P20–P23)	VOL2	When LED drive mode is selected	IOL2 = +10mA $V_{DD} \geq$ 5.0V	—	—	0.5		
			IOL2 = +8mA $V_{DD} \geq$ 3.0V	—	—	0.5		
Output voltage 3 (P40 to P41) (P50 to P51)* (P60 to P61)* (P80 to P81)	VOL3	When I^2C mode is selected	IOL3 = +3mA $V_{DD} \geq$ 2.0V	—	—	0.4		
			IOL3 = +2mA 2.0V > $V_{DD} \geq$ 1.8V	—	—	VDD* 0.2		
Output leakage current (P20 to P23) (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		–1	—	—		

DC Characteristics (IIHL)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input current 1 (RESET_N) (TEST1_N)	IIH1	VIH1 = V_{DD}	0	—	1	μA	4
	IIL1	VIL1 = V_{SS}	–1500	–300	–20		
Input current 2 (P00 to P05)* (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	IIH2	VIH2 = V_{DD} (when pulled down)	2	30	250		
	IIL2	VIL2 = V_{SS} (when pulled up)	–250	–30	–2		
	IIH2Z	VIH2 = V_{DD} (in high-impedance state)	—	—	1		
	IIL2Z	VIL2 = V_{SS} (in high-impedance state)	-1	—	—		

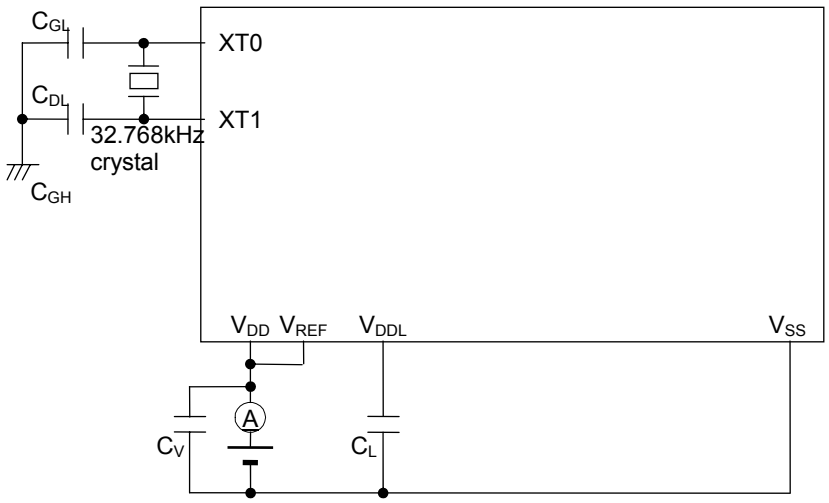
DC Characteristics (VIHL)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Measuring circuit
Input voltage 1 (RESET_N) (P14/TEST0) (TEST1_N) (P00 to P05)* (P12, P13) (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	VIH1	—	0.7× V_{DD}	—	V_{DD}	V	5
	VIL1	—	0	—	0.3× V_{DD}		
Input pin capacitance (RESET_N) (P14/TEST0) (TEST1_N) (P00 to P05)* (P12, P13) (P30 to P37)* (P40 to P47) (P50 to P57)* (P60 to P67)* (P70 to P74)* (P80 to P87)	CIN	f = 10kHz V_{rms} = 50mV Ta = 25°C	—	—	10	pF	—

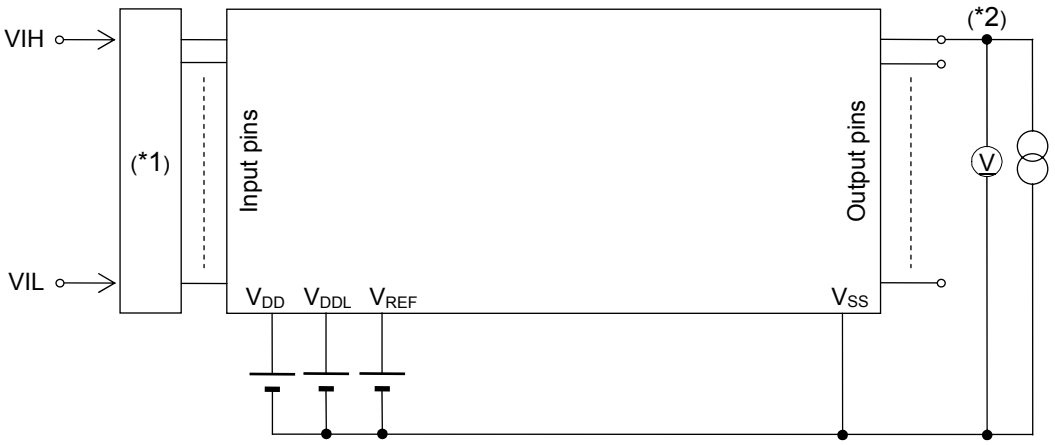
*: ML620Q15X have a different pin configuration for each package. See “LIST OF PINS” for more details.

Measuring circuit 1



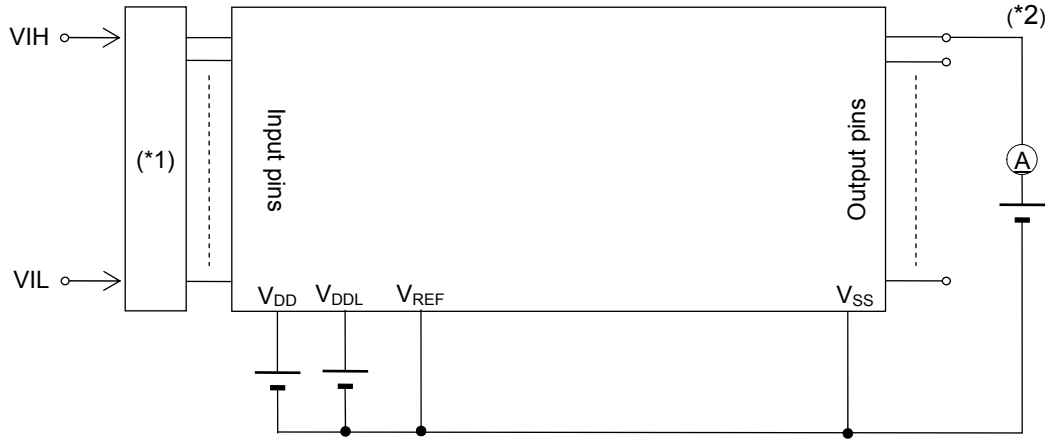
C_V : 2.2µF
C_L : 2.2µF
C_{GL} : 12pF
C_{DL} : 12pF
32.768kHz Crystal oscillator
(DT-26 DAISHINKU Corp.)

Measuring circuit 2



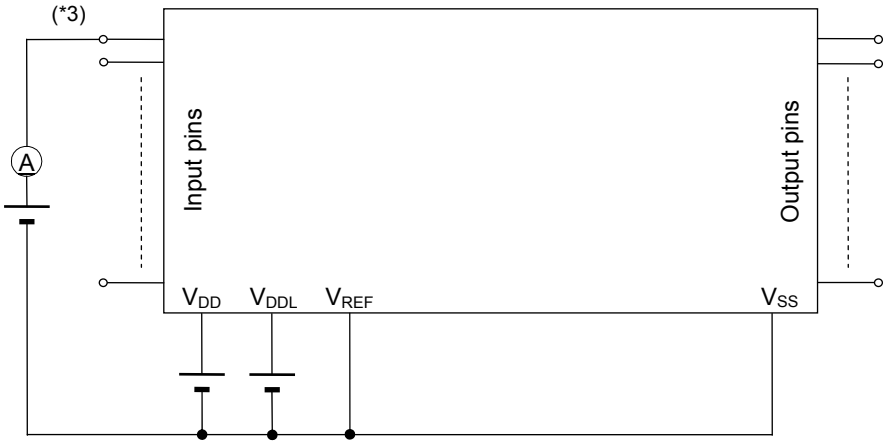
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring circuit 3



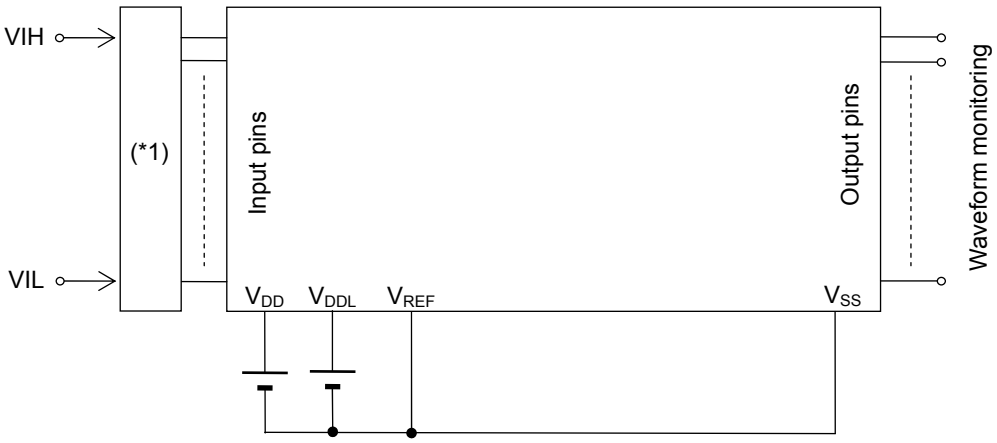
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring circuit 4



*3: Measured at the specified input pins.

Measuring circuit 5

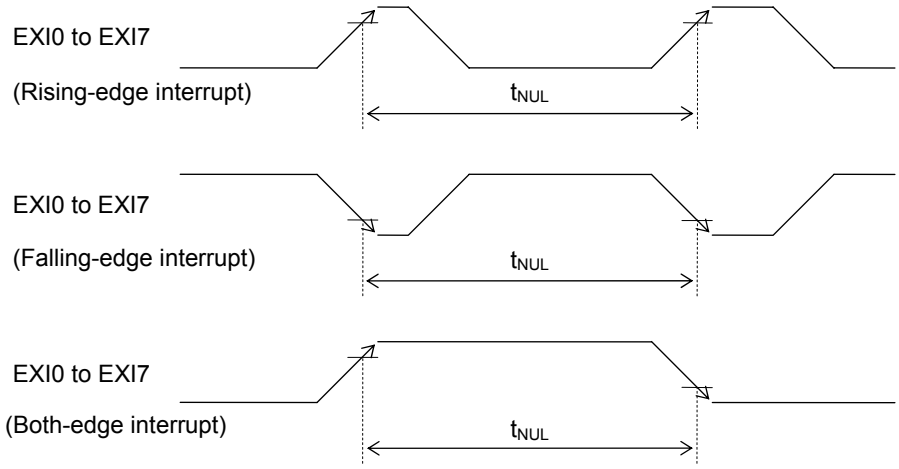


*1: Input logic circuit to determine the specified measuring conditions.

AC Characteristics (External Interrupt)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation	2.5× LSCLK	—	3.5× LSCLK	μs

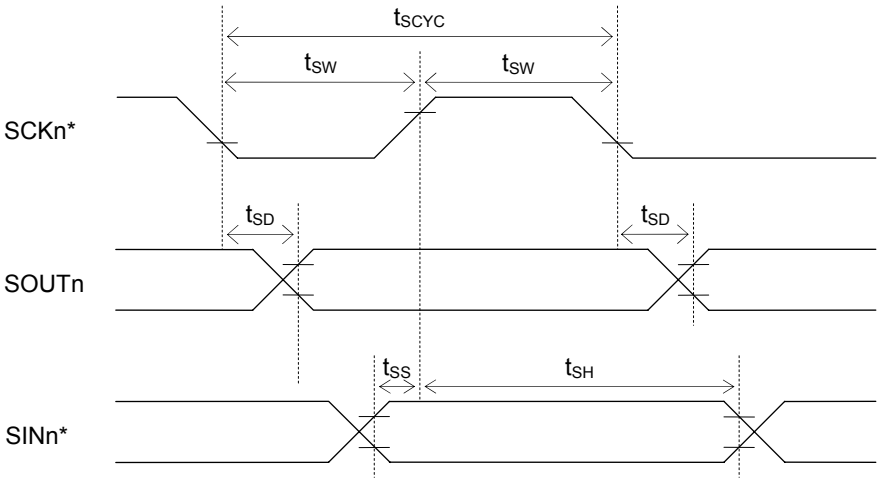


AC Characteristics (Synchronous Serial Port)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCK input cycle (slave mode)	t_{SCYC}	High-speed oscillation stopped	10	—	—	µs
		During high-speed oscillation	500	—	—	ns
SCK output cycle (master mode)	t_{SCYC}	—	—	SCK(*1)	—	sec
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation stopped	4	—	—	µs
		During high-speed oscillation	200	—	—	ns
SCK output pulse width (master mode)	t_{SW}	—	SCK(*1) ×0.4	SCK(*1) ×0.5	SCK(*1) ×0.6	sec
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (Master mode)	t_{SS}	—	240	—	—	ns
SIN input hold time	t_{SH}	—	80	—	—	ns

*1: Clock period selected by SnCK3–0 of the serial port n mode register (SIOnMOD1)



*: Indicates the secondary function of the corresponding port.

AC Characteristics (I2C Bus Interface: Standard Mode 100kHz)

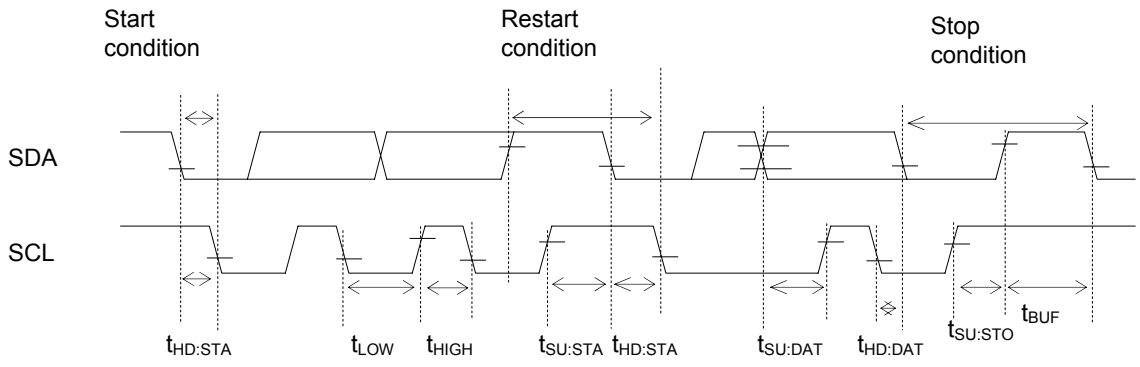
(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	100	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	4.0	—	—	µs
SCL ”L” level time	t_{LOW}	—	4.7	—	—	µs
SCL ”H” level time	t_{HIGH}	—	4.0	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	4.7	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.25	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	4.0	—	—	µs
Bus-free time	t_{BUF}	—	4.7	—	—	µs

AC Characteristics (I2C Bus Interface: Fast Mode 400kHz)

(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

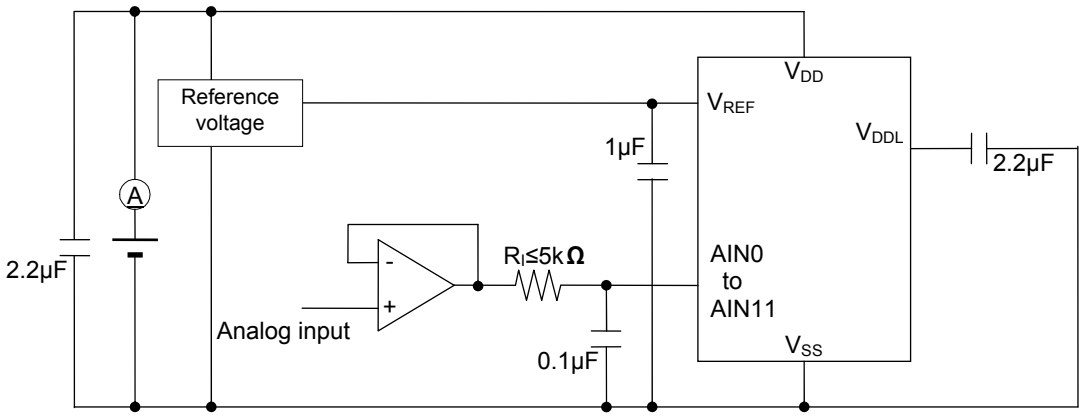
Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	—	0	—	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	—	0.6	—	—	µs
SCL ”L” level time	t_{LOW}	—	1.3	—	—	µs
SCL ”H” level time	t_{HIGH}	—	0.6	—	—	µs
SCL setup time (restart condition)	$t_{SU:STA}$	—	0.6	—	—	µs
SDA hold time	$t_{HD:DAT}$	—	0	—	—	µs
SDA setup time	$t_{SU:DAT}$	—	0.1	—	—	µs
SDA setup time (stop condition)	$t_{SU:STO}$	—	0.6	—	—	µs
Bus-free time	t_{BUF}	—	1.3	—	—	µs



Characteristics of Successive Approximation Type A/D Converter

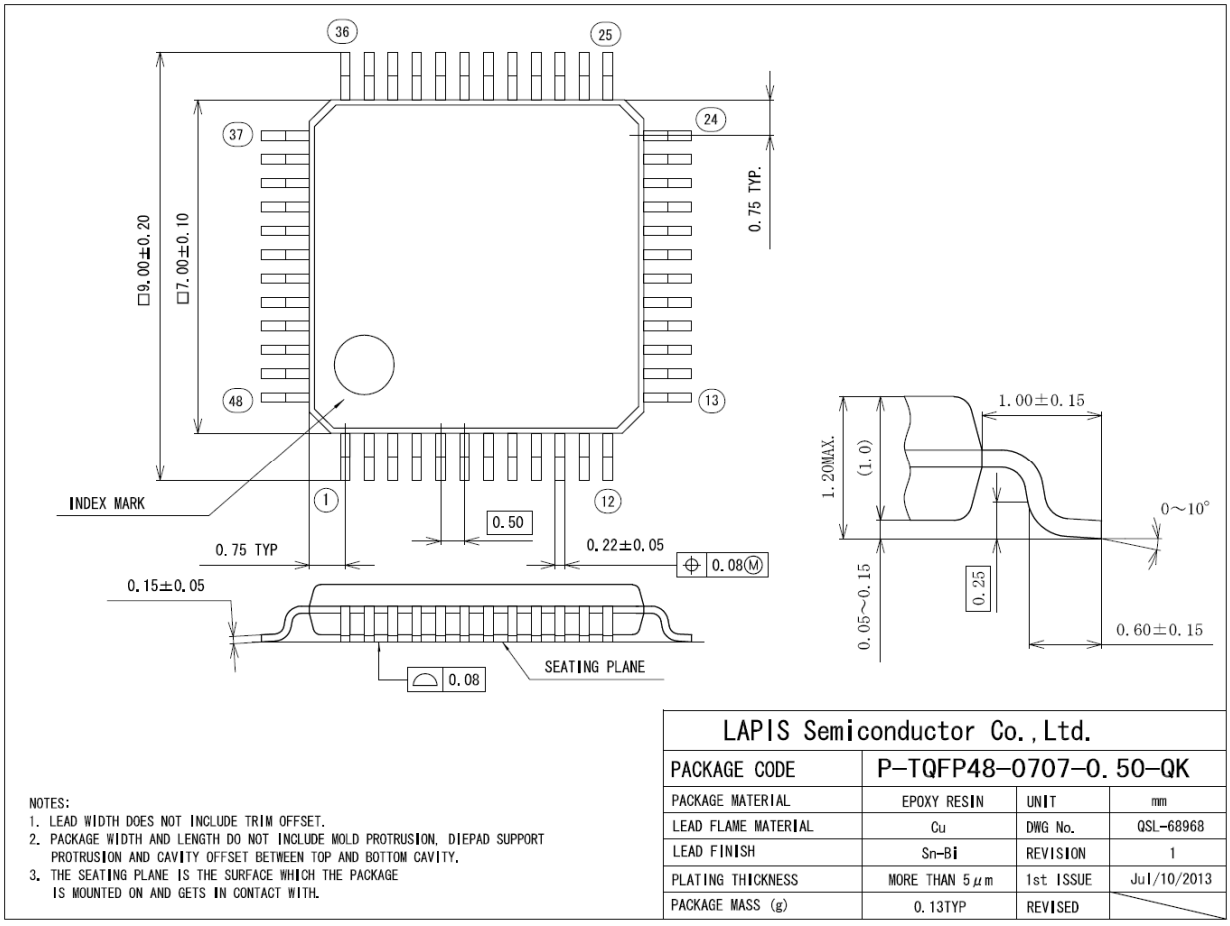
(V_{DD}=1.8 to 5.5V, V_{SS} =0V, Ta=–40 to +105°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n	—	—	—	10	bits
Integral non-linearity error	INL	2.7V ≤ V_{REF} ≤ 5.5V	–4	—	+4	LSB
		2.2V ≤ V_{REF} < 2.7V	–6	—	+6	
		1.8V ≤ V_{REF} < 2.2V	–10	—	+10	
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 5.5V	–3	—	+3	
		2.2V ≤ V_{REF} < 2.7V	–5	—	+5	
		1.8V ≤ V_{REF} < 2.2V	–9	—	+9	
Zero-scale error	V_{OFF}	RI ≤ 5kΩ	–6	—	+6	
Full-scale error	FSE	RI ≤ 5kΩ	–6	—	+6	
Input impedance	R_I	—	—	—	5k	Ω
A/D operating voltage	V_{REF}	V_{REF} ≤ V_{DD}	2.7	—	5.5	V
Conversion time	t_{CONV}	CPU works in PLL oscillation mode SACK bit = 0 2.7V ≤ V_{REF} ≤ 5.5V	—	13.5	—	µs
		CPU works in PLL oscillation mode SACK bit = 1 1.8V ≤ V_{REF} ≤ 5.5V	—	43	—	



PACKAGE DIMENSIONS

ML620Q151A/ML620Q152A/ML620Q153A Package Dimension (48pin TQFP)



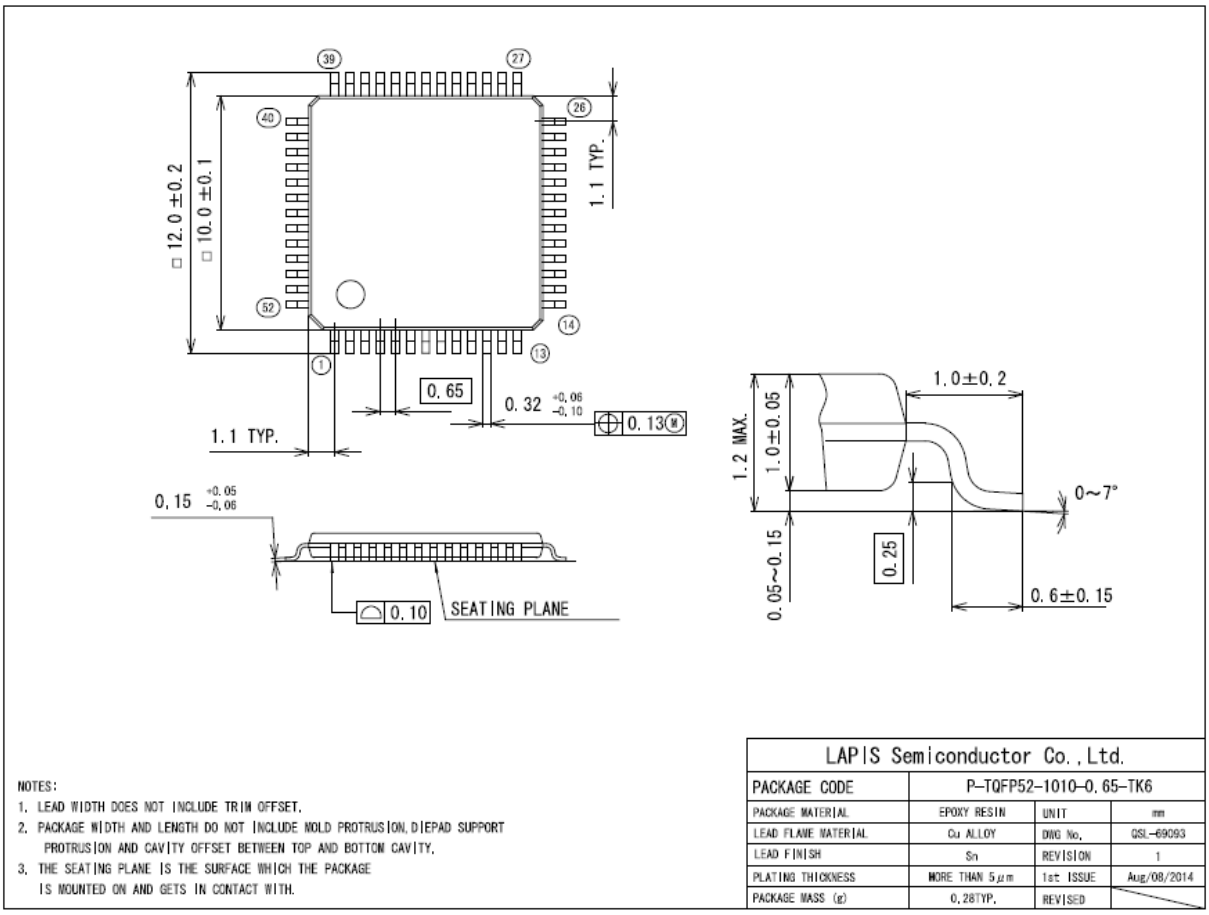
NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-TQFP48-0707-0.50-QK		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu	DWG No.	QSL-68968
LEAD FINISH	Sn-Bi	REVISION	1
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/10/2013
PACKAGE MASS (g)	0.13TYP	REVISED	

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

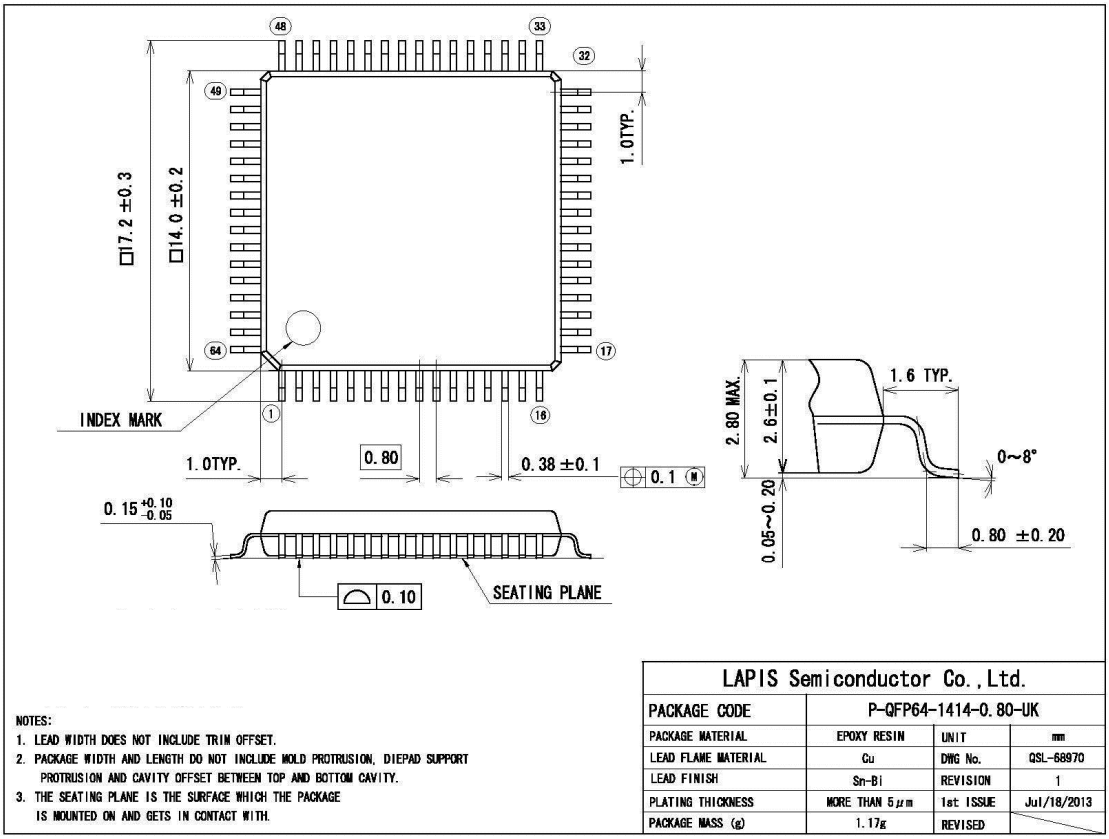
ML620Q154A/ML620Q155A/ML620Q156A Package Dimension (52pin TQFP)



Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

ML620Q157A/ML620Q158A/ML620Q159A PACKAGE DIMENSION (64PIN TQFP)



NOTES:
1. LEAD WIDTH DOES NOT INCLUDE TRIM OFFSET.
2. PACKAGE WIDTH AND LENGTH DO NOT INCLUDE MOLD PROTRUSION, DIEPAD SUPPORT PROTRUSION AND CAVITY OFFSET BETWEEN TOP AND BOTTOM CAVITY.
3. THE SEATING PLANE IS THE SURFACE WHICH THE PACKAGE IS MOUNTED ON AND GETS IN CONTACT WITH.

LAPIS Semiconductor Co.,Ltd.			
PACKAGE CODE	P-QFP64-1414-0.80-UK		
PACKAGE MATERIAL	EPOXY RESIN	UNIT	mm
LEAD FLAME MATERIAL	Cu	DWG No.	QSL-68970
LEAD FINISH	Sn-Bi	REVISION	1
PLATING THICKNESS	MORE THAN 5μm	1st ISSUE	Jul/18/2013
PACKAGE MASS (g)	1.17g	REVISED	

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL620Q150-01	Jul 15, 2014	–	–	Preliminary First Edition
PEDL620Q150-02	Aug 14, 2014	P2-P4	P2-P4	Changed English expression for some descriptions.
		P5-P7	P5-P7	Added notes (*) about some pins.
		P10	P10	Corrected pin names of 57pin and 58pin.
		P11	P11	Deleted the 2nd function of P02 and P03.
		P13	P13	Corrected the tertiary function name of P70 and P71.
		P15	P15	Changed English expression for the note(*).
		P16	P16	Corrected description about PW45EVn and PW67EVn.
		P17	P17	Corrected description about EXI0-7 and TMHnOUT.
		P18	P18	Changed English expression for the note(*).
		P21	P21	Added Power On Reset Rising Time (T_{POR}).
		P24	P24	Corrected pin name and Change English expression for the note(*).
		P32	P32	Added 52pin TQFP package dimension.
FEDL620Q150A-01	May 7, 2015	–	–	Formal First Edition
		–	–	● Changed the part numbers. (Old) ML620Q151/152/153/154/155/156/157/158/159 (New) ML620Q151A/152A/153A/154A/155A/156A/157A/158A/159A
		1	1	● Made a list of ROM size and rewrite cycle. ● Made a list of the number of interrupt.
		3	3	Made a list of the number of ports.
		4	4	Made a list of the kinds of package.
		16	16	Corrected the port name PWMn assigned.

Notes

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